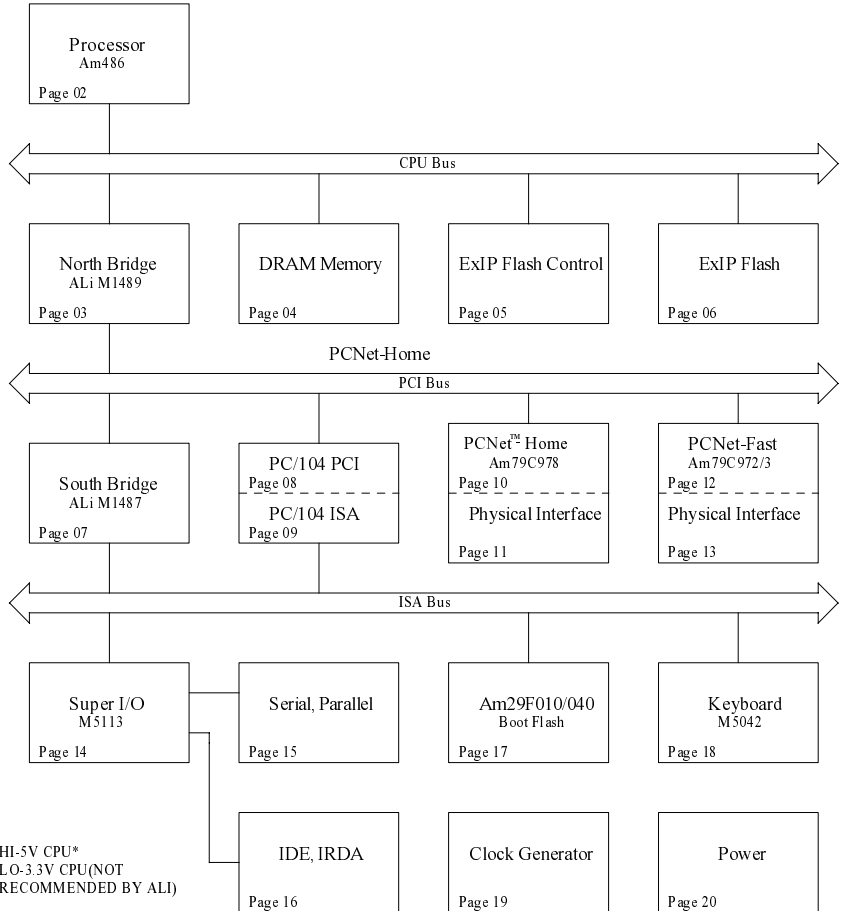




# NET486

## Am486<sup>®</sup> Microprocessor Demonstration Board

### Revision 01



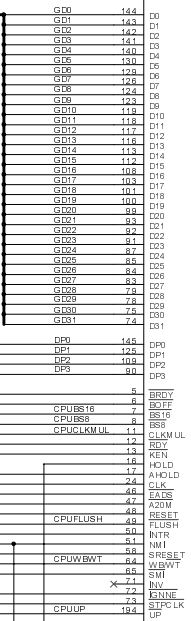
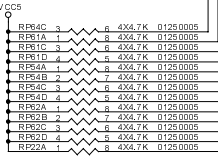
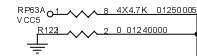
GW2317 Revision Tracking		
Revision	Sheet	Description
01	All	Initial Release

M1489 Power-on Configuration	
Signal	Configuration (asterisk is default)
CMPST	HI-PCICLK=CPUCLK* LO-PCICLK=1/2CPUCLK
CLEAROK	HI-L2CSJ LO-DRAM PARITY*
PCIPERR	HI-PCI PERR* LO-MEM BUF DIR
MWE	I-5V CPU* LO-3.3V CPU (NOT RECOMMENDED BY ALI)

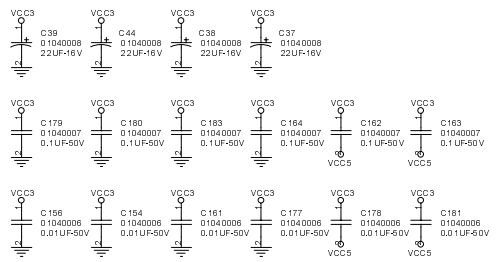
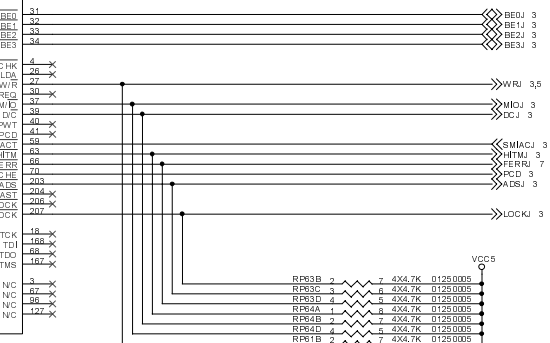
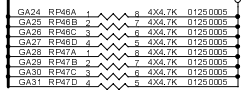
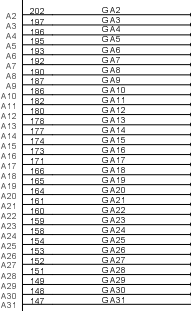
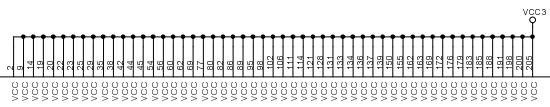
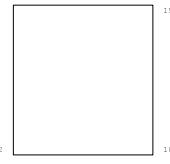
M1487 Power-on Configuration	
Signal	Configuration (asterisk is default)
XBUSCS	HI-8BIT BOOT FLASH* LO-16BIT BOOT FLASH
ENRTC	HI-ENABLE RTC* LO-DISABLE RTC
IBCST	HI-ENABLE KBD LO-DISABLE KBD*
CMPST	HI-PCICLK=CPUCLK* LO-PCICLK=1/2CPUCLK
CMPGNT	HI-5V CPU* LO-3.3V CPU (NOT RECOMMENDED BY ALI)
IGNNE	HI-NORMAL OPERATION* LO-TEST OPERATION

PCI Bus Mapping			
Device	Address	Interrupt	Function
0	AD16	INT1/INTB	NOT USED
1	AD17	INT2/INTC	NOT USED
2	AD18	INT3/INTD	NOT USED
3	AD19	INT0/INTA	NOT USED
4	AD20	INT1/INTB	NOT USED
5	AD21	INT2/INTC	AM97C972/3
6	AD22	INT3/INTD	AM97C978
7	AD23	INT0/INTA	PC/104 PLUS
8	AD24	INT1/INTB	PC/104 PLUS
9	AD25	INT2/INTC	PC/104 PLUS
10	AD26	INT3/INTD	PC/104 PLUS

	SPEED	RL
Am4 0 6DX2-66	2X	IN
Am4 0 6DX4-100	3X	OUT
Am4 0 6DX5-133	4X	IN



### AM486<sup>®</sup> PROCESSOR SQFP208



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Title		NET486	
Size	Document Number	Processor	Rev 01
Date: Friday, May 21, 1989		Sheet 2 of 20	

2,5,7,17,18 GA2..31

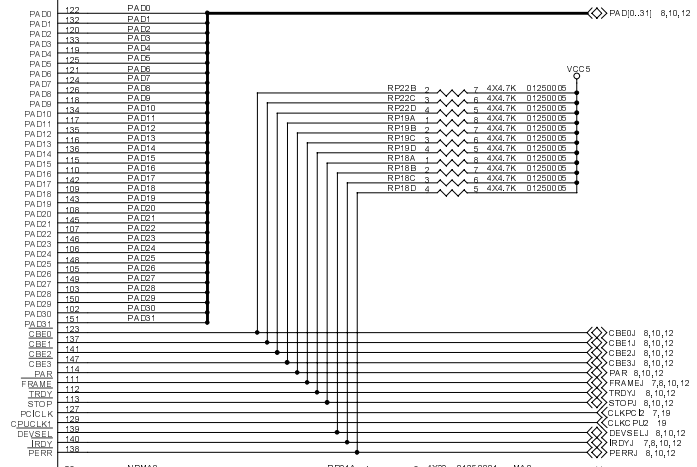
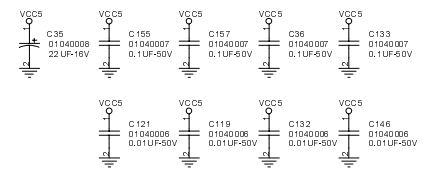
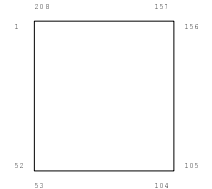
2,4,6 GD0..31

2 BE0J  
2 BE1J  
2 BE2J  
2 BE3J  
2 LOCKJ  
2 ASUJ  
2 MD1J  
2 DJJ  
2 WRJ  
2 RDJ  
2 HTMJ  
2 RDYJ  
2 BOFFJ  
2 AHOLDJ  
2 EASDJ  
2 KENUJ  
2 BRDYJ  
2,5,7,8,14 RSTDRV  
16 HDD0..15J

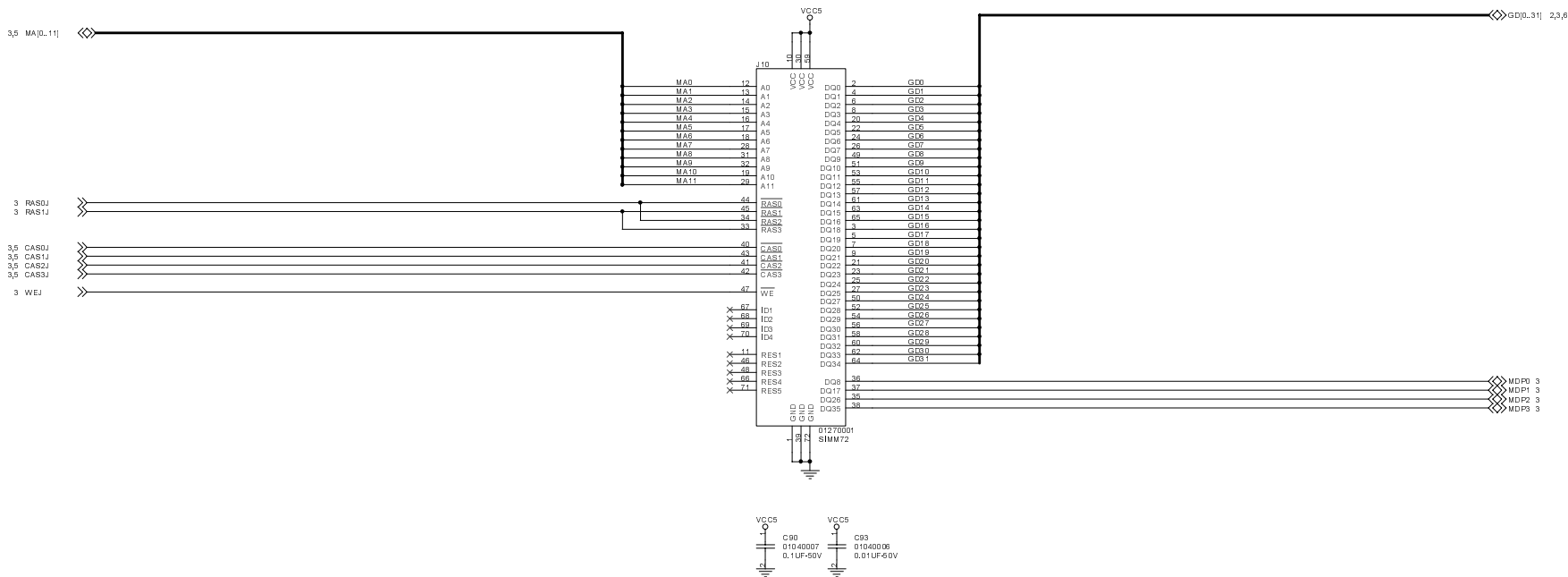
16 HD00WJ  
16 HD00RJ  
16 HD00RDYJ  
16 HD00HJ  
16 HD00A  
16 HD00S0J  
16 HD00S1J



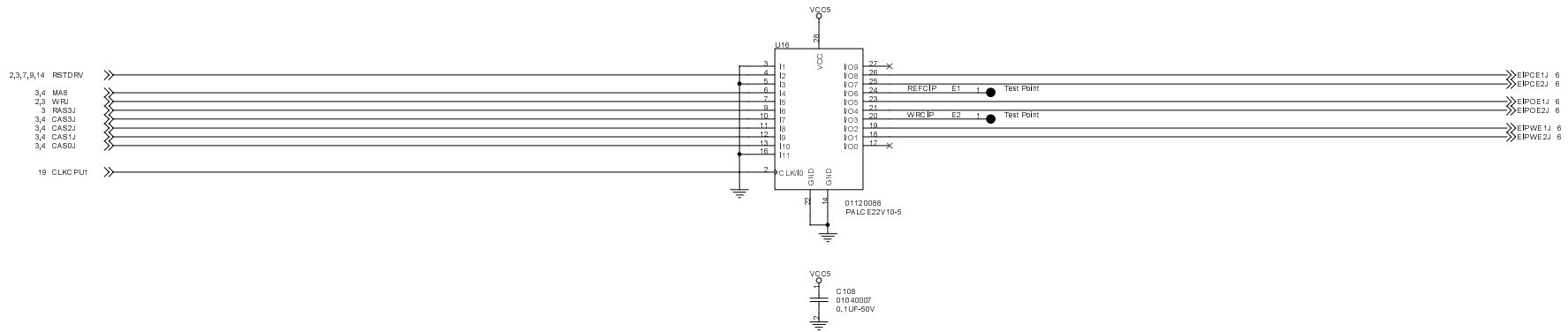
### M1489 NORTH BRIDGE PQFP208



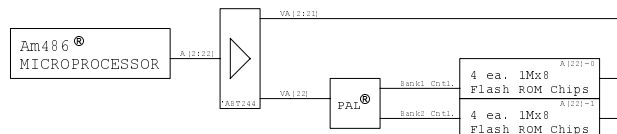
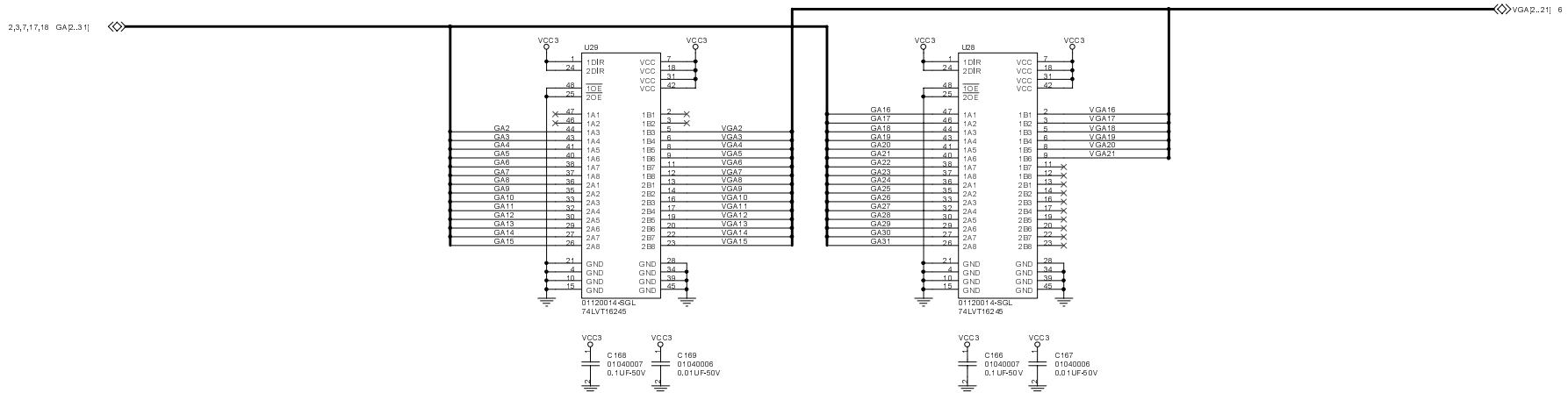
**72 PIN SIMM DRAM**  
5V/16MBIT DRAM TECHNOLOGY



## EXECUTE-IN-PLACE FLASH CONTROL



## EXECUTE-IN-PLACE FLASH BUFFERING



CPU Address Bit A(22) Used As Flash Bank Select

### EXIP Flash [Execute In Place]

#### Operation:

Makes two banks of 1Mx32 flash appear as one bank of 2Mx32 DRAM [70ns, FPM] to M1489 memory controller

Multiply the flash address by four to determine the CPU address [e.g. flash AAAh is accessed at CPU 2AAAh]

Flash start address moves depending on how much DRAM is installed [e.g. 48Mbytes of dram puts flash start address at 40Mbytes or 3000000h for the first bank of flash and 3400000h for the second bank

#### Programming:

Program the M1489 for 2Mx8 [11/10] dram architecture and "fast" timings. Address MA8 [CPU A22] is used as a flash bank select when RAS3 is asserted by 1489 memory controller.

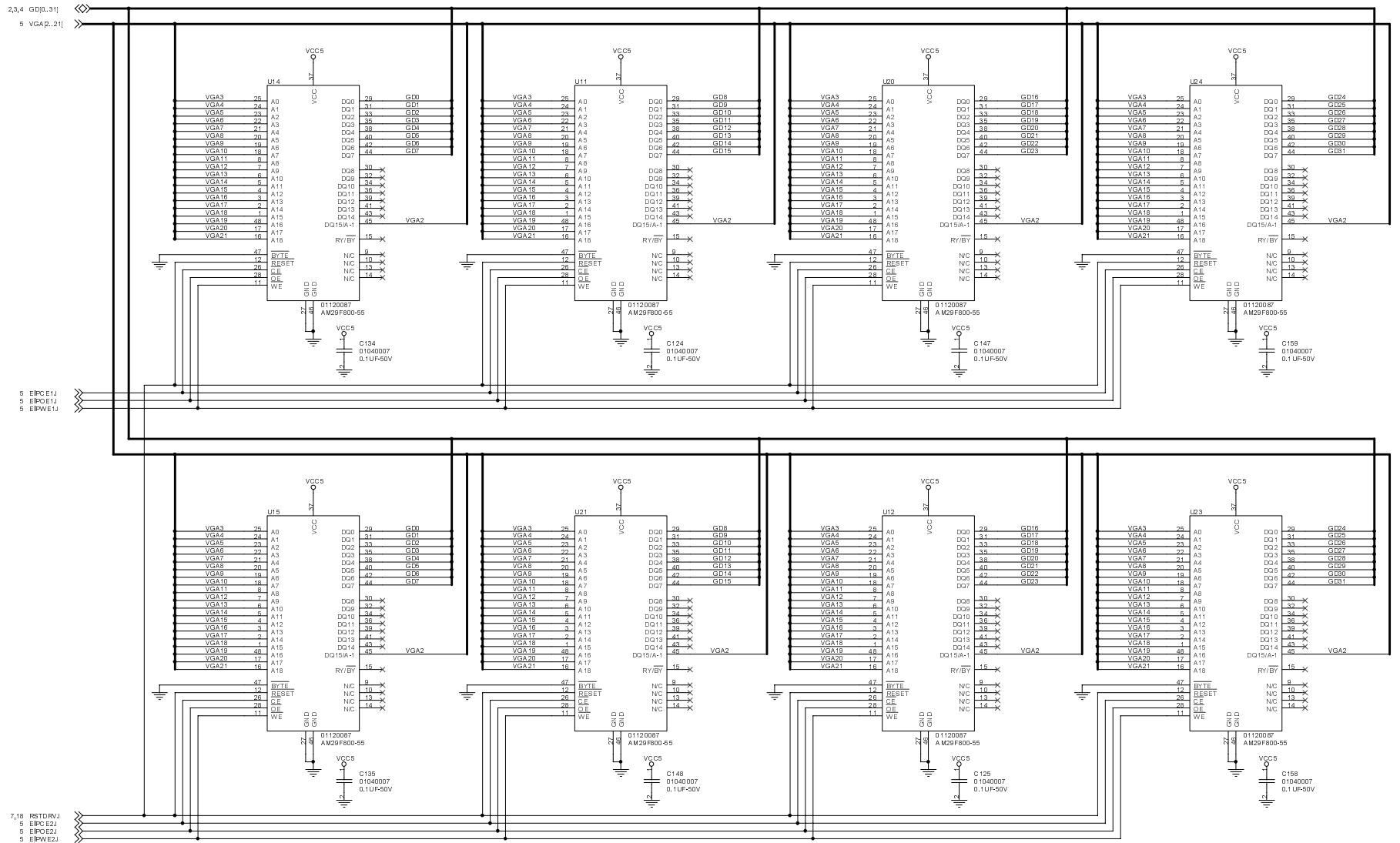
#### Limitations:

- Must access as 32-bit data
- Supports burst read or single-beat read
- Supports single-beat write only. Back-to-back write cycles are not supported
- Compatible with cas-before-ras refresh cycles only
- Not accessible from pci bus masters
- Flash devices are 29F800-55 configured for byte operation

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Title		NET486	
Size	Document Number	EXIP Flash Control	Rev 01
Date:	Monday, May 24, 1999	Sheet	5 of 20

# EXECUTE-IN-PLACE FLASH TSOP48



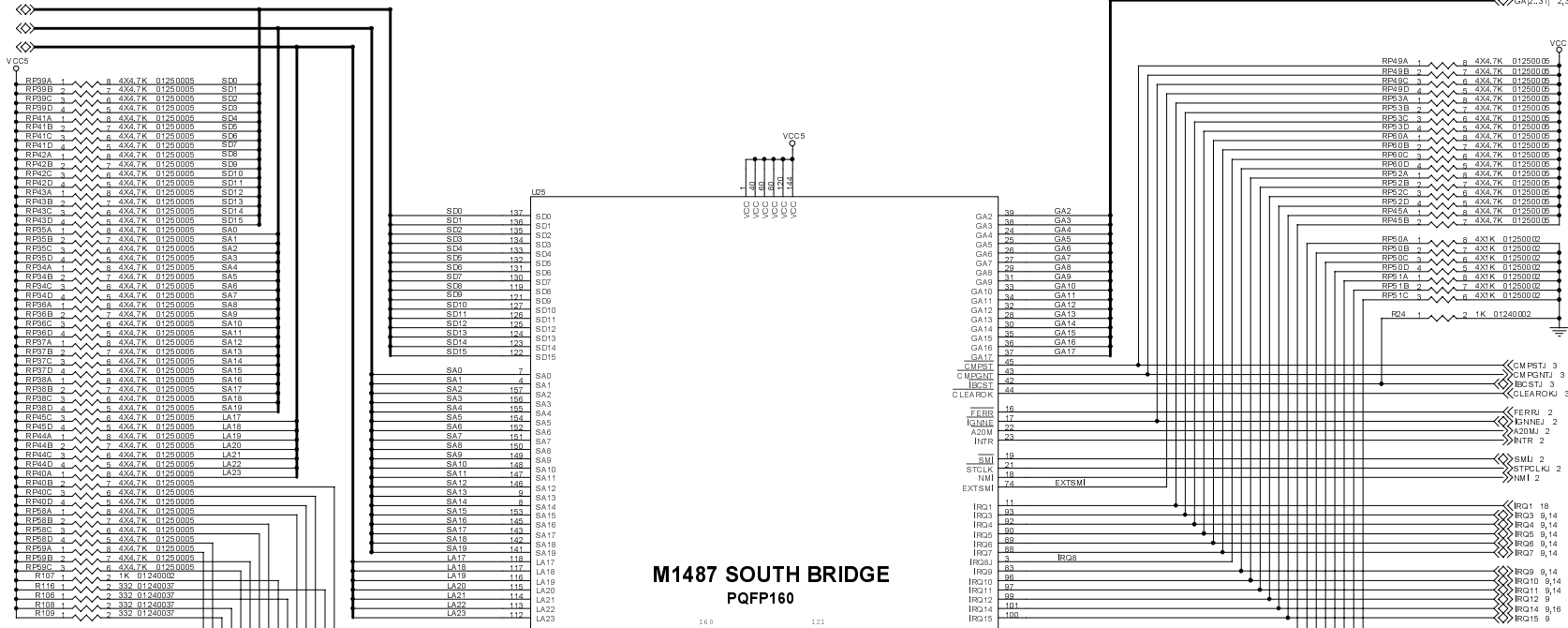
2,3,4 GD[0..3]1  
5 VGA2..21

5 EIPCE11  
5 EIPCE12  
5 EIPWE11

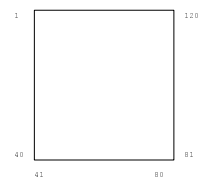
7,18 RSTDRV1  
5 EIPCE21  
5 EIPCE22  
5 EIPWE21

9,14 SD[0..15]  
9,14,17,18 SA[0..19]  
9 LA[17..23]

GA2..3[1] 2,3,5,17,18

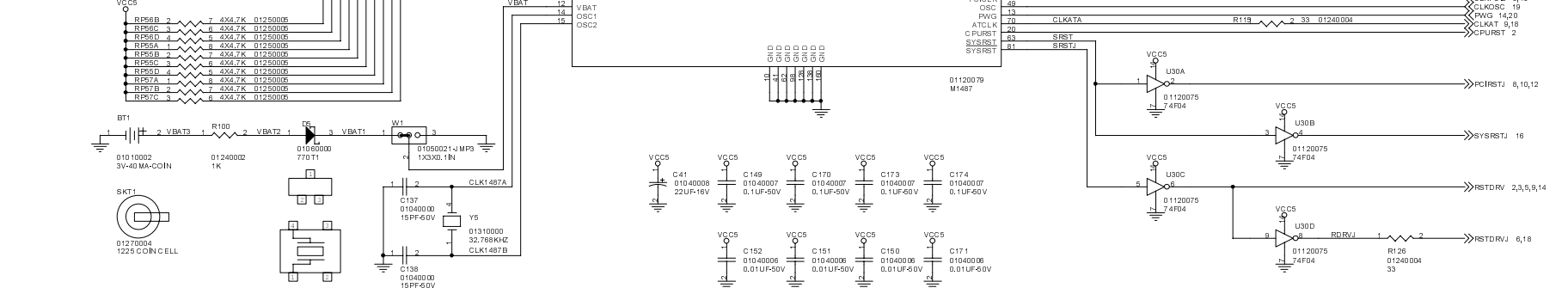


### M1487 SOUTH BRIDGE PQFP160



9 SBHEJ  
9,14 AEN  
9 I16I  
9 MEMEJ  
9,17 MEMRJ  
9 MEMWJ  
9 S1MEMWJ  
9,17 I2CHNDY  
9 NDWSJ  
9 BLE  
9,14,16 I2RU  
9,14,18 I2WJ  
9 MASTERJ  
9 I2CHJ

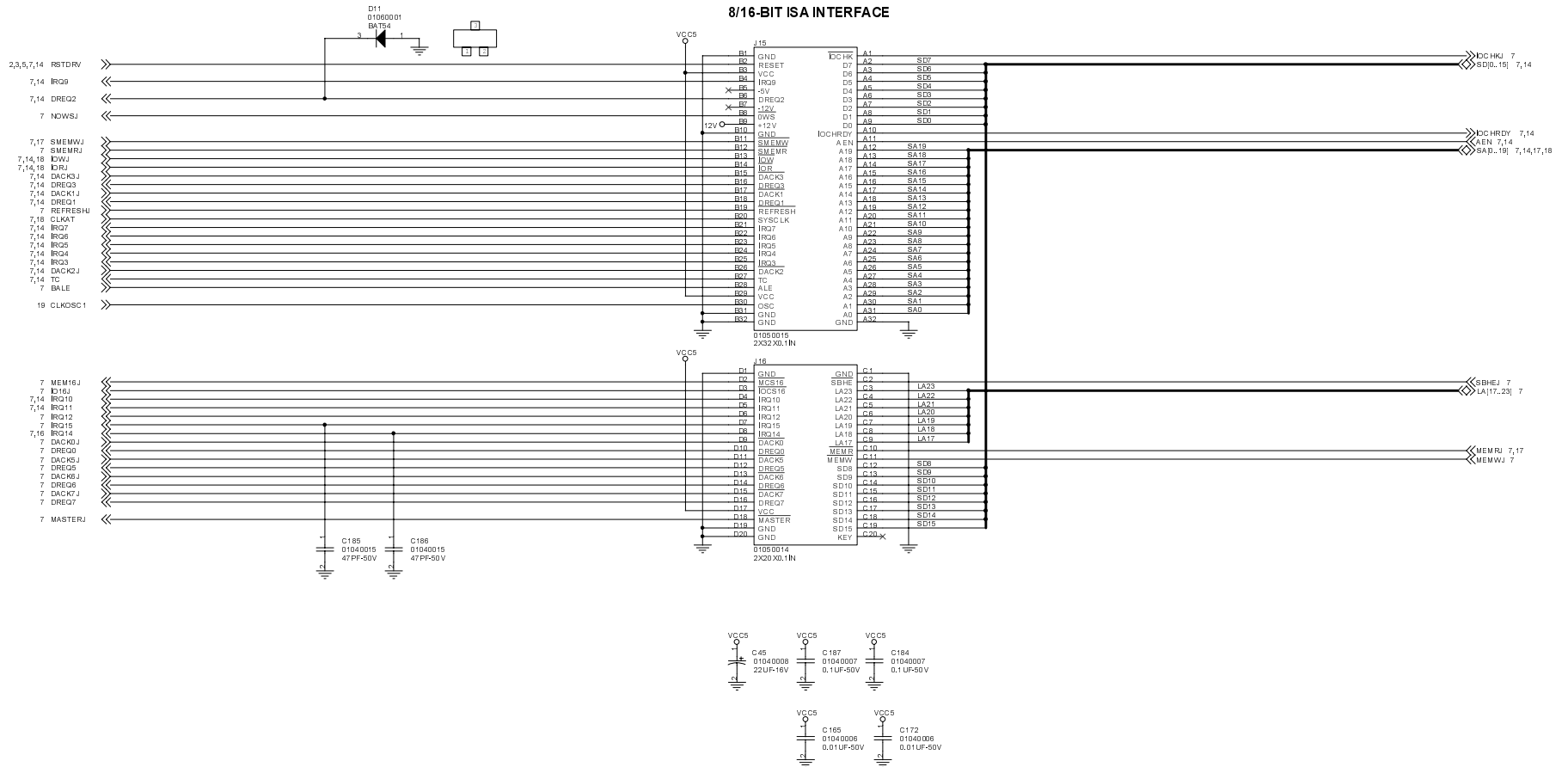
REFRESH  
KBCLK  
KBDATA  
ENRTC  
XBUSCS  
R1CAS  
SPEAK  
C.PUSPD  
C.PUCLK  
PCICLK  
OSC  
PWG  
ATCLK  
C.PURST  
SVSDST  
SYSRST

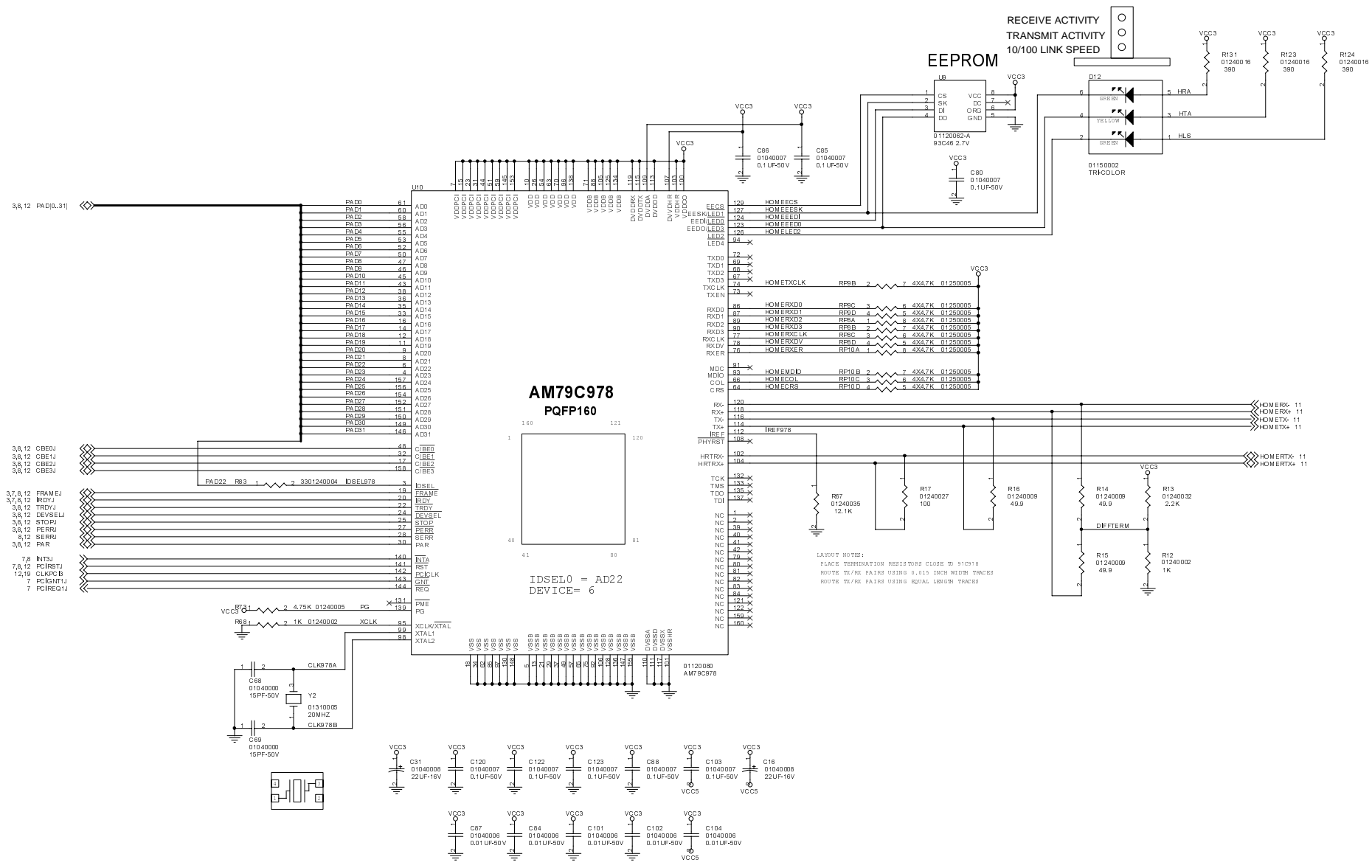


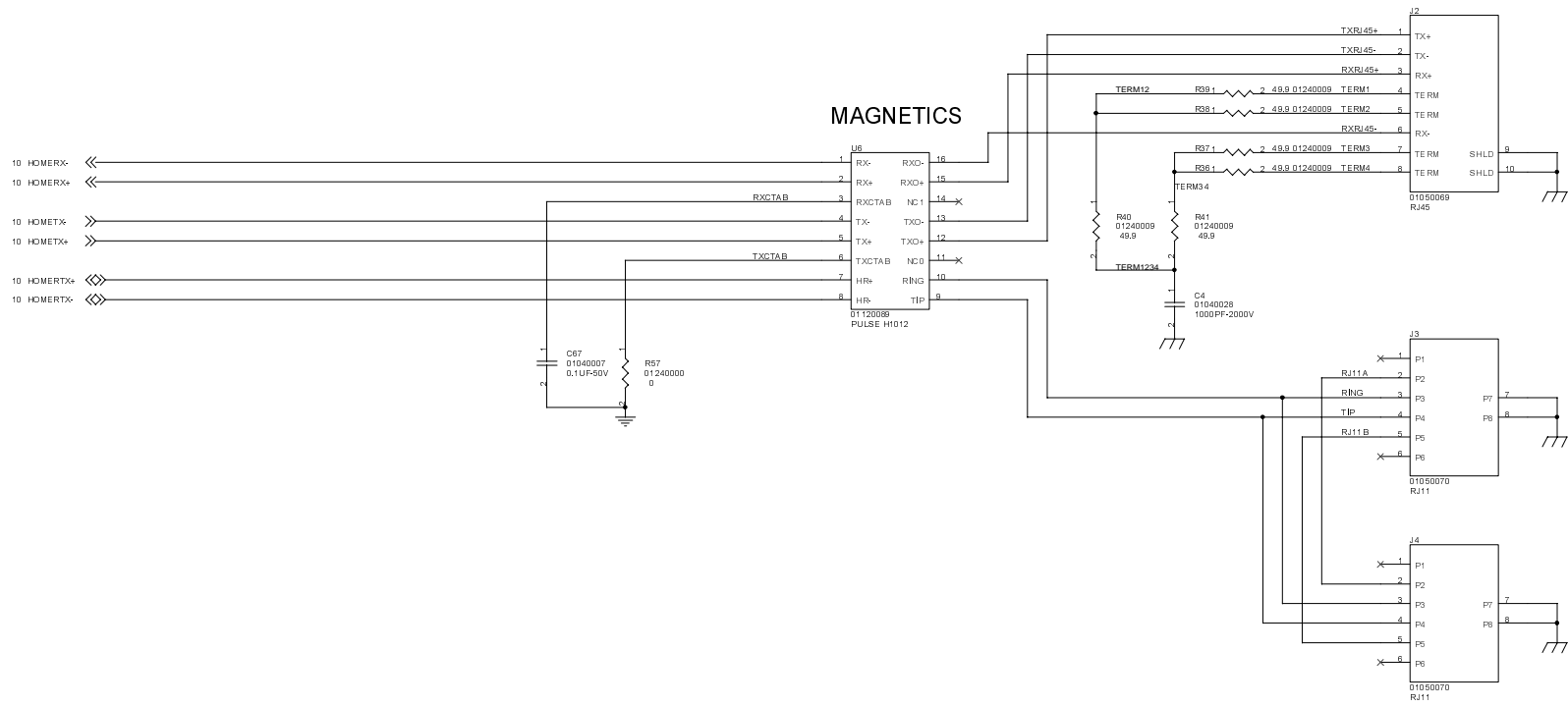




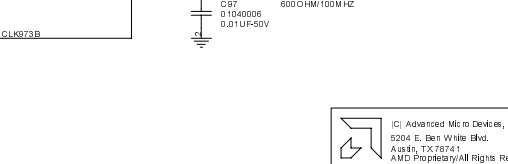
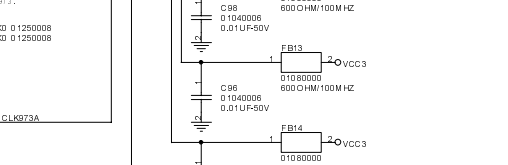
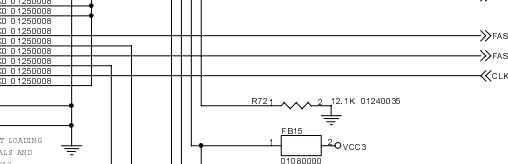
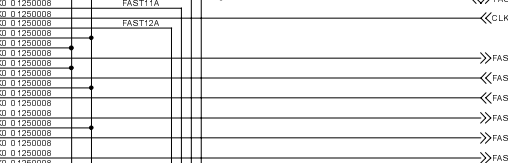
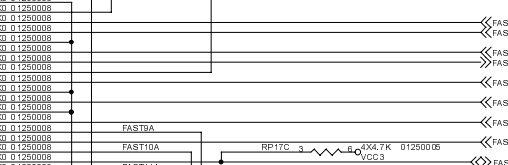
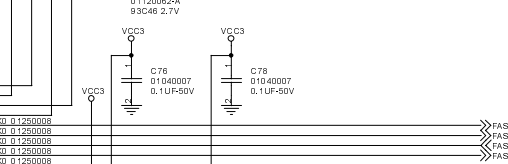
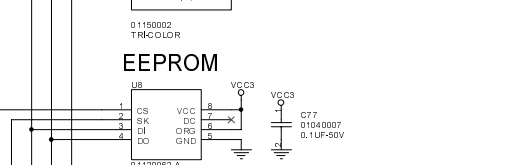
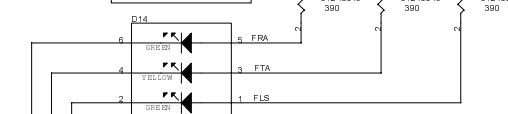
## PC/104 PLUS 8/16-BIT ISA INTERFACE



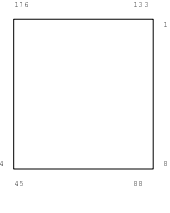




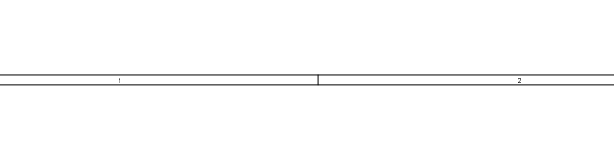
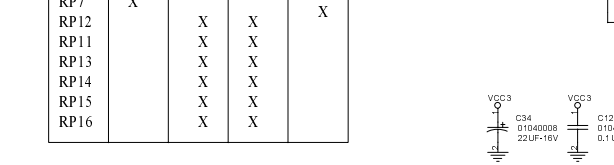
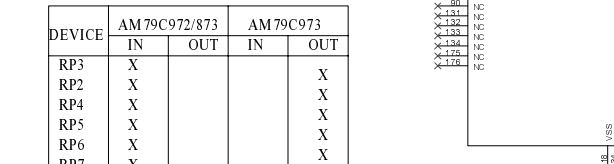
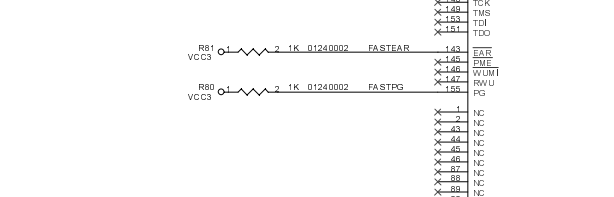
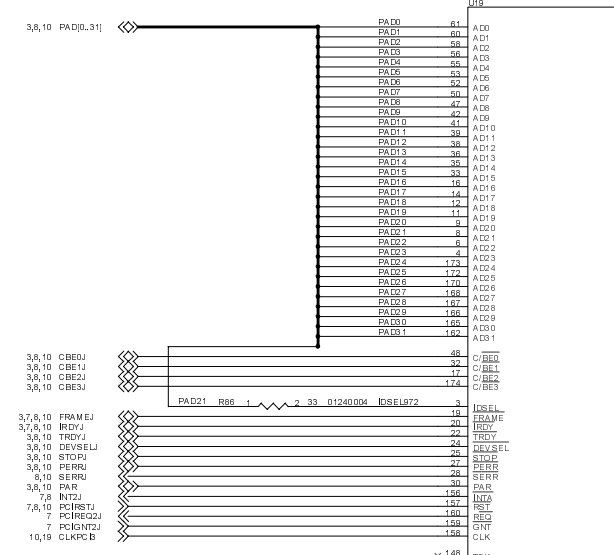
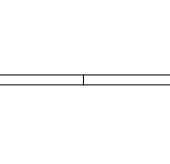
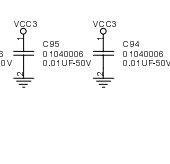
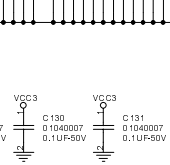
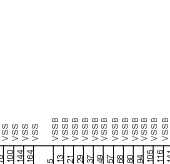
RECEIVE ACTIVITY  
TRANSMIT ACTIVITY  
10/100 LINK SPEED



### AM79C972/3 TQFP176



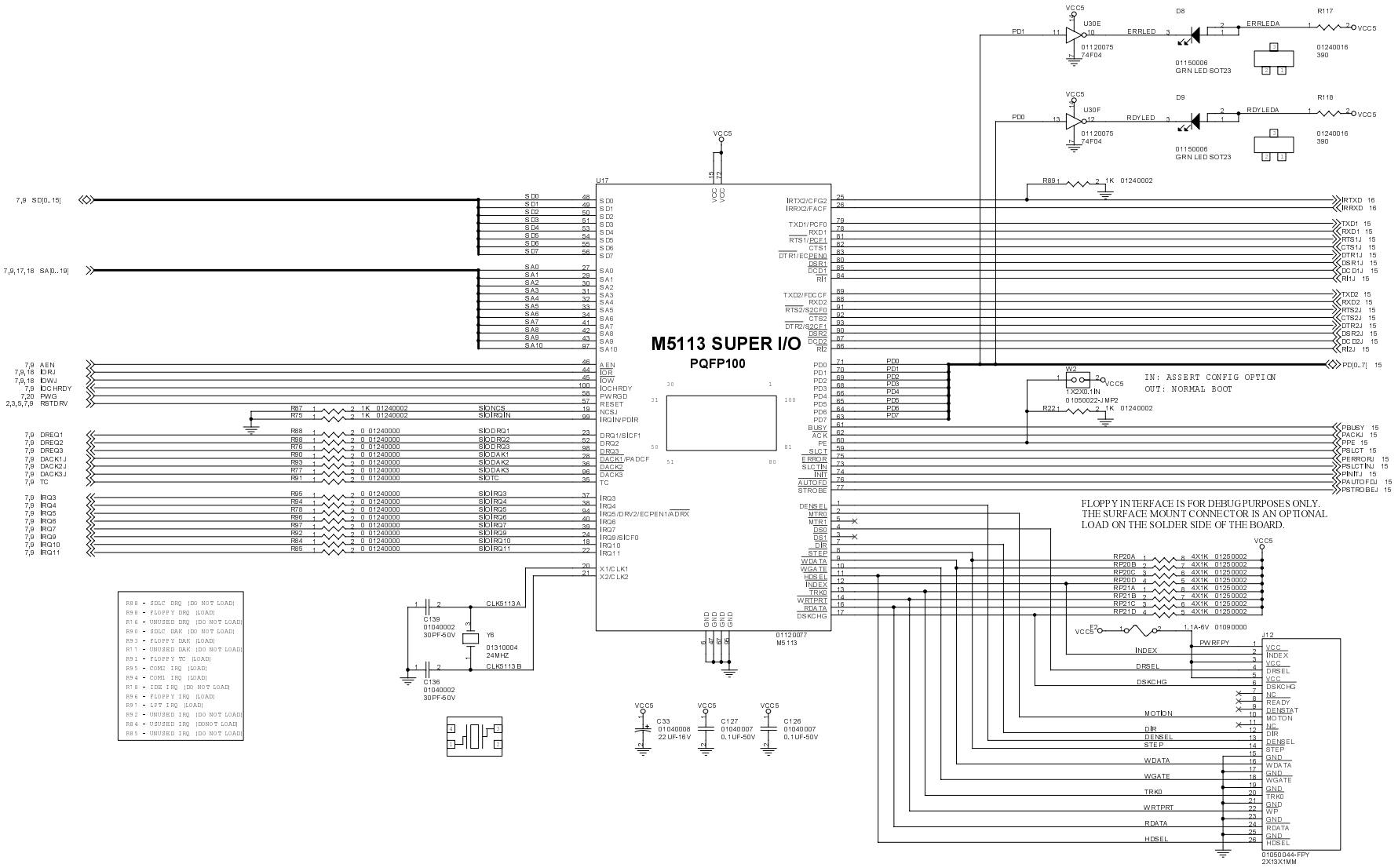
IDSELO = AD21  
DEVICE = 5



DEVICE	AM79C972/873		AM79C973	
	IN	OUT	IN	OUT
RP3	X			X
RP2	X			X
RP4	X			X
RP5	X			X
RP6	X			X
RP7	X			X
RP12		X	X	
RP11		X	X	
RP13		X	X	
RP14		X	X	
RP15		X	X	
RP16		X	X	

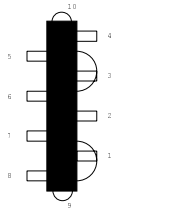
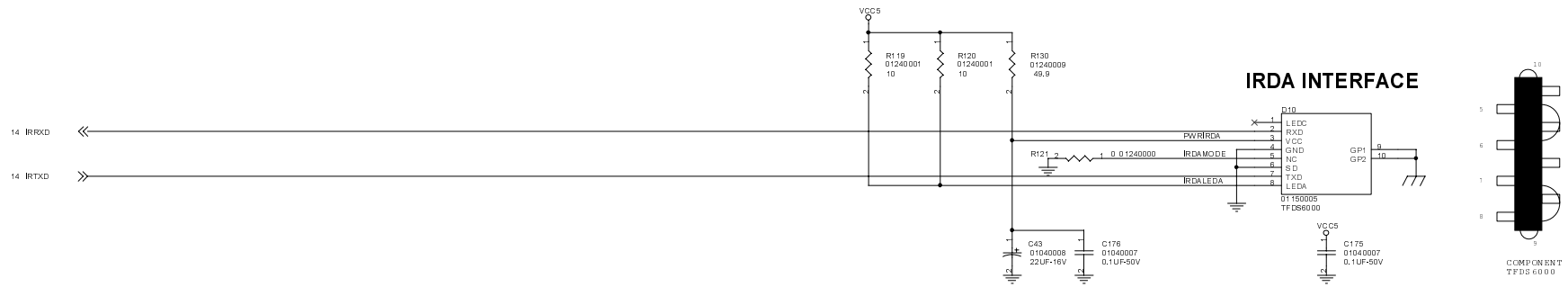
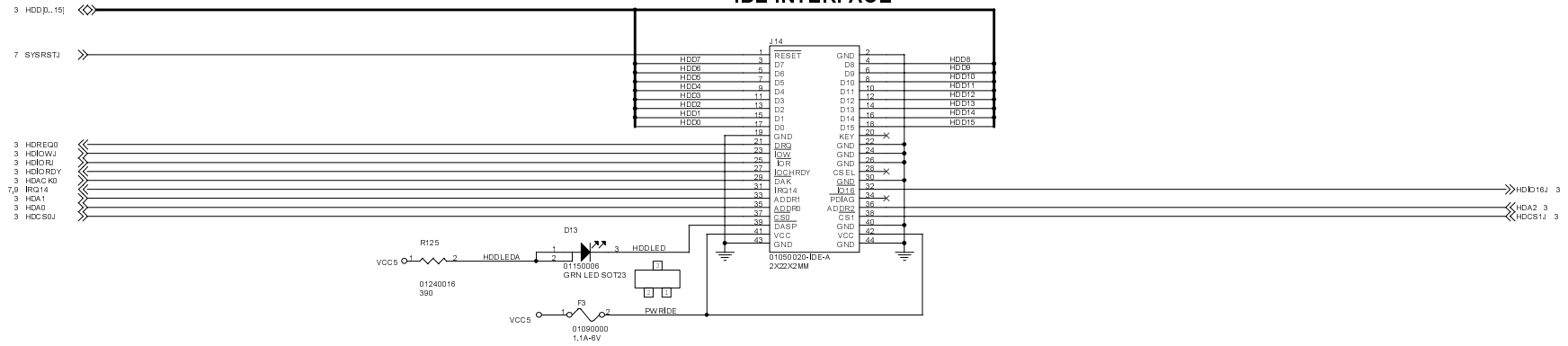


# STATUS LEDs





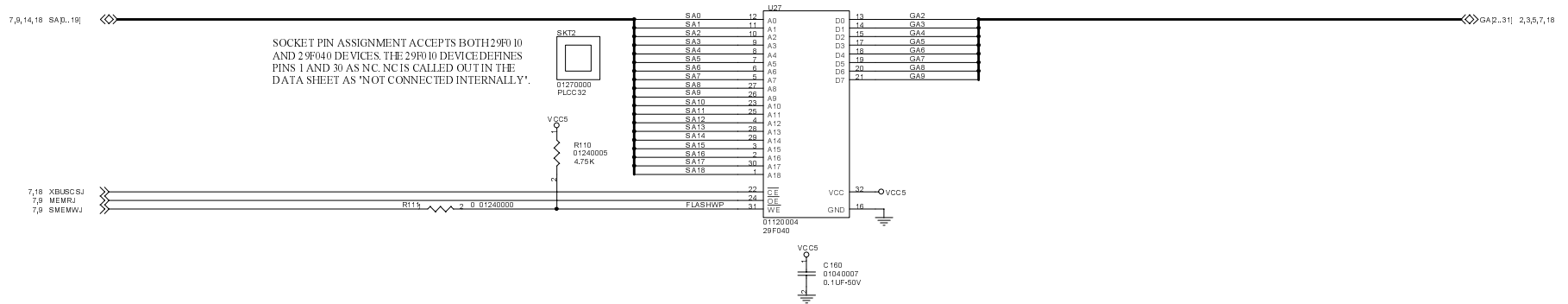
### IDE INTERFACE



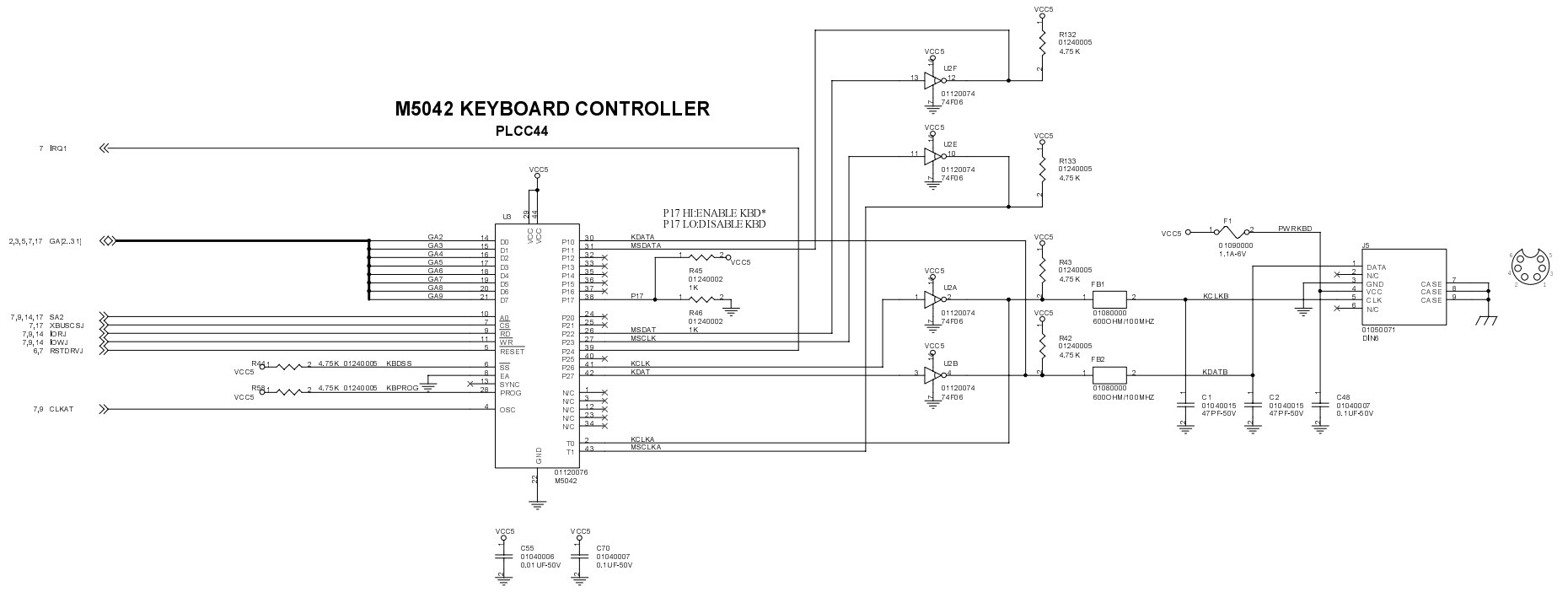
COMPONENT SIDE VIEW  
TFDS 6000



## BOOT FLASH SOCKET PLCC32

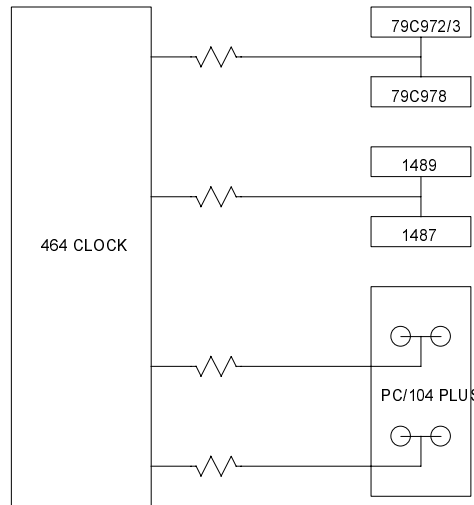
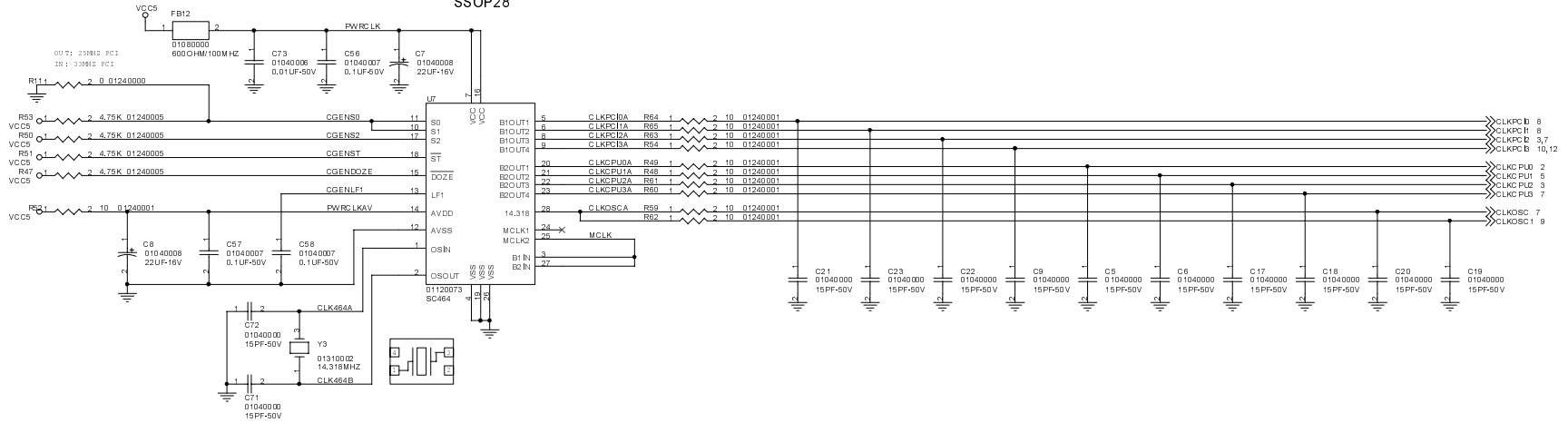


# M5042 KEYBOARD CONTROLLER PLCC44



# 464 CLOCK GENERATOR

SSOP28

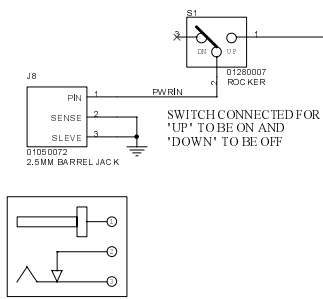


SOURCE	DESTINATION
CLKPCI0	PC/104 PLUS
CLKPCI1	PC/104 PLUS
CLKPCI2	PC/104 PLUS
CLKPCI3	M1489
CLKCPU0	M1487
CLKCPU1	AM97C978
CLKCPU2	AM97C972/973
CLKCPU3	AM486
	ExIP CONTROL
	M1489
	M1487

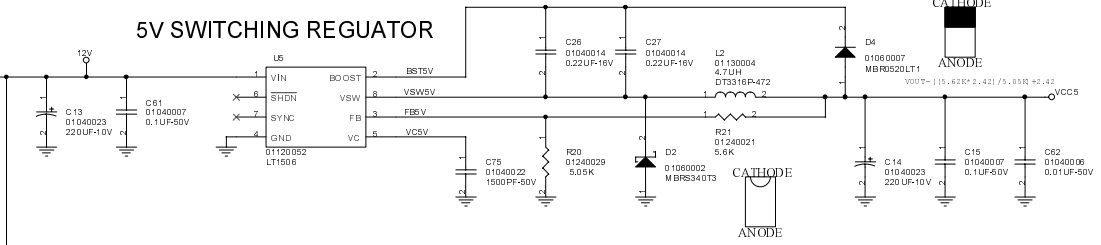
PCI CLOCK ROUTING ARCHITECTURE. FOR EACH CLOCK, THE DISTANCE FROM THE "T" TO THE DESTINATION SHOULD BE THE SAME. FOR ALL CLOCKS, THE DISTANCE FROM THE THE 464 SOURCE TO ANY ONE DESTINATION SHOULD BE THE SAME.

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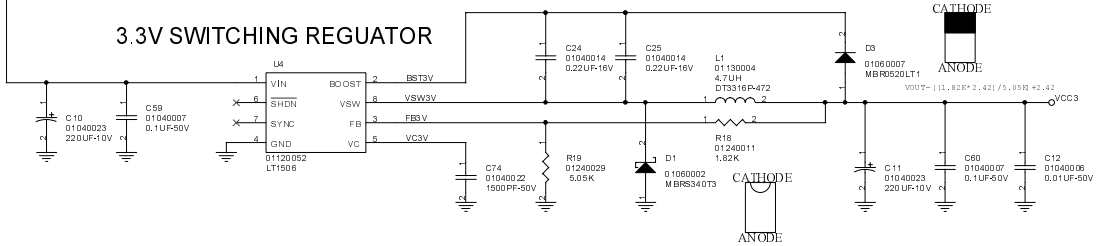
### POWER CONNECTOR AND SWITCH



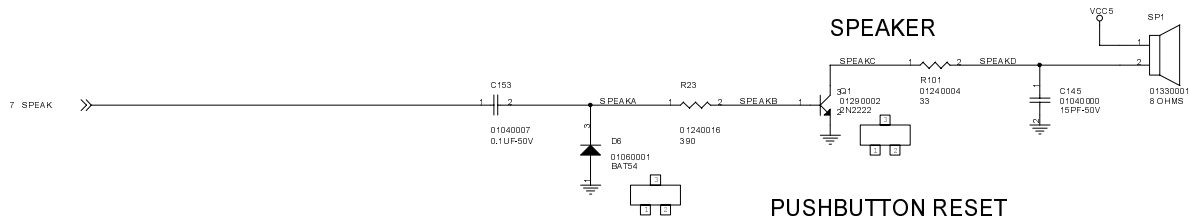
### 5V SWITCHING REGULATOR



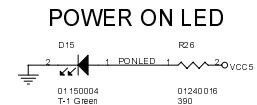
### 3.3V SWITCHING REGULATOR



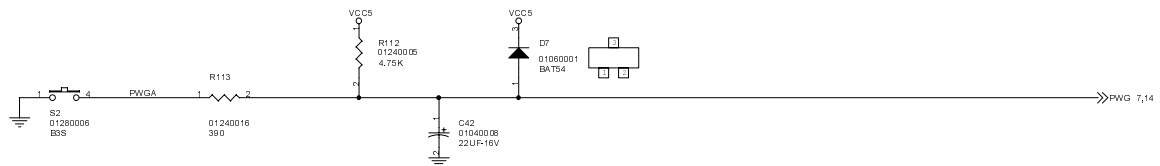
### SPEAKER



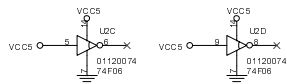
### POWER ON LED



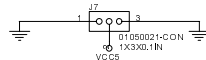
### PUSHBUTTON RESET



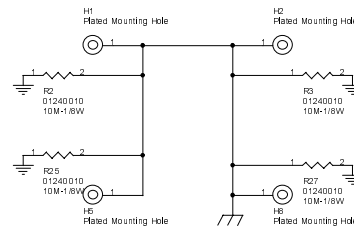
### SPARE GATES



### + 5V POWER



### SHIELD GROUND



REFER TO LAYOUT NOTES FOR LOCATION OF BOARD MOUNTING HOLES. HOLES ARE PLATED AND TAGGED INTO THE FRAME GROUND SHIELD. HOLES ARE 0.125 INCH DIAMETER WITH A 0.250 INCH PAD. LOCATE GROUND BRIDGE RESISTOR AT EACH HOLE.

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Title	NET-498		
Size	Document Number	Power	Rev 01
Date	Friday, May 21, 1999	Sheet	20 of 20