

# Am9511A

Arithmetic Processor

MILITARY INFORMATION

Am9511A

## DISTINCTIVE CHARACTERISTICS

- 2 and 3 MHz operation; fixed point 16-bit and 32-bit operations
- Floating point 32-bit operations; binary data formats
- Add, Subtract, Multiply and Divide; trigonometric and inverse trigonometric functions
- Square roots, logarithms, exponentiation; float-to-fixed fixed-to-float conversions
- Stack-oriented operand storage; DMA or programmed I/O data transfers
- End signal simplifies concurrent processing; Synchronous/Asynchronous operations
- General purpose 8-bit data bus interface; standard 24-pin package

## GENERAL DESCRIPTION

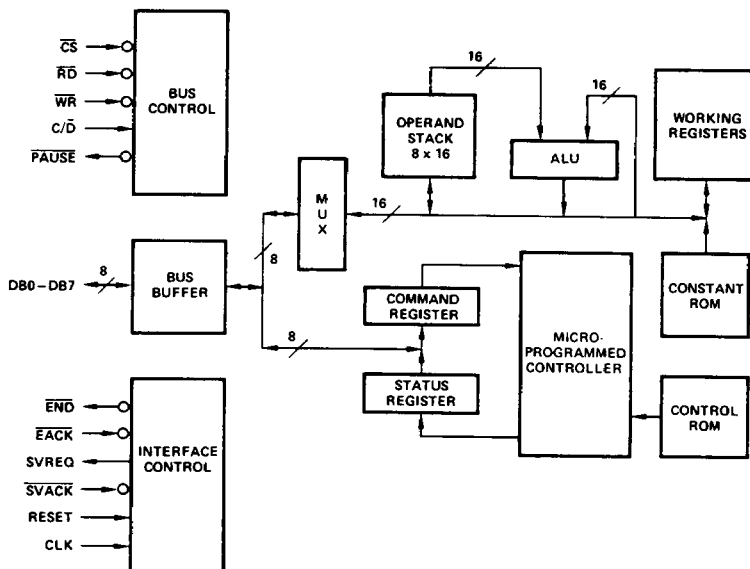
The Am9511A Arithmetic Processing Unit (APU) is a monolithic MOS/LSI device that provides high-performance fixed and floating point arithmetic and a variety of floating point trigonometric and mathematical operations. It may be used to enhance the computational capability of a wide variety of processor-oriented systems.

All transfers, including operand, result, status, and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack, and a command is issued to perform operations on the data in

the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end-of-execution signal that may be used as an interrupt by the CPU to help coordinate program execution.

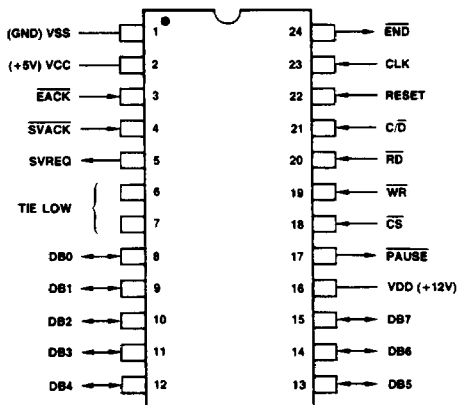
## BLOCK DIAGRAM



BD003340

Publication #	Rev.	Amendment
09224	A	/0
Issue Date: December 1987		

**CONNECTION DIAGRAM  
Top View**



CD005172

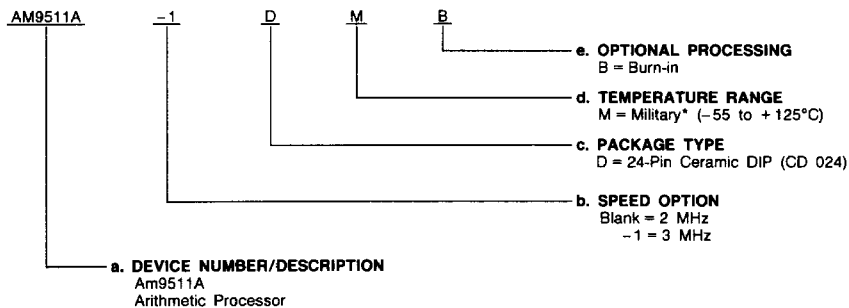
Note: Pin 1 is marked for orientation.

**MILITARY ORDERING INFORMATION**

**NPL Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9511A	DMB
AM9511A-1	

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

\*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65 to +150°C
V <sub>DD</sub> with Respect to V <sub>SS</sub> .....	-0.5 V to +15.0 V
V <sub>CC</sub> with Respect to V <sub>SS</sub> .....	-0.5 V to +7.0 V
All Signal Voltages with Respect to V <sub>SS</sub> .....	-5.0 V to +7.0 V
Power Dissipation (Package Limitation) .....	2.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Military (M) Devices	
Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	5 V ±10%
(V <sub>DD</sub> ) .....	12 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating range

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -200 μA	3.7		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 3.2 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage			V <sub>CC</sub> *	V
V <sub>IL</sub>	Input LOW Voltage			0.8	V
I <sub>Ix</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		±10	μA
I <sub>OZ</sub>	Data Bus Leakage	V <sub>O</sub> = 0.4 V	10		μA
		V <sub>O</sub> =		10	
I <sub>CC</sub>	V <sub>CC</sub> Supply Current			100	mA

**CAPACITANCE**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C <sub>O</sub>	Output Capacitance	f <sub>C</sub> = 1.0 MHz, Inputs = 0 V		10*	pF
C <sub>I</sub>	Input Capacitance			8*	pF
C <sub>I/O</sub>	I/O Capacitance			12*	pF

\*Not tested; guaranteed by design.

**SWITCHING TEST INPUT WAVEFORM**

WF004060

## SWITCHING CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Am9511A		Am9511A-1		Unit	
		Min.	Max.	Min.	Max.		
TAPW	EACK LOW Pulse Width	100		75		ns	
TCDR	C/D to RD LOW Setup Time	0		0		ns	
TCDW	C/D to WR LOW Setup Time	0		0		ns	
TCPH	Clock Pulse HIGH Width	200		140		ns	
TCPL	Clock Pulse LOW Width	240		160		ns	
TCSR	CS LOW to RD LOW Setup Time	0		0		ns	
TCSW	CS LOW to WR LOW Setup Time	0		0		ns	
TCY	Clock Period	480	5000	320	3300	ns	
TDW	Data Bus Stable to WR HIGH Setup Time	150		150		ns	
TEAE	EACK LOW to END HIGH Delay		20		175	ns	
TEPW	END LOW Pulse Width (Note 4)	400		270		ns	
TOP	Data Bus Output Valid to PAUSE HIGH Delay	0		0		ns	
TPPWR	PAUSE LOW Pulse Width Read (Note 5)	Data	3.5TCY + 50	5.5TCY + 300	3.5TCY + 50	5.5TCY + 200	ns
		Status	1.5TCY + 50	3.5TCY + 300	1.5TCY + 50	3.5TCY + 200	
TPPWW	PAUSE LOW Pulse Width Write (Note 8)		50		50	ns	
TPR	PAUSE HIGH to RD HIGH Hold Time	0		0		ns	
TPW	PAUSE HIGH to WR HIGH Hold Time	0		0		ns	
TRCD	RD HIGH to C/D Hold Time	0		0		ns	
TRCS	RD HIGH to CS HIGH Hold Time	0		0		ns	
TRO	RD LOW to Data Bus ON Delay	50		50		ns	
TRP	RD LOW to PAUSE Delay (Note 6)		150		150	ns	
TRZ	RD HIGH to Data Bus OFF Delay	50	200	50	150	ns	
TSAPW	SVACK LOW Pulse Width	100		75		ns	
TSAR	SVACK LOW to SVREQ LOW Delay		300		200	ns	
TWCD	WR HIGH to C/D Hold Time	60		30		ns	
TWCS	WR HIGH to CS HIGH Hold Time	60		30		ns	
TWD	WR HIGH to Data Bus Hold Time	20		20		ns	
TWI	Write Inactive Time	Command	4TCY		4TCY	ns	
		Data	5TCY		5TCY		
TWP	WR LOW to PAUSE LOW Delay (Note 6)		150		150	ns	

- Notes: 1. Typical values are for  $T_A = 25^\circ\text{C}$ , nominal supply voltages and nominal processing parameters.  
2. Switching parameters are listed in alphabetical order.  
3. Test conditions assume transition times of 20 ns or less, output loading of one TTL gate plus 100 pF  $\pm$  20 pF and timing reference levels of 0.8 V and 2.0 V.  
4. END low pulse width is specified for EACK tied to  $V_{SS}$ . Otherwise TEAE applies.  
5. Minimum values shown assume no previously entered command is being executed for the data access. If a previously entered command is being executed, PAUSE LOW Pulse Width is the time to complete execution plus the time shown. Status may be read at any time without exceeding the time shown.  
6. PAUSE is pulled low for both command and data operations.  
7. TEX is the execution time of the current command (see the Command Execution Times table).  
8. PAUSE low pulse width is less than 50 ns when writing into the data port or the control port as long as the duty requirement (TWI) is observed and no previous command is being executed. TWI may be safely violated up to 500 ns as long as the extended TPPWW that results is observed. If a previously entered command is being executed, PAUSE LOW Pulse Width is the time to complete execution plus the time shown.

CHAPTER 6

General Information

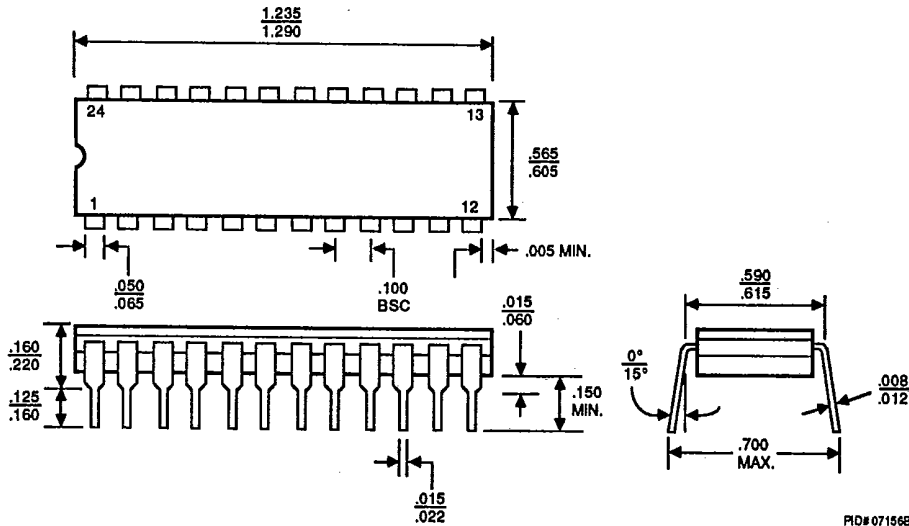


T-90-20

PACKAGE OUTLINES\*

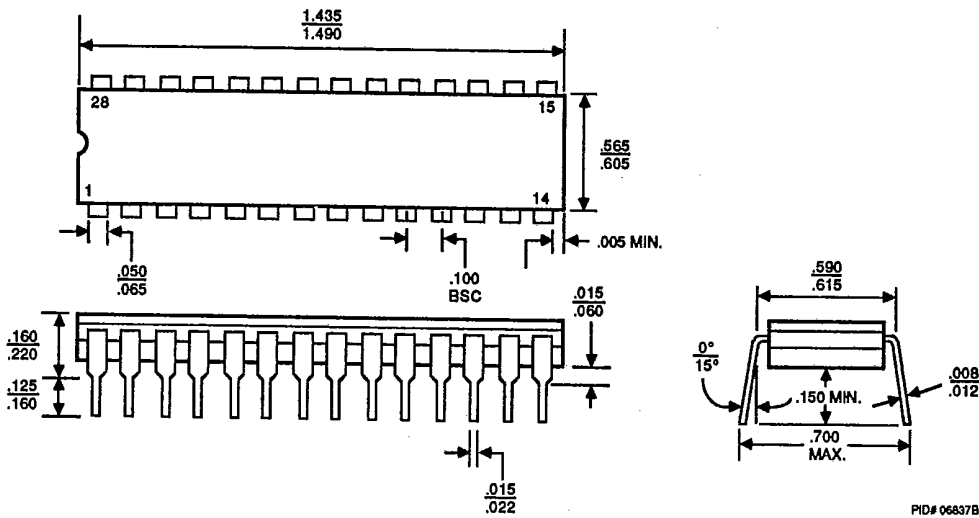
Ceramic DIPs (CD)

CD 024



PID# 07156B

CD 028



PID# 06837B

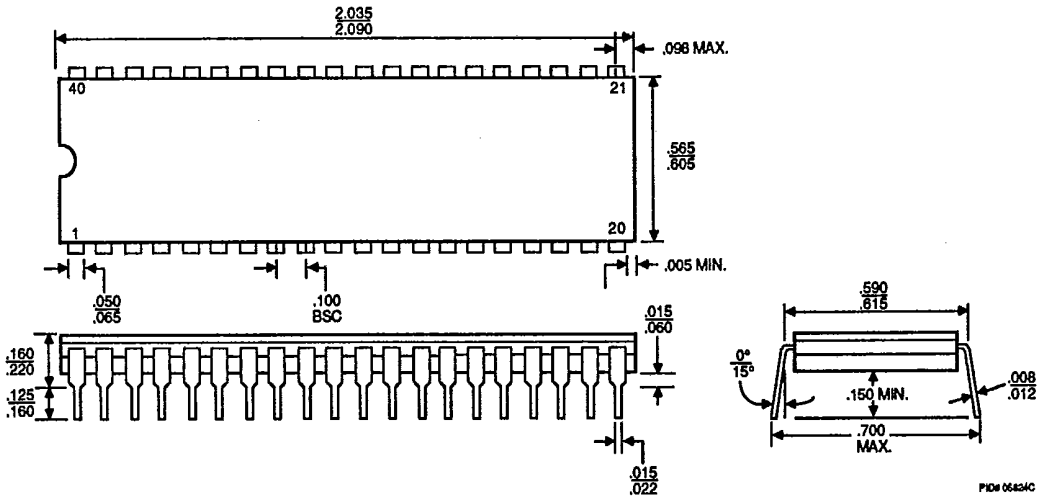
\* For reference only.

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

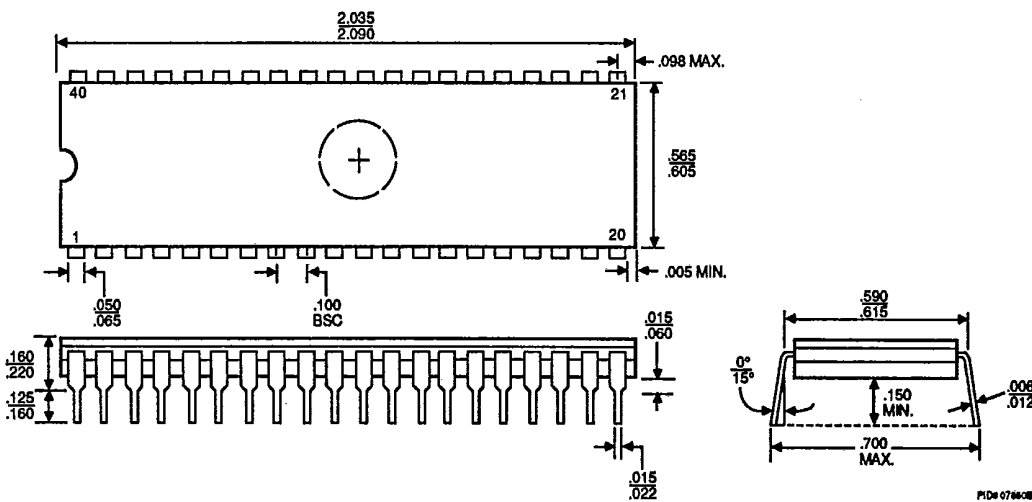
PACKAGE OUTLINES (Continued)

Ceramic DIPs (CD) (Continued)

CD 040



CDV040



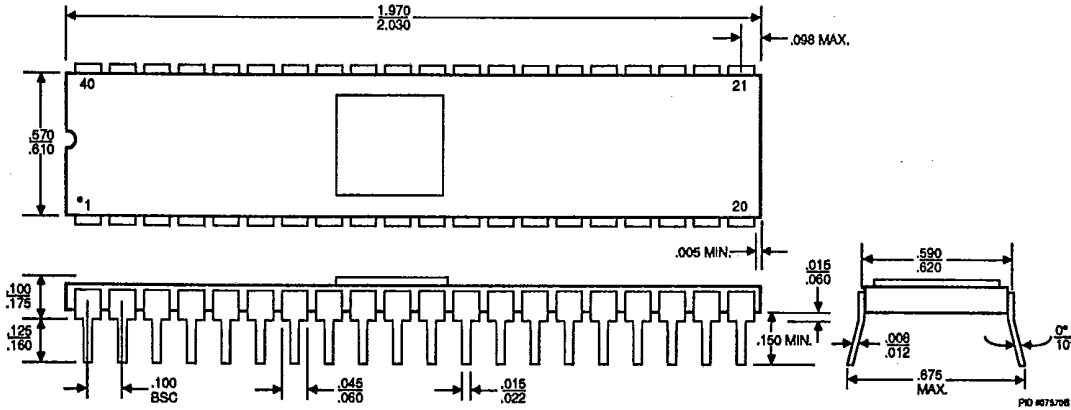
NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

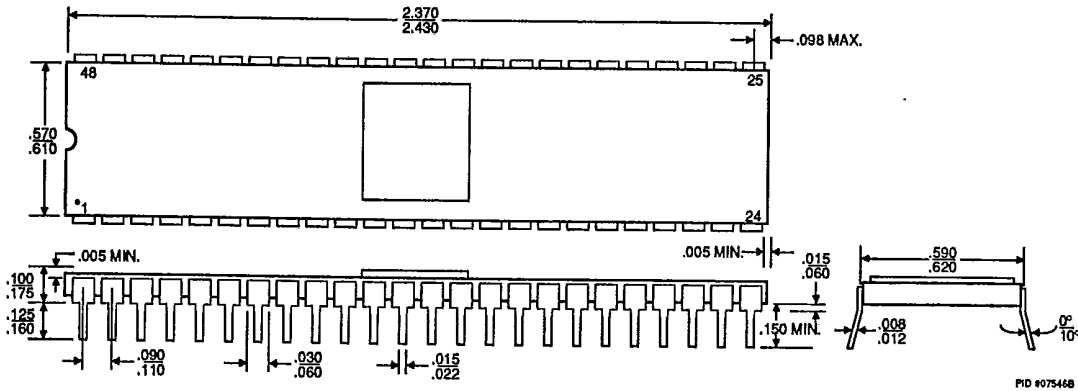
T-90-20

Ceramic Sidebraced DIPs (SD)

SD 040

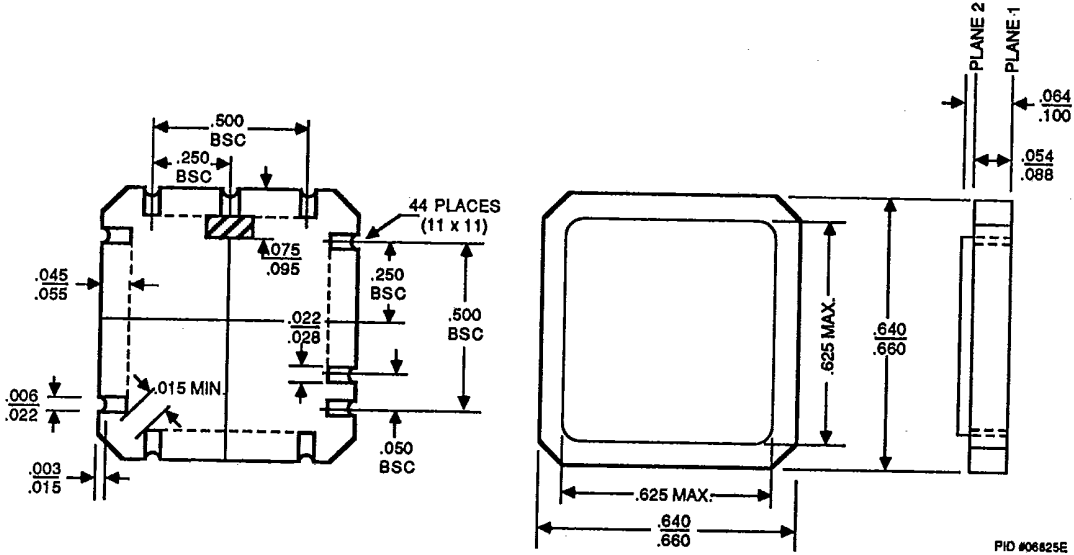


SD 048

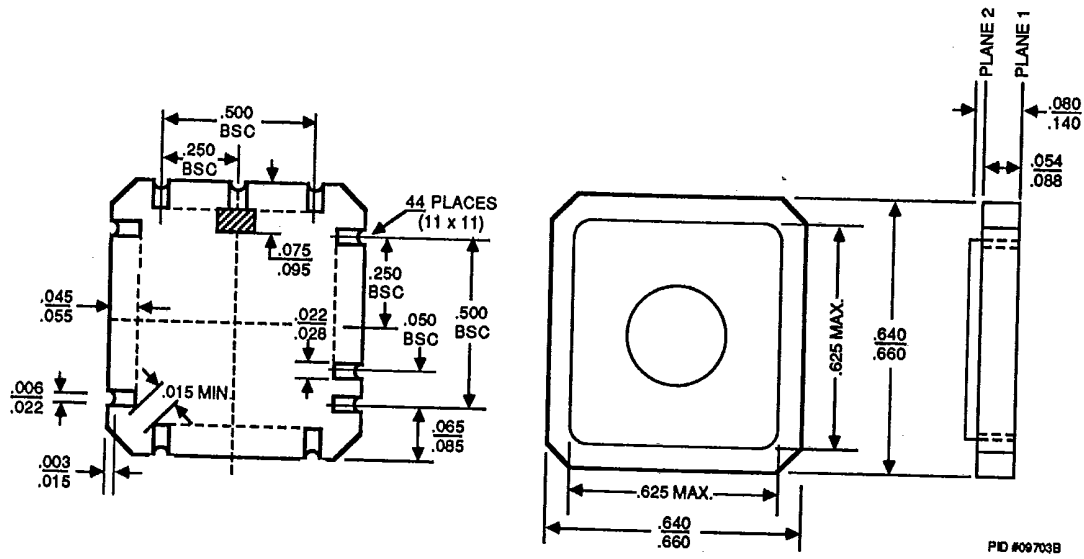


NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

**PACKAGE OUTLINES (Continued)**  
**Ceramic Leadless Chip Carriers (CL/CLV)**  
**CL 044**



**CLV044**

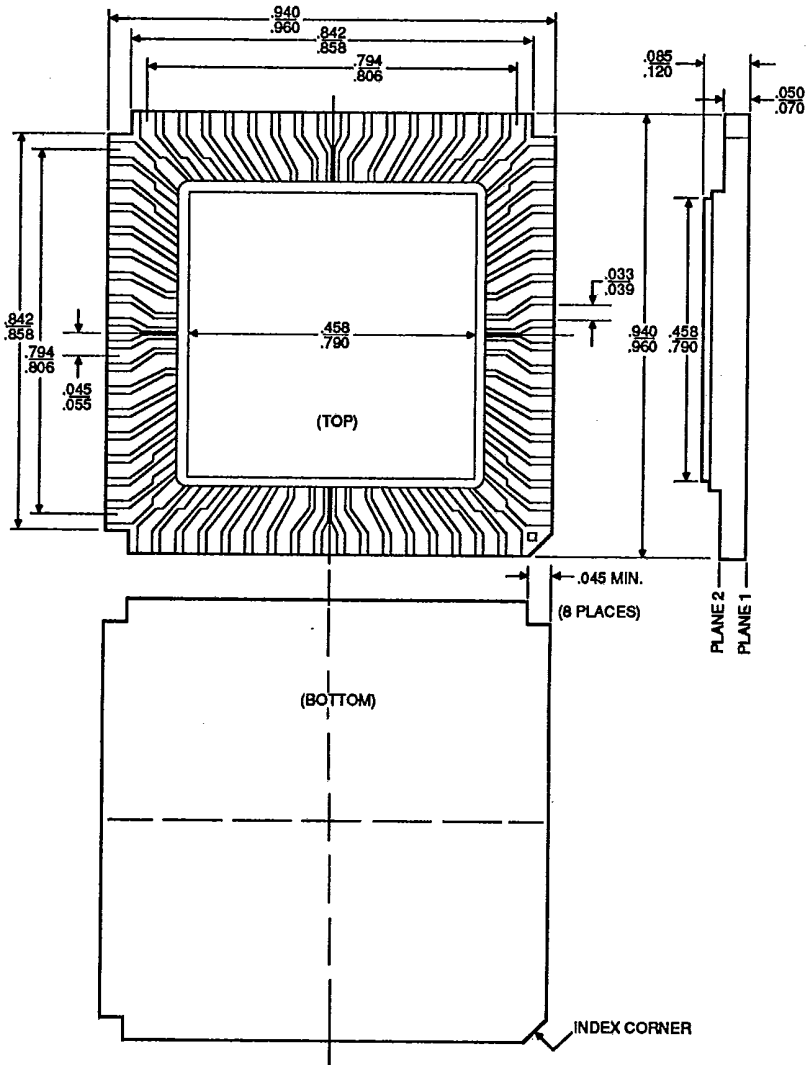


NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.



PACKAGE OUTLINES (Continued)

68-Pin Square Leadless Chip Carrier (CA2)  
CA2068

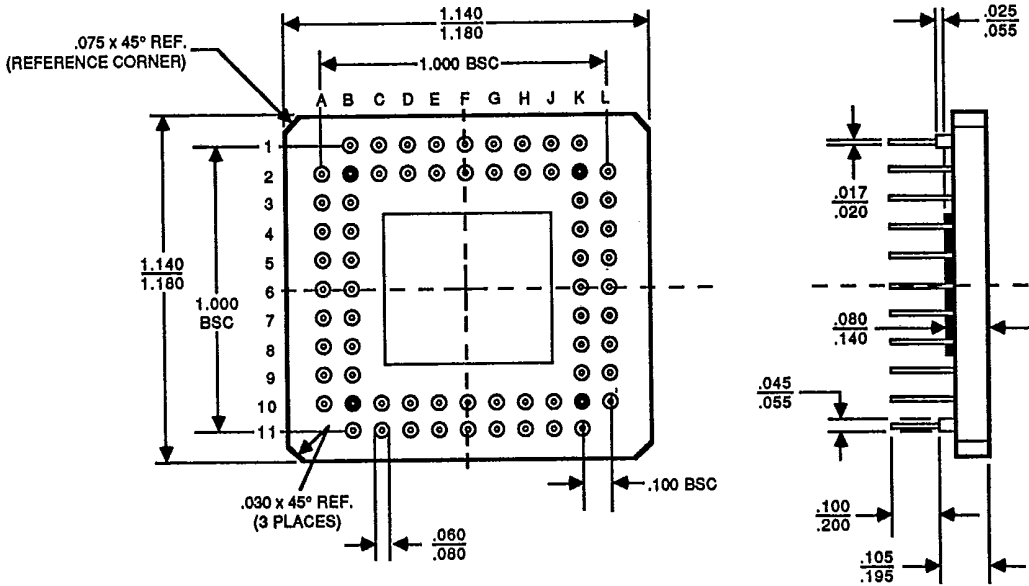


PID #07287B

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

**PACKAGE OUTLINES (Continued)**  
**Ceramic Pin-Grid-Array Package (CG/CGX)**  
**CGX068**

**BOTTOM VIEW**



PID # 07547B

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.