ÉlanSC300 Microcontroller
Evaluation Board
User's Manual

ÉlanSC300 Microcontroller Evaluation Board, Revision 1.1

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About the ÉlanSC300 Microcontroller Evaluation Board

Congratulations on your decision to design with the ÉlanSC300 microcontroller! This sophisticated, integrated device is uniquely suited to meet the needs of the next generation of handheld devices. From its high integration to PC/AT compatibility to remarkable power management, the ÉlanSC300 microcontroller is the ideal device to enable compact, fully functional, battery-powered designs with a quick time to market.

The ÉlanSC300 microcontroller evaluation board has been provided as a test and development platform for ÉlanSC300 microcontroller-based designs. Most of the possible options and features of the ÉlanSC300 microcontroller can be exercised on this board. Since there are numerous options available, this board is a much larger form factor than could be achieved with a dedicated set of features. Refer to "Schematics" on page D-1 for more realistic system design reference examples. This evaluation board is provided as a reference only and should only be used to experiment with the design trade-offs of the ÉlanSC300 microcontroller, make power measurements, and develop operating and application software.

NOTE: Advanced Micro Devices does not assume any responsibility for the maintenance of this evaluation tool. Changes to the schematics will only be made if the board is required to go back through a CAD layout.

Refer to the *ÉlanSC300 Microcontroller Data Sheet* and the *ÉlanSC300 Microcontroller Programmer's Reference Manual* for detailed information on the ÉlanSC300 microcontroller.

Features

External Connectors

- Two serial port connections
  - One internal ÉlanSC300 16C450-compatible port (COM1 or COM2 configurable)
  - One Super I/O 16C550-compatible port (COM1 through COM4 configurable)
- One parallel port connection from the ÉlanSC300 microcontroller
- Four PCMCIA 2.1-compliant sockets (jumper configurable for buffered or unbuffered socket pairs)
- Two 16-bit ISA slots (for evaluation of ISA-based devices only)
- One IDE connector (connected to the ÉlanSC300 ISA bus)
- One floppy-drive connector (connected to the Super I/O floppy-drive controller)
- One AT-style keyboard connector (connected to the 8042 keyboard controller)
- One PS/2-style mouse connector (connected to the 8042 keyboard controller)
- One 20-pin Berg strip for LCD connection (note this is not a standard connector and will require the user to adapt the cable depending on the LCD display used)

Main Memory Configurations

- DRAM
  - 512 Kbyte, 1 Mbyte, 2 Mbyte, 4 Mbyte, 8 Mbyte and 16 Mbyte DRAM configurations supported
  - 3-V or 5-V DRAM support
  - Four standard 30-pin DRAM SIMM sockets
  - One standard, 72-pin DRAM, 16-bit SIMM socket (can be used instead of the 30-pin sockets)
- SRAM
  - Four 32-pin DIP SRAM sockets for 512Kx8 SRAM modules
  - 1 Mbyte (2 socket) or 2 Mbyte (4 socket) configurations supported

Power Management

- Power planes are isolated and jumpers are provided to measure current consumption. The CPU voltage sources are: V_{CC}, V_{CCMEM}, V_{CCSYS}, V_{CCSYS2}, V_{CC5}, V_{CC1}, A_{VCC}
- Suspend/Resume button provided (note that BIOS' enable the suspend/resume function)
- MicroPower Off button provided for testing
- DIP switch for transitioning battery-low and ACIN pins for testing

Bus Modes

- Full ISA mode (full 16-bit ISA bus support)
- Local Bus mode (16-bit bus support for high speed video)
- Internal Video mode (LCD connector provided with negative contrast voltage—depending on LCD panel used, a separate circuit for contrast and bias voltage may need to be provided)

PCMCIA

- Two pairs of buffered/unbuffered PCMCIA sockets are provided (a jumper option selects which sockets are used)
- Support for 5-V cards
- Support for programming 12-V Flash cards
- Both Phoenix PicoCard and SystemSoft CardSoft card and socket services are provided on the evaluation diskettes

BIOS ROM

- Two 32-pin DIP sockets are provided to allow for BIOS ROMs (which socket is enabled is selected via JP32)
- Either a 128Kx8 or 256Kx8 EPROM/Flash is supported (AMD's 27C010 or 27C020 EPROM, and AMD's 12-V 28F010, 5-V 29F010, 12-V 28F020, or 12-V 28F020A Flash are recommended)
- 12-V programming voltage is available
- Evaluation copies of PhoenixPICO BIOS and SystemSoft BIOS are provided in the sockets of the evaluation board

Application ROM (DOS ROM)

- Four 32-pin DIP sockets are provided for application ROM space
- 256Kx8 or 512Kx8 EPROM/ROM devices are supported (AMD's 27C020 or 27C040 are recommended)
- 256Kx8 Flash devices are supported (AMD's 12-V 28F020 or 12-V 28F020A Flash are recommended)

  NOTE: 512Kx8 Flash can be supported after a minor board rework. Contact your local AMD or distributor Field Application Engineer for more information.
- Application ROM space is 16-bits wide (two or four devices must be used)
- 12-V programming voltage is available
- Datalight ROM-DOS mini-SDK (software developer's kit) is provided with the evaluation kit

Debugging

- Headers for all 208 signals on the ÉlanSC300 microcontroller
- Supports DOS Soft ICE tools and ROM ICE tools
- Support for standard x86 application debugging tools

OS Support

- Compatible with standard 32-bit operating systems
- DOS, WinLight, Windows 3.1, GEOS, QNX

Chapter 1

Quick Start

This chapter provides information that helps you quickly set up and start using the ÉlanSC300 microcontroller evaluation board.

The ÉlanSC300 microcontroller evaluation board is shipped with evaluation BIOS' from Phoenix and SystemSoft, which have been configured specifically for this board. (A jumper, JP32, selects which BIOS is used at power-up.) The BIOS contains the code which allows the ÉlanSC300 microcontroller evaluation board to function just like a standard AT-compatible PC. The ÉlanSC300 microcontroller evaluation board can boot from standard AT-compatible diskettes and can use AT-compatible displays, display adapters and keyboards.

This chapter describes how to set up the ÉlanSC300 microcontroller evaluation board in Full ISA Bus mode and boot DOS from a diskette. In this mode, the Trident ISA bus VGA card is used to drive a common video monitor.

The end of the chapter explains how to connect an IDE hard drive to configure your ÉlanSC300 microcontroller evaluation board to operate like a standard 386 desktop computer.

Booting DOS From a Diskette

CAUTION: As with all computer equipment, the ÉlanSC300 microcontroller evaluation board may be damaged by electrostatic discharge (ESD). Please take proper ESD precautions when handling any board.

Warning: Read before using this evaluation board

Before applying power, the following precautions should be taken to avoid damage or misuse of the board:

- Make sure power supply connectors (from a standard AT system power supply) are plugged onto the board correctly. The grounds (usually black wires) should meet at the center of the two power supply connectors on the board.
- See "Board Layout" on page 2-3 for important information.
- See appendix B for a list of peripherals that have been used to test the evaluation board prior to shipping.

The following documents are updated on an ongoing basis and contain important errata information regarding the evaluation board.

- The Evaluation Board Errata document discusses hardware issues pertaining to the evaluation board.The current version is shipped with the kit; contact your local AMD representative for any updates.
- The BIOS Errata document discusses software issues pertaining to the Phoenix and SystemSoft BIOS' that are shipped with your evaluation board. This document is available through your local AMD representative.

1.1

Installation Requirements

First you need the following from the ÉlanSC300 microcontroller evaluation board kit:

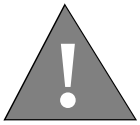
- ÉlanSC300 microcontroller evaluation board
- VGA display adapter

You need to provide the following items (see the appendix “Verified Peripherals” on page B-1 for a list of peripherals that are known to work with the ÉlanSC300 microcontroller evaluation board):

- An AT-compatible 3.5" disk drive
- A standard 34-wire AT disk-drive cable
- A VGA monitor
- A cable to connect the VGA monitor to the VGA display adapter
- An AT-compatible keyboard
- A standard PC power supply (at least 230 watts)
- A bootable 3.5" DOS diskette

Board Installation

NOTE: See "ÉlanSC300 Microcontroller Evaluation Board" on page 2-2 for a layout diagram of the board.



DANGER: Make sure the power supply and the VGA monitor are *not* plugged into an electrical outlet during the following steps.

1. Remove the board from the shipping carton. Visually inspect the board to verify that it was not damaged during shipment. The board contains several jumpers. The following steps assume all jumpers are in the factory default configuration.
2. Inspect the 34-wire disk-drive cable that you are providing. The red wire along one edge of the ribbon cable indicates wire 1. Connect one end of the 34-wire disk-drive cable to the disk drive just as you would for a standard PC installation. The disk-drive documentation should indicate where to put wire 1.

   Connect the other end of the 34-wire disk-drive cable to the 34-pin connector P27 on the ÉlanSC300 microcontroller evaluation board with wire 1 toward the ROM sockets.

3. Insert the VGA adapter into either of the ISA slots on the ÉlanSC300 microcontroller evaluation board. The ISA slots are labeled P21 and P22.
4. Connect the VGA monitor cable from the monitor to the D-connector at the end of the VGA display adapter just as you would for a standard PC.
5. Connect the keyboard to the keyboard connector at P10.
6. Connect the connectors marked P8 and P9 from the standard PC power supply into the board's power connectors at P25 and P26. P8 connects to P25 (the six pins closest to the corner of the board); P9 to the other six pins. (See Figure 2-1 on page 2-2 for the connector locations.) *Make sure the black ground wires from P8 and P9 meet in the middle of the board's P25 and P26 connectors.*

DANGER: Failure to verify and check the power supply connections may result in total destruction of the ÉlanSC300 microcontroller evaluation board.

7. Find one of the 4-wire power connectors from the PC power supply and attach it to the 4-pin connector on the disk drive just as you would for a standard PC installation. The disk-drive documentation should indicate the proper orientation of the power cable.
8. Insert the bootable DOS diskette (not included) in the disk drive.
9. Plug the VGA monitor into an electrical outlet.
10. Apply power to the ÉlanSC300 microcontroller evaluation board by connecting the PC power supply to an electrical outlet. If equipped, turn on the power-supply switch. The power supply fan should be operating. Press the black MicroPower Off button, SW5. The red LED should now be lit.
11. Press the red RESET button, SW2. You should see the BIOS boot message on the monitor. When booting after being powered off, the CMOS ROM is not configured and you need to use the BIOS setup utility to configure the system. Follow the instructions shown on the screen to enter the Setup utility. Once you are in the Setup utility, you can set the system's processor speed, date, time, and other options (see "SystemSoft BIOS Set-Up Screen Options" on page 2-7 or "PhoenixPICO BIOS Main Menu Setup Screen Options" on page 2-11).
12. Save and exit the setup utility.

    NOTE: The evaluation board does not have a battery backup. You need to run the setup utility each time the system is powered off.

13. The system should now boot from the DOS diskette just like a standard PC.

Table 1-1. Installation Troubleshooting

Problem	Solution
The board's power LED does not light when the power supply is turned on.	The black MicroPower Off button, SW5, needs to be pressed after power-up.
The board's power LED does not light even after the MicroPower Off button, SW5 is pressed.	Check power supply connections at P25 and P26.
The red power LED is on but I see nothing on the VGA monitor and do not hear any beeps from the speaker nor hear the head synchronization on the disk drive.	Ensure processor reset by pressing the red Reset button, SW2.
I hear a beep on the speaker but see nothing on the VGA monitor.	Check that the monitor has AC power. Check that the monitor is correctly connected to the VGA display adapter. Check that the display adapter is correctly seated in the ISA slot.
I get the startup message on the monitor but it says there's a CMOS checksum error and doesn't finish booting.	This is the normal condition after power-up. The ÉlanSC300 microcontroller evaluation board's CMOS RAM does not have battery backup. Follow the BIOS' instructions to run the Setup utility to configure the CMOS RAM. Once configured, the CMOS RAM can be saved by leaving the power supply on but using the MicroPower Off button, SW5, to power down the board.
I've configured the CMOS RAM but I don't hear any sound from the disk drive and the system does not boot from the diskette.	Check that the 34-wire cable to the disk drive is properly connected at both the disk-drive end and the board end (board connector P27). Check that the CMOS setup indicates that drive A is a 3.5" 1.44 Mbyte drive.
I hear the diskette being accessed but get an error message "Non System disk".	Check that the diskette in the drive is indeed bootable, just as you would on a standard PC.

Problem	Solution
I get a "Missing Keyboard" error message on the monitor during boot-up.	Check that keyboard is properly connected.
There is a problem you cannot resolve.	Contact the AMD Technical Support Hotline at 1-800-222-9323.

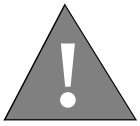
Connecting an IDE Hard Drive

This section describes how to connect an IDE hard drive to the ÉlanSC300 microcontroller evaluation board. You need to provide the following additional items:

- An IDE-compatible hard drive of size not more than 512 Mbyte. See the appendix “Verified Peripherals” on page B-1 for a list of hard drives that are known to work. Note that Connor and Fujitsu hard drives do not work with the ÉlanSC300 microcontroller evaluation board.
- A standard 40-wire AT IDE cable.

Assuming you have successfully booted to DOS from a disk drive as described in “Booting DOS From a Diskette” on page 1-2, do the following:

1. Disconnect power by unplugging the PC power supply from the AC outlet.



WARNING: If the PC power supply is on but the board has been put in a standby mode using the MicroPower Off button, there is still some power on the board. Completely unplug the power supply before continuing.

2. Inspect the 40-wire IDE cable that you are providing. The red wire along one edge of the ribbon cable indicates wire 1. Connect one end of the 40-wire IDE cable to the hard drive just as you would for a standard PC installation. The hard drive documentation should indicate where to put wire 1. Connect the other end of the 40-wire IDE cable to the 40-pin connector P28 on the ÉlanSC300 microcontroller evaluation board with wire 1 toward the ROM sockets.

3. Find one of the 4-wire power connectors from the PC power supply and attach it to the 4-pin connector on the hard drive just as you would for a standard PC installation. The hard drive documentation should indicate the proper orientation of the power cable.

4. Apply power to the ÉlanSC300 microcontroller evaluation board by connecting the PC power supply to an electrical outlet. Then press the black MicroPower Off button, SW5. The red LED should now be lit.

5. Press the red Reset button, SW2. You should see the BIOS boot message on the monitor. When booting after a power-up, the CMOS ROM is not configured and you need to use the BIOS setup utility. Follow the instructions shown on the monitor to enter the Setup utility.

6. In the BIOS setup utility, you need to configure Drive C for the proper number of heads, cylinders and sectors. (Some BIOS products have an AutoDetect feature that automatically detects this information; some require you enter this information manually.) You should be able to get these numbers from your hard drive documentation. Follow the prompts to save this configuration and exit the BIOS setup utility.

7. Whether or not your hard drive contains an already installed bootable disk image (written from some other PC), you should still keep your bootable diskette in the A drive and boot from that. After you boot properly from A, try to do a directory listing of C. If the directory listing of C works, you can try removing the diskette from A and booting from C (Ctrl-Alt-Delete). Note that not all BIOS' have the same mapping of logical to physical sectors on a hard drive, so if your hard drive was written by the BIOS on some other computer, it may not be readable by the BIOS on the ÉlanSC300 microcontroller evaluation board. If you are unable to boot from C, you should reformat the hard drive for use on the ÉlanSC300 microcontroller evaluation board (see your DOS documentation for how to reformat your hard drive).

For More Information ...

If you need more information about:

- How to setup and use the serial ports or parallel port, including a serial mouse, see “Serial Ports” on page 2-23.
- How to setup and use the parallel port, see “Parallel Port” on page 2-23.
- How to add a PS/2 mouse, see “PS/2 Mouse” on page 2-22.
- How to change the processor speed, see “SystemSoft BIOS” on page 2-6 or “PhoenixPICO BIOS” on page 2-10.
- How to change the amount of DRAM, see “DRAM Main Memory” on page 2-20.
- How to use an LCD panel, see “Internal Video Mode” on page 2-18.
- How to use a local bus card, see “Local Bus Mode” on page 2-19.
- How to enable Power Management functions, see “SystemSoft BIOS” on page 2-6 or “PhoenixPICO BIOS” on page 2-10.

Chapter 2

Board Functional Description

The ÉlanSC300 microcontroller evaluation board provides a development platform for ÉlanSC300 microcontroller-based designs. Read the following sections to learn more about the board:

See "Evaluation Board Setup Summary" on page A-1 for a summary of the board settings. See "Board Layout Suggestions" on page C-1 for board layout strategy for the 32-kHz oscillator, the PLLs, and the power supplies.

Board Layout

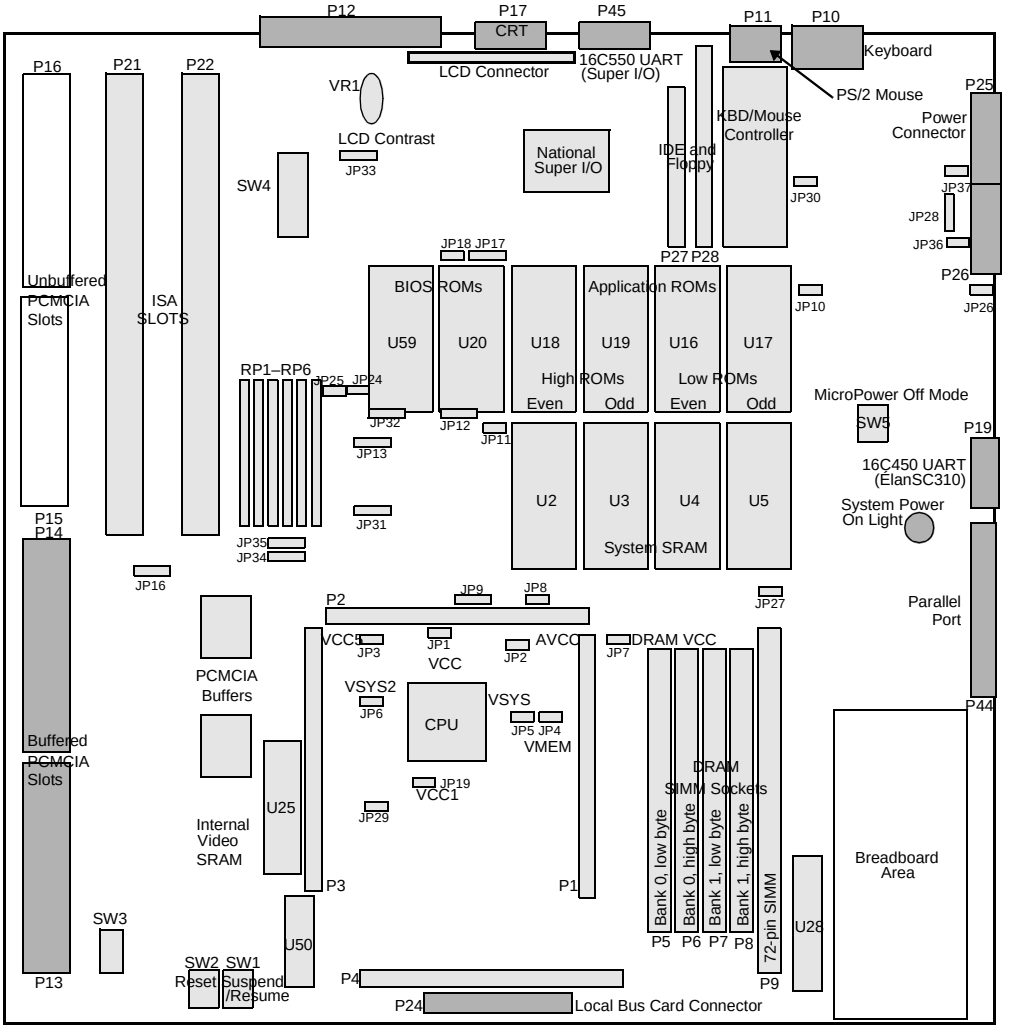


Figure 2-1. ÉlanSC300 Microcontroller Evaluation Board

Table 2-1. Board Layout

Part	Description	Page Number
JP1–JP8	Power measurement	2-26
JP9	SRAM size	2-21
JP10–JP11	Power measurement	2-26
JP12	ROM type	2-25
JP13	Application ROM size	2-25
JP16	LCD display	2-17
JP17	Super I/O UART/mouse	2-17, 2-22
JP18	PS/2 mouse	2-17, 2-22
JP19	Power measurement	2-26
JP32	BIOS ROM selection	2-5, 2-25
JP34–JP35	PCMCIA slot selection	2-24
RP1–RP6	Bus mode selection	2-17
SW1	Suspend/Resume	
SW2	Reset	
SW3	Local Bus RDY config.	2-19
SW4-1	Memory voltage setting	2-21
SW4-2	PIRQ1 connect	2-28
SW4-3	IRQ1 connect	2-28
SW4-4—SW4-7	Battery status	2-27
SW4-8	ACIN	2-28
SW5	MicroPower Off mode	2-29

Evaluation Board Restrictions

- This revision of the evaluation board is not backwards compatible with the Rev. A ÉlanSC300 microcontroller.
- The evaluation board ISA bus can only run at 5 V. In normal designs this is not a restriction.
- The ÉlanSC300 microcontroller integrates two PCMCIA type II controllers. The evaluation board muxes these two controllers to four physical connectors (two hot swap slots, two minimum buffered slots) to demonstrate the ability to support hot-swap or low-cost PCMCIA solutions. Either the buffered or the unbuffered sockets can be used, but not both at the same time.
- The DRAM SIMM modules must have a 70-ns or less RAS access time, for 33 MHz operation.
- The DRAM on the SIMM modules must be x4, x8 or x16. The ÉlanSC300 microcontroller cannot drive x1 DRAM due to the large capacitance associated with 32 loads.
- System DRAM and system SRAM cannot be supported simultaneously.
- System DRAM population of both the 30-pin SIMM sockets and the 72-pin SIMM socket is not supported simultaneously.
- On the 72-pin SIMM socket, only 16-bit SIMM modules are fully supported. 32-bit SIMMs can be used in the 72-pin SIMM socket but only half of the memory will be visible.
- Software cannot be used to switch between ISA, Video, and local bus configurations. One of the configurations must be set up before power-up.
- The BIOS ROM sockets (U20 and U59) can only be populated with the following (the AMD recommended part is also listed):
  - 128Kx8 ROM/EPROM (AMD 27C010)
  - 256Kx8 ROM/EPROM (AMD 27C020)
  - 128Kx8 Flash (AMD 12-V 28F010 or 5-V 29F010)
  - 256Kx8 Flash (AMD 12-V 28F020 or 28F020A)

- Application (DOS) ROM space is 16-bits wide (two or four devices must be used).
- The DOS ROM sockets (U16–U19) can only be populated with the following (the AMD recommended part is also listed):
  - 256Kx8 ROM/EPROM (AMD 27C020)
  - 512Kx8 ROM/EPROM (AMD 27C040)
  - 256Kx8 Flash (AMD 12-V 28F020 or 28F020A)

  NOTE: 512Kx8 Flash can be supported after a minor board rework. Contact your AMD FAE for more information.

- Some ISA signals are not available when using Internal Video or Local Bus modes. Refer to the *ÉlanSC300 Microcontroller Data Sheet* and *Programmer's Reference Manual* for detailed information on the ÉlanSC300 functionality.
- The RTC RAM (integrated in the ÉlanSC300 microcontroller)—which is used to maintain time, date and system configuration data—is cleared (lost) when power is removed from the V_{CC} & AV_{CC} power planes.
- Connectors are available to test local bus operation and modes. However due to bus loading, High Speed operation is not possible without depopulating several components.

BIOS

The ÉlanSC300 microcontroller evaluation board comes with SystemSoft BIOS programmed into the ROM in socket U20, and PhoenixPICO BIOS programmed into the ROM in socket U59. Jumper JP32 selects which ROM socket is used when the system boots (JP32 =1-2 selects socket U59, JP32=2-3 selects socket U20). Each BIOS is an evaluation version specific to the evaluation board.

An evaluation diskette for each BIOS is shipped with your kit. The BIOS ROM images are located on their respective diskettes.

NOTE: These are evaluation BIOS' only. Each BIOS has been tested on the evaluation board and a list of know errata is available on the AMD Utilities diskette. For the most recent errata listing, contact your local AMD representative.

SystemSoft BIOS

On system power-up, the SystemSoft BIOS tests the system and determines if there are any problems with the setup configuration. Since there is no CMOS backup power on the evaluation board, it uses the default BIOS settings upon initial power-up.

NOTE: You need to run setup each time the system is powered off and on again.

SystemSoft BIOS also monitors the Valid RAM and Time (VRT) bit in the RTC. This bit gets reset every time a hardware reset occurs. Therefore, every time the system is reset using the red Reset button, SystemSoft BIOS flags a setup error. If this occurs, press F1 to continue booting with the previous setup information.

If a setup error occurs, the BIOS prompts the user to press the CNTL-ALT-S keys to enter the setup screen. The setup screen can also be entered while in DOS by pressing the CNTL-ALT-S keys.

SystemSoft has a familiar menu-driven setup screen. The options are listed in the table below. The default options are indicated in bold.

1.1

Table 2-2. SystemSoft BIOS Set-Up Screen Options

Menu-Bar Item	Option	Description	Parameters
Standard	Set Date	Sets system date	(User enters)
	Set Time	Sets system time	(User enters)
	Diskette Disk	Selects disk drive type	2.88MB **1.44MB (default for drive A)** 1.7MB 720KB 360KB **none (default for drive B)**
	Hard Disk 1	Sets parameters for Hard Drive 1	Standard (select from list) Custom (enter your own) **Auto** (auto-detects drive parameters; works for most drives)
	HD1 Translate Parameters	Leave this unchecked	
	Hard Disk 2	Sets parameters for Hard Drive 2	Standard (select from list) Custom (enter your own) **Auto** (auto-detects drive parameters; works for most drives)
	HD2 Translate Parameters	Leave this unchecked	
	Internal COM Port	Sets the ÉlanSC300 internal COM port	COM1 COM2 **Disabled**
	Super I/O COM Port	Sets the Super I/O port	COM1 COM2 COM3 COM4 **Disabled**
	LPT Port Address	Sets parallel port base address	3BC 378 278 **Disabled**

Menu-Bar Item	Option	Description	Parameters
	Video Display	Sets video display type	**EGA/VGA** CGA80 CGA40 Monochrome
	CPU Speed	Sets processor speed	Low **20MHz** 25MHz 33MHz
Preferences	NumLock on	Turns on NumLock	**On** Off
	Fast Boot	When On, does not perform memory check	**On** Off
	Virus Alter	When On, alerts user of boot sector writes	On **Off**
	First Boot	Selects which drive is booted from first	**Drive A** Drive C
	Typematic Rate	Selects keyboard typematic rate	**10CPS with 500ms delay**
	Boot Password	Sets power-on password	**None**
	SCU Password	Sets password to enter setup screen	**None**
Memory	Video & BIOS shadow	When On, shadows video and BIOS code to DRAM	**On** Off
PowerMgmt	Enable PowerMgmt	When On, sets up the ÉlanSC300 timers to transition into Low, Doze and Suspend Power modes. When Off, the ÉlanSC300 always runs at the CPU SPEED set in the Standard Menu.	On **Off**

1.1

Menu-Bar Item	Option	Description	Parameters
	Idle	Amount of time the ÉlanSC300 remains in High Speed mode with no activity prior to transitioning to Low Speed mode.	**Off** 0.5 seconds 1 seconds 2 seconds 4 seconds 8 seconds 12 seconds 16 seconds
	Doze	Amount of time the ÉlanSC300 remains in Low Speed mode with no activity prior to transitioning to Doze mode.	**Off** 5 seconds 10 seconds 20 seconds 30 seconds 40 seconds 50 seconds 60 seconds
	Suspend	Amount of time the ÉlanSC300 remains in Doze mode with no activity prior to transitioning to Sleep/Suspend mode.	**Off** 2 minutes 4 minutes 6 minutes 8 minutes 10 minutes 12 minutes 14 minutes
Defaults	Defaults	Sets all setup screen settings to default values.	N/A
Exit	Exit	Prompts the user to save the setup and reboot.	N/A

PhoenixPICO BIOS

On system power-up, the PhoenixPICO BIOS tests the system and determines if there are any problems with the setup configuration. Since the evaluation board does not have CMOS back-up power, it uses the default BIOS settings on initial power-up. The user therefore needs to run setup each time the system is powered off and then on again.

BIOS prompts the user to press F2 to enter Setup mode and display the setup screen. BIOS uses the following keys for navigating the setup screens and editing or selecting options.

Key	Function
Up Arrow	Move cursor up
Down Arrow	Move cursor down
Left Arrow	Move cursor left
Right Arrow	Move cursor right
+ or –	Toggle through options
ESC	Exit menu
F1	Help screen
F9	Setup defaults
F10	Previous values
Enter	Execute command

Four menus are available through the menu bar at the top of the window:

- **MAIN:** Use this menu for basic system configuration.
- **ADVANCED:** Use this menu to set the advanced features available on your system's chipset.
- **POWER:** Use this menu to specify your settings for Power Management.
- **EXIT:** Exits the current menu.

The PhoenixPICO BIOS setup screen options for each menu are shown in the tables on the following pages. Option defaults are indicated in bold.

Table 2-3. PhoenixPICO BIOS *Main* Menu Setup Screen Options

Option	Description	Parameters
System Time	Hour, Minute, and Second	(User enters)
System Date	Month, Date, and Year	(User enters)
Diskette A Diskette B	Selects the type of floppy disk drive(s) installed in your system.	**Not Installed (for B)** 2.88MB/3.5" **1.44MB/3.5" (for A)** 720KB/5.25" 1.2MB/5.25" 360KB/5.25"
IDE Adapter Master IDE Adapter Slave	IDE adapters control the hard disk drive(s). The IDE adapter supports one master drive and one optional slave drive. A separate sub-menu is used to configure each hard drive.	**Not Installed** Types 1–49*
Video System	Selects video type.	**EGA/VGA** CGA 80x25 Monochrome

Option	Description	Parameters
Shadow Options: Video Shadow	Shadows Video BIOS ROM.	**Enabled** Disabled
Memory Shadow	Shadows memory in the region specified.	Enabled **Disabled** If enabled, options are: C800–CBFF CC00–CFFF D000–D3FF D400–D7FF D800–DBFF DC00–DFFF E000–E3FF E400–E7FF E800–EBFF EC00–EFFF
Boot Sequence	Order in which the system searches drives for a boot disk.	**C: then A:** C: only A: then C:

Option	Description	Parameters
Embedded Features: ROM DOS Support	Enables booting from the ROM DOS image.	Enabled **Disabled**
PCMATA Enabled	Enables booting from a PCMCIA ATA card at the configuration byte or the PCMCIA card configuration register selected.	Enabled **Disabled** If PCMATA is enabled, register location options are: 256 bytes **512 bytes** 1024 bytes 2048 bytes 4096 bytes 8192 bytes If PCMATA is enabled, config. byte options are: 1 **2** 3 4 5 6
ROM/RAM Disk 0	Non-magnetic boot device	None Serial **ROM/XMS** PCMCIA
ROM/RAM Disk 1	Non-magnetic boot device	**None** Serial ROM/XMS PCMCIA
System Memory	Amount of conventional memory detected during boot-up.	N/A

Option	Description	Parameters
Extended Memory	Amount of extended memory installed on the system. It is detected automatically, so it should not require any manipulation.	N/A

* – If user type 48 is chosen, the following parameters must be set (they are usually found on the drive label):

- Type Number designation for the drive (user type = 48)
- Cyl Number of cylinders on specified drive (see drive label or documentation)
- Hd Number of heads on specified drive (see drive label or documentation)
- Pre Designates the starting cylinder of the read delay circuitry (set to 0)
- LZ Designates cylinder location where heads normally park when system is down (set to 0)
- Sec Number of sectors per track (see drive label or documentation)

Table 2-4. PhoenixPICO BIOS *Advanced* Menu Setup Screen Options

Option	Description	Parameters
CPU Speed	Sets processor speed	9.2 MHz 20 MHz 25 MHz **33 MHz**
Advanced Chipset Control	Sets the divisor for the AT CLK.	CLK/6 CLK/5 CLK/4 **CLK/3**
Large Disk Access Mode	Select "DOS" if you have DOS; select "Other" if you use another operating system such as UNIX.	**DOS** Other

1.1

Table 2-5. PhoenixPICO BIOS *Power* Menu Setup Screen Options

Option	Description	Parameters
Power Management Mode	Turning this feature On enables power management.	On **Off**
Power Savings	Selects power management mode. "Max. Battery Life" and "Max. Performance" set power management options with predefined values. "Customize" enables you to make your own selections. "Disabled" turns off all power management.	Disabled **Customize** Max. Battery Life Max. Performance
Standby Timeout	Sets inactivity period required to put the system in Standby (partial power shutdown).	Disabled 1 sec 4 sec 8 sec 1 min **2 min** 4 min 6 min 8 min 12 min 16 min
Suspend Timeout	Sets inactivity period required after Standby to Suspend (maximum power shutdown).	Disabled 1 min 2 min 4 min 6 min 8 min 12 min **15 min** 16 min

Fixed Disk Timeout	Sets inactivity period of fixed disk required before Standby (motor off).	Disabled 10 sec **15 sec** 30 sec 45 sec 1 min 2 min 4 min 8 min 12 min 16 min
Video Timeout	Length of time either the keyboard or mouse remains inactive before the screen is turned off.	Disabled 10 sec 15 sec 30 sec 45 sec 1 min **2 min** 4 min 8 min 12 min 16 min

1.1

Table 2-6. PhoenixPICO BIOS *Exit* Menu Setup Screen Options

Option	Description
Save changes & exit	Exit after writing all changed setup values to CMOS.
Exit without saving changes	Exit without writing changed setup values to CMOS.
Get default values	Load default values for all setup items.
Load previous values	Read previous values from CMOS for all setup items.
Save changes	Write all setup item values to CMOS.

Bus Modes

The ÉlanSC300 microcontroller allows designs to utilize three different bus options: ISA, Internal Video, or Local Bus. While in ISA mode, all of the device's ISA bus signals are available (refer to the *ÉlanSC300 Microcontroller Data Sheet* for a detailed description of the ISA bus). When in Internal Video mode, LCD control signals are available from the ÉlanSC300 microcontroller as well as a limited subset of the ISA bus signals. Local Bus mode provides a 386 local bus in addition to a subset of ISA bus signals. Refer to the *ÉlanSC300 Microcontroller Data Sheet* for a description of the signals available in each of these modes.

The ÉlanSC300 microcontroller evaluation board allows testing in each of the three bus modes available from the ÉlanSC300 microcontroller. Bus mode selection must be made before applying power to the board and cannot be changed while the board is in operation. Selection of the bus mode is determined by the resistor packs labeled RP1–RP6 (see Table 2-7).

When adjusting the Bus mode jumpers, be sure to follow pin 1 designations. Pin 1 on the resistor packs must correspond to pin 1 on the evaluation board. JP16–JP18 must be set based on what bus mode is selected (see Table 2-7).

Table 2-7. Bus Mode Selection and Affected Jumpers

Bus Mode	Resistor Pack Setting	JP16		JP17		JP18	
		1-2	2-3	1-2	2-3	open	closed
Full ISA	Install RP1 & RP2 only	N/A	N/A	Connects IRQ3 from Super I/O	N/A	N/A	Connects IRQ12 from mouse
Internal Video	Install RP3 & RP4 only	LCD display	N/A	Connects IRQ3 from Super I/O	Connects IRQ12 from mouse	Allows FRM to LCD panel	Not allowed, must be open
Local Bus	Install RP5 & RP6 only	2x CPU clock	N/A	Connects IRQ3 from Super I/O	N/A	N/A	Connects IRQ12 from mouse

ISA Mode

Provided on the ÉlanSC300 microcontroller evaluation board are two physical 16-bit ISA bus connectors. These slots are available for use when the board is configured for ISA mode. The ÉlanSC300 microcontroller ISA bus is a subset of a full ISA bus. Some signals are not available, therefore some ISA cards may not function properly on the evaluation board (refer to the *ÉlanSC300 Microcontroller Data Sheet* for a detailed description of the ISA bus). The ISA bus is wait-state programmable (refer to the *ÉlanSC300 Microcontroller Programmer's Reference Manual* for details on programming ISA bus timings).

Internal Video Mode

The ÉlanSC300 microcontroller evaluation board allows the testing of the internal video controller on the ÉlanSC300 microcontroller. When this mode is selected, the LCD connector on the evaluation board is enabled. Make sure JP16 is set to 1-2.

JP16 Setting	Internal Video Mode
1-2	LCD

1.1

JP18 must be left open in Internal Video mode. This jumper connects IRQ12 from the 8042 to pin 181 on the ÉlanSC300 microcontroller, which is the FRM signal in this mode. Refer to "I/O" on page 2-22 for a detailed description of this jumper.

Bus Mode	JP18
Internal Video	Must be open
ISA/Local Bus	Closed to enable PS/2 port

Provided on the evaluation board is an easily customized connector for LCD operation. A specific panel header is not included due to the lack of an industry standard LCD interface. All of the necessary LCD signals are provided through this connector. A 5-V power plane is provided as well as an adjustable negative 17-V contrast voltage at VR1. Refer to "Schematics" on page D-1 for a description of the LCD interface on the evaluation board.

Local Bus Mode

The ÉlanSC300 microcontroller evaluation board provides a proprietary local-bus connector for testing of local-bus designs. Since this connector is not standard, a custom interface is required to test the local-bus functionality of the ÉlanSC300 microcontroller on the evaluation board. In Local Bus mode, some of the ISA bus signals are lost. Refer to the *ÉlanSC300 Microcontroller Data Sheet* for more details on what signals are available in this mode. Since different local-bus implementations require different signal connections, the local bus signal $\overline{\text{VLRDYI}}$ can be connected to either $\overline{\text{VGARDY}}$ (from the local bus device) or to $\overline{\text{VLRDYO}}$ (from the ÉlanSC300) using switches 2 and 3 on SW3 (switches 1 and 4 are no connects). Note that $\overline{\text{VLRDYI}}$ corresponds to $\overline{\text{LRDY}}$ on the ÉlanSC300 microcontroller, and $\overline{\text{VLRDYO}}$ corresponds to $\overline{\text{CPURDY}}$.

SW3-2	Affected Signals
ON	Connects $\overline{\text{VGARDY}}$ to $\overline{\text{VLRDYI}}$
OFF	Open

SW3-3	Affected Signals
ON	Connects $\overline{\text{VLRDYO}}$ to $\overline{\text{VLRDYI}}$
OFF	Open

NOTE: Due to loading, High Speed operation is not possible without depopulating several components.

Memory

The ÉlanSC300 microcontroller evaluation board supports up to 16 Mbyte of memory in three different formats: 72-pin, 16-bit SIMM; 30-pin, 8-bit SIMMs; or 512-Kbyte x 8 SRAMs. Only one of these options can be used at a time. (That is, if SRAM is used, the 30-pin and 72-pin DRAM sockets must be empty. If the 30-pin DRAM sockets are used, the 72-pin DRAM socket and the SRAM sockets must be empty. If the 72-pin DRAM socket is used, the 30-pin DRAM sockets and the SRAM sockets must be empty.)

DRAM Main Memory

The ÉlanSC300 microcontroller evaluation board comes standard with 2 Mbyte of standard 30-pin, 70-ns DRAM SIMMs installed on the board. The evaluation board requires DRAMs with access times of 70 ns or less (for 33 MHz operation). The DRAM memory can be upgraded using 30-pin SIMMs with 4- or 8-bit DRAMs; SIMMs with 1-bit DRAMs cannot be used on the evaluation board due to loading restrictions associated with 32 loads.

Total Memory	Bank 0	Bank 1
1 Mbyte	Two 512-Kbyte	Empty
2 Mbyte	Two 512-Kbyte	Two 512-Kbyte
2 Mbyte	Two 1-Mbyte	Empty
4 Mbyte	Two 1-Mbyte	Two 1-Mbyte
8 Mbyte	Two 4-Mbyte	Empty
16 Mbyte	Two 4-Mbyte	Two 4-Mbyte

16 Mbyte of main DRAM memory can also be installed using a 72-pin, 16-bit SIMM module. This can be installed in the 72-pin SIMM socket located next to main memory bank 1 on the evaluation board (see Figure 2-1 on page 2-2). On the 72-pin SIMM socket, only 16-bit SIMM modules are fully supported. 32-bit SIMMs can be used in the 72-pin SIMM socket but only half of the memory will be visible.

BIOS automatically detects the amount of DRAM installed.

SRAM Main Memory

When using SRAM for system memory, populate sockets U2 and U3 with 512Kx8 for 1 Mbyte total system memory, or sockets U2–U5 for 2 Mbyte total system memory.

NOTE: Currently only a special SystemSoft BIOS supports SRAM. This BIOS is available on the SystemSoft diskette included with your kit.

JP9 Setting	System SRAM Size
2-3	512Kx8

Memory Voltage Setting

The ÉlanSC300 microcontroller evaluation board allows system memory to operate at either 5 V or 3.3 V. When operating in Local Bus mode, 3.3 V memory must be used. In order to operate memory at 3.3 V, ensure that the memory is rated for 3.3-V operation. SW4-1 controls the voltage for the system memory.

SW4-1 Setting	Memory V_{CC}
OFF	3.3 V
ON	5 V

I/O

The ÉlanSC300 microcontroller integrates several standard I/O interfaces. A 16C450-compatible UART, bidirectional parallel port is controlled by the ÉlanSC300 microcontroller. In addition, the ÉlanSC300 microcontroller evaluation board contains a Super I/O, which contains a 16C550 UART, a floppy disk controller, and IDE hard drive interface.

A standard 9-pin connector is provided for an extended PC keyboard. A PS/2 port is provided for use with a PS/2 style mouse. Both the keyboard and PS/2 mouse are driven by the 8042.

PS/2 Mouse

A PS/2 port has been provided on the evaluation board for a PS/2-style mouse. This device is driven by the 8042 keyboard controller.

While in ISA or Local Bus mode, the ÉlanSC300 microcontroller IRQ12 signal is connected to the IRQ12 signal on the 8042 to control the PS/2 mouse. (See the settings for JP17 and JP18 in the table below.)

In Internal Video mode, the ÉlanSC300 microcontroller IRQ12 signal becomes FRM, and therefore is not available to the 8042. In order to use the PS/2 mouse in Internal Video mode, PIRQ0 from the ÉlanSC300 microcontroller (which is normally used for the Super I/O serial port) must be redirected to the 8042 IRQ12 signal. By redirecting this signal, the serial port on the Super I/O is disabled. While in Internal Video mode, the Super I/O serial port and the PS/2 mouse port cannot be used simultaneously.

Bus Mode	**JP17**		**JP18**
	1-2	2-3	
Full ISA	Enables Super I/O serial port IRQ	Do not use	Closed to enable PS/2 mouse IRQ
Internal Video	Enables Super I/O serial port IRQ	Enables PS/2 mouse IRQ	Must be open
Local Bus	Enables Super I/O serial port IRQ	Do not use	Closed to enable PS/2 mouse IRQ

Serial Ports

The evaluation board has two serial ports. Connector P19 is connected to the ÉlanSC300 internal 16C450-compatible UART. Connector P45 is connected to the Super I/O 16C550 UART. The BIOS determines how the UART is set up, e.g., SystemSoft BIOS allows the ÉlanSC300 to be set up as COM1, COM2, or disabled; and the Super I/O UART as COM1, COM2, COM3, COM4, or Disabled. (Note that when the Super I/O UART is configured as COM1 or COM3, the IRQ4 line from the Super I/O is not connected, therefore polling must be used.)

After DOS is booted, the DOS utility **EVALSET.EXE** provided on the AMD Utilities diskette included in your kit can be used to reinitialize either UART to the desired configuration. Refer to the documentation on the diskette for how to do this.

Parallel Port

Connector P20 is connected to the ÉlanSC300 parallel port. Most BIOS' let you configure the parallel-port base address in the set-up screen. In Internal Video mode, you can also use **EVALSET.EXE** to set the base address (see page 3-11).

IDE Hard Drive

The ÉlanSC300 microcontroller evaluation board contains a standard 40-pin connection for an IDE drive at location P28 (see the figure on page 2-2). Pin 1 is at the end near the ROM sockets. See "Connecting an IDE Hard Drive" on page 1-7 for a step-by-step guide.

PCMCIA

The ÉlanSC300 microcontroller evaluation board provides two buffered and two unbuffered PCMCIA slots controlled by the PCMCIA controllers on the ÉlanSC300 microcontroller. The signals to the buffered and unbuffered slots have been muxed together to allow testing of either a buffered or unbuffered PCMCIA solution. All four slots cannot be used simultaneously. The selection of PCMCIA slots is controlled by JP34 and JP35.

JP34 Setting	PCMCIA Socket A Selection
1-2	Unbuffered
2-3	Buffered

JP35 Setting	PCMCIA Socket B Selection
1-2	Unbuffered
2-3	Buffered

The two buffered PCMCIA slots allow hot-swapping of PCMCIA cards while the system is in operation, demonstrating a high-end PCMCIA solution based on the ÉlanSC300 microcontroller. These slots are buffered from the system by two CHIPS F87000 PCMCIA buffers.

The two unbuffered PCMCIA slots demonstrate the functionality of a unbuffered, low cost PCMCIA implementation using the ÉlanSC300 microcontroller. Since there is no buffering, hot-swapping is not supported by these slots.

Phoenix PicoCard and SystemSoft CardSoft are provided on diskettes for evaluating the ÉlanSC300 PCMCIA capabilities. Refer to the documentation provided on the diskettes for how to install and use the PCMCIA drivers.

ROMs

The ÉlanSC300 microcontroller evaluation board provides two BIOS ROM sockets and four application ROM sockets capable of handling up to 256 Kbyte of BIOS ROM and up to 2 Mbyte of application ROM. The evaluation board supports BIOS and application ROMs as either Flash or EPROM devices. JP12 must be set to select either Flash or EPROM devices.

JP12	Type of ROM
1-2	Flash
2-3	EPROM

Two BIOS ROM sockets, U59 and U20, are available on the evaluation board. Each BIOS ROM socket is capable of supporting 128-Kbyte or 256-Kbyte Flash or EPROM BIOS ROMs. The active BIOS ROM is selectable by JP32.

JP32	BIOS ROM Selection
1-2	U59 (Phoenix)
2-3	U20 (SystemSoft)

Four 8-bit application ROM sockets, U16–U19, are provided on the evaluation board for ROM-based applications such as ROM-DOS. U16 (Even) and U17 (Odd) make up one logical 16-bit ROM (Low) beginning at offset 0 in application ROM space. U18 (Even) and U19 (Odd) make up a second logical 16-bit ROM (High) beginning where U16 and U17 end in application ROM space. These sockets can be populated with either 256 Kbyte 8-bit Flash, or 256 Kbyte or 512 Kbyte 8-bit EPROM devices. JP13 selects the size of application ROMs that can be used.

JP13	Application ROM Size
1-2	256Kx8 (Flash or EPROM)
2-3	512Kx8 (EPROM only)

NOTE: 512Kx8 Flash can be supported after a minor board rework. Contact your local AMD or distributor Field Application Engineer for more information.

Power Measurement

The evaluation board allows for measurement of current flow in separate V_{CC} planes for power budget analysis. The following table summarizes the connections to the V_{CC} jumpers. **Be sure to turn off system power before removing JP1–JP11. Replace JP1–JP11 before power-up or the system will not work.**

Jumper	V_{CC}	Logic connected to V_{CC} plane
JP1	V_{CC}	ÉlanSC300 core V_{CC} only. Always 3.3 V.
JP2	V_{CC3}	ÉlanSC300 AV_{CC} pin. Analog V_{CC}. Always 3.3 V.
JP3	V_{CC5}	ÉlanSC300 V_{CC5} pin. Diode clamp refs except V_{CCMEM} and AV_{CC} source pins. Always 5 V except in full 3.3-V designs. (Evaluation board limits to 5 V.)
JP4	V_{CCMEM}	ÉlanSC300 memory interface V_{CC}. See the SW4 table on page 2-21 for 3.3-V or 5-V setting. Restrictions do apply. Also the diode clamp ref for pins sourced by the V_{CCMEM} pin.
JP5	V_{CCSYS}	ÉlanSC300 ISA bus V_{CC} and other misc. pins. 5 V or 3.3 V. Refer to datasheet for details.
JP6	V_{CCSYS2}	ÉlanSC300 alternate pin V_{CC}. 5 V or 3.3 V. Refer to datasheet for details.
JP7	$V_{CCMEM53}$	System DRAM V_{CC} plane.
JP8	V_{CCSRAM}	System SRAM V_{CC} plane.
JP10	V_{CCKBOS}	8042 V_{CC}
JP11	V_{CCROM}	BIOS and Application ROM V_{CC}
JP19	V_{CC1}	ÉlanSC300 V_{CC1} pin 176. 5 V or 3.3 V.

A DOS application program has been provided to aid in placing the system in the various power management modes for power measurement. **ELANPMU.EXE** is on the AMD utilities diskette included with your kit. See “Elan PMU Evaluation Utility” on page 3-4 for more information on **ELANPMU.EXE**.

1.1

BL1–BL4 Pins

These signals are used to indicate the current status of the battery to the ÉlanSC300 microcontroller. A high signal indicates normal operating conditions, while a low indicates a warning condition. Access to these signals has been provided on the evaluation board to allow designers to test their functionality. Switches 4–7 on SW4 allow the $\overline{BL1}$–$\overline{BL4}$ signals to be toggles between GND (warning) and 5 V (normal).

SW4 Switches	Signal	ON	OFF
4	$\overline{BL1}$	GND	5 V
5	$\overline{BL2}$	GND	5 V
6	$\overline{BL3}$	GND	5 V
7	$\overline{BL4}$	GND	5 V

Breadboard Area

A breadboard area has been provided on the ÉlanSC300 microcontroller evaluation board. This area can be used as a convenient place to build custom circuits to interface to the evaluation board. The pins in this breadboard are all isolated from other pins and the rest of the board.

Power Management

The ÉlanSC300 microcontroller offers unparalleled power management in its class. In addition to low operating current, six power management modes are available: High Speed, Low Speed, Doze, Sleep, Suspend, and Off. Refer to the *ÉlanSC300 Microcontroller Data Sheet* and *Programmer's Reference Manual* for an in-depth discussion of these modes.

Suspend/Resume

The ÉlanSC300 microcontroller evaluation board provides a hardware option to allow the user to toggle between the High Speed and Suspend modes. By pressing the Suspend/Resume button after the system has powered up, the system enters the Suspend mode (assuming the ACIN signal is low). By pressing the Suspend/ Resume button again, the system returns to High Speed mode. The behavior of the system in Suspend mode depends on the BIOS.

Power Management Simulation

Battery backup conditions can be simulated on the evaluation board by controlling the ACIN signal to the ÉlanSC300 microcontroller. When ACIN is low, power management functions on the ÉlanSC300 microcontroller are enabled. When ACIN is high, power management functions on the ÉlanSC300 microcontroller are disabled. Switch 8 on SW4 controls the ACIN pin on the ÉlanSC300, allowing power management functions to take effect if they are enabled.

SW4-8	ACIN
ON	GND
OFF	5 V

In order to get true power measurements while in Suspend mode, IRQ1 and PIRQ1 must be disconnected from the ÉlanSC300 microcontroller. The ÉlanSC300 microcontroller drives these signals low during Suspend mode. Since the peripherals connected to these lines drive them high, this creates the appearance of additional power drain. These signals can be easily disconnected while in Suspend mode using switches 2 and 3 on SW4.

SW4-2	PIRQ1
ON	Connect
OFF	Disconnect
SW4-3	**IRQ1**
ON	Connect
OFF	Disconnect

Before exiting from Suspend mode, IRQ1 and PIRQ1 must be reconnected for the system to function properly.

MicroPower Off Mode

This mode is the lowest power mode for the ÉlanSC300 microcontroller. When the system is initially powered by turning on the power supply and then pressing the MicroPower Off button, SW5, the system enters High Speed mode. The red power light indicates that the system is fully powered on. Pressing the MicroPower Off button, SW5, again, causes the ÉlanSC300 microcontroller to enter MicroPower Off mode. During MicroPower Off mode, only AV_{CC}, V_{CC}, and the 32-KHz crystal remain active. The system is essentially off, but the RTC remains in operation. Please refer to the *ÉlanSC300 Microcontroller Data Sheet* for a more detailed explanation of this feature.

Chapter 3

Using the Software

The ÉlanSC300 microcontroller evaluation board kit currently ships with four diskettes: the SystemSoft Evaluation diskette, the PhoneixPICO Evaluation diskette, the Datalight Software Evaluation Kit diskette, and the AMD Utilities diskette.

SystemSoft Evaluation Diskette

This diskette contains the evaluation version of SystemSoft's CardSoft PCMCIA software, the BIOS ROM image programmed into the ROM on the evaluation board, and a BIOS ROM image that can be used with SRAM as main memory. Please refer to the documentation on the diskette for further information about these files.

PhoenixPICO Evaluation Diskette

This diskette contains the evaluation version of the Phoenix PCMCIA software, and the PhoenixPICO BIOS ROM image programmed into the ROM on the evaluation board. Please refer to the documentation on the diskette for further information about these files.

Datalight Software Evaluation Kit Diskette

This diskette contains software for evaluating Datalight's ROM-DOS and WinLight software on the evaluation board. Please refer to the documentation on the diskette for further information about these files.

AMD Utilities Diskette

This diskette contains several utilities developed specifically for the evaluation board to assist the user in their evaluation and design with the ÉlanSC300 microcontroller. Some of these utilities may work on other ÉlanSC300 microcontroller-based platforms, but their functionality outside of the evaluation board cannot be guaranteed and therefore is not supported. The following utilities are included on the AMD Utilities diskette:

ELANINIT.ZIP	Initialization example for the ÉlanSC300.
ELANPMU.ZIP	Utility for demonstrating the ÉlanSC300 power-management features.
EVALSET.ZIP	Utility to configure the two serial ports on the evaluation board. Source code is provided.
FLASH.ZIP	Utility for Flashing AMD's 12-V 28F010, 5-V 29F010, 12-V 28F020, or 12-V 28F020A Flash parts on the evaluation board. Source code is provided.
LCDAPP.ZIP	Utility for developing and debugging LCD panel setup with the ÉlanSC300.
MMSINFO.ZIP	Utility for displaying MMS window configuration information. Source code is provided.
MMSVIEW.ZIP	Utility for viewing data through the MMSA pages.
REGDUMP.EXE	Utility for displaying the ÉlanSC300 registers.
SDB.ZIP	Simple, debug utility for command-line accesses to ÉlanSC300 registers.

ELANINIT.ZIP

This zipfile contains assembly language routines that give an example of how to initialize the ÉlanSC300 microcontroller registers, enable DRAM, handle SMI events, and report status through the serial port. The unzipped files compile to form a binary image that can be programmed into a ROM and placed in the BIOS ROM socket. Refer to the **README** and ***.TXT** files in this zipfile for more information.

ELANPMU.ZIP

This zipfile contains **ELANPMU.EXE**, which can be used to place the ÉlanSC300 microcontroller into various PMU modes. It allows the user to modify certain settings for each PMU mode. The user can then measure current consumption of the ÉlanSC300 microcontroller cores and see how the current changes, depending on the current settings and PMU mode. Refer to “Elan PMU Evaluation Utility” on page 3-4 for more information.

EVALSET.ZIP

This zipfile contains **EVALSET.EXE**, which has been provided to allow easy activation of the serial and parallel ports on the ÉlanSC300 microcontroller evaluation board. The BIOS on this board was designed to be generic, therefore these functions are not enabled by the BIOS on the evaluation board. This utility can be used to set up the base addresses for serial port 1, serial port 2 and parallel port 1 on the evaluation board. For complete operating instructions on **EVALSET.EXE**, refer to “EvalSet Serial and Parallel Port Setup Utility” on page 3-10.

FLASH.ZIP

This zipfile contains **FLASH.EXE**, which can be used to program 28F010, 29F010, 28F020, and 28F020A Flash parts on the ÉlanSC300 microcontroller evaluation board. Source code is provided for this utility to be able to modify it for other platforms and other AMD Flash devices. Refer to the **README** and ***.TXT** files in this zipfile for more information.

LCDAPP.ZIP

This zipfile contains the C source code and executable image for a utility, **LCD.EXE**, which can be used to program the ÉlanSC300 microcontroller’s internal video controller for a number of different modes and for LCD panel sizes, which can be selected on the command line. Refer to the **README** and ***.TXT** files in this zipfile for more information.

MMSINFO.ZIP

This zipfile contains **MMSINFO.EXE**, a utility for displaying the current status of the MMSA and MMSB windows. If an MMS window is enabled, then information for each page within the window is displayed. If an MMS window is disabled, then the information on each page within the window is not displayed. Source code for this utility is also provided. The source code contains routines that show how to manipulate the ÉlanSC300 microcontroller’s MMS window registers. Refer to the **README** and ***.TXT** files in this zipfile for more information.

MMSVIEW.ZIP

This zipfile contains **MMSVIEW.EXE**, which is a DOS application that may be used to inspect various resources that are accessible by the ÉlanSC300 microcontroller MMS subsystem. These resources include SYSTEM RAM, the BIOS ROM (or resources accessed by the $\overline{\text{ROMCS}}$ signal), the DOS ROM (or resources accessed by the $\overline{\text{DOSCS}}$ signal), or the PCMCIA slots. For complete operating instructions on **MMSVIEW.EXE**, refer to "Memory Management System (MMS) Viewer Utility" on page 3-12.

REGDUMP.EXE

This register dump utility has been provided for use on the ÉlanSC300 microcontroller evaluation board. It is intended to provide a user with an easy-to-use register manipulation program. This program displays the index register in the ÉlanSC300 microcontroller, grouped by functionality. For complete operating instructions on **REGDUMP.EXE**, refer to "Register Dump Utility" on page 3-20.

SDB.ZIP

This zipfile contains **SDB.EXE**, a simple debug utility useful when working with the ÉlanSC300 microcontroller. It allows the user to easily access the ÉlanSC300 microcontroller's index registers, video registers, and I/O ports from the command line. This way the user can place several SDB command lines in a batch file and just execute the batch file. Source code is provided. Refer to the **README** and ***.TXT** files in this zipfile for more information.

Elan PMU Evaluation Utility

The Elan PMU Evaluation Utility is a DOS utility designed to demonstrate the power management capabilities of the ÉlanSC300 microcontroller. This utility only runs on Rev. 2.2 or later of the ÉlanSC300 microcontroller evaluation board (the revision number is silkscreened on the board next to the AMD logo and name). By using a current meter attached to the ÉlanSC300 microcontroller's various voltage plains, the user can see how different PMU setups affect power consumption. It is recommended that the user read through the *ÉlanSC300 Microcontroller Programmer's Reference Manual* to gain an understanding of the ÉlanSC300 microcontroller's power management functions.

To bring up the main menu, type the following at the DOS prompt:

```
elanpmu
```

The following main menu appears:

```
                ELAN PMU Evaluation Utility
                       Version 1.0

A: Setup PMU Mode Characteristics (PMCx Pins, CPU Speed)
B: Force PMU State Transitions
C: Test Battery Level & ACIN Pins

X: Restore PMU State and Exit to DOS
Z: Leave current PMU values and Exit to DOS

Enter Selection =>/
```

The spinning cursor "/" is used to emulate typical CPU activity. This activity gives a lower current reading for core ÉlanSC300 microcontroller current than if the processor was sitting idle waiting for keyboard input. This is because cycles to the ISA devices (which occur as a result of this activity) are run at 9.2 Mhz. CPU idle cycles occur at the High Speed PLL mode frequency (33/25/20/9.2 Mhz).

A: Setup PMU Mode Characteristics (PMCx Pins, CPU Speed)

This menu selection brings up a matrix of options that can be set for each PMU mode. The value of the highlighted matrix item can be changed by pressing the "+" or "–" keys on the keyboard. The arrow keys control which item is highlighted. Matrix items with a "*" after them are fixed in the ÉlanSC300 microcontroller and cannot be highlighted or changed. Matrix items with a "#" after them are fixed at the current state due to a requirement of the evaluation board. These items cannot be highlighted or changed.

Changes made to this screen do not take effect until either the "S" key is pressed (Program Elan), or the "X" key is pressed (Program Elan & Return to Main Menu). To exit this screen without programming the ÉlanSC300 microcontroller with any changes, press the "Q" key. To restore the values to those currently programmed in the ÉlanSC300 microcontroller, press the "L" key.

While in this screen, the CPU is running in High Speed PLL mode. When any changes to the High Speed PLL mode column are saved, the results are immediately noticeable (e.g., the effect CPU Speed has on core current). Changes to other columns on the screen are not noticeable until those PMU modes are entered.

The state of the PMC pins can be set for each PMU mode. While the particular state the PMC pin is in does not significantly affect the ÉlanSC300 microcontroller's power consumption, this matrix allows the user to see what control the user has for external control of the PMC pins for each PMU mode. Note that the PMC pin setting for the Low and High Speed PLL modes mirror each other. Changing the value in one column causes the value in the other column to change also.

High Speed PLL Mode Column

- The CPU speed can be set to 33 Mhz, 25 Mhz, 20 Mhz, or 9.2 Mhz.
- Both the High Speed and Low Speed PLLs for this mode are enabled.
- The state of the PMC pins for this mode mirror the settings in Low Speed PLL mode. Changing the state in this mode also changes the state for Low Speed PLL mode.
- Auto Low Speed mode, when enabled, switches the CPU clock speed to operate at 9.2 Mhz for the duration of time listed in ALS Duration matrix item (0.25, 0.50, 1.0, 2.0 seconds). This switch is triggered at a rate determined by the ALS Trigger matrix item, which can be set to 4, 8, 16, or 32 seconds. The ALS trigger period and ALS Duration time are stored in write-only registers. Therefore it is not possible to read the current ÉlanSC300 programed value when this utility is started. The default values of 4 seconds for the ALS Trigger and 0.25 seconds for the ALS Duration are programmed at start-up time.
- The CPU Idle Speed can be set to "HIGH" or "LOW." "HIGH" means that during idle cycles the CPU runs at the current High Speed CPU speed (33, 25, 20, or 9.2 Mhz); "LOW" means 9.2 Mhz. The CPU Idle Speed can only be set "LOW" if the High Speed CPU is set to 20 Mhz or 9.2 Mhz. If the High Speed CPU speed is set to 33 Mhz or 25 Mhz and the CPU Idle Speed is then set to "LOW", the CPU speed changes to 20 Mhz. Similarly, if the CPU Idle Speed is set to "LOW" and the High Speed CPU speed is changed to 33 Mhz or 25 Mhz, the CPU Idle speed is changed to "HIGH."

Low Speed PLL Mode Column

- The CPU speed can be set to 4.61 Mhz, 2.30 Mhz, 1.15 Mhz, or 0.58 Mhz.
- The High Speed PLL can be enabled or disabled in this mode.
- The Low Speed PLL is always enabled for this mode.
- The state of the PMC pins for this mode mirror the setting in High Speed PLL mode. Changing the state in this mode also changes the state for High Speed PLL mode.

Doze Mode Column

- The CPU for this mode can be turned "OFF," or it can be enabled to run at 9.2 Mhz in response to IRQ0 being generated. "IRQ0-9.2Mhz" appears as the matrix item. For this mode, the CPU only runs at 9.2 Mhz during the time IRQ0 is being processed. Setting this matrix item to "IRQ0+64 R" enables the CPU to run at 9.2 Mhz while processing IRQ0 and the CPU remains running for 64 refresh cycles after IRQ0 processing is completed.
- The High Speed PLL is always disabled for this mode.
- The Low Speed PLL and Video PLL (controlled by the same bit) can be enabled or disabled for this mode. If these PLLs are disabled and you are using the ÉlanSC300 microcontroller's LCD controller, the LCD screen goes blank.

Sleep Mode Column

- The CPU is always off in this mode.
- The High Speed PLL is always off in this mode.
- The Low Speed PLL and Video PLL (controlled by the same bit) can be enabled or disabled for this mode.

Suspend & Off Mode Column

- The CPU is always off in these modes.
- The High Speed PLL is always off in these modes.
- The Low Speed PLL and Video PLL (controlled by the same bit) can be enabled or disabled for these modes.

B: Force PMU State Transitions

```
                ELAN PMU Evaluation Utility
                     Force PMU Modes

A: Force PMU to Low Speed PLL Mode xxxMhz
B: Force PMU to Doze Mode
C: Force PMU to Sleep Mode
D: Force PMU to Suspend Mode

X: Return to Main Menu

Enter Selection=>/
```

Below this menu, the current PMU mode that the ÉlanSC300 microcontroller is in is displayed along with any options set using option A from the main menu. For modes where the CPU clock is running, the spinning activity cursor "/" helps show the speed of the CPU.

A: Force PMU to Low Speed PLL Mode *xxx*Mhz

- The CPU Clock slows to the speed shown.
- If set up to do so, the High Speed PLL is shut off.
- Pressing any key or toggling the ACIN pin brings the system back to High Speed PLL mode.

B: Force PMU to Doze Mode

- If the CPU clock speed is off, no spinning activity cursor is displayed.
- If the CPU clock is enabled for IRQ0 processing only, then the spinning activity cursor transitions about once every 10 seconds.
- If the CPU clock is enabled for IRQ0+64 Refresh cycles, then the spinning activity cursor spins.
- If the Low Speed PLL (and Video PLL) are disabled in this mode, and an LCD is being used, the screen goes blank when this mode is entered.
- Pressing any key or toggling the ACIN pin brings the system back to High Speed PLL mode.

C: Force PMU to Sleep Mode

- The keyboard is disabled in this mode. Pressing the Suspend/Resume key or toggling the ACIN pin returns the system to High Speed PLL mode.
- If using an LCD Screen, the user is prompted to hit a key prior to entering Sleep mode. This is because the LCD screen goes blank as the first step of the LVDD/LVEE power sequencing is implemented.

D: Force PMU to Suspend Mode

- The keyboard is disabled in this mode. Pressing the Suspend/Resume key or toggling the ACIN pin returns the system to High Speed PLL mode.
- If using an LCD screen, the user is not allowed to force the system into this mode because the LCD Screen power sequencing of the LVDD/LVEE pins that normally occurs as a result of transitioning from Sleep to Suspend would be violated.

C: Test Battery Level & ACIN Pins

This menu item shows how the battery level and ACIN pins are tied to the PMU. Pin $\overline{BL1}$ can be used to force the CPU to run at 9.2 Mhz. Pin $\overline{BL2}$ can be used to transition the PMU into Sleep mode. Pin $\overline{BL4}$ can be used to transition the PMU into Suspend mode. Each of the above transitions can be enabled or disabled by selecting item "A: Change BL Transition Masks", highlighting the appropriate field, and using the "+" and "–" keys to enable or disable the transitions. There is also an option to enable/disable a transition message. If enabled, a Transition message is displayed as the ÉlanSC300 microcontroller transitions from Low Speed to Doze mode, prompting the user to press a key before the system transitions to Sleep or Suspend mode.

The box on the top right of the screen displays the current state of the BL and ACIN pins. Status for the $\overline{BL4}$ pin is not directly readable by the ÉlanSC300. On the ÉlanSC300 microcontroller evaluation board, the state of the BL pins and ACIN pins are controlled by the Red 8 bank DIP switch SW4. Switches 4–7=$\overline{BL1}$–$\overline{BL4}$; Switch 8=ACIN.

ACIN must be set to 0 in order for any of the BL pins to cause a PMU state change. Once a BL pin is used to cause a PMU state change, setting ACIN to 1 (active) wakes up the system and returns the PMU to High Speed PLL mode.

X: Restore PMU State and Exit to DOS

This option restores the ÉlanSC300 microcontroller's index registers to the value they were set to when the program was entered, and returns the user to the DOS prompt.

Z: Leave Current PMU Values and Exit to DOS

This option leaves the ÉlanSC300 microcontroller's index registers set at their current value, and returns the user to the DOS prompt.

EvalSet Serial and Parallel Port Setup Utility

EVALSET.EXE has been provided to allow easy activation of the serial and parallel ports on the ÉlanSC300 microcontroller evaluation board. The BIOS on this board was designed to be generic, therefore these functions are not enabled by the BIOS on the evaluation board. This utility can be used to set up the base addresses for serial port 1, serial port 2 and parallel port 1 on the evaluation board.

Serial Port 1

Serial Port 1 is the 16C450 UART internal to the ÉlanSC300 microcontroller. Its base address can be set to either 3f8h or 2f8h. The IRQ level can be set to either 3 or 4. If you enter a base address of 0, the internal UART is disabled. If you enter a valid base address but an IRQ of 0, then the UART is enabled but it is not attached to an interrupt line.

Examples

`evalset ser1 0x3f8 4`	Sets the internal UART to be COM1:
`evalset ser1 0x2f8 3`	Sets the internal UART to be COM2:
`evalset ser1 0 0`	Disables the internal UART

NOTE: Once the base address is set, the UART is programmed to 9600 baud, no parity, 8 data, 1 stop.

Serial Port 2

Serial Port 2 is connected to the 16C550 UART1 of the Super I/O chip (UART2 is not connected). Its base address can be set according to the table below. Note that if you want serial port 2 to generate an interrupt, only IRQ3 can be used. This is because IRQ4 from the Super I/O is not connected. However, the base addresses that are associated with an IRQ4 configuration can still be set as long as the port is used in polled mode.

IRQ	Base addresses
3	2f8, 2e8, 238, 2e0, 228
4 (polled only)	3f8, 3e8, 338, 2e8, 220

Examples

```
evalset ser2 0x2f8 3    Sets the Super I/O UART to be COM2:
evalset ser2 0 0        Disables the Super I/O UART
```

NOTE: Once the base address is set, the UART is programmed to 9600 baud, no parity, 8 data, 1 stop.

Parallel Port 1

This is the internal parallel port on the ÉlanSC300 microcontroller. Its base address can be set to 3b8h, 378h, or 278h. Along with setting the base address, the mode of the parallel port can also be set for EPP and Bidirectional modes.

NOTE: The parallel port base address is controlled through the Bus Configuration Registers (see the *ÉlanSC300 Microcontroller Programmer's Reference Manual*). These bus configuration registers can only be programmed before ISA or Local Bus accesses are made, so setting the parallel port base address or disabling the parallel port can only be done at boot time. In addition, the base address can only be set when in Internal Video mode. The parallel port base address is controlled through the internal video registers of the ÉlanSC300 microcontroller. If the internal video was disabled to support an external video card, then the parallel port base address does not change. Because the registers are write only, this program does not have a way to verify that the base address has been changed.

Examples

`evalset par1 0x3b8 epp_on bi_on`	Turns on EPP and Bidirectional modes.
`evalset par1 0x3b8 epp_off bi_off`	Turns off EPP and Bidirectional modes.

Usage

EVALSET.EXE can be called from the DOS prompt, **autoexec.bat** file, or **config.sys** file with the proper parameters.

config.sys Example

```
install=evalset.exe ser1 0x3f8 4
install=evalset.exe ser2 0x2f8 3
install=evalset.exe par1 0x3b8 epp_off bi_on
```

Memory Management System (MMS) Viewer Utility

1.1

This utility is part of the collateral for the ÉlanSC300 microcontroller. The ÉlanSC300 microcontroller is a highly integrated device with many subsystems. Many of these subsystems are unique to the ÉlanSC300. The purpose of the **MMSVIEW** utility is to provide the new ÉlanSC300 microcontroller user with the ability to explore the capabilities of the ÉlanSC300 MMS subsystem without having to invest much in the way of software development or chip register learning time.

Description

MMSVIEW is a DOS application that may be used to inspect various resources that are accessible by the ÉlanSC300 MMS subsystem. These resources include SYSTEM RAM, the BIOS ROM (or resources accessed by the $\overline{\text{ROMCS}}$ signal), the DOS ROM (or resources accessed by the $\overline{\text{DOSCS}}$ signal), or the PCMCIA slots. With this utility, the following operations may be performed:

- Directly display any region of the system RAM (0–16 Mbyte range), BIOS ROM (0–16 Mbyte range), DOS ROM (0–16 Mbyte range), and PCMCIA (0–64 Mbyte range).

- Step forward or backward through the data in 256-byte steps or 16-Kbyte steps.
- Select to view PCMCIA common or attribute memory.
- Choose between viewing data from PCMCIA slot 1 or slot 2.
- Select any ÉlanSC300 MMS page from MMSA to view system resources through.
- Fill areas of PCMCIA SRAM card memory or system RAM memory with a selected byte.
- Append the currently displayed page of data to a log file in either ASCII or binary formats.
- View DOS ROM using an 8- or 16-bit interface.
- Perform continuous read/compare operations from a selected resource, and indicate miscompares on the display.

Scope

MMSVIEW is provided to enable discovery and understanding of the capabilities of the ÉlanSC300 microcontroller MMS system. It has other uses such as looking at the contents of PCMCIA card attribute memory to view CIS (Card Information Structure) or common memory to view card data, filling areas of system RAM and PCMCIA SRAM cards, and looking at DOS ROM disks to ensure that the odd/even parts are placed in the sockets correctly, to name a few. It is not designed to be a comprehensive or automated diagnostic program, although its use may help in the debug of certain problems.

MMSVIEW uses MMSA only. To retain compatibility with systems using VGA video, MMSB was left outside the scope of this tool. It was designed on, tested on, and meant for use on the ÉlanSC300 microcontroller evaluation board revision 2.2 or later. The fact that it may run on other customer platforms is purely coincidental

NOTE: No support of any kind is provided for porting this utility to any platform other than the ÉlanSC300 microcontroller evaluation board revision 2.2 or later except by special agreement between AMD and the customer.

Operating Instructions

Command-Line Parameters

MMSVIEW assumes that MMS page 4 (resides at D0000h when MMS page 0 is set up to reside at C0000h) is available for use. This default may be overridden using a command-line parameter as shown below.

Syntax: MMSVIEW [*page*]

where:

page is a number from 0–7 to indicate the initial MMS page to view the system resources through.

If an invalid command-line parameter is detected (not a number, out of range, etc.) the default MMS page (4) is used. This option is provided to allow resolution of system address space conflicts that may occur when using this program while some other driver is loaded (EMM386, etc.).

There are no other command-line parameters available.

1.1

Initial State

After **MMSVIEW** has been invoked from the DOS command line, data is displayed in a fashion similar to DOS debug. MMSA page 4 at D0000h is selected, and the device that is accessed is system RAM. The first 256 bytes of the selected device are displayed starting at offset 0 (i.e., the start of the interrupt vector table at 0:0 in RAM.)

Keystroke Commands

Keystroke commands are invoked by simply pressing the keys noted below. Whenever a keystroke command requires user input, prompts request the required data. If a command that requires user input is to be aborted without invoking the command, press the Escape key, and the main data display returns. A command summary follows.

?

Pressing the question-mark key from the main data-display screen displays a quick help list of the keystroke commands available to the utility. Press the Space Bar from the quick help screen to return to the normal main display screen.

+

The plus key moves forward through the data 256 bytes at a time. The plus key thus makes it simple to view the next 100h bytes of data on the selected device.

–

The minus key performs the inverse operation of the plus key, and causes the previous 256 bytes of device data to be displayed. The program disallows negative addresses, and gives a warning click from the speaker if you press the minus key when the first address displayed on the screen is 0.

Home Key

The Home key displays the data at offset 0 on the current device.

Escape

The Escape key causes the utility to return control to the DOS prompt. *Note that no cleanup is done as the program exits, so it is recommended that the user COLD BOOT before performing any other important operations, especially if PCMCIA, ROMDOS, or EMM386 drivers were loaded on the system when MMSVIEW was invoked.*

Page Up

The Page Up key displays data on the *previous* 16-Kbyte boundary. For example, if the current device data starting at offset 4100h is being displayed, and Page Up is pressed, the data from device offset 0100h is displayed.

Page Down

The Page Down key does the inverse of the Page Up key; it displays data from the *next* 16-Kbyte boundary.

Space Bar

The Space Bar (or any key besides the other command keys listed in this section) simply rereads the data from the selected resource, and refreshes the main data display screen. The main data screen does not constantly update normally. If, for example, you are viewing PCMCIA PC Card Information Structure (CIS) data for one card, and you replace this card with another, the data printed on the screen does not automatically update. To view the data from the new card, press the Space Bar (or any other non-command key as specified in this list) to refresh the screen with the new data. For a continuous read mode, see the **c** command below.

a

The **a** key toggles between common and attribute memory for the current PCMCIA slot. When switching between slots using the **s** command, the state of the –REG line is remembered for each slot. This allows you to switch back and forth between the CIS of cards in slot A and slot B for comparison purposes.

c

The **c** key is useful for detecting changes in reading the data from a given resource. An example application for this feature is in the detection of timing problems (incorrect wait-state setup, etc.). When you press the **c** key, a "snapshot" of the current device data is taken, and stored into a local buffer. After this, continuous reads of the current device data are compared to the buffer. Miscompares cause the offending byte location to Flash, and the result of an Exclusive OR between the buffer (snapshot) and the current device data is displayed. This allows bit errors to be picked out easily.

Upon leaving Continuous Read/Compare mode, the blink attribute is removed from the characters for easier reading of the resulting data. The bytes which have the bit miscompares are left highlighted in white (versus light gray for the normal data). Any new command which causes the data to be read from the device again removes the highlight attribute from the displayed data completely. If the highlight attribute needs to be removed without losing the bit error data which may have been captured, the **r** command may be used (see below).

1.1

d

The **d** key selects which device the current MMS page points to. Pressing the **d** key causes the system to prompt for the new device. Enter a number from 0–3 (0 = DOS ROM, 1 = system RAM, 2 = PCMCIA, 3 = BIOS ROM), and press enter. Invalid input is not accepted. Once a new device has been entered, the main data display returns showing the data read from the selected device *at the current offset*. For example, if you are looking at the DOS ROM at offset 4000h, and you use the **d** command to select the BIOS ROM, the data displayed is from offset 4000h of the BIOS ROM.

f

The **f** command allows a range of memory to be filled with a user-selectable byte. Pressing the **f** command brings up prompts for the start and stop fill addresses, and requests the fill byte. Fill operations are available only when PCMCIA or RAM is the selected device. This command does not know how to write to Flash devices in a DOS ROM socket, or any PCMCIA card type other than SRAM.

g

The **g** command allows you to "go" to any place in the memory map desired. It is the random access equivalent to the plus and minus keys. It provides one additional benefit in that the data byte which resides at the address specified by the user to go to is highlighted for easy recognition.

i

The **i** key allows the DOS ROM interface to be toggled between the 8- and 16-bit interfaces supported on the ÉlanSC300 microcontroller. This is useful if running the utility on a hardware platform that has an 8-bit DOS ROM interface as opposed to the 16-bit DOS ROM interface on the ÉlanSC300 Microcontroller Evaluation Board.

l

The **l** command allows one screen's worth of data to be appended to a log. Successive screens can be captured to the same file in this manner. Pressing the **l** command prompts the user as to whether the output file should be a binary image of the data, or whether a DOS debug-like ASCII representation should be saved. If the binary option is chosen, data is logged to a file named **MMSVIEW.BIN**. If the ASCII option is selected, the output file is **MMSVIEW.ASC**.

n

The **n** command allows the user to select the use of a new MMS page (0–7). This can be useful in avoiding system conflicts. The default page can be changed before entering the program using the command-line capability to set this option as described on page 3-14.

p

The **p** command is essentially a **g** command that accepts its input in terms of 16K pages. In other words, you can randomly access data on specific 16-Kbyte boundaries using this command. For example, if you want to view the start of the first 16-Kbyte boundary of a device, select the **p** command, and input 0 when prompted to specify page 0. This can be done just as easily using the **g** command and supplying an address that's a multiple of 4000h.

r

The **r** command resets the miscompare indicators as explained earlier in the section that explains the **c** command. See the **c** command on page 3-16 for more detail.

s

The **s** command toggles between viewing data from PCMCIA slot 1 and slot 2. Each time the **s** command is pressed, the slot that is not currently being viewed becomes the active slot. This command only applies if the PCMCIA device is selected.

Restrictions on Use

Although designed for the ÉlanSC300 microcontroller evaluation board, this utility may work on other vendor's platforms. (However, its functionality outside of the ÉlanSC300 microcontroller evaluation board cannot be guaranteed and therefore is not supported.) There are three key elements for compatibility:

1. **MMSVIEW** assumes that MMSA is programmed to begin page 0 at C0000h. The starting location of MMSA is not reset by the utility in an attempt to maintain software compatibility with customer platforms as this would probably cause the customer's platform to crash. Use this utility on a customer platform only if customer-platform initialization programs MMSA page 0 to start at C0000h.
2. The second element of compatibility is the use of the MMS windows on the customer platform. **MMSVIEW** assumes that MMS page 4 (resides at D0000h when MMS page 0 is set up to reside at C0000h) is available for use. This may conflict with drivers loaded on the evaluation board platform that require the use of MMS (ROMDOS, PCMCIA, EMM386, etc.). It may also conflict with customer resources located on customer platforms. See "Operating Instructions" on page 3-14 for details on how to change MMS windows.
3. The third element of compatibility is not as major. **MMSVIEW** reprograms the I/O locations of the REGA and REGB signals to reside at 108h and 10Ch respectively (most BIOS ports to the ÉlanSC300 microcontroller set up these I/O addresses). These I/O locations are set up in this utility in case it is run on a vendor platform in order to achieve some level of software compatibility. When **MMSVIEW** exits, these locations cannot be reprogrammed back to the initial values because these registers are write only.

It is recommended that the test platform/evaluation system be “cold” booted (using reset button) after **MMSVIEW** exits so that the ÉlanSC300 microcontroller setup registers are restored to the proper values before doing further work on the platform. This is required not only on customer platforms, but on any ÉlanSC300 microcontroller evaluation board that has any PCMCIA, ROMDOS, EMM386, or other drivers installed that require use of the MMS, or memory regions that are controlled by the MMS. Again, **MMSVIEW** makes no attempt to restore the system to its initial state: *reset the system when finished*.

Use caution when selecting the MMS page to use. Selecting a page that causes conflicts with other system resources can lock the system. For example, using a VGA card in the ISA slot of the evaluation board, and selecting pages 0 or 1 of MMSA causes system conflicts since VGA BIOS decodes at C0000h for 32 Kbyte, and MMSA pages 0 and 1 also use that address space.

Register Dump Utility

This register dump utility has been provided for use on the ÉlanSC300 microcontroller evaluation board. It is intended to provide an easy-to-use register-manipulation program. This program displays the index registers in the ÉlanSC300 microcontroller, grouped by functionality:

- ÉlanSC300 PMU Registers Screen 1
- ÉlanSC300 PMU Registers Screen 2
- ÉlanSC300 PCMCIA Registers
- ÉlanSC300 MMU/ISA Registers

These registers can be read or written by simply entering a new value and pressing Return. Some registers do not allow full read/write access. Read-only registers display the contents of the register but do not allow the user to write a new value. Write-only registers allow a user to write a new value to the register. When a value is read from the register, it displays meaningless values. The following is a list of commands available in **REGDUMP.EXE**:

Arrow Keys	Move the cursor from register to register within the screen.
s	Toggles between the register screens.
v	Allows user to enter a new value for the selected register.
b	Switches the display to a bit-by-bit definition of the selected register.
m	Switches the display to an options menu screen.
p	Dumps all four register screens to an ASCII text file called **REGDUMP.LOG**.
q	Exits from **REGDUMP.EXE**.

NOTE: The register value display is read from the registers each time the screen is toggled. Since the display is not updated with each write, it is possible that a register could appear to be written to, but if it is a read-only register it remains unchanged. Please refer to the *ÉlanSC300 Microcontroller Programmer's Reference Manual* to determine if the register being manipulated has any read/write restrictions.

Chapter 4

Developing Code

This document is meant to aid the programmer who is developing BIOS code, Power Management code, PCMCIA code, etc. using the ÉlanSC300 microcontroller evaluation board. This evaluation board was designed to support a number of different system configurations (e.g., Full ISA Bus mode, Internal Video mode, Application ROM support, PCMCIA support, IDE drives, Floppy drive, etc.). This document explains how to configure the ÉlanSC300 microcontroller on the evaluation board in order to support these configurations.

See the following sections for more information:

For more information on the ÉlanSC300 microcontroller, see the *ÉlanSC300 Microcontroller Data Sheet* and the *ÉlanSC300 Microcontroller Programmer's Reference Manual*.

Programmable General Purpose (PGP) Pins

The ÉlanSC300 microcontroller has four Programmable General Purpose (PGP) pins which can be set up as inputs, outputs, address decodes, and address decodes that are gated with the I/O read or I/O write pulse.

Index registers for the PGP pins are write only. Keep this in mind when writing to Index 91h, which controls all PGP pins.

Remember, this particular implementation of the PGP pins is specific to the ÉlanSC300 microcontroller evaluation board *only*. Other system designs may implement these pins differently.

The ÉlanSC300 microcontroller evaluation board makes use of the PGP pins as follows.

PGP0

This pin in used to clock data from the data bus into three flip-flops that are used to control the programming voltage to the ROM and the PCMCIA sockets. PGP0 must be set up to gate with the I/O Write Command. This is done by setting the ÉlanSC300 Index 91h to xxxxxx10b. Index 89h is used to set up the I/O address for PGP0. Setting Index 89h to a 20h programs PGP0 to respond to writes to I/O addresses 100h–107h. PGP0 must also be enabled as an output. This is done by writing bit 6 of the ÉlanSC300 Index 70h to a 1. By programming this pin as just described, the ÉlanSC300 microcontroller is now able to write to the 3 bit register at I/O port 100h. When set up as described, the write-only register at I/O address 100 is as shown in the table below.

NOTE: This pin is referenced as PGPA on the evaluation board schematics beginning in “Schematics” on page D-1.

Table 4-1. I/O Address 100–107

Bit	Description
7–3	Reserved
2	1 = V_{pp} line to ROM sockets set to 12 V 0 = V_{pp} line to ROM sockets set to 5 V
1	1 = PCMCIA Socket 2 configured for 12 V 0 = PCMCIA Socket 2 configured for 5 V
0	1 = PCMCIA Socket 1 configured for 12 V 0 = PCMCIA Socket 1 configured for 5 V

PGP1

This pin is used as an address decode for the IDE $\overline{CS0}$. It should be programmed as an address decode for I/O addresses 1F0H–1F7H. Setting the ÉlanSC300 microcontroller's Index 91h to xxxx11xxb programs PGP1 as an address decode. Setting ÉlanSC300 Index 9Ch to 3Eh sets the address range to 1F0h–1F7h. PGP1 must also be enabled as an output for the evaluation board. This is done by setting Bit 2 of the ÉlanSC300 Index 74h.

NOTE: This pin is referenced as PGPB on the evaluation board schematics beginning in "Schematics" on page D-1.

PGP2

This pin is used as an address decode for the IDE $\overline{CS1}$. It should be programmed as an address decode for I/O addresses 3F0h–3F7h. Setting the ÉlanSC300 Index 91h to xx11xxxxb programs PGP2 as an address decode. Setting the ÉlanSC300 Index 94h to 7Eh sets the address range to 3F0h–3F7h.

NOTE: This pin is referenced as PGPC on the evaluation board schematics beginning in "Schematics" on page D-1.

PGP3

This pin has no specific function on the ÉlanSC300 microcontroller evaluation board.

NOTE: This pin is referenced as PGPD on the evaluation board schematics beginning in "Schematics" on page D-1.

Power Management Control (PMC) Pins

The ÉlanSC300 microcontroller has five Power Management Control (PMC) pins that can be programmed high or low based on the current power management mode. The ÉlanSC300 microcontroller evaluation board makes use of the PMC pins as follows.

PMC0

This pin is logically ORed with the system Reset pin from the ÉlanSC300 microcontroller (RSTDRV) and fed to the reset pin of the 8042 keyboard controller. It is used to perform a software reset to the 8042. A value of 1 drives the reset pin of the 8042 active. A value of 0 allows for normal operation. The ÉlanSC300 microcontroller Index ACh bits 3:0 control PMC0 and are set to 0 on power-up.

If you are not using PMU states that turn off the Low Speed PLL (i.e., Doze, Sleep or Suspend modes) then you do not need to change the settings for this pin. Refer to "8042 Keyboard Controller" on page 4-16 for a further explanation of when you need to do a software reset.

PMC1

This pin is ANDed together with the card detect from slot 1 of the unbuffered PCMCIA slot. It is used to control V_{CC} power to both the buffered and unbuffered PCMCIA slot 1. A value of 0 will cause V_{CC} power to be applied to PCMCIA slot 1 at all times. A value of 1 will disable V_{CC} power to PCMCIA slot 1 except for the case when a card is inserted into the unbuffered slot 1. In this case V_{CC} is applied to both buffered and unbuffered PCMCIA slot 1.

PMC1 Pin	PCMCIA Unbuffered Slot 1, Card Detect	V_{CC} Power to PCMCIA Unbuffered Slot 1	V_{CC} Power to PCMCIA Buffered Slot 1
0	Card present	5 V	5 V
1	Card present	5 V	5 V
0	Card not present	5 V	5 V
1	Card not present	Disabled	Disabled

PMC2

This pin is used to select whether the internal ÉlanSC300 microcontroller (serial port 1) and the Super I/O (serial port 2) are enabled for RS232 serial data (PMC2=1), or whether the IR Transmitter/Receiver pair is used to send and receive serial data on serial port 1, and serial port 2 transmission is disabled (PMC2=0). The ÉlanSC300 Indexes 80h and 81h control the state of PMC2.

PMC3

This pin is ANDed together with the card detect from slot 2 of the unbuffered PCMCIA slot. It is used to control V_{CC} power to both the buffered and unbuffered PCMCIA slot 2. A value of 0 will cause V_{CC} power to be applied to PCMCIA slot 2 at all times. A value of 1 will disable V_{CC} power to PCMCIA slot 2 except for the case when a card is inserted into the unbuffered slot 2. In this case V_{CC} is applied to both buffered and unbuffered PCMCIA slot 2.

PMC3 Pin	PCMCIA Unbuffered Slot 2, Card Detect	V_{CC} Power to PCMCIA Unbuffered Slot 2	V_{CC} Power to PCMCIA Buffered Slot 2
0	Card present	5 V	5 V
1	Card present	5 V	5 V
0	Card not present	5 V	5 V
1	Card not present	Disabled	Disabled

NOTE: PMC3 is different from the other PMC pins in that the value on the pin is the inverse of the value programmed into the ÉlanSC300 Index register ABh.

PMC4

This pin is used to mask the system reset pin from the 8042 keyboard controller that is fed to the Reset CPU pin ($\overline{RC}$) of the ÉlanSC300 microcontroller. A value of 1 holds the CPU's $\overline{RC}$ input High, and prevents the 8042 keyboard controller's reset output from reaching the CPU. A value of 0 allows for normal operation. The ÉlanSC300 Index ACh bits 3:0 control this pin and are set to 0 on power-up. If you are not using PMU states Doze, Sleep, Suspend or Off, then you do not need to change the settings for this pin.

Programming BIOS Flash/EPROM or Application Flash/EPROM

This section describes how to program a Flash or EPROM device located in the BIOS sockets (U20 or U59), and the application sockets (U16, U17, U18, U19). The following items need to be addressed:

- Controlling the programming voltage for 12-V parts such as the AMD 28F020A
- Enabling writes to the BIOS and application ROM sockets
- Address mapping of the Flash sockets
- Evaluation board jumper settings

Controlling V_{PP}

There is one control for the V_{pp} line for *all* BIOS and application ROM sockets (i.e., there is no way to individually control the V_{pp} line for each socket). As described in the section "Programmable General Purpose (PGP) Pins" on page 4-2, PGP0 is used to clock the flip flops that control the programming voltage to the ROM sockets. When Data Bit 2 is set to 1, V_{pp} is set to 12 V for all ROM sockets. See "Initialization Example for Flash Programming" on page 4-8.

1.1

Enabling Writes to the BIOS and Application ROM Sockets

Writes to the BIOS sockets and application sockets need to be specifically enabled (they are disabled by default). This is accomplished by setting to a 1 bits 6 and 5 of the ÉlanSC300 Index 62h.

NOTE: Accesses to the BIOS socket or application socket are ISA cycles plus the additional $\overline{\text{ROMCS}}$ or $\overline{\text{DOSCS}}$ signal going active. No special logic has been added to the evaluation board to stop a $\overline{\text{ROMCS}}$ or $\overline{\text{DOSCS}}$ cycle from going to the ISA bus. Because of this, if the ÉlanSC300 microcontroller is in Full ISA mode, an ISA card (such as a VGA card) set up to respond to a memory range interferes with cycles going to the application or BIOS sockets. For example, a VGA card with on-board BIOS responds to the address range from A0000h through C7FFFh. An access to the application ROM socket through the MMS page to an offset in this range causes both the VGA card and the application ROM to respond. The only way to avoid this is by either not accessing this range, or reworking the evaluation board.

Address Mapping of the Flash/EPROM Sockets

The BIOS sockets have an 8-bit interface. Only one socket (U20) or (U59) can be enabled depending on the setting of jumper JP32. Address lines A0–A17, 256K addressing, are connected to the socket. The BIOS ROM can be accessed for programming by either using an MMS page, or setting up a linear decode region (see the *ÉlanSC300 Microcontroller Programmer's Reference Manual*). Typically, an MMS page is used.

The application sockets have a 16-bit interface. If BIOS does not already enable the 16-bit interface, this needs to be done after boot-up by setting to a 1 bit 1 of the ÉlanSC300 Index 51h. Even addresses access sockets U16 and U18. Odd addresses access sockets U17 and U19. Support for both 256Kx8 Flash or EPROM, and 512Kx8 EPROM parts exists. Jumper JP13 controls which is selected.

NOTE: 512Kx8 Flash can be supported after a minor board rework. Contact your local AMD or distributor Field Application Engineer for more information.

When set for 256Kx8 parts: even addresses from 0–7FFFEh access socket U16; odd addresses from 1–7FFFFh access socket U17; even addresses from 80000h–FFFFEh access socket U18; and odd addresses from 80001h–FFFFFh access socket U19.

When set for 512Kx8 parts: even addresses from 0–FFFFEh access socket U16; odd addresses from 1–FFFFFh access socket U17; even addresses from 100000h–1FFFFEh access socket U18; and odd addresses from 100001h–1FFFFFh access socket U19. The application address space is accessed by using an MMS page or by enabling the linear decode for the application ROM. Using an MMS page is recommended because it can be accessed using real mode addressing.

Evaluation Board Jumper Settings

There are three jumpers which affect Flash programming on the ÉlanSC300 microcontroller evaluation board.

JP32: This jumper controls whether BIOS socket U20 (JP32=2-3) or socket U59 (JP32=1-2) is used.

JP12: This jumper must be set to 1-2 when Flash parts are used (JP12=2-3 indicates EPROM parts).

JP13: This jumper must be set to 1-2 to indicate 256Kx8 parts are in the application sockets. (JP13=2-3 indicates 512Kx8 parts, and 512Kx8 Flash is only supported after a minor board rework. Contact your local AMD or distributor Field Application Engineer for details.)

Initialization Example for Flash Programming

1. Set up PGP0 for I/O address 100h:

```
Elan Index 91H = 3Eh  ;sets up PGP0 to be gated with
                      I/O write, keep settings for PGP1 and 2
Elan Index 89H = 20h  ;set up PGP0 to respond to addresses
                       100-107.
Elan Index 70H = 40h; ;set up PGP0 as an output. Do a read,
                       modify, write, setting bit 6.
```

2. Enable writes to BIOS and application ROM:

```
Elan Index 62H = 70   ;set bits 6,5 = 1. Note: bit 4 = 1
                       assuming 33Mhz operation.
```

3. Enable 16-bit interface to application ROM:

```
Elan Index 51H = 02h   ;bit 1 =1, indicates 16-bit
                        application ROM size.
```

1.1

PCMCIA Programming Voltage

The ÉlanSC300 microcontroller provides a control for enabling and disabling the programming voltage to PCMCIA sockets 1 and 2. Control for selecting whether that programming voltage is 12 V or 5 V is handled by logic external to the ÉlanSC300. Bits 1 and 0 of the register connected to pin PGP0 of the ÉlanSC300 control this selection. (Refer to “Programmable General Purpose (PGP) Pins” on page 4-2 for more information.) Enable/Disable control for this voltage (V_{PP}) is done through I/O ports. The addresses for these I/O ports are set using the ÉlanSC300 Index register E8h for slot 0, and ECh for slot 1.

Assume the typical values of I/O port E8h (ÉlanSC300 Index 07h=3Ah) for controlling V_{PP} for slot 0; ECh (ÉlanSC300 Index 17h=3Bh) for controlling V_{PP} for slot 1; and 100h for access to the register clocked by PGP0 (see “PGP0” on page 4-2 for PGP0 setup).

With the above I/O addressed configured, in order to turn on 12 V_{PP} to slot 0, the following I/O writes would occur:

```
out 100h, 01h     ;set VPP for socket 0 to 12 volts,
                  socket 1 to 5 volts, VPP for ROM
                  sockets disabled.
out  E8h,  01h    ;enable VPP PCMCIA socket 0.
```

(perform write operation to PCMCIA card....)

```
out  E8h, 0h      ;disable VPP to socket 0
```

Evaluation Board's Memory Map

Because the ÉlanSC300 microcontroller and the evaluation board are so configurable, there is not one single memory map that covers all cases. What is illustrated here is a typical memory map for the evaluation board configured in Full ISA mode with a Trident VGA ISA card, ROM-DOS kernel, PCMCIA card and socket services, and 2 Mbyte DRAM.

Table 4-2. Typical Full ISA Memory Map

386 Physical Address	Memory Type Accessed	Special Notes
1FFFFFh–100000h	DRAM.	
FFFFFh–E0000h	BIOS ROM ($\overline{\text{ROMCS}}$). 64K BIOS image + ROM-DOS kernel.	$\overline{\text{ROMCS}}$ is set up for linear decode. May be shadowed to DRAM.
DFFFFh–D0000h	PCMCIA slots. Controlled by socket services.	MMSA page 4–7.
CFFFFh–CC000h	Application ROM ($\overline{\text{DOSCS}}$). Used by ROM-DOS.	MMSA page 3.
CBFFFh – C8000h	DRAM at offset C8000h–CBFFFh. Used for SMM save state area.	MMSA page 2.
C7FFFh–C0000h	ISA bus. VGA card 32K BIOS ROM.	MMSA pages 0 & 1. Disabled to allow accesses to pass through to ISA bus.
BFFFFh – A0000h	ISA bus. VGA card display buffers.	MMSB is disabled which allows accesses to propagate to ISA bus.
9FFFFh – 00000h	DRAM.	

NOTE:

1. In the above configuration, MMSB is disabled, and MMSA is defined to start at base address C0000h (i.e., ÉlanSC300 Index 6Dh=00).
2. MMSA pages 0 and 1 are disabled allowing accesses to the address range at C0000h–C7FFFFh to propagate to the ISA bus where the VGA BIOS is located.
3. Addresses E0000h–FFFFFh are set up as linear decodes to the BIOS ROM (Index 65h, bit 0=0, bit 1=1, bit 2=0, bit 3=0). During BIOS initialization, if shadowing is enabled (ÉlanSC300 Index 65h bit 4=1, ÉlanSC300 Index 69h=FFh), then accesses to this address range go to DRAM.
4. Refer to the *ÉlanSC300 Microcontroller Programmer's Reference Manual* for information on ROM BIOS and ROM DOS accesses using the MMS pages.

DOS ROM/Application ROM Mapping

The application ROM space (also known as DOS ROM space) is selected by the $\overline{\text{DOSCS}}$ chip select. Only 256Kx8 Flash parts are supported; 256Kx8 and 512Kx8 EPROMs are supported. JP12 selects between Flash/EPROM (1-2 = Flash, 2-3 = EPROM). JP13 selects between 256Kx8 and 512Kx8 parts (1-2 = 256K, 2-3 = 512K).

NOTE: 512Kx8 Flash can be supported after a minor board rework. Contact your local AMD or distributor Field Application Engineer for more information.

Access to the application ROM begins at offset 0h, and extends up to 1FFFFFh, depending on the size and number of parts installed. Application ROM is accessed through the MMS windows.

It is also possible to access linear decoded application ROM. This requires setting up ÉlanSC300 Index B8h. However, the processor must be set up to access memory above the 1 Mbyte boundary.

BIOS ROM Mapping

BIOS ROM mapping is similar to application ROM mapping. BIOS ROM is selected by the $\overline{\text{BIOSCS}}$ chip select. 128Kx8 and 256Kx8 Flash and EPROM devices are supported.

Access to the BIOS ROM begins at offset 0h, and extends up to 3FFFFh, depending on the size of the device. Typically the BIOS ROM is accessed through a linear decode set up for the address range E0000h through FFFFFh. This is set up using ÉlanSC300 Index register 65h. It is also possible to access the BIOS ROM using pages in the MMS windows.

Evaluation Board's I/O Map

Because the ÉlanSC300 microcontroller and the evaluation board are so configurable, there is not one single I/O map that covers all cases. What is illustrated here is a typical memory map for the evaluation board configured in Full ISA mode with the ÉlanSC300 microcontroller internal serial port enabled as COM1, the Super I/O floppy drive controller enabled, an IDE hard drive, and the Super I/O serial port enabled as COM2.

Table 4-3. Typical Full ISA I/O Map

I/O Address	Device Accessed	Special Notes
3F8h–3FFh	ÉlanSC300 internal 16C450 UART	
3F0h–3F7h	IDE drive CS1, Super I/O floppy drive controller	IDE CS1 selected using PGP2. Only addresses 3F6 and 3F7 bit 7 are used for IDE accesses.
3B0h–3DFh	Trident VGA card	3BCh–3BFh should be excluded from this range. They are used for parallel port accesses. Note this is a general address range. Not all I/O locations in this range are used.
3BCh–3BFh	ÉlanSC300 parallel port enabled as LPT1:	Other I/O ranges for the ÉlanSC300 parallel port are 378h–37Fh and 278h–27Fh.
398h–399h	Super I/O index and data ports	Used to enable Super I/O functions.
2F8h–2FFh	Super I/O serial port enabled as COM2	
1F0h–1F7h	IDE drive CS0	IDE CS0 selected using PGP1.
10Ch–10Fh	Socket 1 reg line control	Set up using ÉlanSC300 Index 9Eh = 42h.
108h–10Bh	Socket 0 reg line control	Set up using ÉlanSC300 Index 8Ah = 42h
100h–107h	PGP0 decode for V_{PP} control	Set up using ÉlanSC300 Index 89h. (Refer to "Programmable General Purpose (PGP) Pins" on page 4-2.)
ECh–EFh	Socket 1 V_{PP} enable control	Set up using ÉlanSC300 Index 17h = 3Bh.
E8h–EBh	Socket 0 V_{PP} enable control	Set up using ÉlanSC300 Index 07h = 3Ah

I/O Address	Device Accessed	Special Notes
C0h–DEh	DMA controller channels 4–7 (internal to the ÉlanSC300)	See 8237A Spec.
A0h, A1h	Programmable IRQ slave controller (internal to the ÉlanSC300)	See 8259 Spec.
92h	ÉlanSC300 internal gate A20 and reset control (internal to the ÉlanSC300)	Refer to the *ÉlanSC300 Microcontroller Programmer's Reference Manual*.
80h–8Fh	DMA page registers. Channels 0–7 (internal to the ÉlanSC300).	
70h–71h	RTC index and data registers (internal to the ÉlanSC300). NMI enable/disable (Bit 7 of Port 70).	MMSB is disabled which allows accesses to propagate to ISA bus.
60h, 64h	8042 keyboard control and data register	See 8042 Spec.
61h	Port B control (internal to the ÉlanSC300)	
40h–43h	Programmable timer registers (internal to the ÉlanSC300)	See 8254 Spec.
20h, 21h	Programmable IRQ master controller (internal to ÉlanSC300)	See 8259 Spec.
0h–Fh	DMA controller channels 0–3 (internal to the ÉlanSC300)	See 8237A Spec.

NOTE:

1. PCMCIA reg line control, PCMCIA V_{PP} enables and V_{PP} control I/O address can be set up for other I/O locations. This is just an example.
2. Except for the non-AT controls mentioned in note 1, all I/O addresses are at AT-compatible locations.

Evaluation Board's IRQ Mapping

Because the ÉlanSC300 microcontroller and the evaluation board are so configurable, there is not one single IRQ map that covers all cases. What is illustrated here is a typical memory map for the evaluation board configured in Full ISA mode with the ÉlanSC300 microcontroller internal serial port enabled as COM1, the Super I/O floppy drive controller enabled, an IDE hard drive, and the Super I/O serial port enabled as COM2.

Table 4-4. Typical Full ISA IRQ Mapping

IRQ	Device Assigned	Special Notes
15	Available for ISA bus or PCMCIA slots	
14	Connected to IDE interface	
13	Reserved	
12	Available for ISA bus or PCMCIA slots	
11	Available for ISA bus or PCMCIA slots	
10	Available for ISA bus or PCMCIA slots	
9	Available for ISA bus or PCMCIA slots	
8	ÉlanSC300 internal RTC interrupt	
7	ÉlanSC300 internal parallel port	
6	Super I/O floppy drive controller	
5	Available for ISA bus or PCMCIA slots	
4	Internal serial port; COM1	
3	Connected to Super I/O for COM2	Connects to IRQ3 pin on Super I/O
2	Used to cascade to Slave PIC (8259)	
1	Keyboard buffer full (driven by 8042)	
0	Timer 0 output (internal to ÉlanSC300)	Typically used for DOS Clock

NOTE:

1. IRQ lines 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 and 15 are available on the ISA bus and PCMCIA bus. Care must be taken so that cards on the ISA bus/PCMCIA bus do not use interrupts that conflict with internal ÉlanSC300 devices or each other.

Evaluation Board's DMA Mapping

The following table is the DMA mapping for the ÉlanSC300 microcontroller evaluation board.

Table 4-5. Typical Full ISA DMA Mapping

DMA	Device Assigned	Special Notes
7	ISA bus	16-bit I/O accesses
6	ISA bus	16-bit I/O accesses
5	ISA bus	16-bit I/O accesses
4	Reserved	Used to cascade DMA channels 0–3
3	ISA bus	8-bit I/O accesses
2	Super I/O floppy drive controller	8-bit I/O accesses
1	ISA bus	Also used for memory-to-memory transfers with DMA channel 0
0	ISA bus	Also used for memory-to-memory transfers with DMA channel 1

Evaluation Board's Components

8042 Keyboard Controller

The evaluation board uses a non-static 8042 keyboard controller. What this means to the programmer is that if SysCLK stops being driven to the 8042 for any period of time, the controller must be reset once SysCLK starts being driven again in order for the 8042 to function properly. The ÉlanSC300 microcontroller stops driving SysCLK any time the Low Speed PLL is disabled or when in Sleep, Suspend and Off PMU modes even if the Low Speed PLL is enabled for these modes. One side effect of not driving SysCLK to the 8042 is the RC pin from the 8042 will go active for a short period of time. This active state is latched by the ÉlanSC300 microcontroller. Therefore when the ÉlanSC300 microcontroller goes back to High Speed PLL mode from Sleep, Suspend or Off mode, the CPU is reset.

Note that the above conditions only apply to a non-static 8042. If a static 8042 is used, then these conditions don't apply.

To work around these situations, the evaluation board has been wired to use two pins on the ÉlanSC300 microcontroller to gate RC from the 8042 (PMC4) and to reset the 8042 (PMC0). PMC4 should be programmed to mask off the RC pin from the 8042 while in Sleep, Suspend, and Off modes to prevent the CPU from being reset due to SysCLK not being driven out of the ÉlanSC300. (If the Low Speed PLL is to be disabled in Doze mode then PMC4 should be driven for this mode as well.) When the system goes back to High Speed PLL mode, the 8042 needs to be reset by pulsing PMC0 high for 1 millisecond. Commands should also be issued to the 8042 to re-enable the keyboard. See "PMC0" on page 4-4 and "PMC4" on page 4-5 for more information.

National Super I/O PC87322VF

The Super I/O is set up to decode address 398h and 399h for its index and data registers.

When configuring the serial port on the Super I/O it is important to note that IRQ3 from the chip is connected to PIRQ0 on the ÉlanSC300 microcontroller. (Note: PIRQ0 on the ÉlanSC300 is internally set to IRQ3 when in Full ISA Bus mode; it is programmable in all other bus modes.) IRQ4 from the Super I/O is not connected. Therefore when configuring the serial port in the Super I/O, only configure it to use IRQ3. Also PMC2 must be set to 1 in order to enable the RS232 drivers for the serial port.

The Super I/O parallel port is not connected and therefore should not be enabled.

The floppy drive interface on the Super I/O is enabled. DMA channel 2 is used and the floppy IRQ is connected to PIRQ1 on the ÉlanSC300 microcontroller. (Note: PIRQ1 on the ÉlanSC300 is internally set to IRQ6 when in Full ISA Bus mode; it is programmable in all other bus modes.)

IDE Interface

An IDE drive can be directly connected to the ÉlanSC300 microcontroller. On the evaluation board, data bit 7 is routed through the Super I/O in order to properly handle bit 7 for I/O addresses 3F6 and 3F7, which are jointly used by the Floppy and the IDE interface. The IRQ line from the IDE connector is connected to IRQ14 on the ÉlanSC300 microcontroller. PGP1 is used for the IDE chip select 1 (I/O address 1f0–1F7h). PGP2 is used for IDE chip select 2 (I/O address 3f6–3f7). See “Connecting an IDE Hard Drive” on page 1-7 for the steps to connect the drive.

Enabling the ÉlanSC300 Internal Serial Port

The ÉlanSC300 microcontroller internal serial port is typically configured as COM1. The following ÉlanSC300 index registers need to be set for this configuration:

- Elan Index 77h = 90h ; Enable internal UART to base address 3F8 and IRQ 4 (COM1)
- Elan Index 92h = 01h ; Enable clock to UART
- Elan Index 48h = 02h ; Set for 16C450 compatibility
- Set pin PMC2 active for all PMU modes (refer to “Power Management Control (PMC) Pins” on page 4-4).

The UART’s I/O registers 3F8h–3FFh can now be accessed to perform serial transfers.

Appendix A

Evaluation Board Setup Summary

This appendix summarizes the jumper and switch settings of the ÉlanSC300 microcontroller evaluation board. For the location of these parts on the board, see Figure 2-1 on page 2-2.

Table A-1. Bus Mode Selection and Affected Jumpers

Bus Mode	Resistor Pack Setting	JP16		JP17		JP18	
		1-2	2-3	1-2	2-3	open	closed
Full ISA	Install RP1 & RP2 only	N/A	N/A	Connects IRQ3 from Super I/O	N/A	N/A	Connects IRQ12 from mouse
Internal Video	Install RP3 & RP4 only	LCD display	N/A	Connects IRQ3 from Super I/O	Connects IRQ12 from mouse	Allows FRM to LCD panel	Not allowed, must be open
Local Bus	Install RP5 & RP6 only	2x CPU clock	N/A	Connects IRQ3 from Super I/O	N/A	N/A	Connects IRQ12 from mouse

Table A-2. Configuration Jumpers

3 Position Jumpers	System Affected	1-2	2-3
JP9	System SRAM	N/A	Selects 512Kx8
JP12	DOS ROM & BIOS	Selects Flash	Selects EPROM device
JP13	DOS sockets	256Kx8	512Kx8[1]
JP16			
Local Bus mode	CPU clock	2x	N/A
Internal Video mode	Display device	LCD	N/A
JP17	Super I/O Serial Port PS/2 Mouse	Enables Super I/O serial port IRQ	Enables PS/2 mouse IRQ in Internal Video mode[2]
JP18	(see Table A-3 on page A-3)		
JP32	BIOS ROM socket	U59 (Phoenix)	U20 (SystemSoft)
JP34	Enable the unbuffered or buffered socket A	Enable unbuffered socket A	Enable buffered socket A
JP35	Enable the unbuffered or buffered socket B	Enable unbuffered socket B	Enable buffered socket B

1– 512Kx8 Flash can only be supported after a minor board rework. Contact your local AMD or distributor Field Application Engineer for more information

2– Cannot be set in Full ISA or Local Bus mode.

1.1

Table A-3. JP18 (takes on different functions depending on the bus mode selected)

Mode	Pin Setting	Function
ISA or Local bus	Closed	Enables PS/2 port (Connects IRQ12 from 8042 to IRQ12 on ÉlanSC300 Device)
Internal Video	Open	Pin 181 on ÉlanSC300 device functions as FRM in this mode

Table A-4. Switches

SW3:	**ON**	**OFF**
1	NC	NC
2	Connects $\overline{\text{VGARDY}}$ to $\overline{\text{VLRDYI}}$	Open
3	Connects $\overline{\text{VLRDYO}}$ to $\overline{\text{VLRDYI}}$	Open
4	NC	NC
SW4:	**ON**	**OFF**
1	Memory = 5 V	Memory = 3.3 V
2	Connects PIRQ1 to ÉlanSC300 device	Disconnects PIRQ1 from ÉlanSC300 device
3	Connects IRQ1 to ÉlanSC300 device	Disconnects IRQ1 from ÉlanSC300 device
4	$\overline{\text{BL1}}$ = GND	$\overline{\text{BL1}}$ = 5V
5	$\overline{\text{BL2}}$ = GND	$\overline{\text{BL2}}$ = 5V
6	$\overline{\text{BL3}}$ = GND	$\overline{\text{BL3}}$ = 5V
7	$\overline{\text{BL4}}$ = GND	$\overline{\text{BL4}}$ = 5V
8	ACIN = GND	ACIN = 5V

Table A-5. Power Measurement Jumpers

NOTE: Be sure to turn off system power before removing JP1–JP11. Replace JP1–11 before power-up or the system will not work.

Jumper	V_{CC}	Logic connected to V_{CC} plane
JP1	V_{CC}	ÉlanSC300 core V_{CC} only. Always 3.3 V.
JP2	V_{CC3}	ÉlanSC300 AV_{CC} pin. Analog V_{CC}. Always 3.3 V.
JP3	V_{CC5}	ÉlanSC300 V_{CC5} pin. Diode clamp refs except V_{CCMEM} and AV_{CC} source pins. Always 5 V except in full 3.3-V designs. (Evaluation board limits to 5 V.)
JP4	V_{CCMEM}	ÉlanSC300 memory interface V_{CC}. See the SW4 table on page 2-21 for 3.3-V or 5-V setting. Restrictions do apply. Also the diode clamp ref for pins sourced to the V_{CCMEM} pin.
JP5	V_{CCSYS}	ÉlanSC300 ISA bus V_{CC} and other misc. pins. 5 V or 3.3 V. Refer to datasheet for details.
JP6	V_{CCSYS2}	ÉlanSC300 alternate pin V_{CC}. 5 V or 3.3 V. Refer to datasheet for details.
JP7	$V_{CCMEM53}$	System DRAM V_{CC} plane.
JP8	V_{CCSRAM}	System SRAM V_{CC} plane.
JP10	V_{CCKBOS}	8042 V_{CC}
JP11	V_{CCROM}	BIOS and Application ROM V_{CC}
JP19	V_{CC1}	ÉlanSC300 V_{CC1} pin 176. 5 V or 3.3 V.

1.1

Appendix B

Verified Peripherals

This a list of peripherals that have been verified to work on the ÉlanSC300 microcontroller evaluation board:

Peripheral	Manufacturer	Model #
Floppy Drive	Mitsumi	D359T3
	TEAC	FD-235HF
Hard Drive*	Quantum	ProDrive LPS series
	Western Digital	Caviar series
Power Supply	DTK Computer Inc.	PIP-151
	TransWorld	TW-1800R
	Jabert	WE-D250
Keyboard	Keytronic	KT2000 series
	Mitsumi	KPQ-E99YC
VGA Monitor	CTX	6439
	NEC MultiSync	5FGE
Video Card	AVED	AV540
	Trident	TVGA 9000I
PCMCIA	MiniStor Hard Disk	
	IBM Hard Disk	
	SunDisk ATA	
	Xircom Corporate Ethernet	
	TDK LAN X Ethernet	
	Intel FAX/Modems	
	Various SRAM cards	
LCD Panels	Sharp	LM32K10 – 320x240
		LM48014F – 480x320
	Epson	TCM-A0717 – 480x320
		TCM-A0709-1 – 480x320
	Casio	MD253TS01-00 – 640x200

*– Note that Connor and Fujitsu hard drives do not work with this board.

Appendix C

Board Layout Suggestions

The following suggestions concern the ÉlanSC300 microcontroller evaluation board layout strategy for the 32-kHz oscillator, the PLLs, and the power supplies. The goal is to minimize noise and noise coupling associated with the way the board is laid out. Special care is needed to minimize board leakages which can be fatal to pins that are sensitive to leakage currents, such as the two crystal oscillator pins, XTAl1 and XTAL2.

32-kHz Oscillator

Prudent board layout for the 32-kHz oscillator suggests the following precautions:

- Keep the two traces, XTAL1 and XTAL2, as short as possible, especially the input trace, XTAL1. XTAL1 is extremely sensitive to leakage. Total leakage from/to XTAL1 to/from all the pins on the board must be kept under 300 nA. XTAL2 can tolerate a leakage as high as 900 nA.
- Keep all noisy signals (e.g., PLL outputs and other clocking signals) as far away from XTAL1 and XTAL2 as possible. Again, XTAL1 is much more sensitive to noise coupling than XTAL2.
- Minimize parasitic capacitance between XTAL1 and XTAL2; even a few picofarads can potentially cause the oscillation frequency to be off target.
- Do not use a feedback resistor larger than 20 MΩ; it may fail to start up if the leakage at XTAL1 is equivalent to 5MΩ or less. The feedback resistor value can be lowered to counter leakage at XTAL1, but that increases start-up time. The lower bound for the feedback resistor should be about 10 MΩ.
- The capacitors connected between XTAL1, XTAL2, and analog ground should be between 15 pF and 30 pF, and they should be about equal in value. Increasing the two capacitor values increases start-up time and power consumption, but it does reduce noise coupling into XTAL1 and XTAL2.

Phase-Locked Loops

Board layout considerations for the four PLLs suggest the following precautions:

- Keep the output traces for the four PLLs as short as possible and keep them as far away from each other (and other clocking signals) as possible.
- Do not exceed the specified AC loading for the four PLL outputs. Certainly no DC loading is allowed since they are all CMOS logic outputs. If the PLLs have to drive more load than they are designed for in the actual application, make sure they are properly buffered on the board.

Power Supplies

Board layout considerations for the power supplies suggest the following precautions:

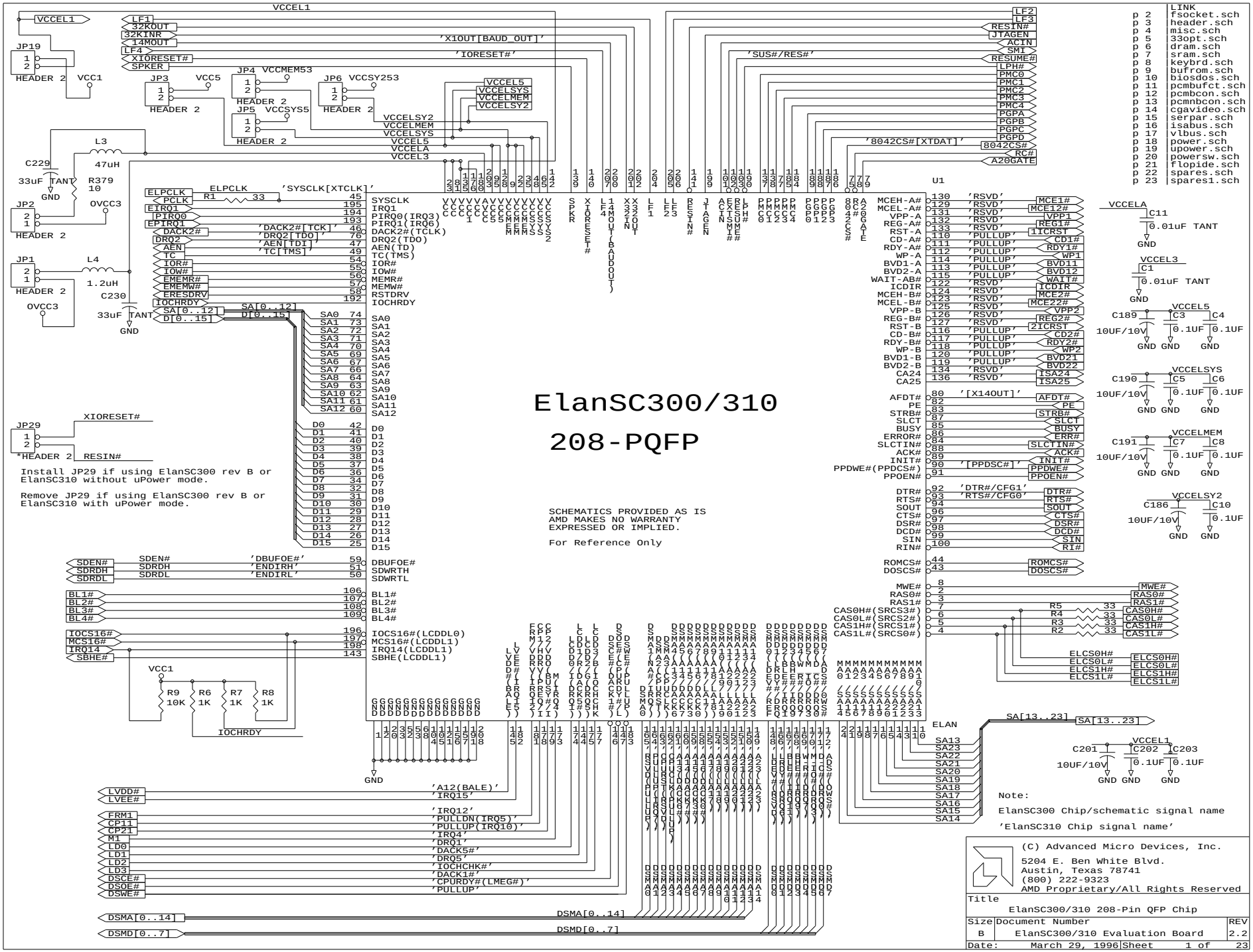
- Bring the analog V_{CC} and digital V_{CC} on separate traces from the output of the voltage regulator to the ÉlanSC300 microcontroller; making sure the traces are thick and wide. Filter the analog V_{CC} with an RLC second-order low-pass filter (e.g., R= 10 Ω, L=47 μH, C=33 μF). Since the digital V_{CC} carries much more current than the analog V_{CC}, a second order LC low-pass filter should be used instead (i.e., the series resistor should be removed). A small capacitor in the order of a few nanofarads can be added in parallel to the large filter capacitor to suppress high-frequency noise.
- Isolate the analog ground plane from the digital ground plane on the board, and connect them after decoupling.

1.1

Appendix D

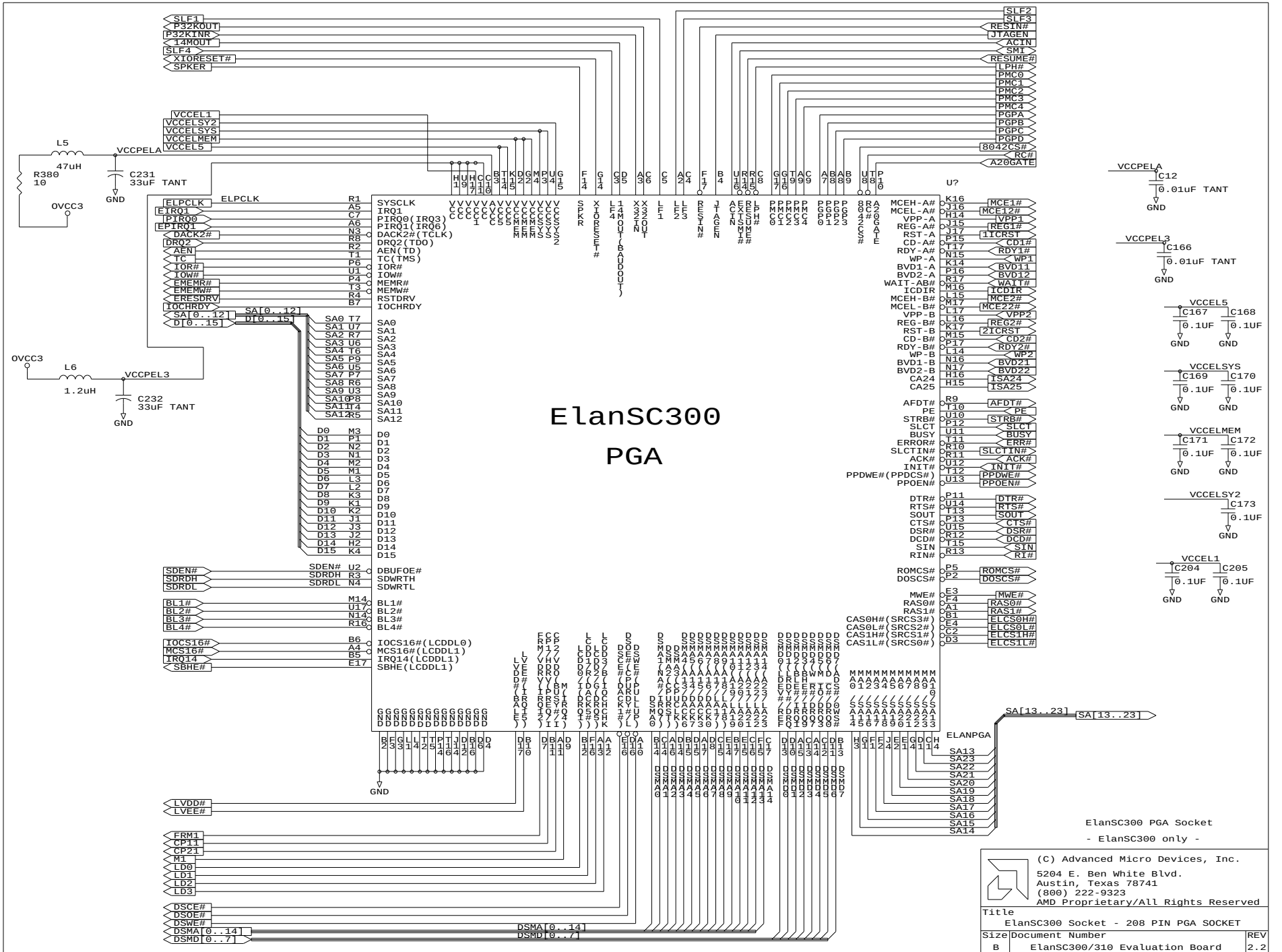
Schematics

The schematics beginning on page D-2 are the actual Orcad schematics used to build the ÉlanSC300 microcontroller evaluation board. These schematics are useful for understanding and modifying the evaluation board. Since the evaluation board incorporates many different possible configurations for the ÉlanSC300 microcontroller, these schematics are not a good place to start for actual ÉlanSC300 microcontroller-based designs. See the Local Bus Reference Design Schematics beginning on page D-25 and the Internal Video Reference Design Schematics beginning on page D-41 for ÉlanSC300 design examples. Note that these reference designs are meant for reference only. Since they have not been built, AMD cannot guarantee functionality.



LINK

p 2 fsocket.sch
p 3 header.sch
p 4 misc.sch
p 5 33opt.sch
p 6 dram.sch
p 7 sram.sch
p 8 keybrd.sch
p 9 bufrom.sch
p 10 biosdos.sch
p 11 pcmbufct.sch
p 12 pcmbcon.sch
p 13 pcmnbcon.sch
p 14 cgavideo.sch
p 15 serpar.sch
p 16 isabus.sch
p 17 vlbus.sch
p 18 power.sch
p 19 upower.sch
p 20 powersw.sch
p 21 flopide.sch
p 22 spares.sch
p 23 spares1.sch


ElanSC300
PGA
U?
SLF1
P32KOUT
P32KINR
14MOUT
SLF4
XIORESET#
SPKER
SLF2
SLF3
RESIN#
JTAGEN
ACIN
SMI
RESUME#
LPH#
PMC0
PMC1
PMC2
PMC3
PMC4
PGPA
PGPB
PGPC
PGPD
8042CS#
RC#
A20GATE
VCCEL1
VCCELSY2
VCCELSYS
VCCELMEM
VCCEL5
L5
47uH
R380
10
VCCPELA
C231
33uF TANT
GND
OVCC3
L6
1.2uH
VCCPEL3
C232
33uF TANT
C12
0.01uF TANT
C166
0.01uF TANT
C167
C168
C169
C170
C171
C172
C173
C204
C205
0.1uF
VCCELSY2
VCCEL1
ELPCLK
EIRQ1
PIRQ0
EPIRQ1
DACK2#
DRQ2
AEN
TC
IOR#
IOW#
EMEMR#
EMEMW#
ERESDRV
IOCHRDY
SA[0..12]
D[0..15]
SYSCLK
IRQ1
PIRQ0(IRQ3)
PIRQ1(IRQ6)
DACK2#(TCLK)
DRQ2(TDO)
AEN(TD)
TC(TMS)
IOR#
IOW#
MEMR#
MEMW#
RSTDRV
IOCHRDY
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
SDEN#
SDRDH
SDRDL
DBUFOE#
SDWRTH
SDWRTL
BL1#
BL2#
BL3#
BL4#
IOCS16#
MCS16#
IRQ14
SBHE#
IOCS16#(LCDDL0)
MCS16#(LCDDL1)
IRQ14(LCDDL1)
SBHE(LCDDL1)
SPKR
XIORESET#
LF4MOUT(BAUDOUT)
X32IOUT
LF1
RESIN#
JTAGEN
MCEH-A#
MCEL-A#
VPP-A
REG-A#
RST-A
CD-A#
RDY-A#
WP-A
BVD1-A
BVD2-A
WAIT-AB#
ICDIR
MCEH-B#
MCEL-B#
VPP-B
REG-B#
RST-B
CD-B#
RDY-B#
WP-B
BVD1-B
BVD2-B
CA24
CA25
AFDT#
PE
STRB#
SLCT
BUSY
ERROR#
SLCTIN#
ACK#
INIT#
PPDWE#(PPDCS#)
PPOEN#
DTR#
RTS#
SOUT
CTS#
DSR#
DCD#
SIN
RIN#
ROMCS#
DOSCS#
MWE#
RAS0#
RAS1#
CAS0H#(SRCS3#)
CAS0L#(SRCS2#)
CAS1H#(SRCS1#)
CAS1L#(SRCS0#)
MCE1#
MCE1#
VPP1
REG1#
1ICRST
CD1#
RDY1#
WP1
BVD11
BVD12
WAIT#
ICDIR
MCE2#
MCE22#
VPP2
REG2#
2ICRST
CD2#
RDY2#
WP2
BVD21
BVD22
ISA24
ISA25
AFDT#
PE
STRB#
SLCT
BUSY
ERR#
SLCTIN#
ACK#
INIT#
PPDWE#
PPOEN#
DTR#
RTS#
SOUT
CTS#
DSR#
DCD#
SIN
RI#
ROMCS#
DOSCS#
MWE#
RAS0#
RAS1#
ELCS0H#
ELCS0L#
ELCS1H#
ELCS1L#
SA[13..23]
ELANPGA
SA13
SA23
SA22
SA21
SA20
SA19
SA18
SA17
SA16
SA15
SA14
LVDD#
LVEE#
FRM1
CP11
CP21
M1
LD0
LD1
LD2
LD3
DSCE#
DSOE#
DSWE#
DSMA[0..14]
DSMD[0..7]
ElanSC300 PGA Socket
- ElanSC300 only -
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(800) 222-9323
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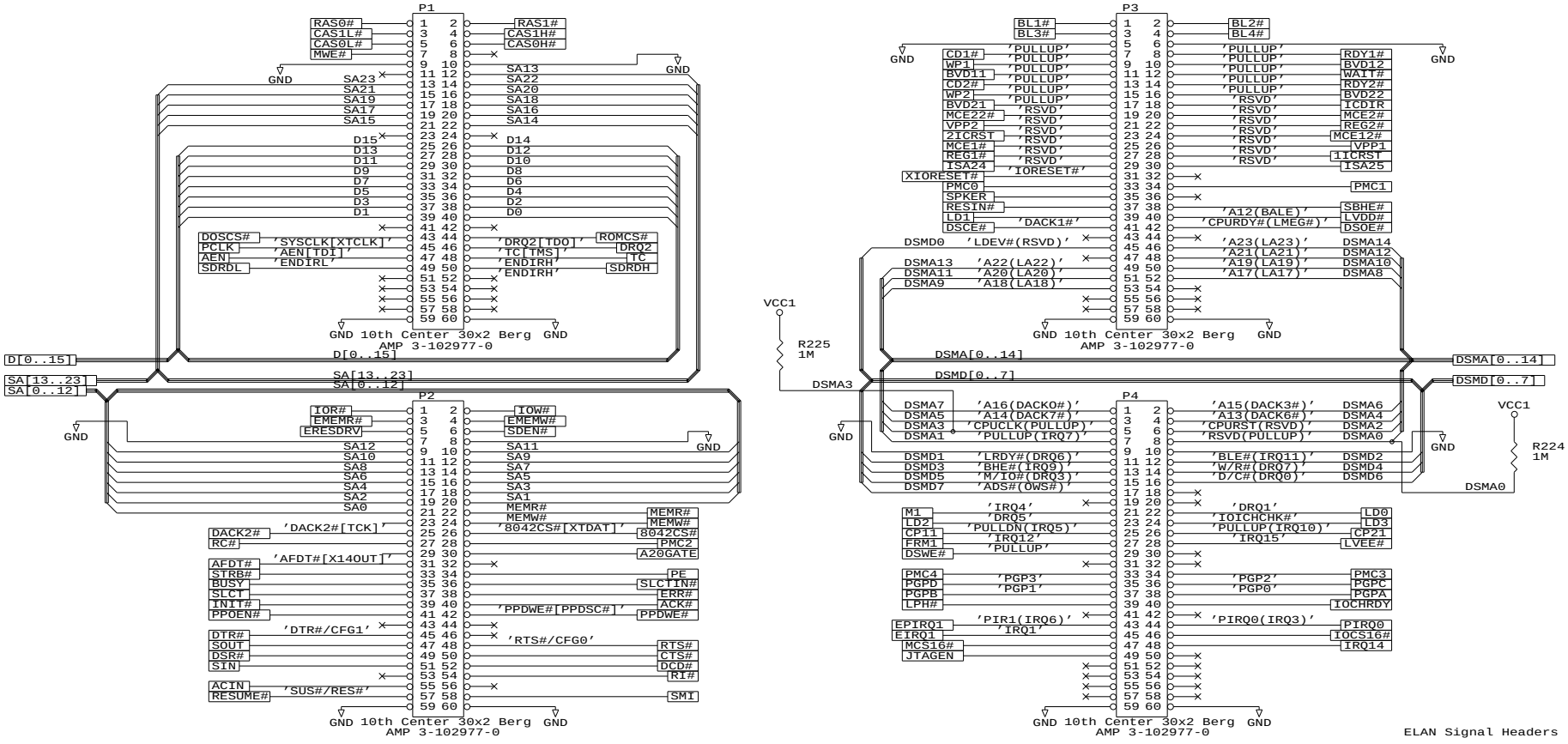
Title
ElanSC300 Socket - 208 PIN PGA SOCKET
Size B
Document Number ElanSC300/310 Evaluation Board
REV 2.2
Date: March 29, 1996
Sheet 2 of 23



Note:

ElanSC300 Chip/schematic signal name

'ElanSC310 Chip signal name'

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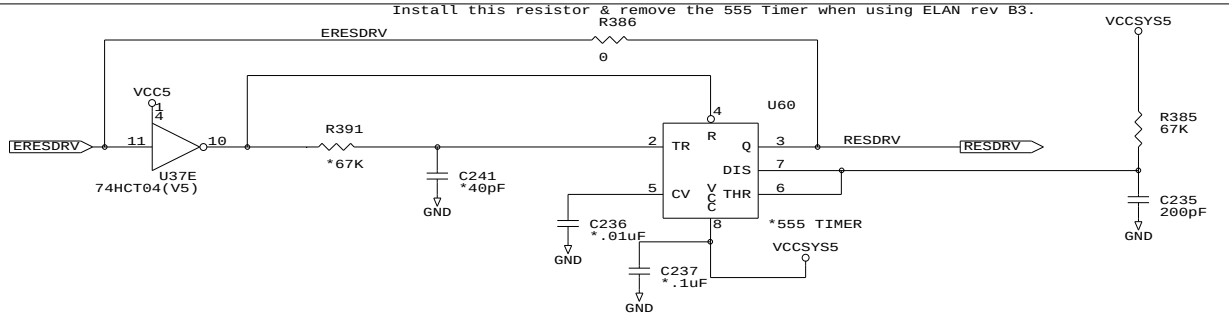
Title		
Debug Headers		
Size	Document Number	REV
B	ElanSC300/310 Evaluation Board	2.2
Date: March 29, 1996	Sheet 3 of 23	

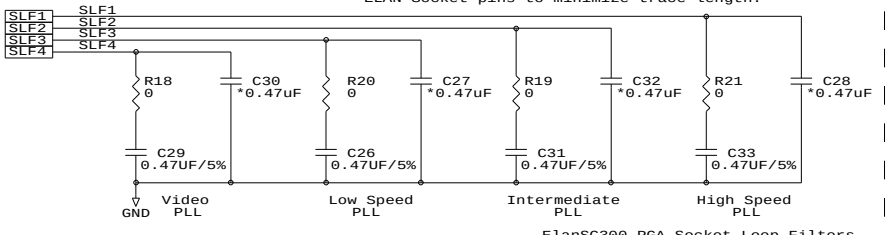
Install this resistor & remove the 555 Timer when using ELAN rev B3.



Note: (ElanSC300 only)
The 555 Timer is configured to function as a one-shot. ElanSC300 revs B1 & B2 deliver a short RESDRV pulse when exiting uPower OFF mode which could cause some issues. That is the reason for this one-shot. The ElanSC300 rev B3 device will address this issue & the one-shot is not needed.

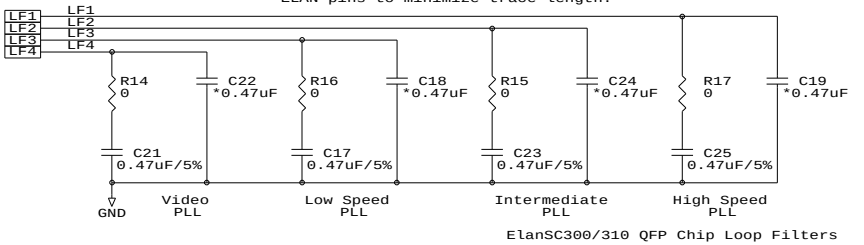
- ElanSC300 only -

NOTE
Place these componments close to the ELAN Socket pins to minimize trace length.

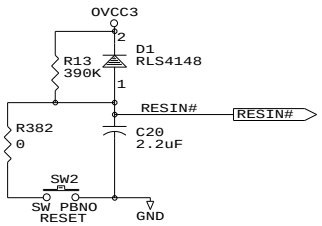


ElanSC300 PGA Socket Loop Filters

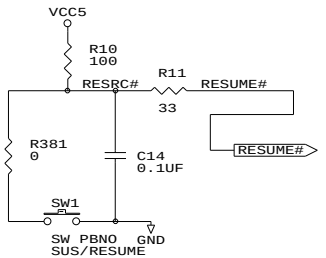
NOTE
Place these componments close to the ELAN pins to minimize trace length.



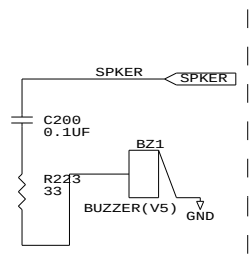
ElanSC300/310 QFP Chip Loop Filters



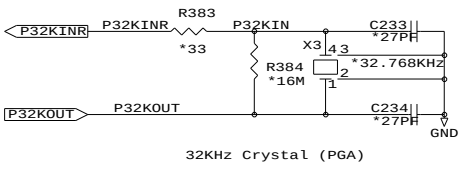
Reset Switch



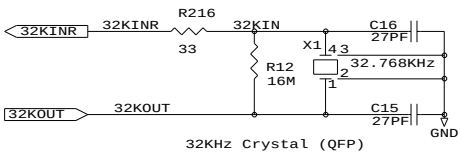
Suspend/Resume Switch



System Speaker



32KHz Crystal (PGA)



32KHz Crystal (QFP)

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Title	XTAL,SWITCHES,LOOP FILTER COMPONENTS,SPEAKER	
Size	Document Number	REV
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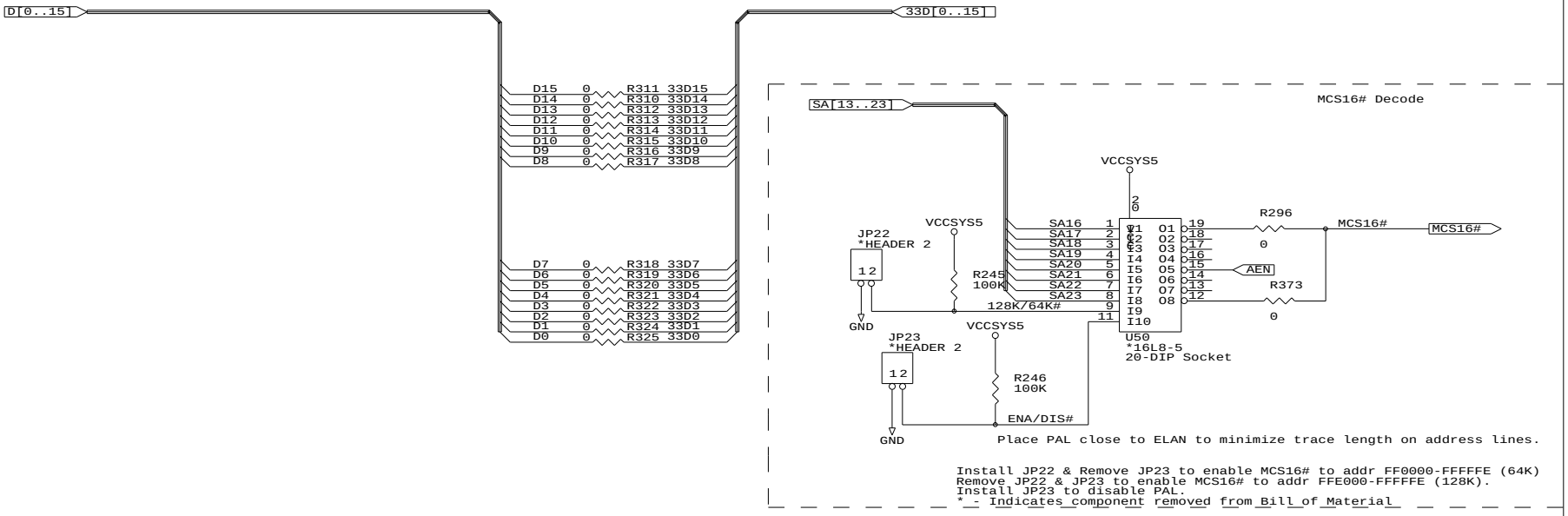
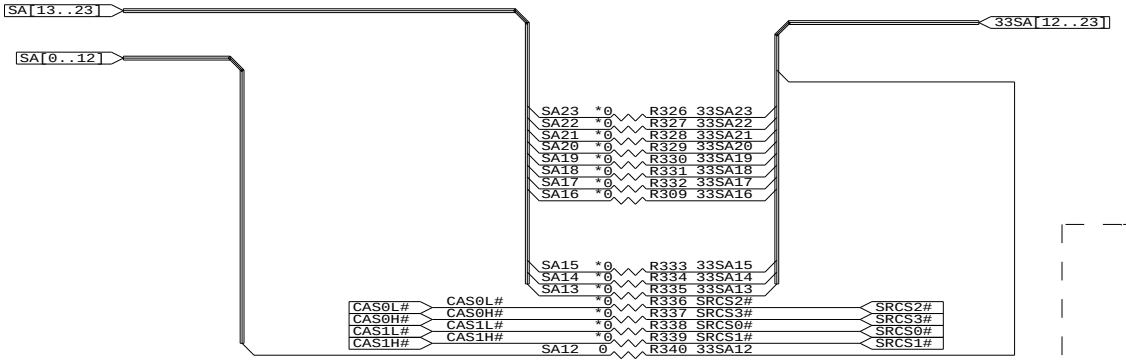
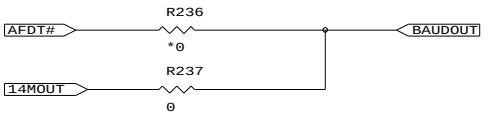
Date: March 29, 1996	Sheet 4 of 23	







Note: (only one resistor can be populated).

If using ElanSC300 rev B or ElanSC310 without the parallel port, install R236 and depop R237.

If using ElanSC300 rev B or ElanSC310 with the parallel port, install R237 and depop R236.

If using ElanSC300 rev A, always install R237 and Depop R236.

* - Note: if using ElanSC310, do not populate R309 and R326 - R339.

ElanSC300 Only: Place Resistors R309-R340 as close as possible to ELAN.
Depop Resistors R309-R340 when running internal CGA mode at 33 MHZ to minimize capacitive loading on DRAM signals.
Removing Resistors will disable local bus video connector and SRAM sockets.

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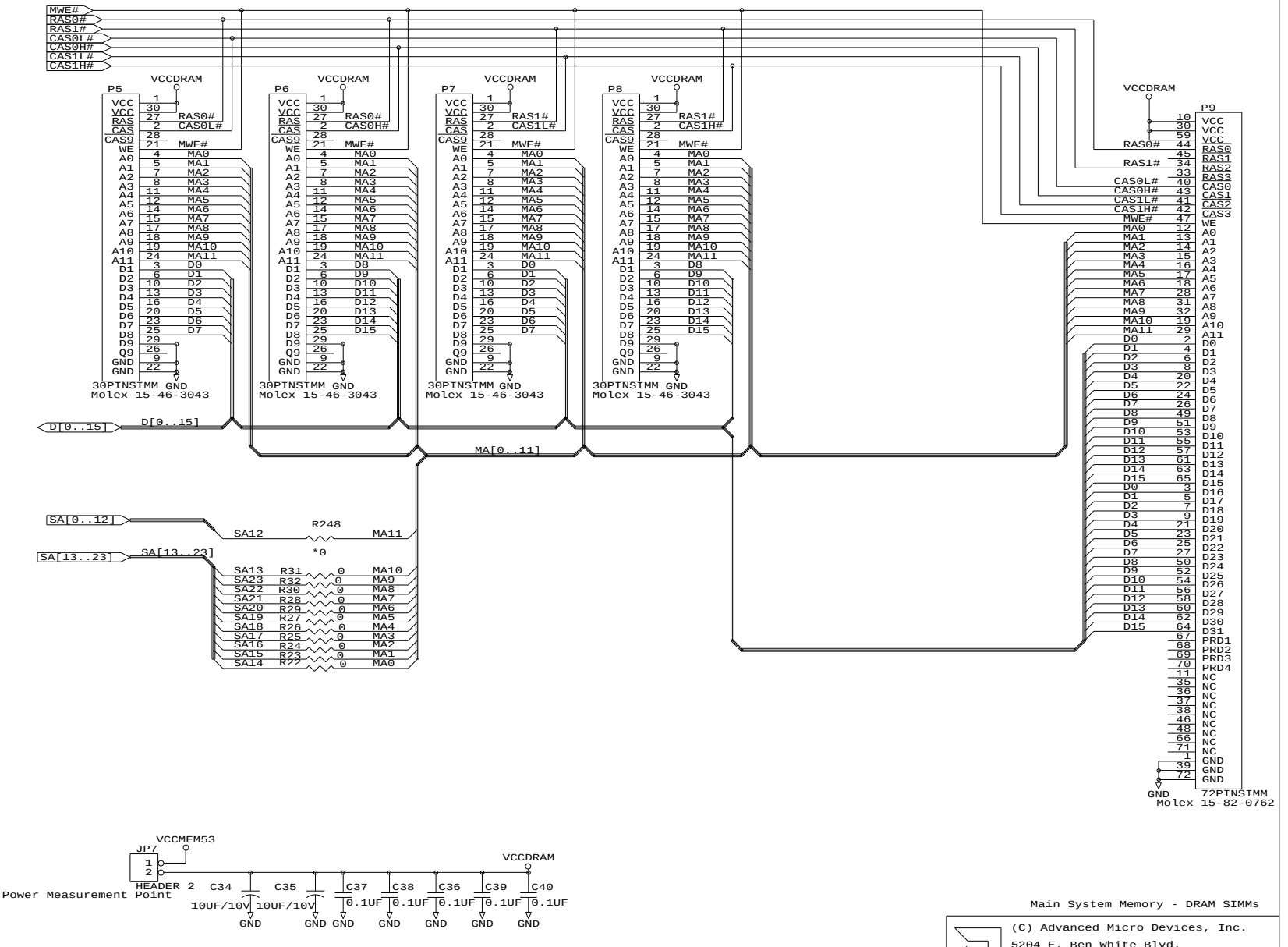
Title
33 MHz RPAK option,MCS16# decode,BAUDOUT opt

Size	Document Number	REV
B	ElanSC300/310 Evaluation Board	2.2

Date: March 29, 1996 Sheet 5 of 23



Main System Memory - DRAM SIMMs

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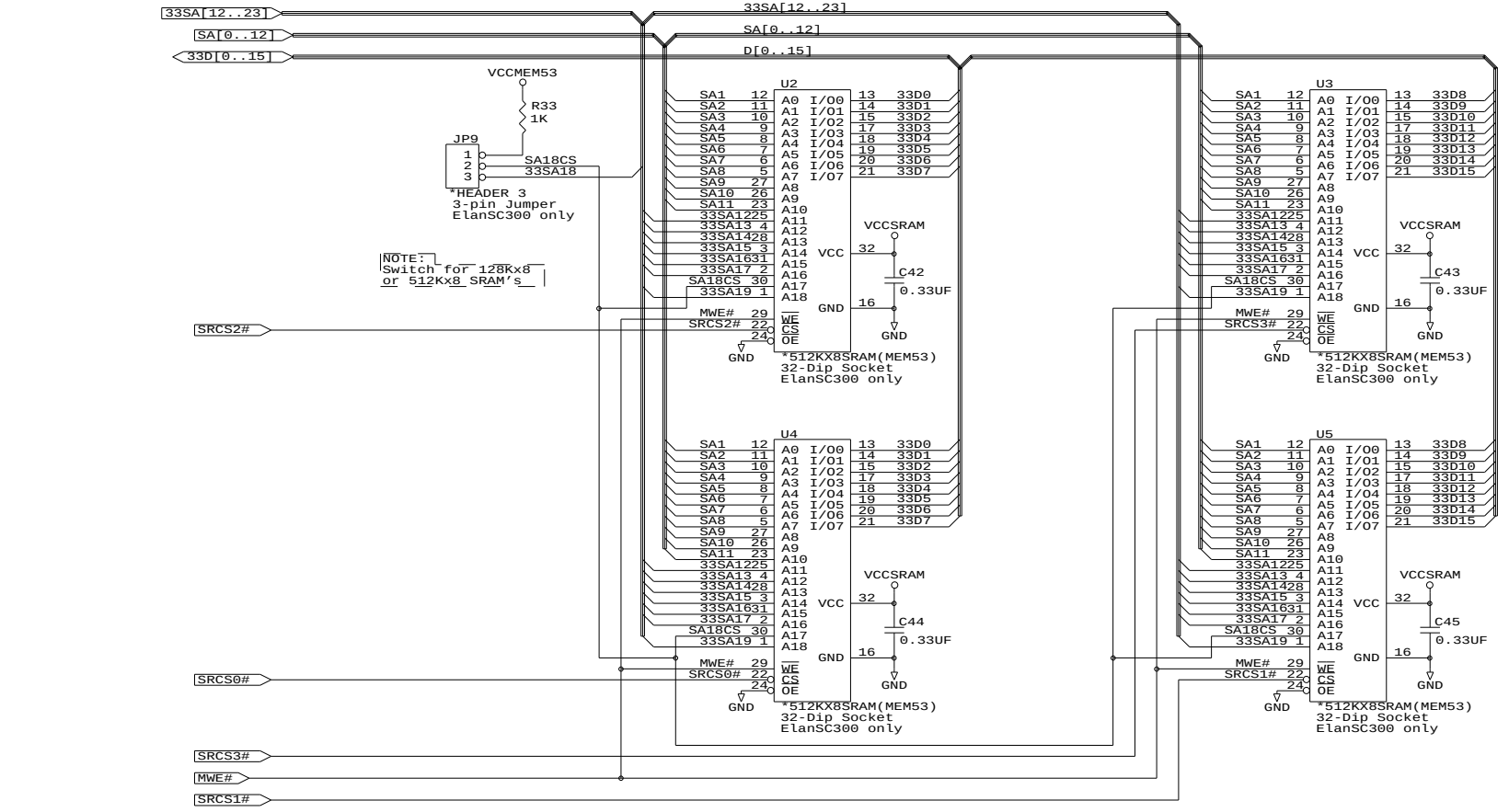
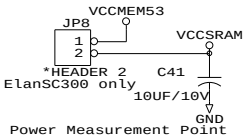
Title		
DRAM Main Memory SIMMS		
Size	Document Number	REV
B	ElanSC300/310 Evaluation Board	2.2
Date: March 29, 1996	Sheet 6 of 23	



* - Note: If using ElanSC310, do not populate: U2 - U5, JP8, JP9



Main System Memory - SRAM

- ElanSC300 only -

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Title		
SRAM Main Memory		
Size	Document Number	REV
B	ElanSC300/310 Evaluation Board	2.2
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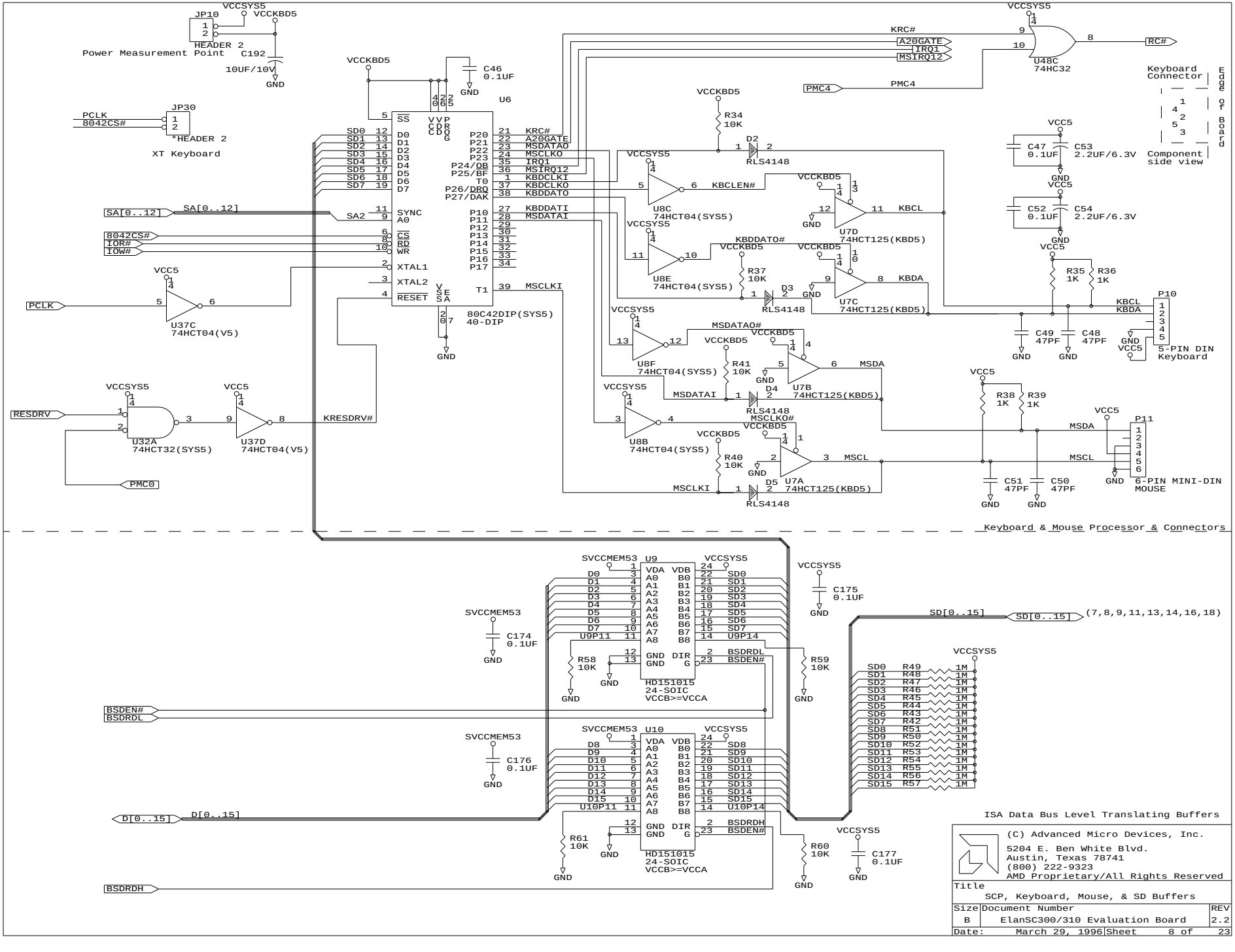
JP10
VCCSYS5
VCCKBD5
HEADER 2
Power Measurement Point
C192
10UF/10V
GND
JP30
PCLK
8042CS#
*HEADER 2
XT Keyboard
U6
80C42DIP(SYS5)
40-DIP
SA[0..12]
8042CS#
IOR#
IOW#
RESDRV
PMC0
U32A
74HCT32(SYS5)
U37D
74HCT04(V5)
U37C
74HCT04(V5)
KRESDRV#
C46
0.1UF
KRC#
A20GATE
IRQ1
MSIRQ12
U48C
74HC32
RC#
PMC4
Keyboard Connector
Edge of Board
Component side view
R34
10K
D2
RLS4148
U8C
74HCT04(SYS5)
KBCLEN#
U7D
74HCT125(KBD5)
KBCL
KBDDATO#
R37
10K
D3
U8E
74HCT04(SYS5)
U7C
74HCT125(KBD5)
KBDA
MSDATAO#
R41
10K
D4
U8F
74HCT04(SYS5)
U7B
74HCT125(KBD5)
MSDA
MSDATAI
MSCLKO#
R40
10K
D5
U8B
74HCT04(SYS5)
U7A
74HCT125(KBD5)
MSCL
MSCLKI
C47
0.1UF
C53
2.2UF/6.3V
C52
0.1UF
C54
2.2UF/6.3V
R35
1K
R36
1K
C49
47PF
C48
47PF
P10
5-PIN DIN Keyboard
R38
1K
R39
1K
C51
47PF
C50
47PF
P11
6-PIN MINI-DIN MOUSE
Keyboard & Mouse Processor & Connectors
U9
U10
HD151015
24-SOIC
VCCB>=VCCA
SVCCMEM53
C174
0.1UF
C175
0.1UF
C176
0.1UF
C177
0.1UF
R58
10K
R59
10K
R61
10K
R60
10K
BSDEN#
BSDRDL
BSDRDH
D[0..15]
SD[0..15]
SD[0..15] (7,8,9,11,13,14,16,18)
R49
1M
R48
1M
R47
1M
R46
1M
R45
1M
R44
1M
R43
1M
R42
1M
R51
1M
R50
1M
R52
1M
R53
1M
R54
1M
R55
1M
R56
1M
R57
1M
ISA Data Bus Level Translating Buffers
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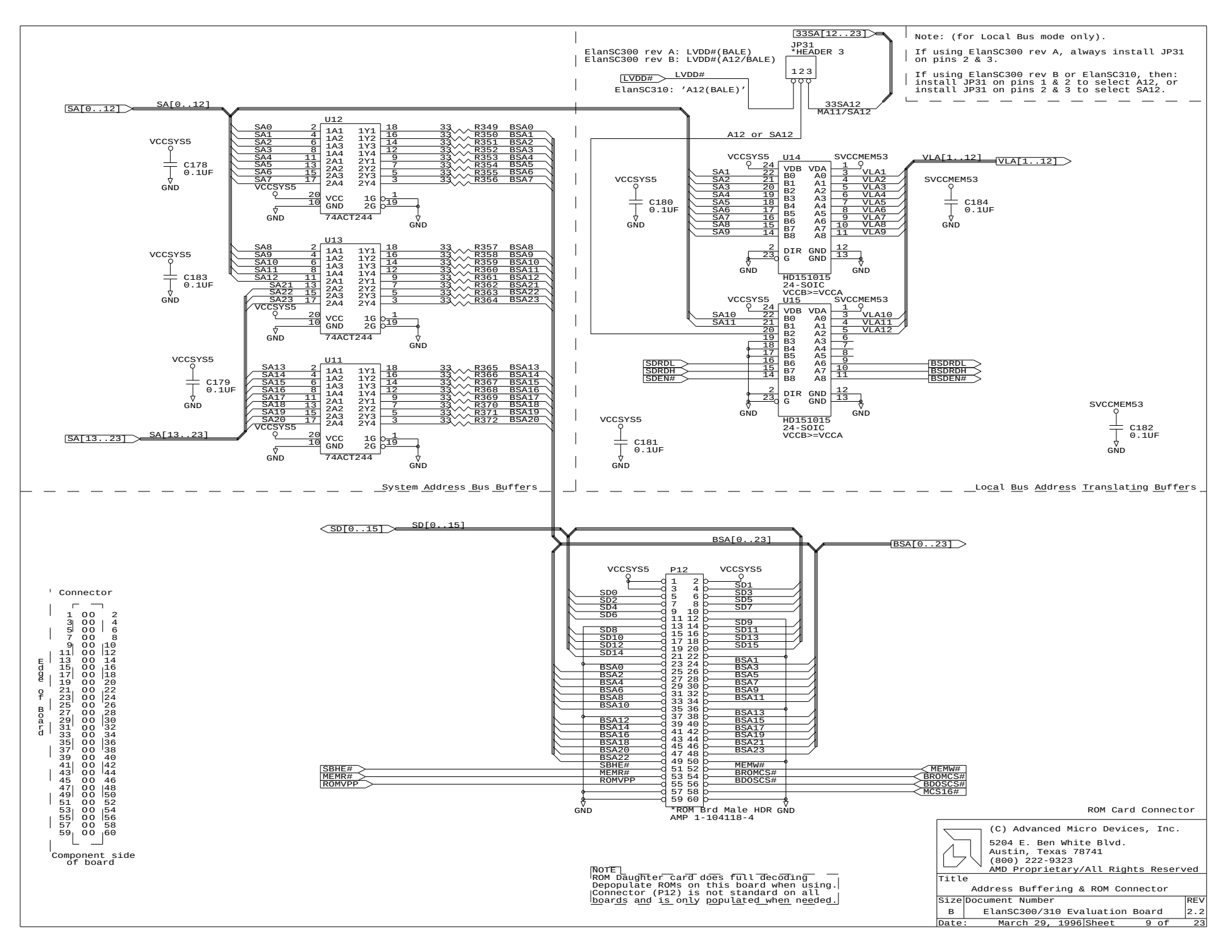
Title
SCP, Keyboard, Mouse, & SD Buffers
Size B
Document Number
ElanSC300/310 Evaluation Board
REV 2.2
Date: March 29, 1996
Sheet 8 of 23



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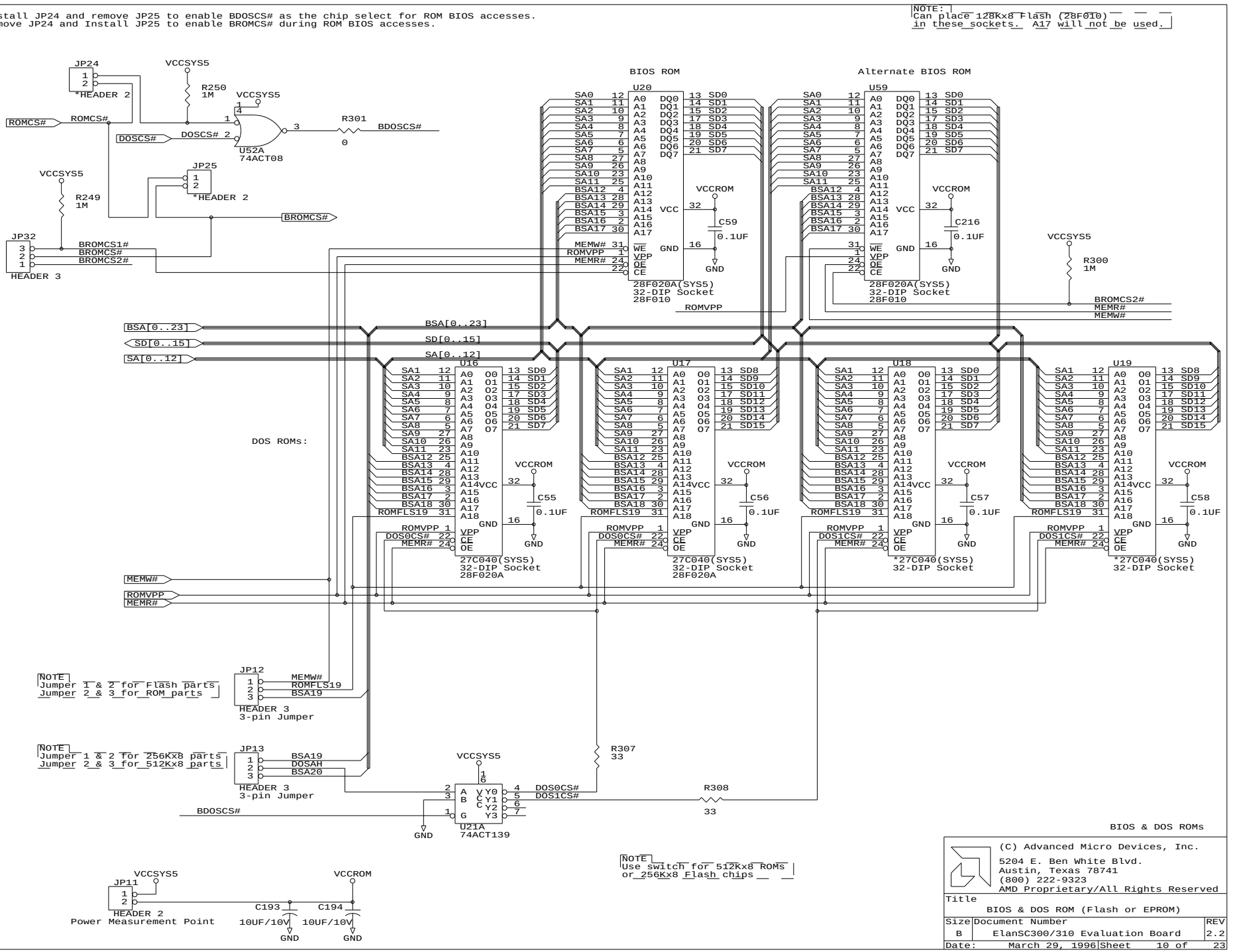
Title		
Address Buffering & ROM Connector		
Size: B	Document Number: ElanSC300/310 Evaluation Board	REV: 2.2
Date: March 29, 1996	Sheet 9 of 23	


Install JP24 and remove JP25 to enable BDOSCS# as the chip select for ROM BIOS accesses.
Remove JP24 and Install JP25 to enable BROMCS# during ROM BIOS accesses.
NOTE:
Can place 128Kx8 Flash (28F010) in these sockets. A17 will not be used.
BIOS ROM
Alternate BIOS ROM
U20
U59
28F020A(SYS5)
32-DIP Socket
28F010
JP24
*HEADER 2
JP25
*HEADER 2
JP32
HEADER 3
JP12
HEADER 3
3-pin Jumper
JP13
HEADER 3
3-pin Jumper
JP11
HEADER 2
Power Measurement Point
U16
U17
U18
U19
27C040(SYS5)
32-DIP Socket
28F020A
*27C040(SYS5)
32-DIP Socket
DOS ROMs:
U21A
74ACT139
U52A
74ACT08
R250 1M
R249 1M
R300 1M
R301 0
R307 33
R308 33
C59 0.1UF
C216 0.1UF
C55 0.1UF
C56 0.1UF
C57 0.1UF
C58 0.1UF
C193 10UF/10V
C194 10UF/10V
VCCSYS5
VCCROM
GND
ROMCS#
DOSCS#
BROMCS#
BROMCS1#
BROMCS2#
BDOSCS#
ROMVPP
MEMW#
MEMR#
BSA[0..23]
SD[0..15]
SA[0..12]
NOTE
Jumper 1 & 2 for Flash parts
Jumper 2 & 3 for ROM parts
NOTE
Jumper 1 & 2 for 256Kx8 parts
Jumper 2 & 3 for 512Kx8 parts
NOTE
Use switch for 512Kx8 ROMs or 256Kx8 Flash chips
BIOS & DOS ROMs
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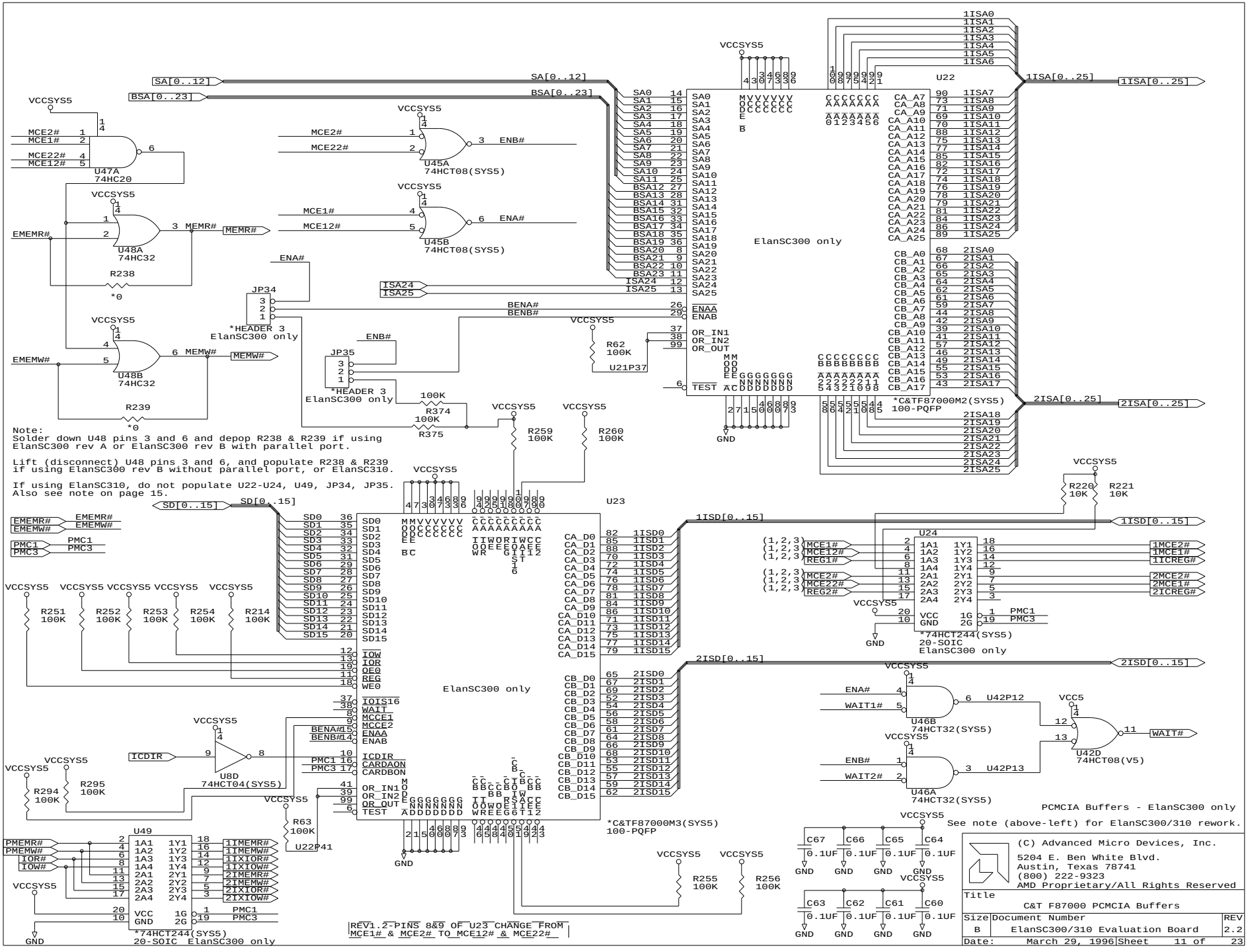
Title
BIOS & DOS ROM (Flash or EPROM)
Size B
Document Number ElanSC300/310 Evaluation Board
REV 2.2
Date: March 29, 1996
Sheet 10 of 23


SA[0..12]
BSA[0..23]
SA[0..12]
BSA[0..23]
VCCSYS5
U22
1ISA[0..25]
2ISA[0..25]
ElanSC300 only
*C&TF87000M2(SYS5)
100-PQFP
U47A
74HC20
U48A
74HC32
U48B
74HC32
U45A
74HCT08(SYS5)
U45B
74HCT08(SYS5)
MCE2#
MCE1#
MCE22#
MCE12#
ENB#
ENA#
MEMR#
MEMW#
EMEMR#
EMEMW#
R238
R239
*0
JP34
JP35
*HEADER 3
ElanSC300 only
ISA24
ISA25
BENA#
BENB#
ENAA
ENAB
OR_IN1
OR_IN2
OR_OUT
TEST
R62
100K
U21P37
R374
100K
R375
100K
R259
100K
R260
100K
GND
Note:
Solder down U48 pins 3 and 6 and depop R238 & R239 if using
ElanSC300 rev A or ElanSC300 rev B with parallel port.
Lift (disconnect) U48 pins 3 and 6, and populate R238 & R239
if using ElanSC300 rev B without parallel port, or ElanSC310.
If using ElanSC310, do not populate U22-U24, U49, JP34, JP35.
Also see note on page 15.
U23
SD[0..15]
SD[0..15]
IOW
IOR
QEQ
REG
WE0
IOIS16
WAIT
MCCE1
MCCE2
ENAA
ENAB
ICDIR
CARDAON
CARDBON
OR_IN1
OR_IN2
OR_OUT
TEST
CA_D0
CA_D1
CA_D2
CA_D3
CA_D4
CA_D5
CA_D6
CA_D7
CA_D8
CA_D9
CA_D10
CA_D11
CA_D12
CA_D13
CA_D14
CA_D15
CB_D0
CB_D1
CB_D2
CB_D3
CB_D4
CB_D5
CB_D6
CB_D7
CB_D8
CB_D9
CB_D10
CB_D11
CB_D12
CB_D13
CB_D14
CB_D15
*C&TF87000M3(SYS5)
100-PQFP
R251
R252
R253
R254
R214
100K
R294
R295
100K
R63
100K
U22P41
U8D
74HCT04(SYS5)
U49
*74HCT244(SYS5)
20-SOIC ElanSC300 only
PMEMR#
PMEMW#
IOR#
IOW#
1IMEMR#
1IMEMW#
1IIOR#
1IIOW#
2IMEMR#
2IMEMW#
2IIOR#
2IIOW#
PMC1
PMC3
REV1.2-PINS 8&9 OF U23 CHANGE FROM
MCE1# & MCE2# TO MCE12# & MCE22#
1ISD[0..15]
2ISD[0..15]
U24
*74HCT244(SYS5)
20-SOIC
ElanSC300 only
1MCE2#
1MCE1#
1ICREG#
2MCE2#
2MCE1#
2ICREG#
R220
10K
R221
10K
U46B
74HCT32(SYS5)
U46A
74HCT32(SYS5)
U42D
74HCT08(V5)
U42P12
U42P13
VCC5
WAIT#
PCMCIA Buffers - ElanSC300 only
See note (above-left) for ElanSC300/310 rework.
R255
100K
R256
100K
C67
C66
C65
C64
C63
C62
C61
C60
0.1UF
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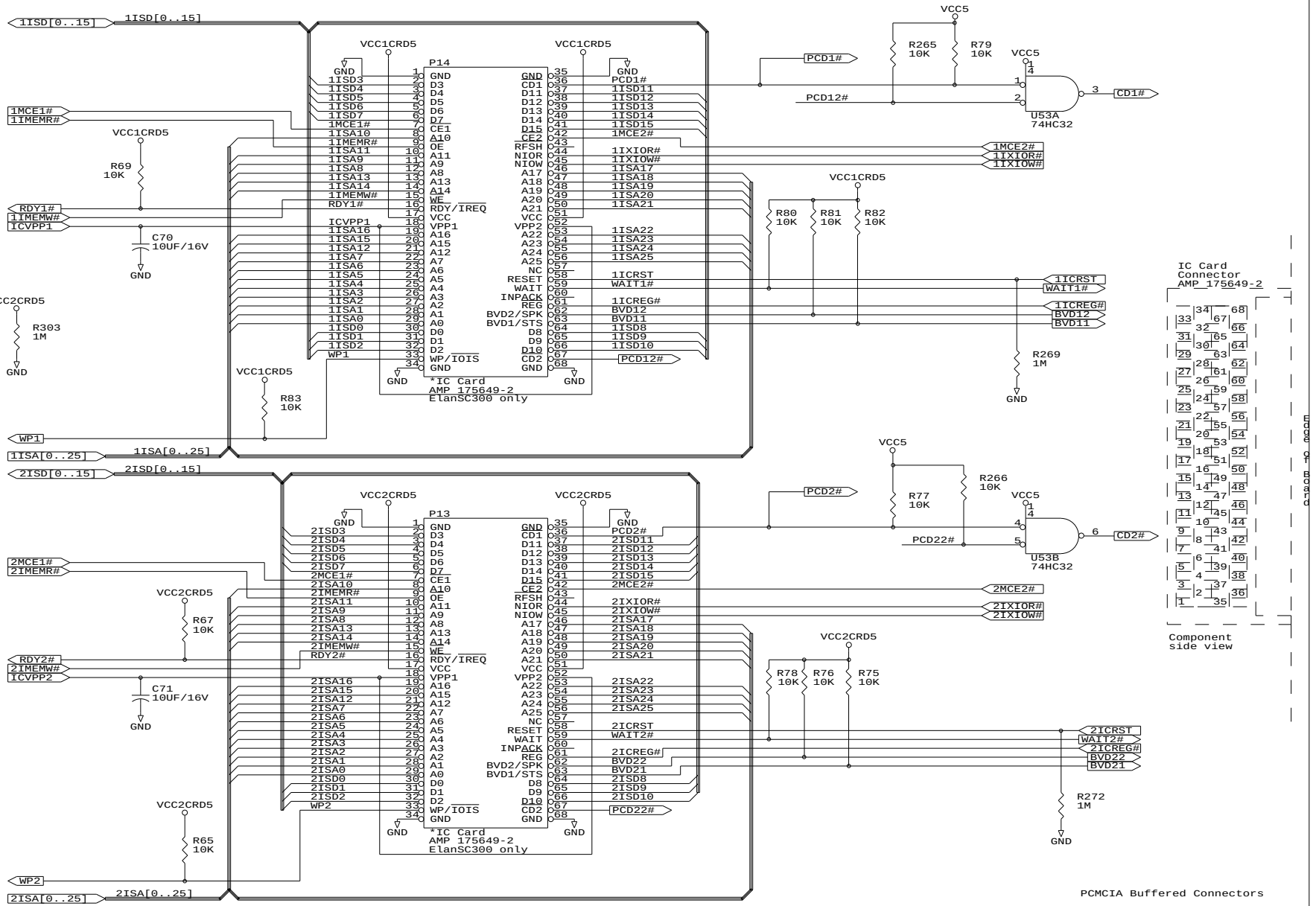
Title
C&T F87000 PCMCIA Buffers
Size
B
Document Number
ElanSC300/310 Evaluation Board
REV
2.2
Date:
March 29, 1996
Sheet
11 of
23


1ISD[0..15]
1ISA[0..25]
2ISD[0..15]
2ISA[0..25]
P14
P13
*IC Card
AMP 175649-2
ElanSC300 only
IC Card
Connector
AMP_175649-2
Component
side view
U53A
74HC32
U53B
74HC32
PCMCIA Buffered Connectors
- ElanSC300 only -
If using ElanSC310, do not populate P13 and P14.
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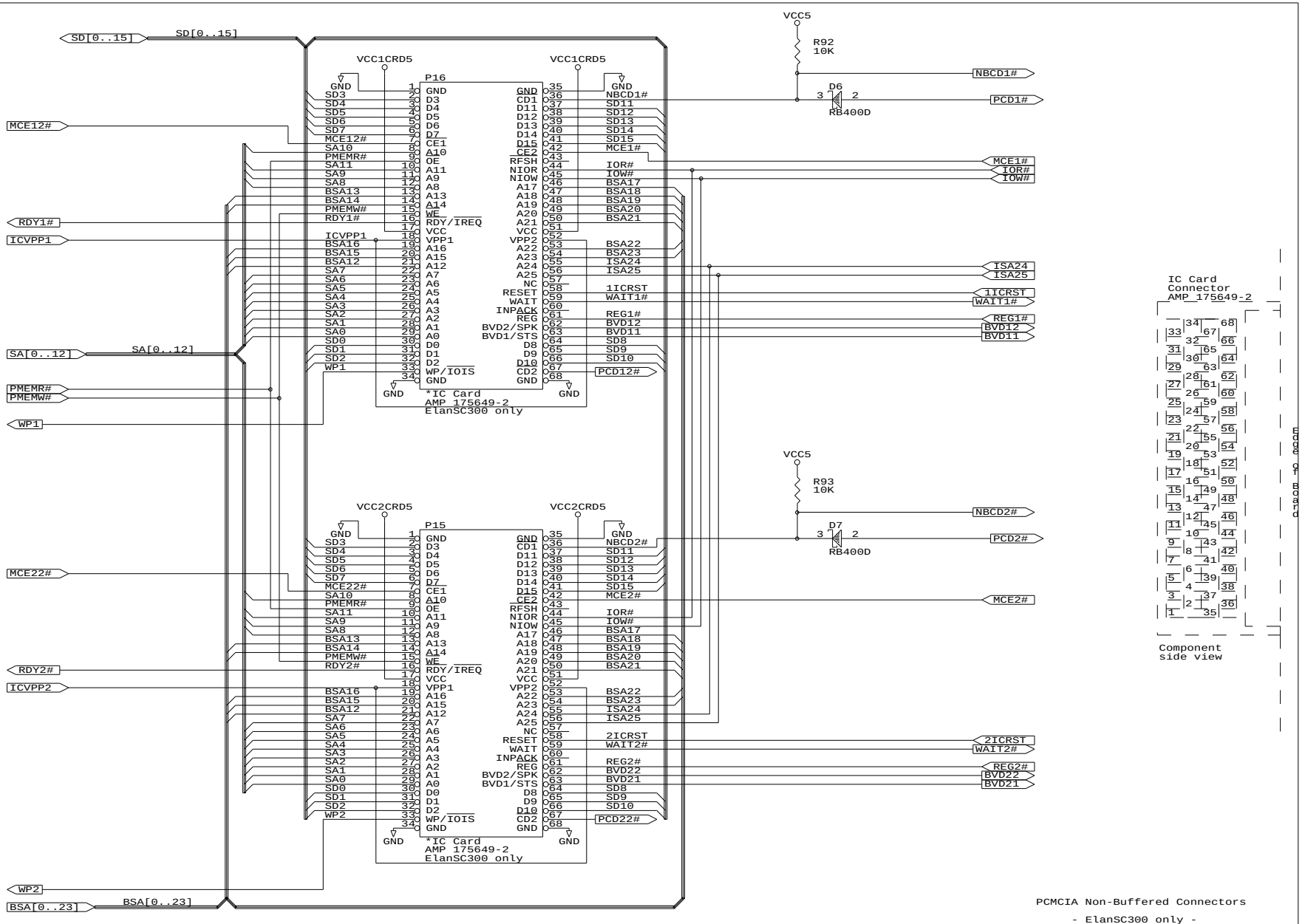
Title
Buffered PCMCIA Connectors
Size B
Document Number
ElanSC300/310 Evaluation Board
REV 2.2
Date: March 29, 1996
Sheet 12 of 23



If using ElanSC310, do not populate P15 and P16.

PCMCIA Non-Buffered Connectors

- ElanSC300 only -

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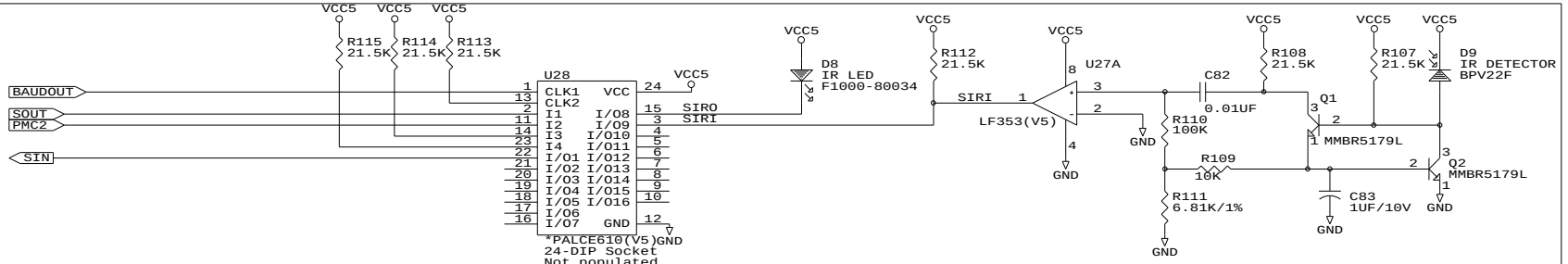
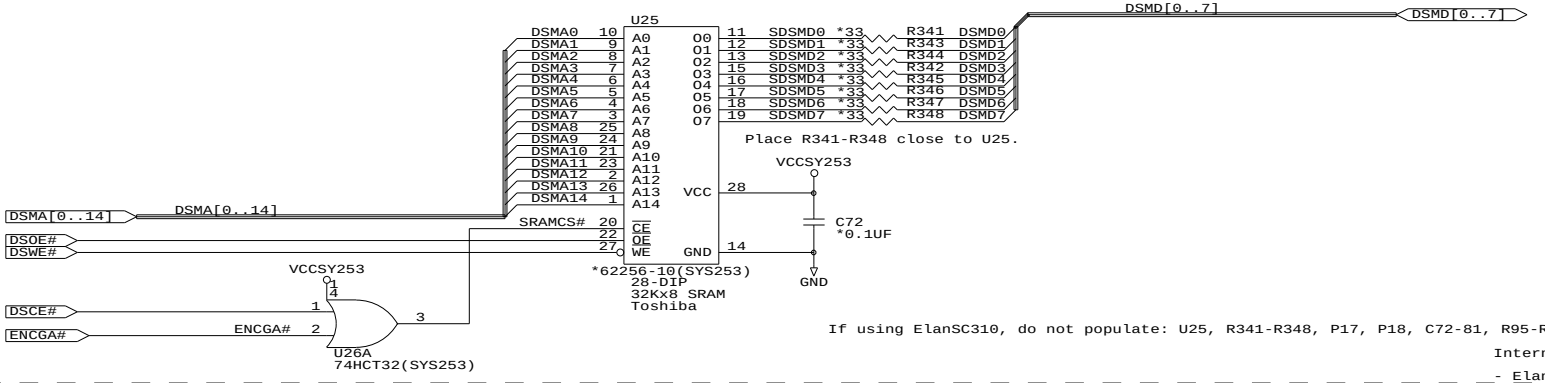
Title		
Non-Buffered PCMCIA Connectors		
Size	Document Number	REV
B	ElanSC300/310 Evaluation Board	2.2
Date: March 29, 1996	Sheet 13 of 23	



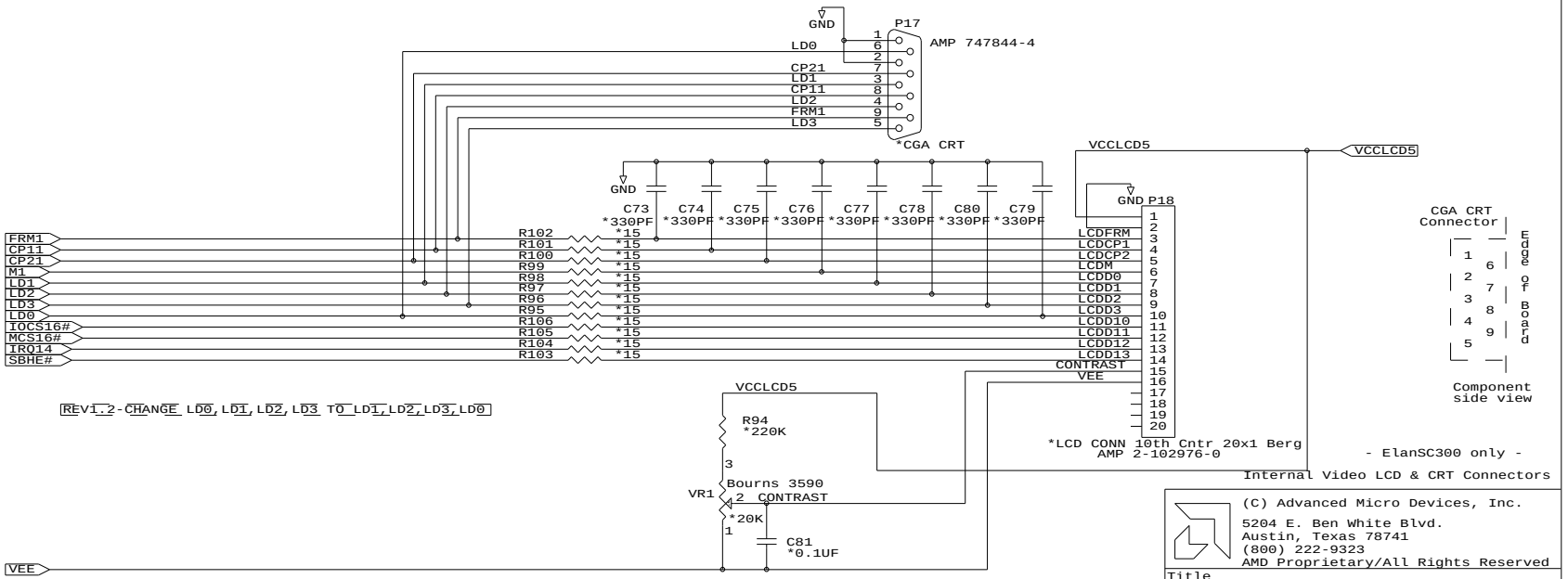
Serial Infra-Red Circuit



If using ElanSC310, do not populate: U25, R341-R348, P17, P18, C72-81, R95-R106, VR1.

Internal Video RAM

- ElanSC300 only -



- ElanSC300 only -

Internal Video LCD & CRT Connectors

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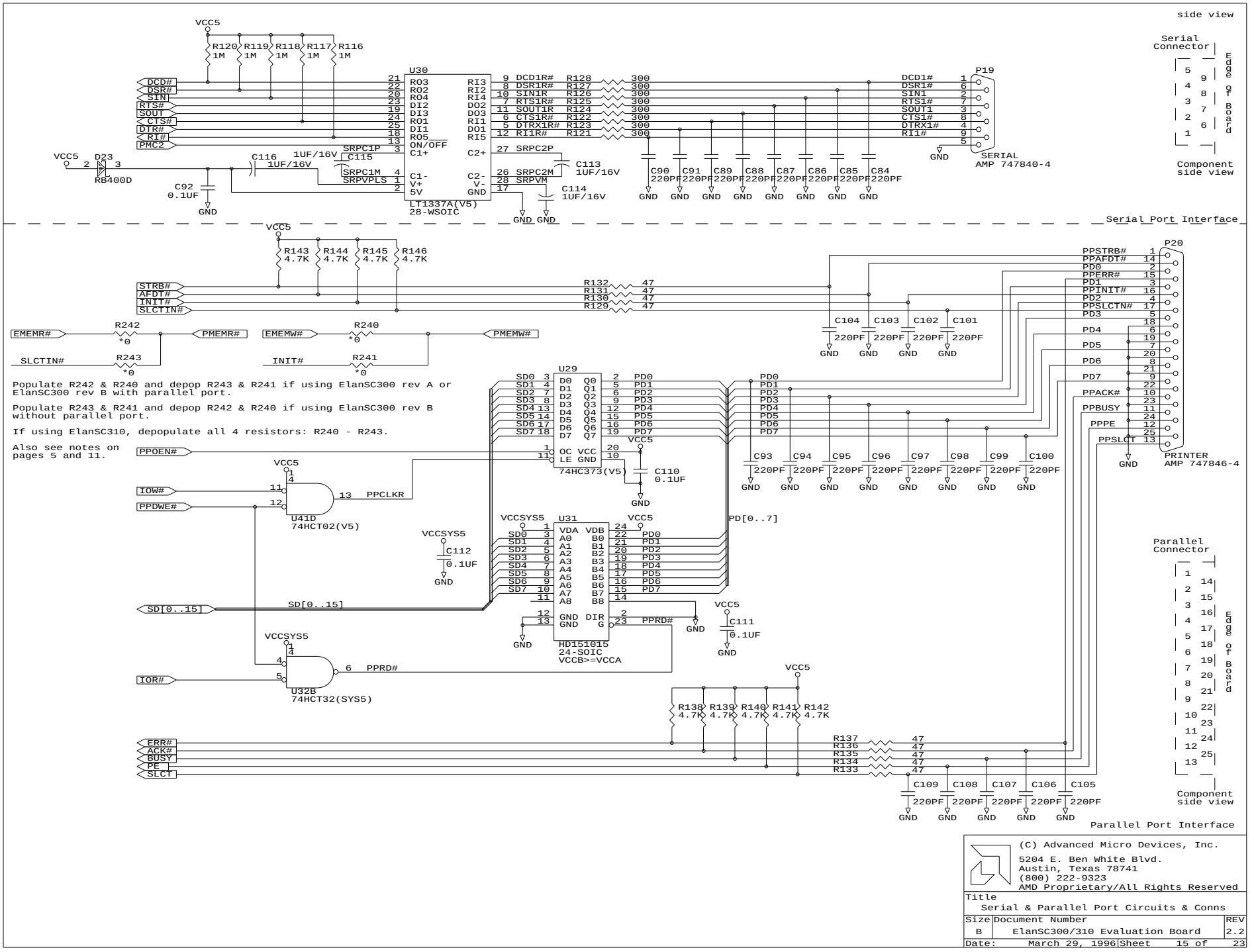
Title	Display SRAM & CRT & LCD Connectors	
Size: B	Document Number: ElanSC300/310 Evaluation Board	REV: 2.2
Date: March 29, 1996	Sheet 14 of 23	



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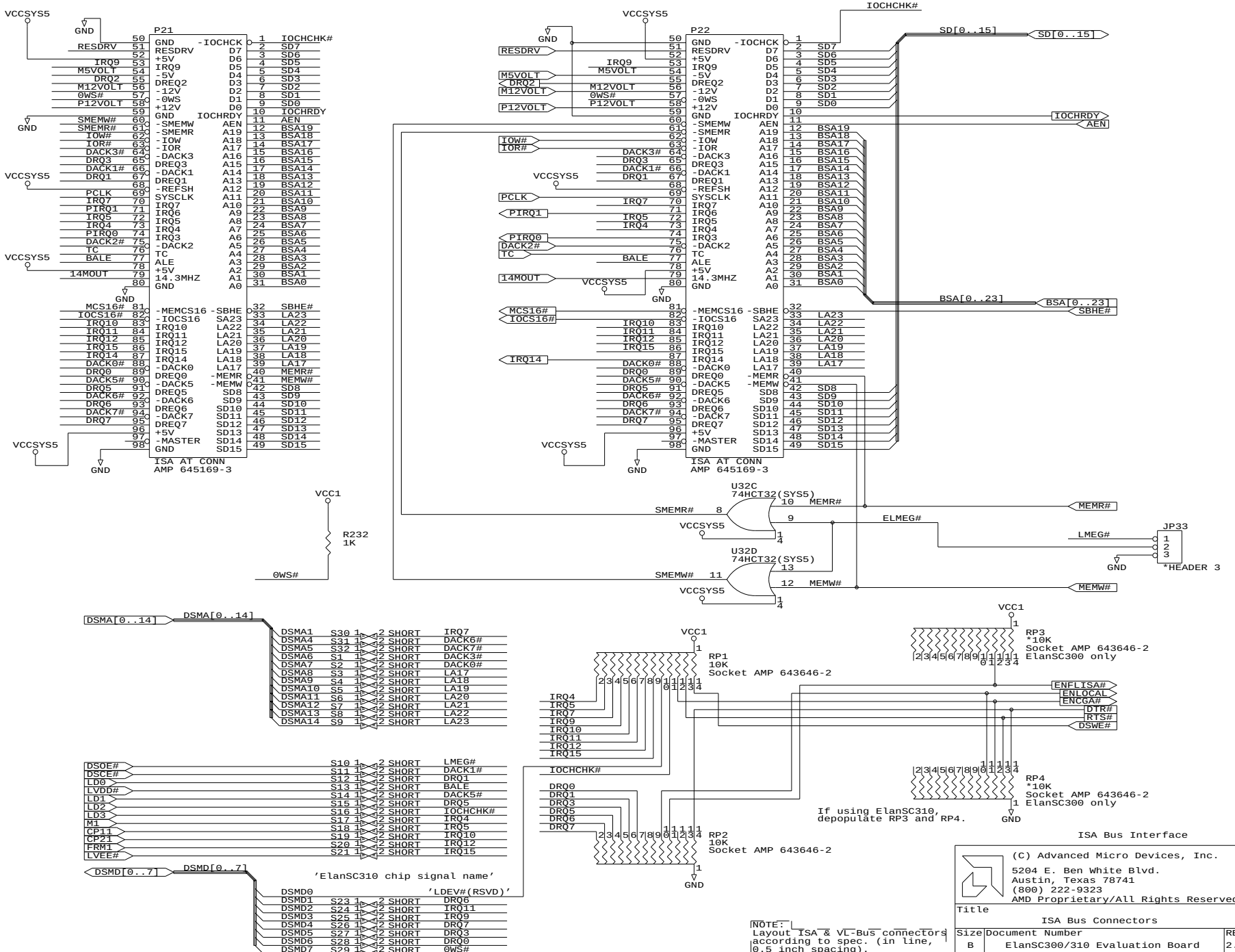
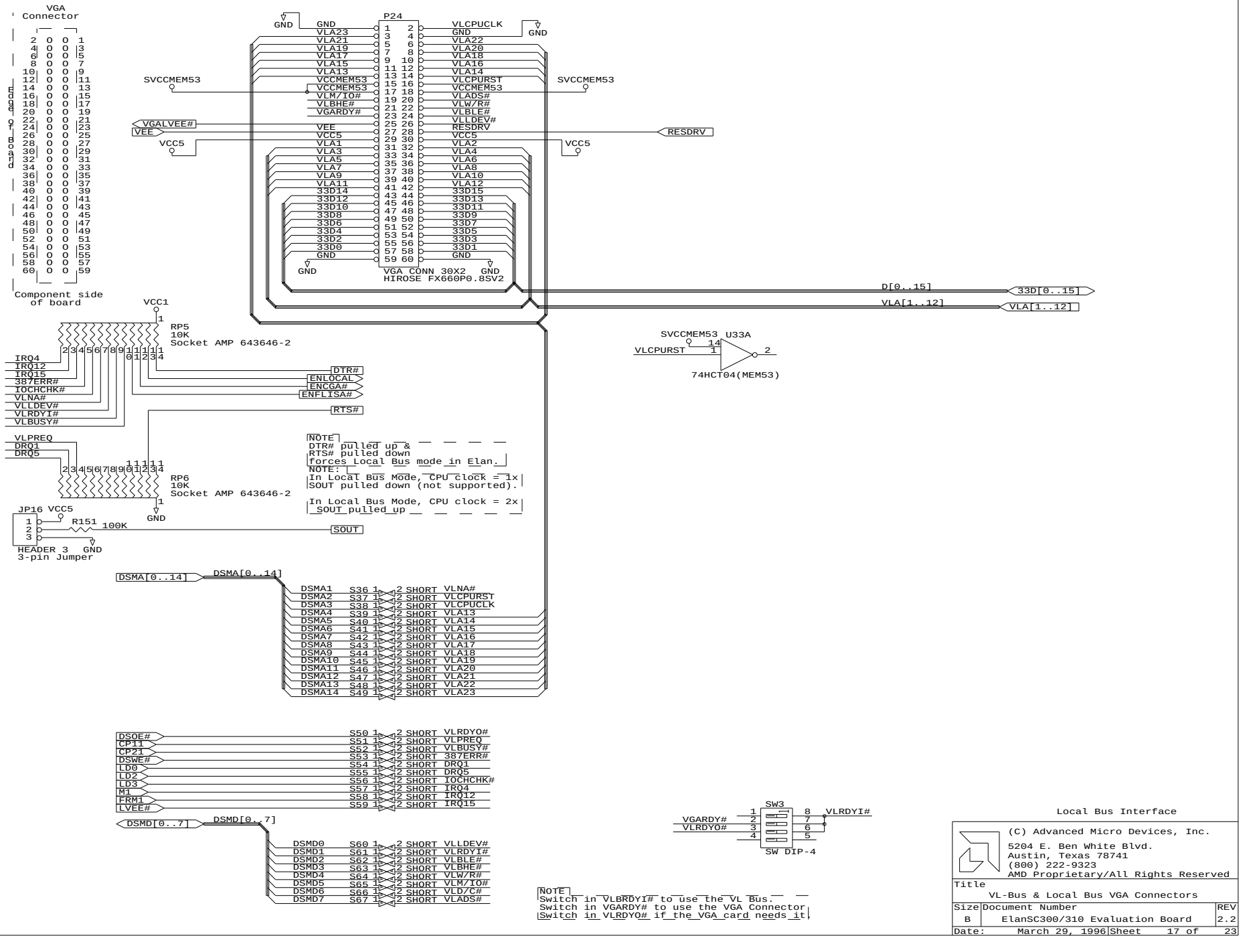
Title	Serial & Parallel Port Circuits & Conns	
Size: B	Document Number: ElanSC300/310 Evaluation Board	REV: 2.2
Date: March 29, 1996	Sheet 15 of 23	



NOTE:
Layout ISA & VL-Bus connectors according to spec. (in line, 0.5 inch spacing).

Note: Pin 1 indicator on Local Bus connector is really Pin 2 in our design.



Local Bus Interface

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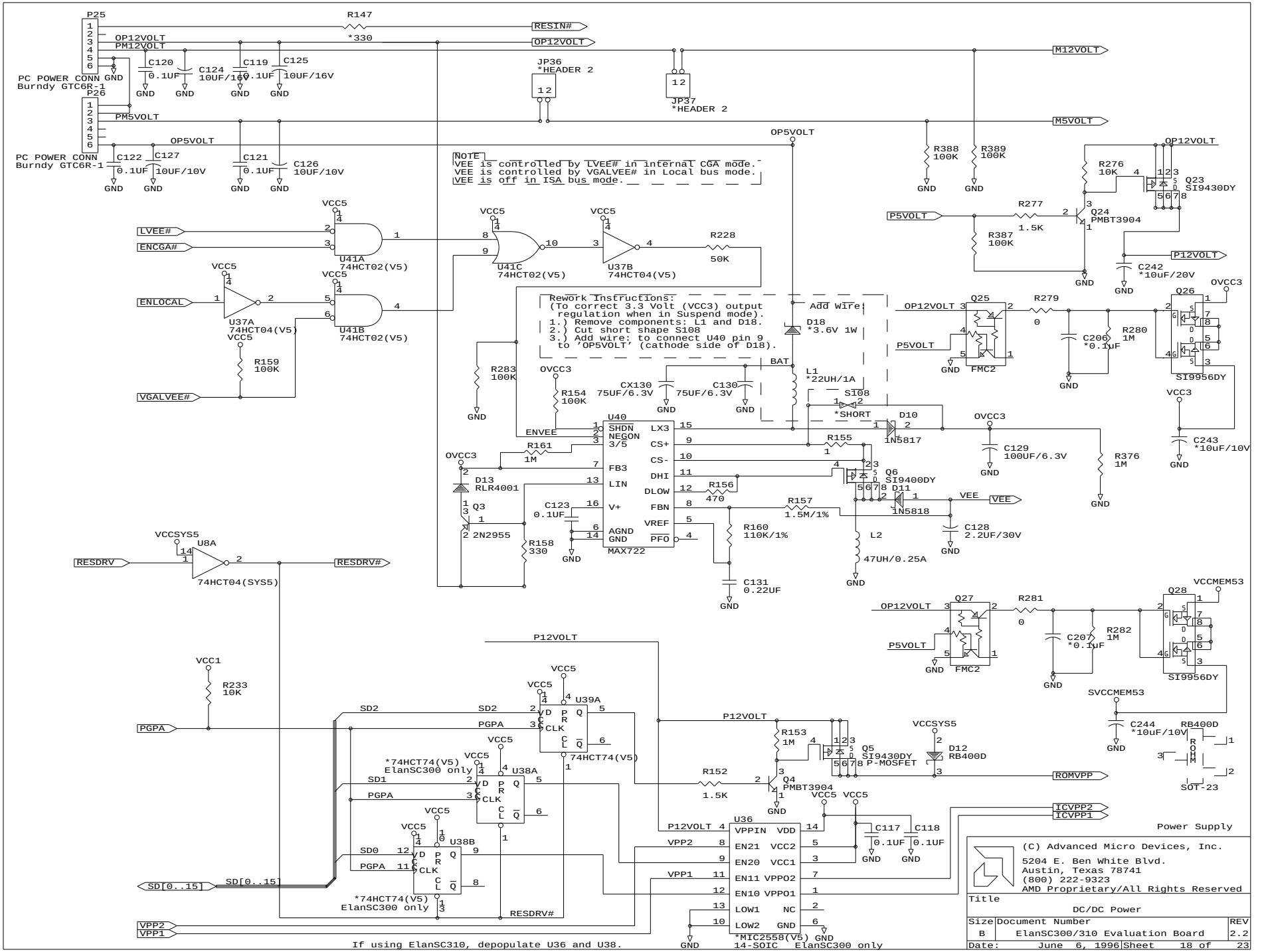
Title	VL-Bus & Local Bus VGA Connectors	
Size: B	Document Number: ElanSC300/310 Evaluation Board	REV: 2.2
Date: March 29, 1996	Sheet 17 of 23	


P25
PC POWER CONN GND
Burndy GTC6R-1
P26
PC POWER CONN
Burndy GTC6R-1
R147
*330
RESIN#
OP12VOLT
PM12VOLT
PM5VOLT
OP5VOLT
M12VOLT
M5VOLT
C120 0.1UF
C124 10UF/16V
C119 0.1UF
C125 10UF/16V
C122 0.1UF
C127 10UF/10V
C121 0.1UF
C126 10UF/10V
GND
JP36 *HEADER 2
JP37 *HEADER 2
NOTE
VEE is controlled by LVEE# in internal CGA mode.
VEE is controlled by VGALVEE# in Local bus mode.
VEE is off in ISA bus mode.
R388 100K
R389 100K
R276 10K
Q23 SI9430DY
R277 1.5K
Q24 PMBT3904
R387 100K
P5VOLT
P12VOLT
C242 *10uF/20V
LVEE#
ENCGA#
ENLOCAL
VGALVEE#
VCC5
U41A 74HCT02(V5)
U41C 74HCT02(V5)
U37B 74HCT04(V5)
U37A 74HCT04(V5)
U41B 74HCT02(V5)
R228 50K
R159 100K
Rework Instructions:
(To correct 3.3 Volt (VCC3) output regulation when in Suspend mode).
1.) Remove components: L1 and D18.
2.) Cut short shape S108
3.) Add wire; to connect U40 pin 9 to 'OP5VOLT' (cathode side of D18).
Add wire
D18 *3.6V 1W
R283 100K
R154 100K
OVCC3
CX130 75UF/6.3V
C130 75UF/6.3V
BAT
L1 *22UH/1A
S108 *SHORT
D10 1N5817
C129 100UF/6.3V
R376 1M
C243 *10uF/10V
VCC3
Q25
Q26
R279 0
C206 *0.1uF
R280 1M
FMC2
SI9956DY
U40
MAX722
SHDN
NEGON
3/5
LX3
CS+
CS-
DHI
DLOW
FBN
VREF
PFO
FB3
LIN
V+
AGND
GND
ENVEE
R161 1M
R155
Q6 SI9400DY
D11 1N5818
VEE
R156 470
R157 1.5M/1%
R160 110K/1%
C123 0.1UF
C128 2.2UF/30V
L2 47UH/0.25A
C131 0.22UF
D13 RLR4001
Q3 2N2955
R158 330
VCCSYS5
U8A
74HCT04(SYS5)
RESDRV
RESDRV#
Q27
Q28
R281 0
C207 *0.1uF
R282 1M
VCCMEM53
SVCCMEM53
C244 *10uF/10V
RB400D
SOT-23
VCC1
R233 10K
PGPA
SD2
SD1
SD0
SD[0..15]
U39A
U38A
U38B
74HCT74(V5)
*74HCT74(V5) ElanSC300 only
R153 1M
Q5 SI9430DY
P-MOSFET
D12 RB400D
ROMVPP
R152 1.5K
Q4 PMBT3904
U36
*MIC2558(V5) 14-SOIC ElanSC300 only
VPPIN
VDD
EN21
EN20
EN11
EN10
LOW1
LOW2
VCC2
VCC1
VPPO2
VPPO1
NC
VPP2
VPP1
ICVPP2
ICVPP1
C117 0.1UF
C118 0.1UF
If using ElanSC310, depopulate U36 and U38.
Power Supply
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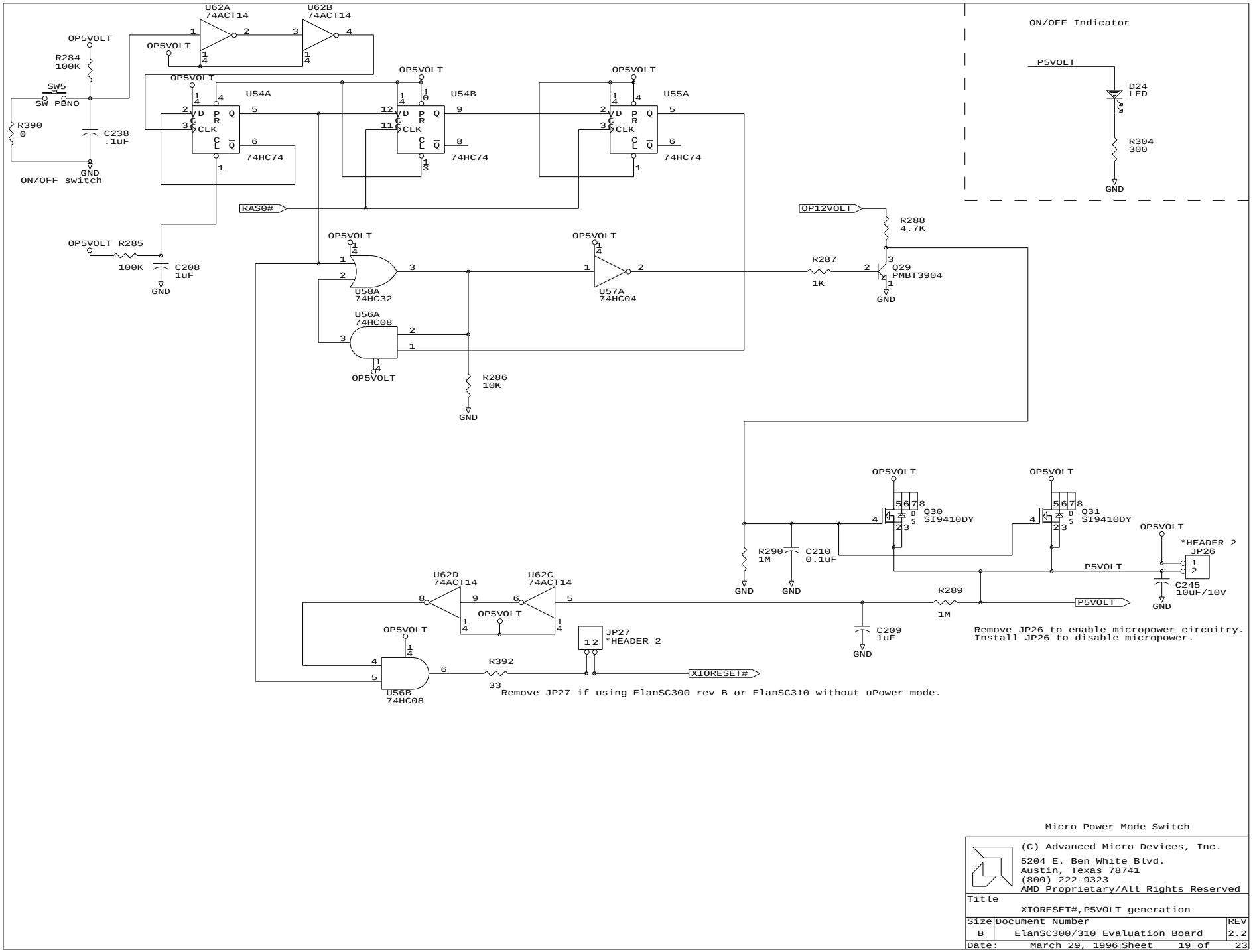
Title
DC/DC Power
Size B
Document Number
ElanSC300/310 Evaluation Board
REV 2.2
Date: June 6, 1996
Sheet 18 of 23



Micro Power Mode Switch

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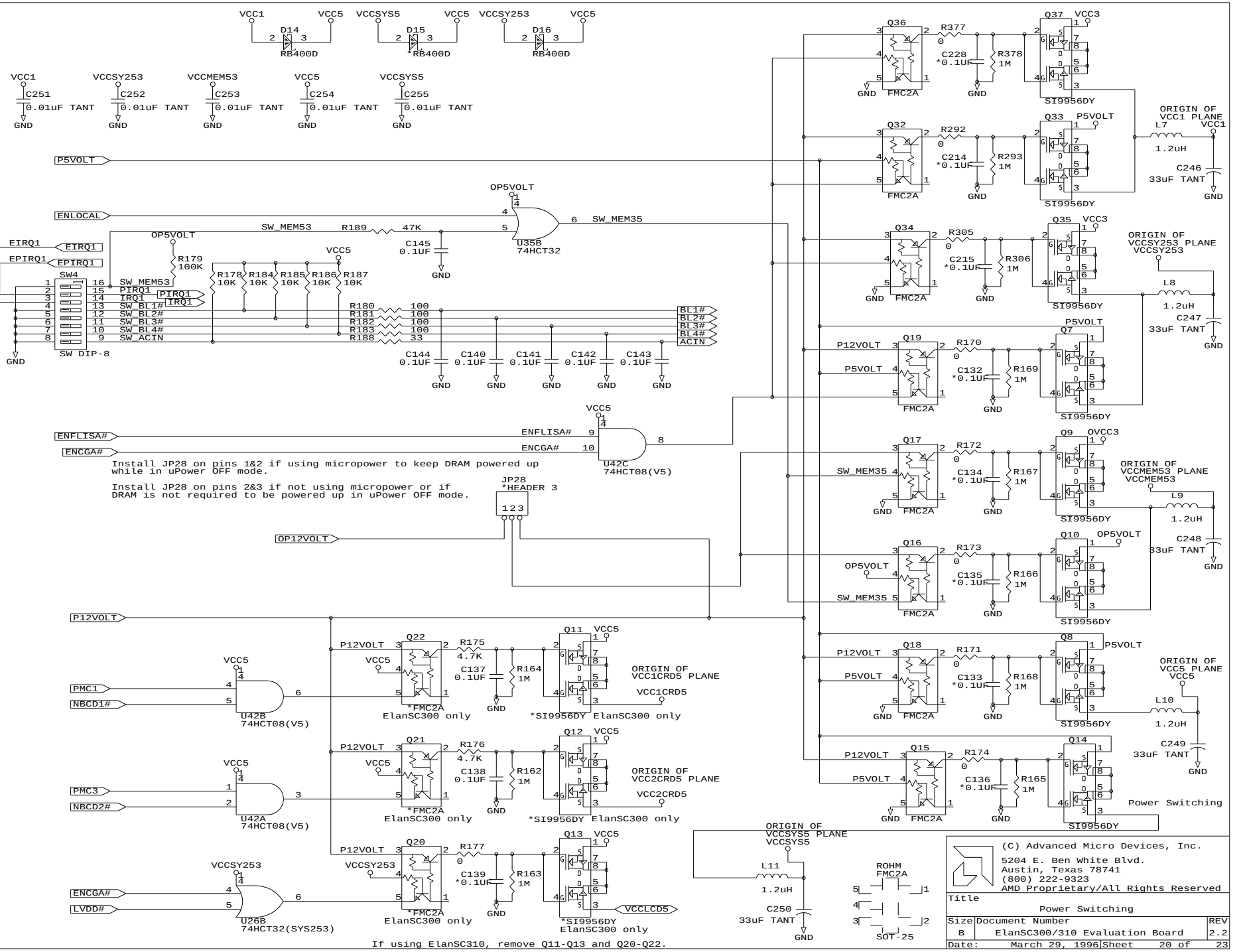
Title		
XIORESET#,P5VOLT generation		
Size	Document Number	REV
B	ElanSC300/310 Evaluation Board	2.2
Date: March 29, 1996	Sheet 19 of 23	


VCC1
VCC5
D14
RB400D
VCCSYS5
D15
VCCSY253
D16
C251
C252
C253
C254
C255
0.01uF TANT
GND
P5VOLT
ENLOCAL
OP5VOLT
SW_MEM53
R189
47K
C145
0.1UF
U35B
74HCT32
SW_MEM35
EIRQ1
EPIRQ1
SW4
SW DIP-8
R179
100K
R178
R184
R185
R186
R187
10K
PIRQ1
IRQ1
SW_BL1#
SW_BL2#
SW_BL3#
SW_BL4#
SW_ACIN
R180
R181
R182
R183
R188
100
33
BL1#
BL2#
BL3#
BL4#
ACIN
C144
C140
C141
C142
C143
ENFLISA#
ENCGA#
U42C
74HCT08(V5)
Install JP28 on pins 1&2 if using micropower to keep DRAM powered up
while in uPower OFF mode.
Install JP28 on pins 2&3 if not using micropower or if
DRAM is not required to be powered up in uPower OFF mode.
JP28
*HEADER 3
OP12VOLT
P12VOLT
PMC1
NBCD1#
U42B
74HCT08(V5)
PMC3
NBCD2#
U42A
74HCT08(V5)
ENCGA#
LVDD#
VCCSY253
U26B
74HCT32(SYS253)
Q22
Q21
Q20
R175
R176
R177
4.7K
C137
C138
C139
*0.1UF
R164
R162
R163
1M
Q11
Q12
Q13
*FMC2A
ElanSC300 only
*SI9956DY ElanSC300 only
ORIGIN OF
VCC1CRD5 PLANE
VCC1CRD5
ORIGIN OF
VCC2CRD5 PLANE
VCC2CRD5
VCCLCD5
If using ElanSC310, remove Q11-Q13 and Q20-Q22.
Q36
Q32
Q34
Q19
Q17
Q16
Q18
Q15
R377
R292
R305
R170
R172
R173
R171
R174
C228
C214
C215
C132
C134
C135
C133
C136
R378
R293
R306
R169
R167
R166
R168
R165
FMC2A
Q37
Q33
Q35
Q7
Q9
Q10
Q8
Q14
SI9956DY
OVCC3
P5VOLT
ORIGIN OF
VCC1 PLANE
L7
1.2uH
C246
33uF TANT
ORIGIN OF
VCCSY253 PLANE
VCCSY253
L8
C247
ORIGIN OF
VCCMEM53 PLANE
VCCMEM53
L9
C248
ORIGIN OF
VCC5 PLANE
VCC5
L10
C249
Power Switching
ORIGIN OF
VCCSYS5 PLANE
VCCSYS5
L11
C250
ROHM
FMC2A
SOT-25
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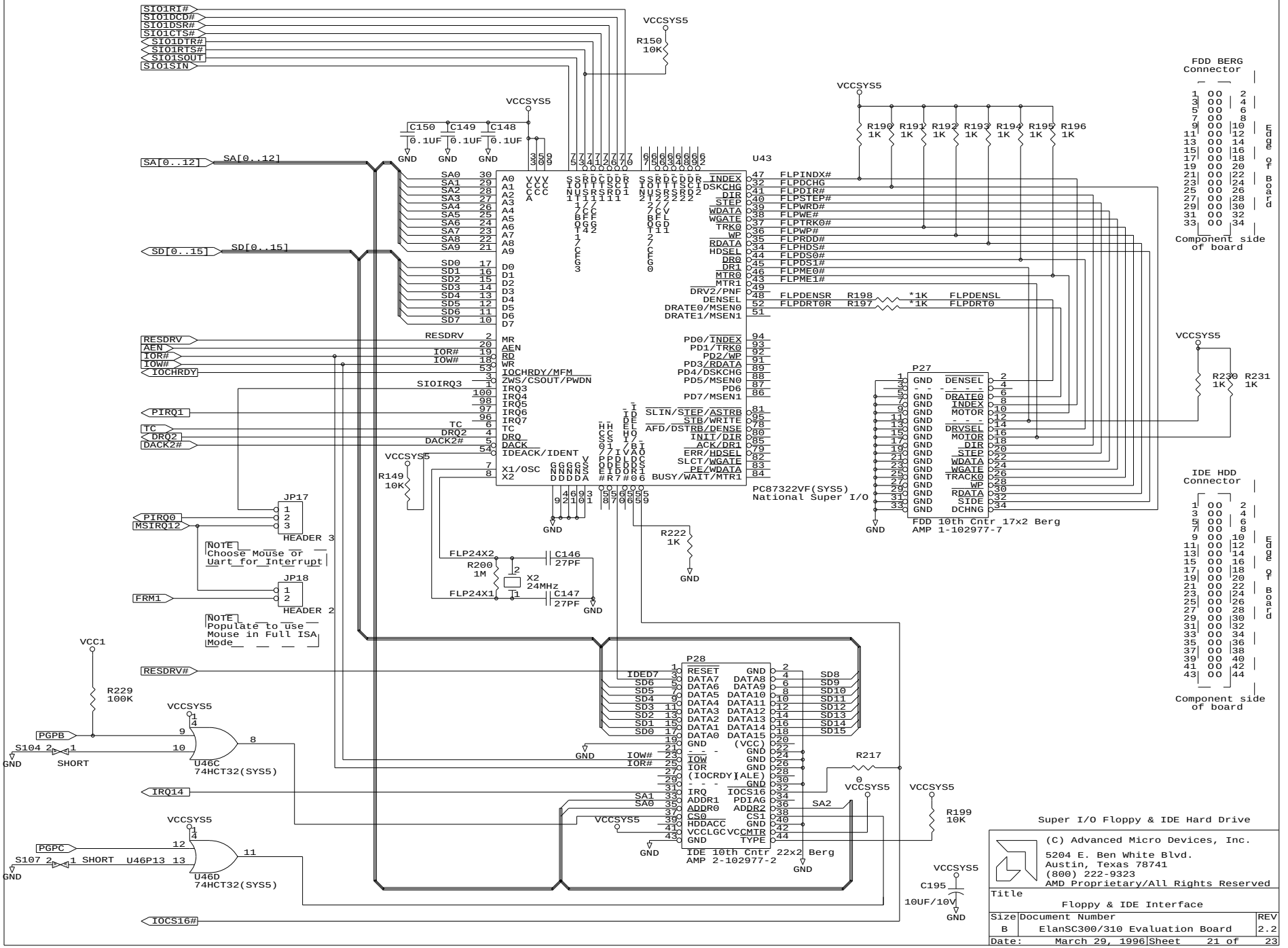
Title
Power Switching
Size
B
Document Number
ElanSC300/310 Evaluation Board
REV
2.2
Date:
March 29, 1996
Sheet
20 of
23


SIO1RI#
SIO1DCD#
SIO1DSR#
SIO1CTS#
SIO1DTR#
SIO1RTS#
SIO1SOUT
SIO1SIN
VCCSYS5
R150 10K
C150 C149 C148
0.1UF 0.1UF 0.1UF
GND GND GND
SA[0..12]
SD[0..15]
U43
PC87322VF(SYS5)
National Super I/O
RESDRV
AEN
IOR#
IOW#
IOCHRDY
PIRQ1
TC
DRQ2
DACK2#
SIOIRQ3
R149 10K
R222 1K
JP17
HEADER 3
PIRQ0
MSIRQ12
NOTE
Choose Mouse or Uart for Interrupt
JP18
HEADER 2
FRM1
NOTE
Populate to use Mouse in Full ISA Mode
FLP24X2
FLP24X1
R200 1M
X2 24MHz
C146 27PF
C147 27PF
VCC1
R229 100K
PGPB
PGPC
S104
S107
SHORT
U46C 74HCT32(SYS5)
U46D 74HCT32(SYS5)
U46P13
IRQ14
IOCS16#
P28
IDE 10th Cntr 22x2 Berg
AMP 2-102977-2
R217 0
R199 10K
SA2
C195 10UF/10V
R190 R191 R192 R193 R194 R195 R196 1K
FLPINDX#
FLPDCHG
FLPDIR#
FLPSTEP#
FLPWRD#
FLPWE#
FLPTRK0#
FLPWP#
FLPRDD#
FLPHDS#
FLPDS0#
FLPDS1#
FLPME0#
FLPME1#
FLPDENSR R198 *1K FLPDENSL
FLPDRT0R R197 *1K FLPDRT0
P27
FDD 10th Cntr 17x2 Berg
AMP 1-102977-7
FDD BERG Connector
Component side of board
Edge of Board
R230 R231 1K 1K
IDE HDD Connector
Component side of board
Edge of Board
Super I/O Floppy & IDE Hard Drive
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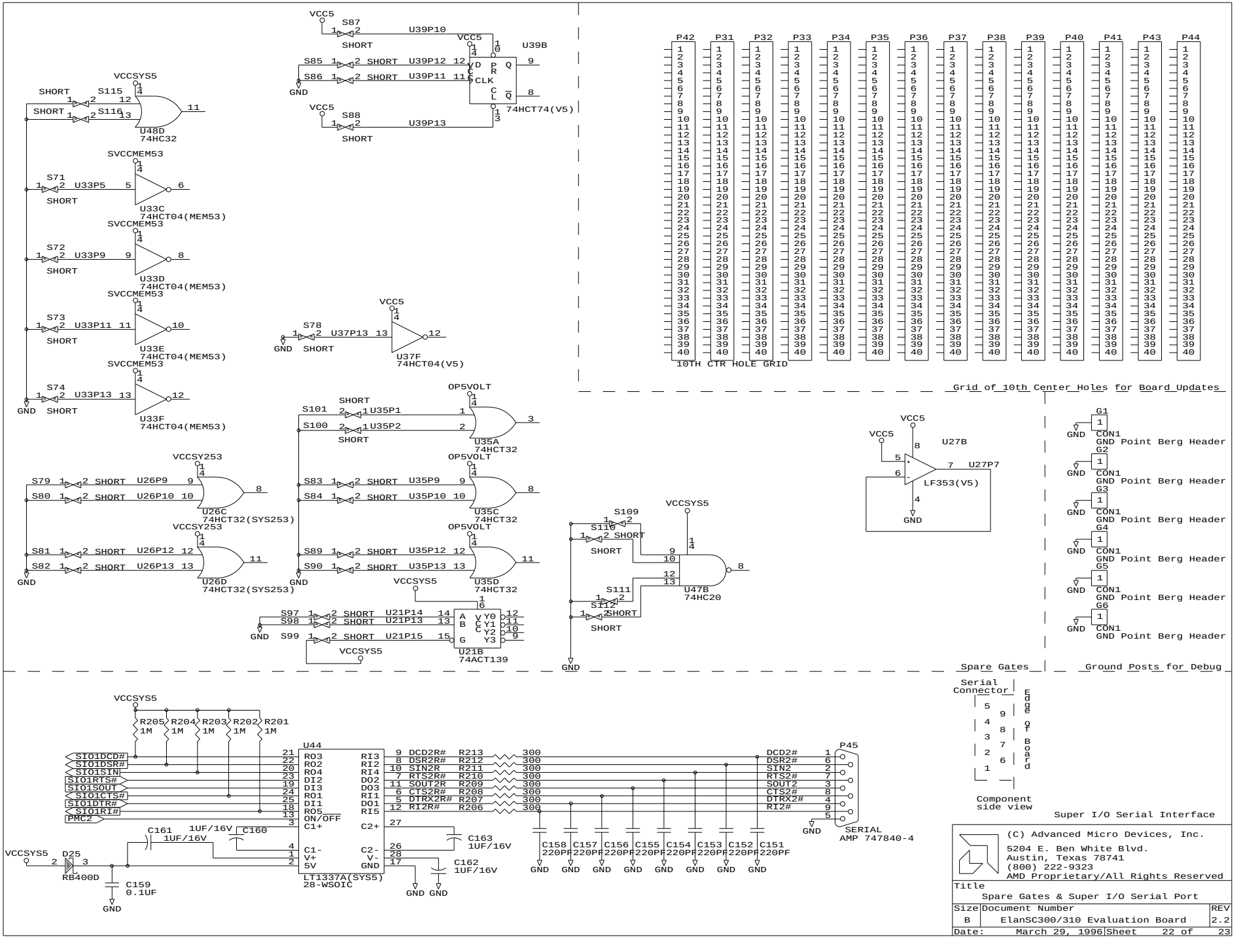
Title
Floppy & IDE Interface
Size B
Document Number ElanSC300/310 Evaluation Board
REV 2.2
Date: March 29, 1996
Sheet 21 of 23



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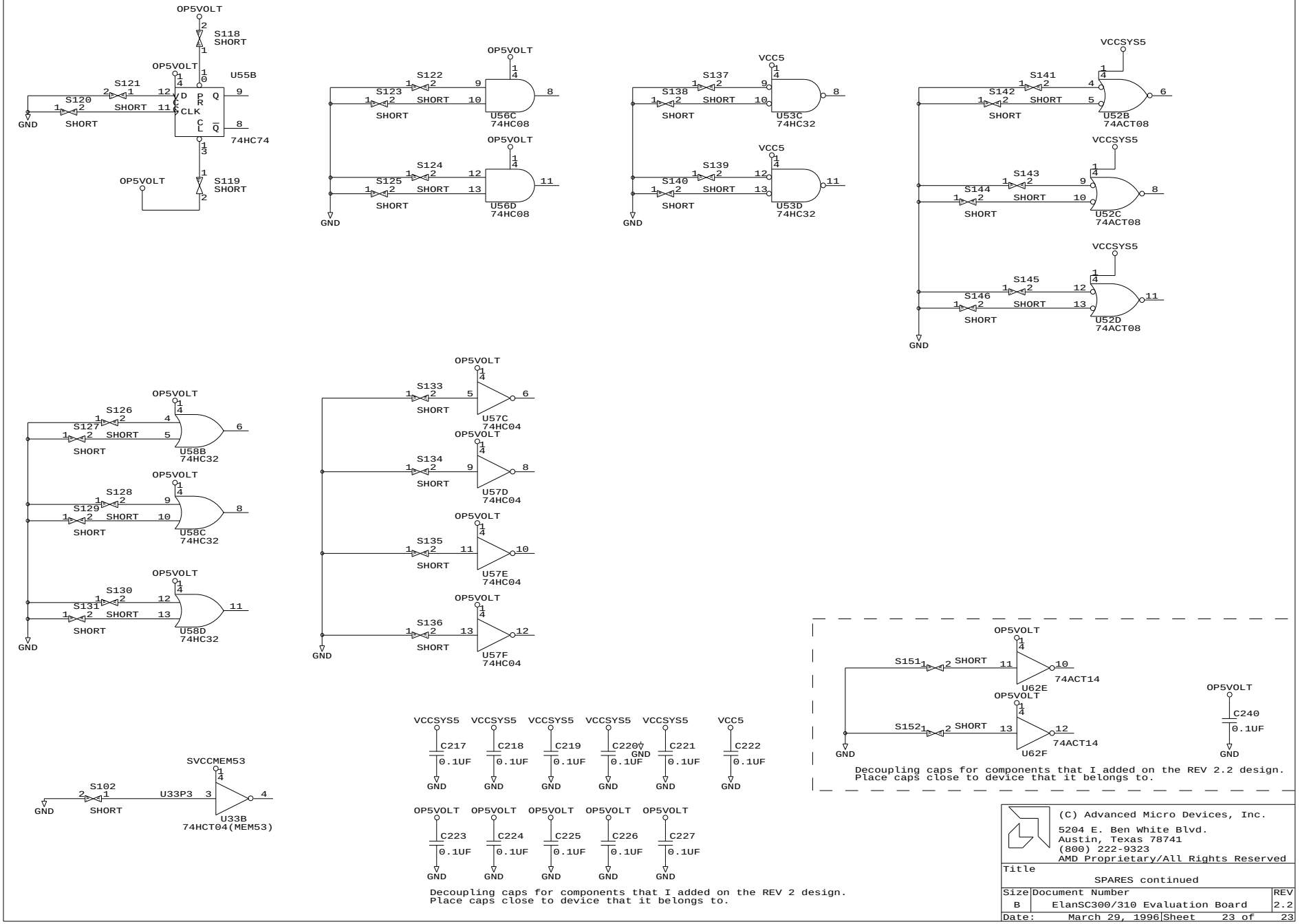
Super I/O Serial Interface

Title	Spare Gates & Super I/O Serial Port	
Size: B	Document Number: ElanSC300/310 Evaluation Board	REV: 2.2
Date: March 29, 1996	Sheet 22 of 23	



Decoupling caps for components that I added on the REV 2.2 design.
Place caps close to device that it belongs to.

Decoupling caps for components that I added on the REV 2 design.
Place caps close to device that it belongs to.

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Title		
SPARES continued		
Size	Document Number	REV
B	ElanSC300/310 Evaluation Board	2.2
Date: March 29, 1996	Sheet 23 of 23	

ElanSC300 Local Bus Reference Design Revision History:

Rev 1.0
Rev 1.1 - 1/24/94 - Added pulldown resistor (R15) to pin 140 of ELAN (page 1).
Rev 1.2 - 1/26/94 - Fixed pinout of ELAN (page 1)

Was: Name - Pin

LF1	- 207
LF2	- 206
LF3	- 205
LF4	- 204

Now: Name - Pin

LF1{HIGHSP PLL}	- 204
LF2{INTERMEDSP PLL}	- 205
LF3{LOWSP PLL}	- 206
LF4{VIDEO PLL}	- 207

- Swapped Intermediate PLL & Low Speed PLL labels on page 2.
- Added this Revision History page.

Rev 1.3 - 3/11/94 - Revisions from debug of Emulation Board.
- Upgraded schematics to OrCad 386+
- Moved this revision page to sheet 1
- Changed signal names for PCMCIA slots:

Old	New	Old	New
MCE1#	MCEHA#	MCE2#	MCEHB#
MCE12#	MCELA#	MCE22#	MCELB#
VPP1	VPPA	VPP2	VPPB
REG1#	REGA#	REG2#	REGB#
1ICRST	RSTA	2ICRST	RSTB
CD1#	CDA#	CD2#	CDB#
RDY1#	RDYA#	RDY2#	RDYB#
WP1	WPA	WP2	WPB
BVD11	BVD1A	BVD21	BVD1B
BVD12	BVD2A	BVD22	BVD2B
		ISA24	PCMSA24
		ISA25	PCMSA25

- sheet 2: renamed LCDD0-3 signals on ELAN (second functions of pins don't change)
- sheet 2: removed REFRESH (REF on pin 148) function from ELAN
- sheet 2: move pullup resistors (R6-9) to VCC3 from VCC5
- sheet 2: add pullup resistors to signals PIRQ0-1
- sheet 2: add better filtering to AVCC (pin 203) of Elan
- sheet 2: add cap to SYSCLK signal for filtering
- sheet 2: run IOCS16# signal off page for IDE HDD on sheet 11
- sheet 2: Elan pin 140 pulldown resistor changed to 1K ohm
- sheet 2: renamed PGPA-D to PGP0-3
- sheet 3: move RESET pullup resistor & diode from VCC3 to VCC5
- sheet 3: move RESUME pullup resistor from VCC3 to VCC5
- sheet 3: fix 32KHz Xtal resistor & cap values, add series resistor to 32KIN signal
- sheet 9: changed series resistor values to 33 ohms
- sheet 9: changed pullup resistor values to 10K ohms
- sheet 9: PCMCIA connector pin changes: pin 7 is MCEHx# & pin 42 is MCELx#
- sheet 11: added inverter to clock line for 80C42
- sheet 11: changed mouse & keyboard clock & data caps to 47pF
- sheet 12: added pullup resistor to PGP1
- sheet 12: added IOCS16# & VCC to IDE connector
- sheet 13: added series resistor to RESIN# signal to power connector
- sheet 14: changed signal name on switch from ACIN to SW_ACIN

Rev 1.4 - 4/19/94 - Revisions from debug of Evaluation Board.
- sheet 2: Change name on ELAN chip pin 183 to PULLUP
- sheet 3: Change DTR#, RTS#, & SOUT pullup & down resistors to 10K ohm
- sheet 3: Fix pinout of 32KHz xtal & component values in circuit
- sheet 5: Add bypass caps to buffers
- sheet 7: Add bypass caps to VGA Controller chip
- sheet 8: fix F87000 enable signals
- sheet 9: fix MCELx# and MCEHx# on connectors
  for the last time:
  CE1# = pin 7 = Even = LOW
  CE2# = pin 42 = Odd = HIGH
- sheet 9: Add OR gates for Card Detect qualification
- sheet 10: Change 74HCT374 to 74HCT373, also change PPCLKR control gate to NOR
- sheet 11: fix way 80C42 connected to keyboard and mouse
- sheet 12: fix floppy connector for 2 drives
- sheet 12: Change PGP0 to PGP3
- sheet 13: Change PGP3 to PGP0
- sheet 13: Tie BAT signal to VCC3 with short
- sheet 14: Change ACIN pullup resistor from VCC3 to VCC5
- sheet 14: Change ACIN series resistor value to 100 ohms
- sheet 14: Stronger ACIN pullup, the Elan has internal Pulldown
- sheet 14: Add 10uF/10v caps to power planes

REV 1.5 - 7/1/94 - SHEET 3: Moved location of R30,series resistor on 32 khz xtal.
- SHEET 3: Changed value of R29, parallel resistor on 32 khz xtal to 15M to allow faster startup.
- SHEET 3: Changed value of R21, reset RC resistor, to 390K to provide longer reset.
- SHEET 3: Changed value of R19 to 100 Ohms to speed up RESUME# edge.
- SHEET 3: Speaker circuit was fixed by installing a .1uF cap and a 33 Ohm res in series with spkr.
- SHEET 3: Changed the value of the PLL caps to .47uF to reduce clock jitter.
- SHEET 5: Changed SDEN#,SDWRTH,SDWRTL to 3V levels.
- SHEET 9: Added 1M pullups to pin 58 of P2 and P3.
- SHEET 11: KB controller mods to allow functionality in SUSPEND/RESUME states.
- SHEET 12: Gated PGP1 and PGP2 thru an OR gate to the HD conn. to fix backdrive issue.
- SHEET 12: Added 1K pullup to VCC3 on PGPB.
- SHEET 13: Added battery to MAX722 to fix 3V powerup issue.
- SHEET 13: Pulled up SHDN# signal on MAX722 to VCC3 instead of VCC5.
- SHEET 13: Added 1M series resistor on ENAVEE.

REV 1.6 - 9/5/94 - This revision of schematics includes rev D rework.
SHEET 2: Changed MEMR# and MEMW# labels to EMEMR# & EMEMW#.
SHEET 2: Changed value of BUSY pullup resistor from 10K to 1K.
SHEET 2: Changed value of NA# pullup resistor from 10K to 1K.
SHEET 2: Changed value of LOCLDEV# pullup resistor from 10K to 1K.
SHEET 2: Changed value of R18 from 1K to 10K.
SHEET 2: Added 10K pullup to IRQ1.
SHEET 3: Modified Loop Filter values and locations.
SHEET 5: Connected DIR pin on U8 & U9 to VCCMEM3 instead of VCCSYS5.
SHEET 6: Changed U15 device type from HCT to ACT.
SHEET 7: Added pullup resistor (1K) to VGARDY#.
SHEET 8: Terminated unused inputs on PCMCIA Buffer with 100K resistors.
SHEET 8: Added logic to gate off the MEMR# & MEMW# signals during PCMCIA cycles.
SHEET 8: Added external buffer for command signals going out to PCMCIA sockets.
SHEET 9: Added resistors to prevent floating inputs on PCMCIA signals.
SHEET 9: Pulled PCMCIA resets down instead of up.
SHEET 10: Made corrections to RS232 driver symbol. Pin 27 is now C2+ & Pin 26 is C1+.
SHEET 13: Deleted RESIN# signal coming from P/S.

|LINK
p 1 revision
p 2 |elanchip.sch
p 3 |elanmisc.sch
p 4 |dram.sch
p 5 |buffs.sch
p 6 |biosdos.sch
p 7 |vga.sch
p 8 |pcmbufct.sch
p 9 |pcmbcon.sch
p 10 |serpar.sch
p 11 |keybrd.sch
p 12 |flopide.sch
p 13 |power.sch
p 14 |psblock1.sch
p 15 |psblock2.sch
p 16 |psblock3.sch

Rev 1.7 - 12/18/94 - Added rev B support circuitry.
Sheet 2: Pulled up IOCS16#,MCS16#,IRQ14,IOCHRDY TO VCC1 INSTEAD OF VCC3.
Sheet 2: Pin 140 on ELAN is XIORESET# on ELAN rev B.
Sheet 2: Seperated VCC core & VCC1 on ELAN.
Sheet 2: Added decoupling caps to VCC1 plane.
Sheet 2: Deleted R12 pulldownon pin 140 of ELAN.
Sheet 2: Added filtering circuitry for the AVCC & VCC core planes.
Sheet 2: Added option to support XIORESET# signal on ELAN rev B.
Sheet 3: Changed C24 & C25 values to 22pF.
Sheet 3: Changed R29 value to 10M.
Sheet 4: Added SA12(MA11) to SIMM socket to allow support for asymmetrical DRAM when using an ELAN rev B device.
Sheet 5: Added option to allow LVDD# or SA12 to function as local bus address 12 when using an ELAN rev B device.
Sheet 8: Added option to allow gating of MEMR# & MEMW# to ISA bus or allowing parallel port signals to be redefined as PCMCIA command signals. This is an option for the ELAN rev B device.
Sheet 10: Added option to allow EMEMR# or SLCTIN# to drive PCMCIA PMEMR#
Sheet 10: Added option to allow EMEMW# or INIT# to drive PCMCIA PMEMW#
Sheet 11: Deleted KB controller suspend errata fix.
Made a note specifying the type of device we recommend.
Sheet 12: Pulled up PGP1 to VCC1 instead of VCC3.
Sheet 14-16: Created Power supply block diagrams showing uPower mode support.

Note: pages 14-16 have to be unlinked from schematic before attempting to generate a netlist or BOM. Pages 13-15 are block diagrams.

Rev 1.8 - 11/13/95 - Fixed the vga.sch page.
There are two different package types for this part (T and F).
Sheet 7: Changed the name of the C&T 65510 to F65510.
Sheet 7: Added a 1.5K pull down resistor to MA4 per the F65510 spec.
This enables clock doubling on the CLKIN input if using a frequency less than 25MHz.

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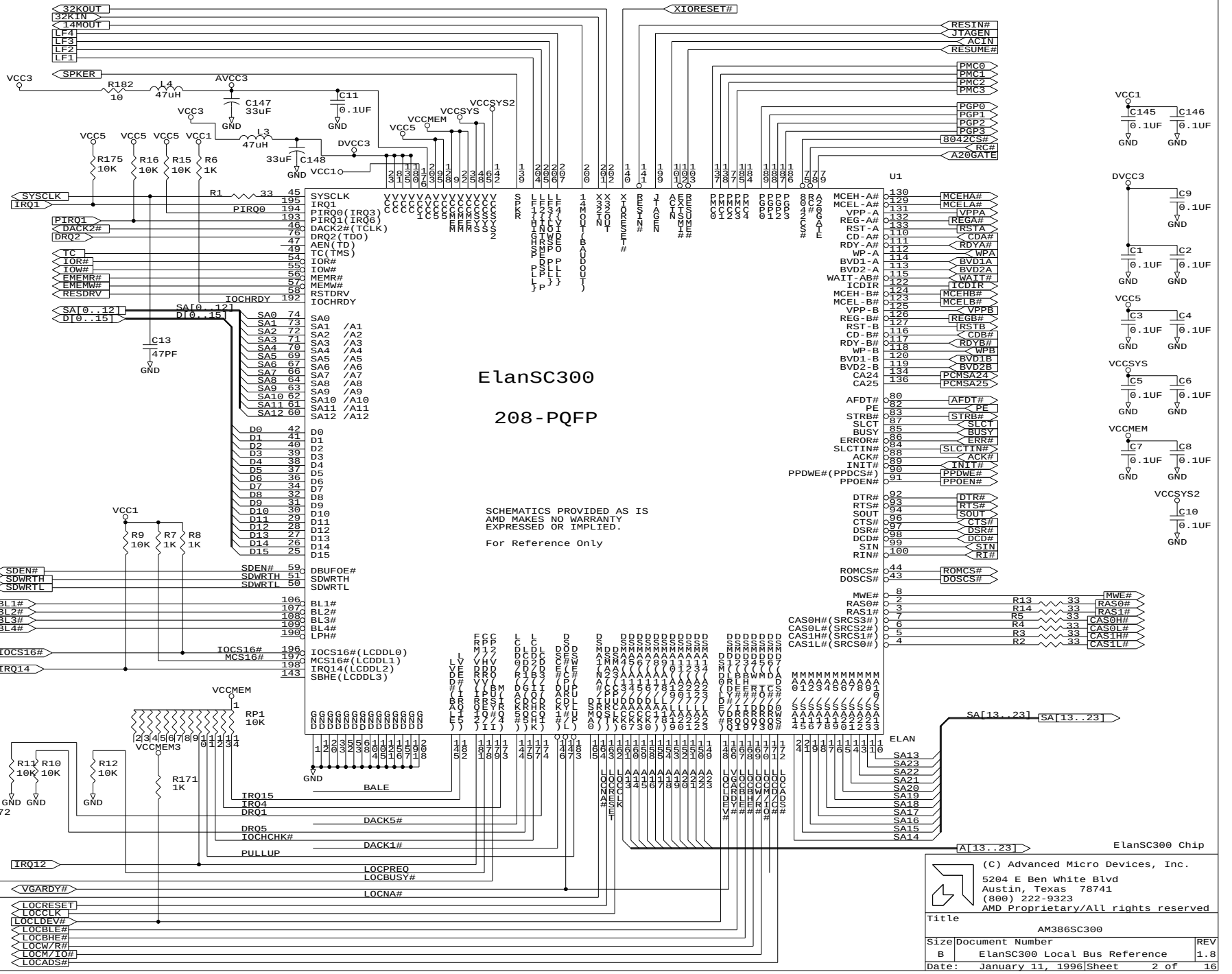
Title: Revision History

Size	Document Number	REV
B	ElanSC300 Local Bus Reference	1.8

Date: January 11, 1996 Sheet 1 of 16


ElanSC300
208-PQFP
SCHEMATICS PROVIDED AS IS
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For Reference Only
U1
ELAN
ElanSC300 Chip
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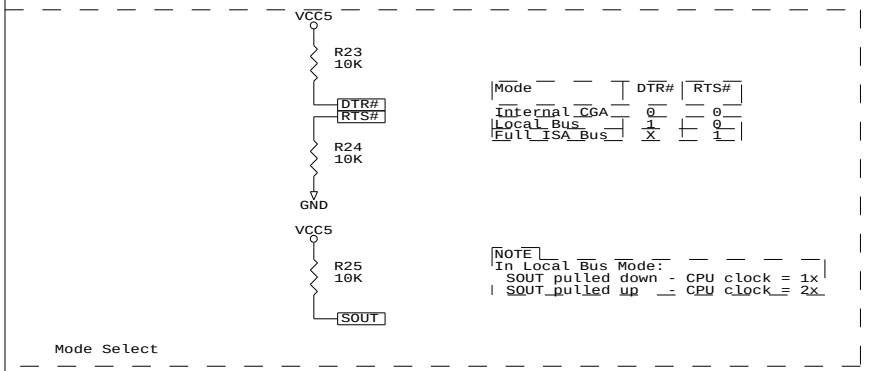
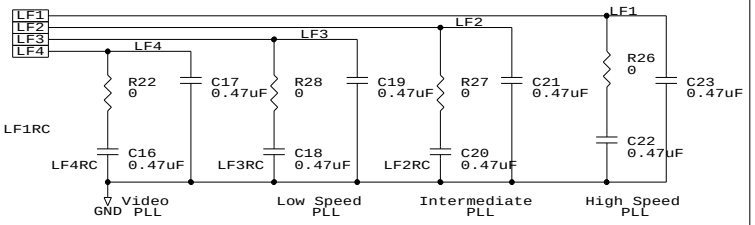
Title
AM386SC300
Size B
Document Number
ElanSC300 Local Bus Reference
REV 1.8
Date: January 11, 1996
Sheet 2 of 16



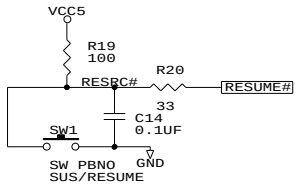
Mode Select

C17,C19,C21 & C23 shpuld not be installed.
Footprints should still be put on board as place holders
for future revisions of the chip.

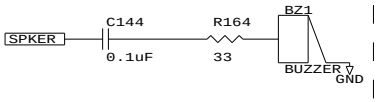


NOTE
Place these componments close to the
ElanSC300 pins to minimize trace length.

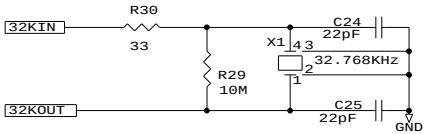
ElanSC300 Chip Loop Filters



Suspend/Resume Switch



System Speaker



32KHz Crystal

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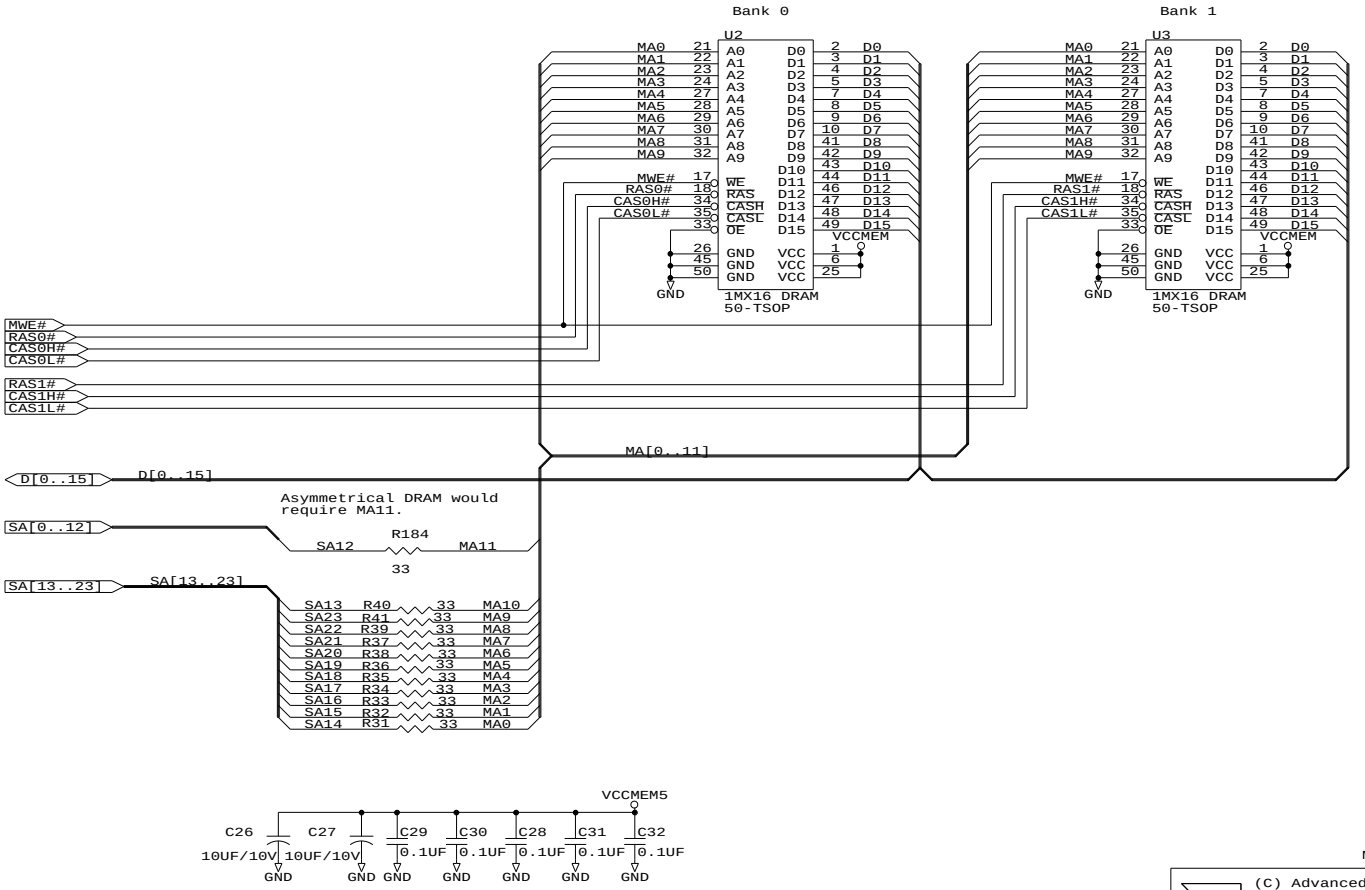
Title	Xtal, Loop Filters, Switches	
Size: B	Document Number: ElanSC300 Local Bus Reference	REV: 1.8
Date: January 11, 1996	Sheet 3 of 16	



Main DRAM System Memory

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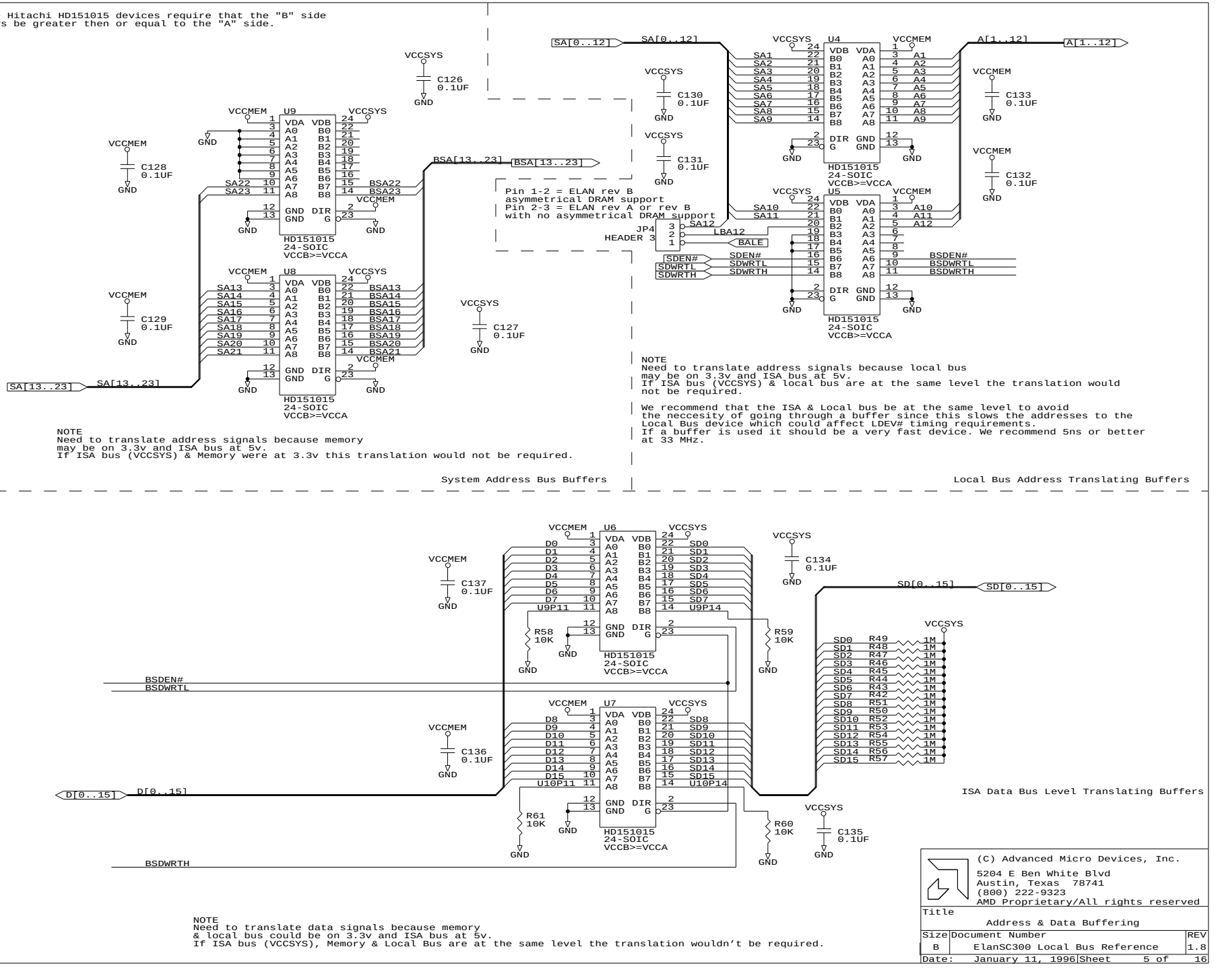
Title		
DRAM Main Memory		
Size: B	Document Number: ElanSC300 Local Bus Reference	REV: 1.8
Date: January 11, 1996	Sheet 4 of 16	


These Hitachi HD151015 devices require that the "B" side always be greater then or equal to the "A" side.
U9
U8
U4
U5
HD151015
24-SOIC
VCCB>=VCCA
VCCSYS
VCCMEM
GND
C126 0.1UF
C128 0.1UF
C129 0.1UF
C127 0.1UF
C130 0.1UF
C131 0.1UF
C133 0.1UF
C132 0.1UF
SA[13..23]
BSA[13..23]
SA[0..12]
A[1..12]
Pin 1-2 = ELAN rev B asymmetrical DRAM support
Pin 2-3 = ELAN rev A or rev B with no asymmetrical DRAM support
JP4
HEADER 3
LBA12
BALE
SA12
SDEN#
SDWRTL
SDWRTH
BSDEN#
BSDWRTL
BSDWRTH
NOTE
Need to translate address signals because memory may be on 3.3v and ISA bus at 5v.
If ISA bus (VCCSYS) & Memory were at 3.3v this translation would not be required.
NOTE
Need to translate address signals because local bus may be on 3.3v and ISA bus at 5v.
If ISA bus (VCCSYS) & local bus are at the same level the translation would not be required.
We recommend that the ISA & Local bus be at the same level to avoid the neccesity of going through a buffer since this slows the addresses to the Local Bus device which could affect LDEV# timing requirements.
If a buffer is used it should be a very fast device. We recommend 5ns or better at 33 MHz.
System Address Bus Buffers
Local Bus Address Translating Buffers
U6
U7
C137 0.1UF
C136 0.1UF
C134 0.1UF
C135 0.1UF
R58 10K
R59 10K
R61 10K
R60 10K
SD[0..15]
D[0..15]
R49 1M
R48 1M
R47 1M
R46 1M
R45 1M
R44 1M
R43 1M
R42 1M
R51 1M
R50 1M
R52 1M
R53 1M
R54 1M
R55 1M
R56 1M
R57 1M
ISA Data Bus Level Translating Buffers
NOTE
Need to translate data signals because memory & local bus could be on 3.3v and ISA bus at 5v.
If ISA bus (VCCSYS), Memory & Local Bus are at the same level the translation wouldn't be required.
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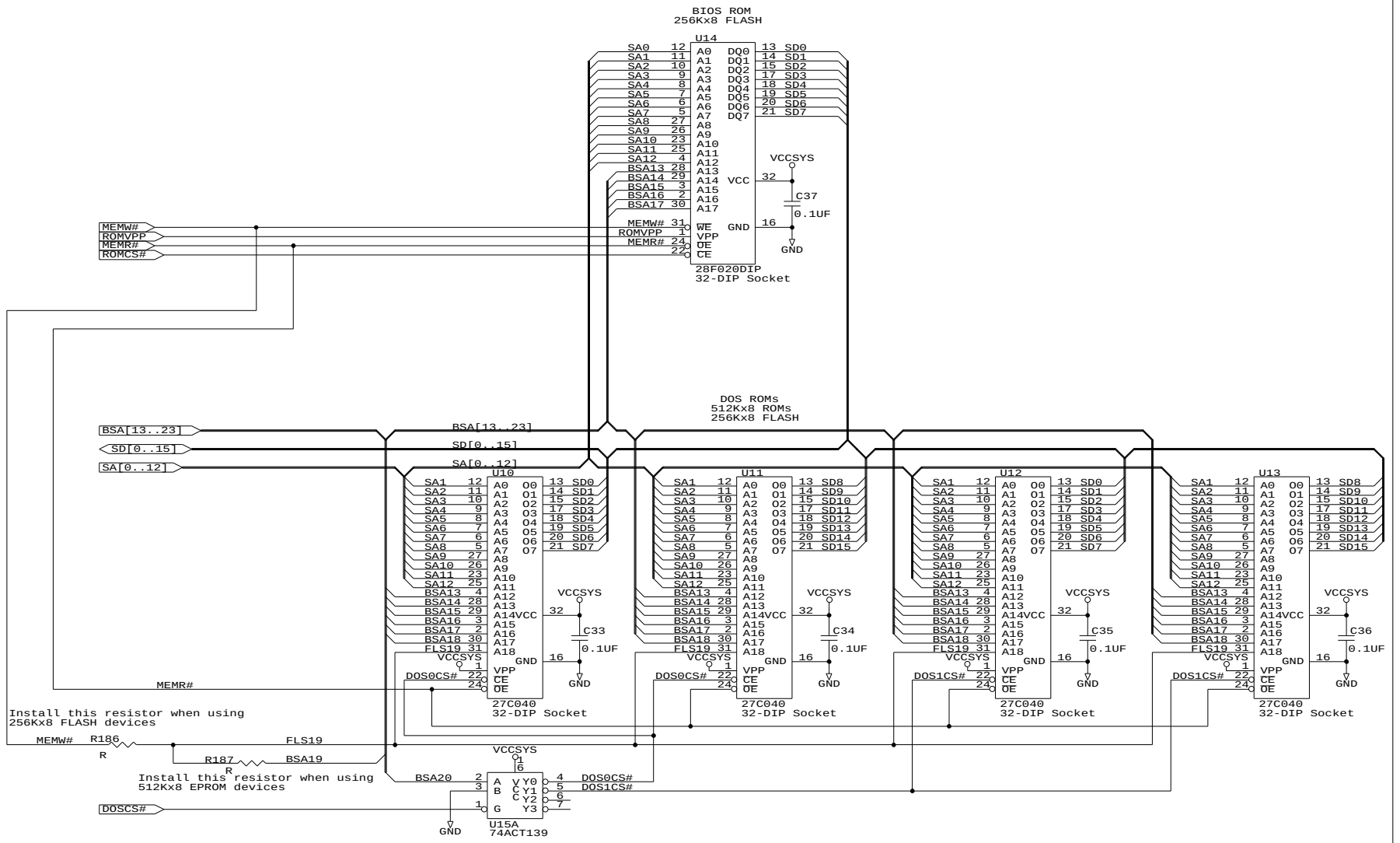
Title
Address & Data Buffering
Size B
Document Number ElanSC300 Local Bus Reference
REV 1.8
Date: January 11, 1996
Sheet 5 of 16



BIOS & DOS ROMs

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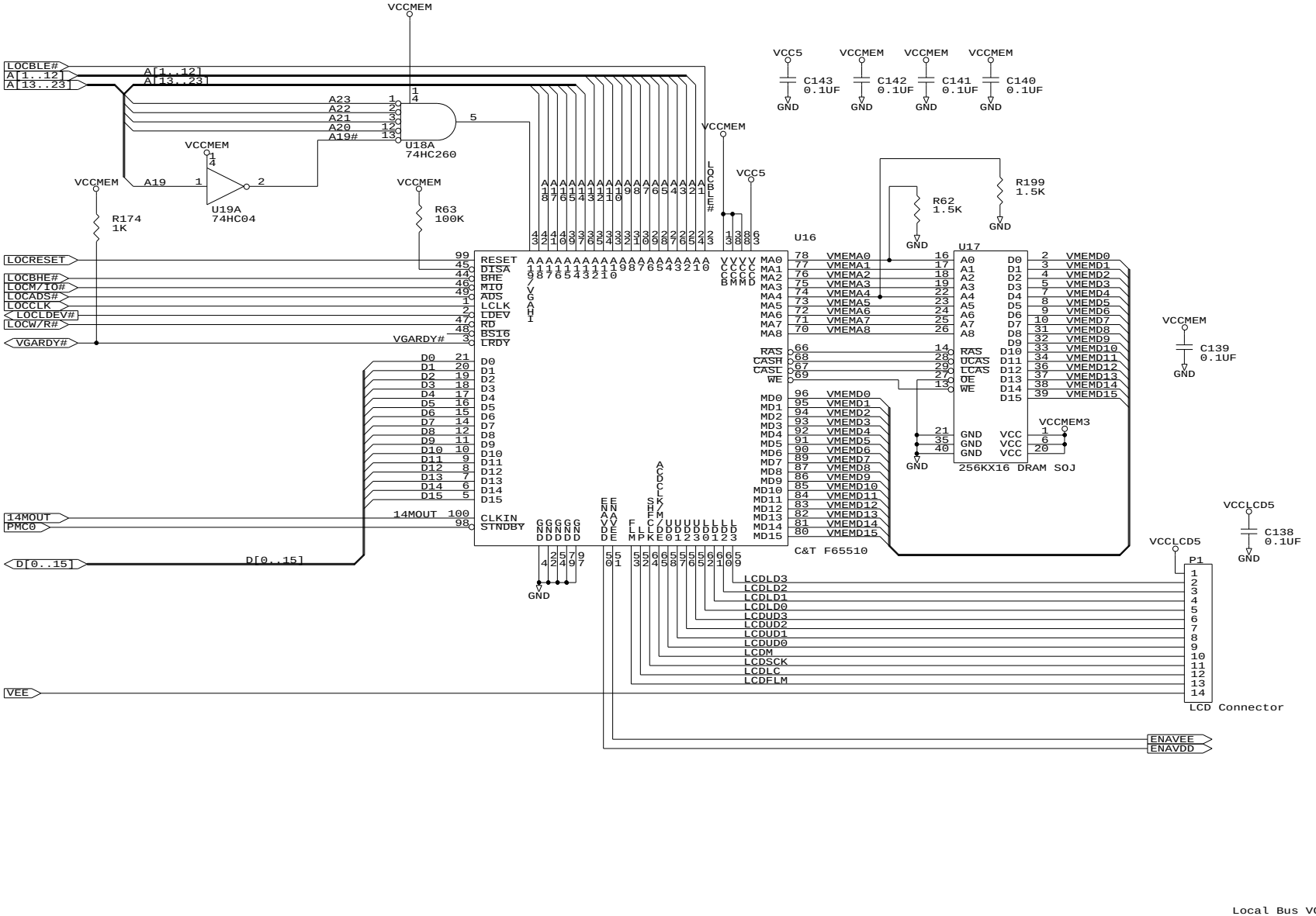
Title		
BIOS & DOS ROMs		
Size	Document Number	REV
B	ElanSC300 Local Bus Reference	1.8
Date: January 11, 1996	Sheet 6 of 16	



Local Bus VGA

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Local Bus VGA		
Size	Document Number	REV
B	ElanSC300 Local Bus Reference	1.8
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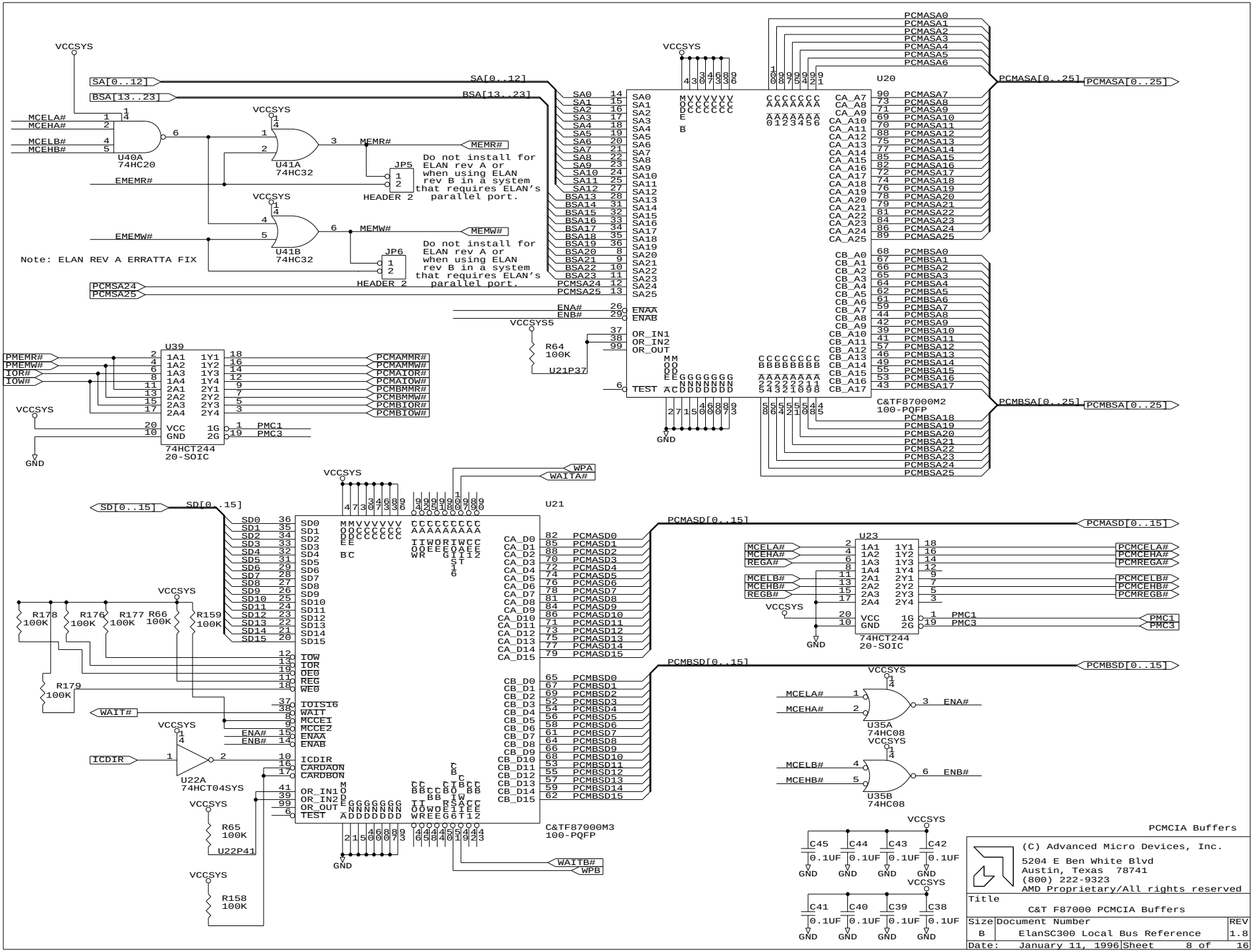
VCCSYS
SA[0..12]
BSA[13..23]
MCELA#
MCEHA#
MCELB#
MCEHB#
U40A
74HC20
U41A
74HC32
MEMR#
EMEMR#
JP5
HEADER 2
Do not install for ELAN rev A or when using ELAN rev B in a system that requires ELAN's parallel port.
U41B
74HC32
MEMW#
EMEMW#
JP6
Note: ELAN REV A ERRATTA FIX
PCMSA24
PCMSA25
U20
PCMASA[0..25]
ENA#
ENB#
VCCSYS5
R64
100K
U21P37
OR_IN1
OR_IN2
OR_OUT
TEST
C&TF87000M2
100-PQFP
PCMBSA[0..25]
U39
PMEMR#
PMEMW#
IOR#
IOW#
PCMAMMR#
PCMAMMW#
PCMAIOR#
PCMAIOW#
PCMBMMR#
PCMBMMW#
PCMBIOR#
PCMBIOW#
74HCT244
20-SOIC
PMC1
PMC3
GND
WPA
WAITA#
U21
SD[0..15]
R178
R176
R177
R66
R159
R179
100K
IOW
IOR
OE0
REG
WE0
IOIS16
WAIT
MCCE1
MCCE2
ENAA
ENAB
ICDIR
CARDAON
CARDBON
U22A
74HCT04SYS
R65
R158
U22P41
C&TF87000M3
100-PQFP
WAITB#
WPB
U23
REGA#
REGB#
U35A
U35B
74HC08
C45
C44
C43
C42
C41
C40
C39
C38
0.1UF
PCMCIA Buffers
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Title
C&T F87000 PCMCIA Buffers
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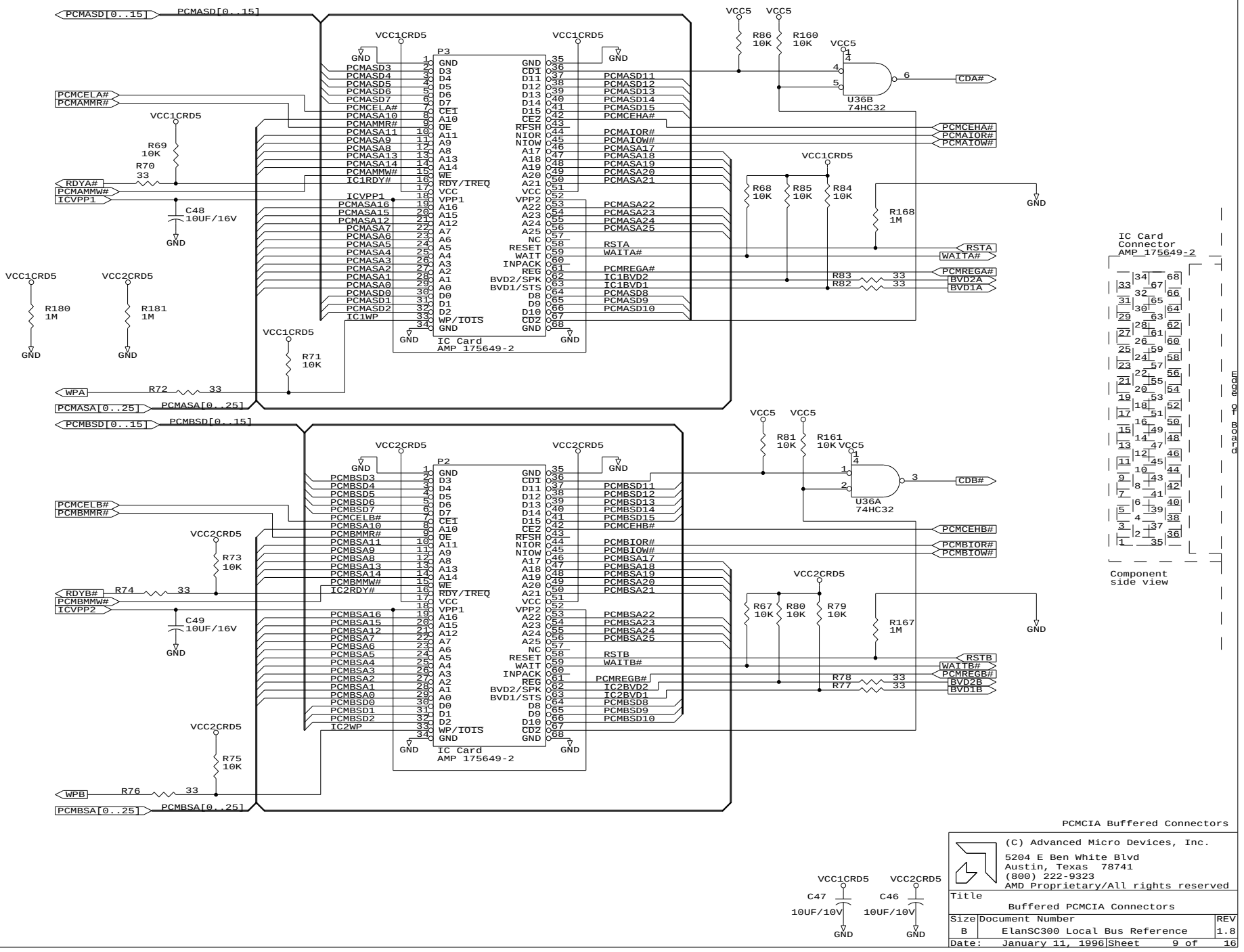
REV 1.8
Date: January 11, 1996
Sheet 8 of 16



PCMCIA Buffered Connectors

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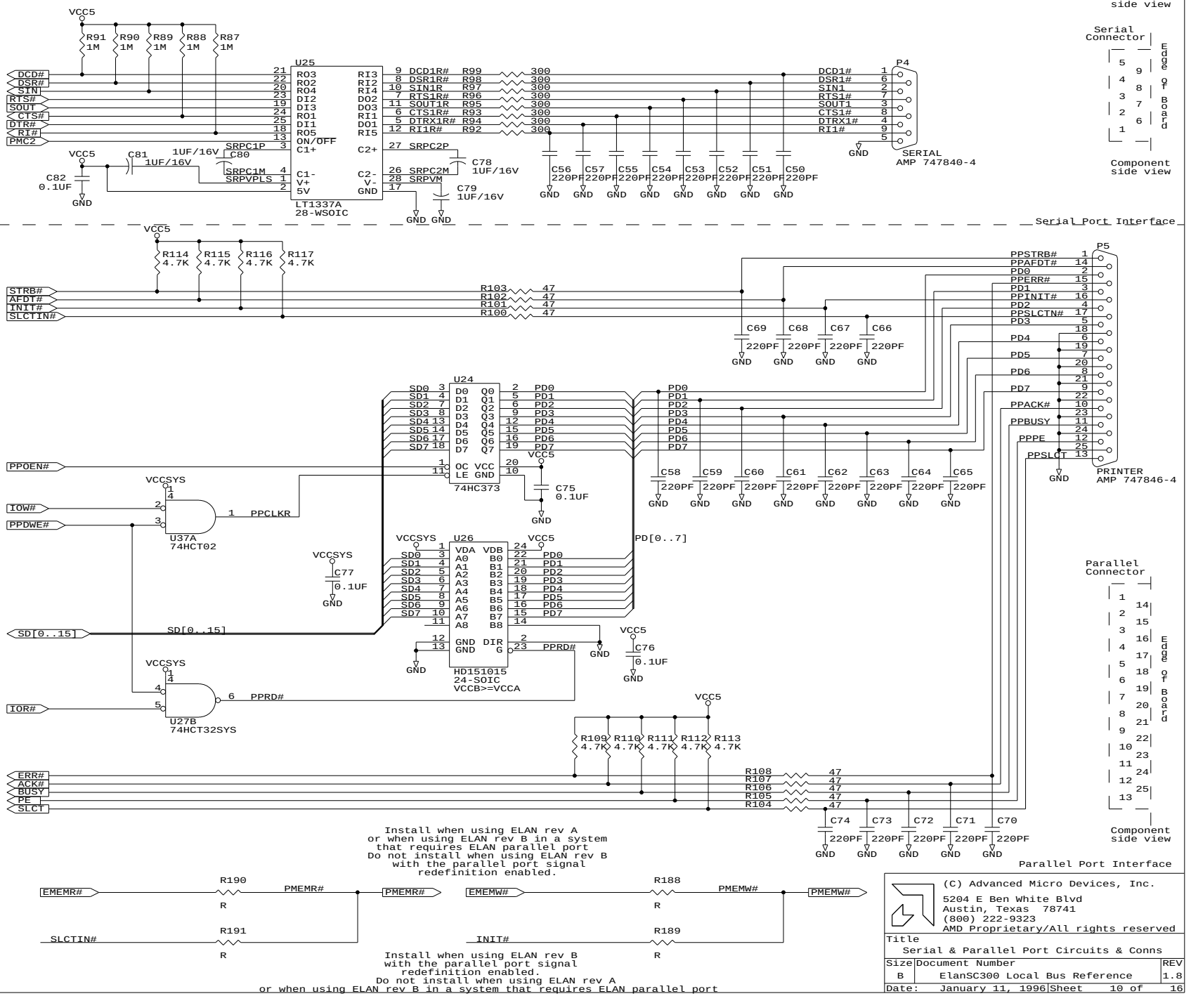
Title	Buffered PCMCIA Connectors	
Size: B	Document Number: ElanSC300 Local Bus Reference	REV: 1.8
Date: January 11, 1996	Sheet 9 of 16	



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Title
Serial & Parallel Port Circuits & Conns

Size	Document Number	REV
B	ElanSC300 Local Bus Reference	1.8

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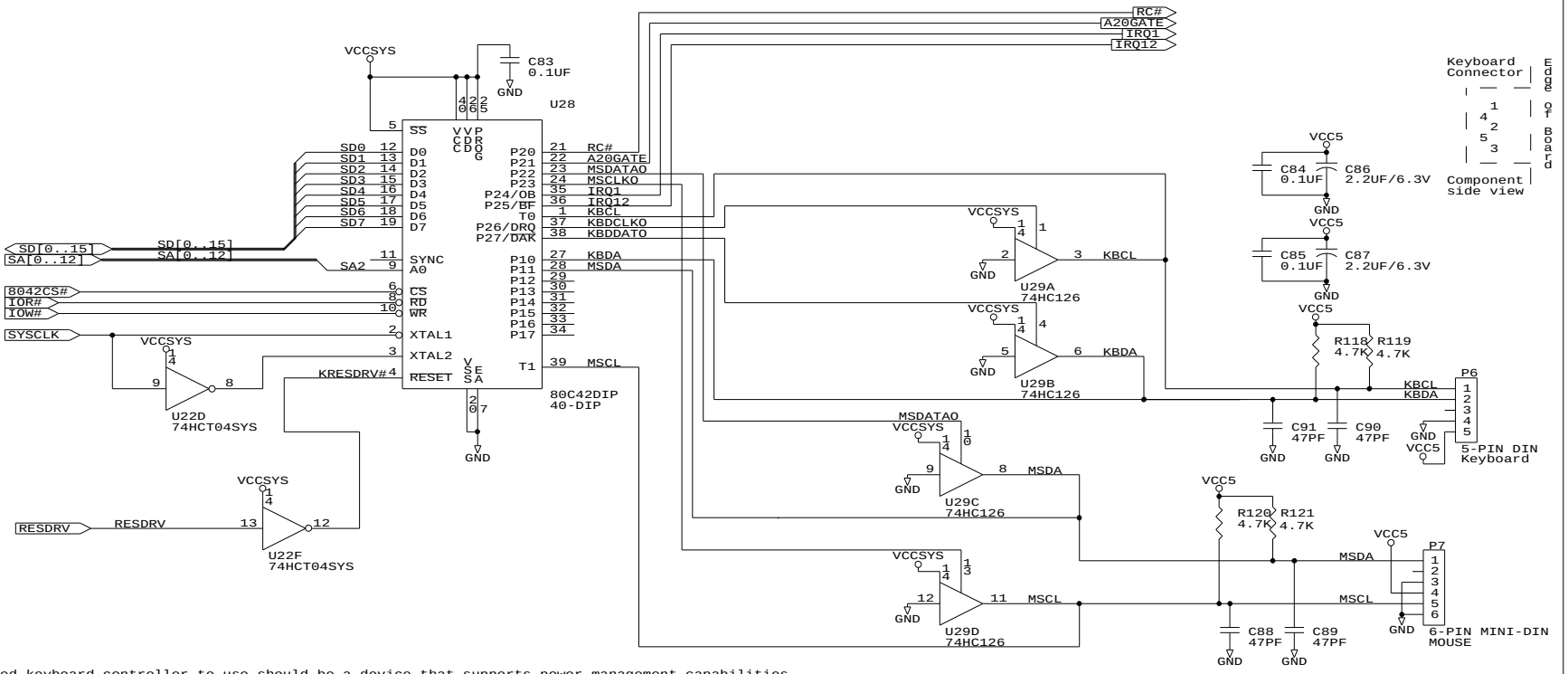

The recommended keyboard controller to use should be a device that supports power management capabilities.
This is neccesary to avoid issues that may arise when suspending the system.

Keyboard & Mouse Processor & Connectors

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Title		
SCP, Keyboard, & Mouse		
Size: B	Document Number: ElanSC300 Local Bus Reference	REV: 1.8
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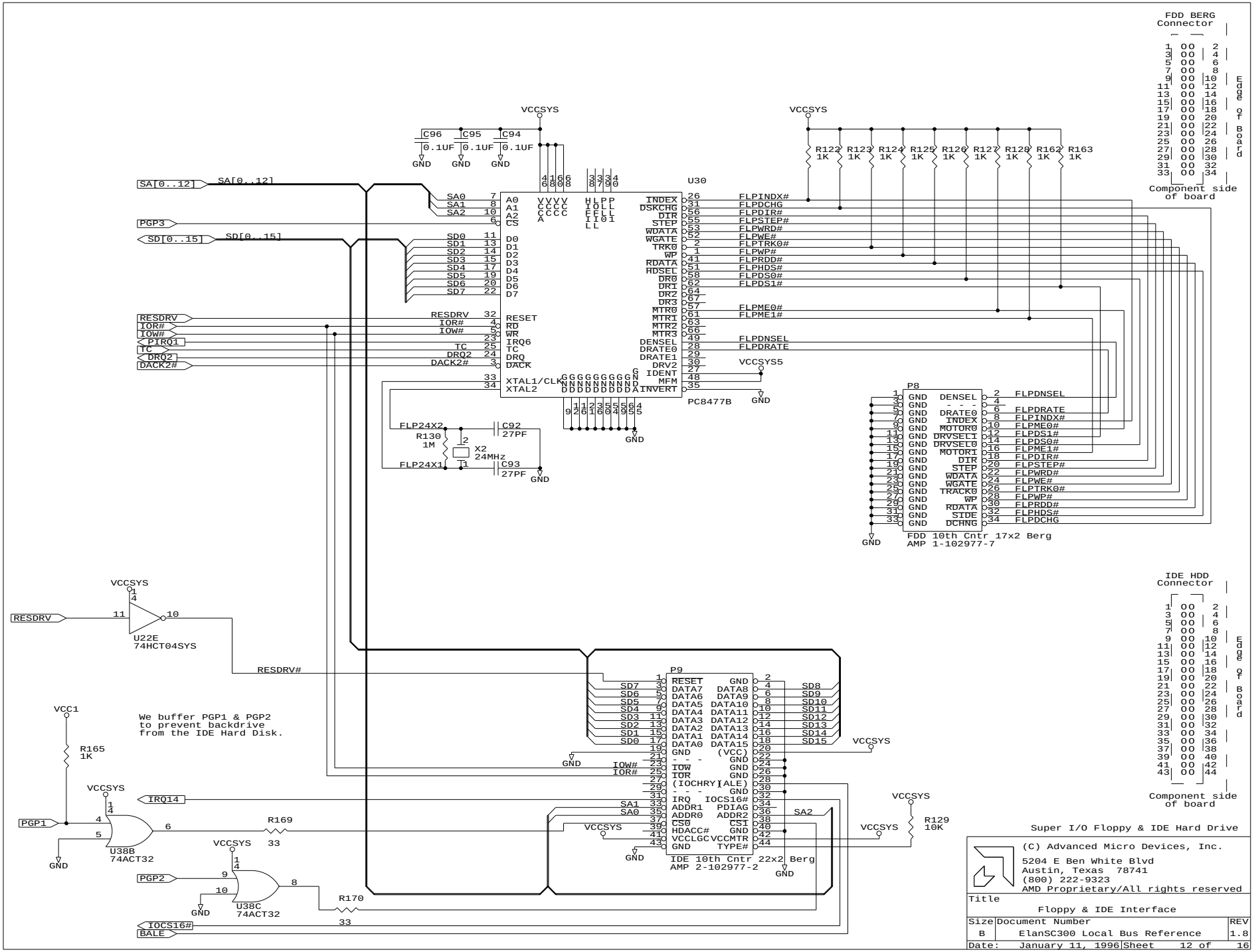
FDD BERG Connector
Edge of Board
Component side of board
VCCSYS
C96 0.1UF
C95 0.1UF
C94 0.1UF
GND
R122 1K
R123 1K
R124 1K
R125 1K
R126 1K
R127 1K
R128 1K
R162 1K
R163 1K
SA[0..12]
SA[0..12]
PGP3
SD[0..15]
SD[0..15]
U30
SA0 SA1 SA2
CS
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7
D0 D1 D2 D3 D4 D5 D6 D7
RESDRV
IOR#
IOW#
PIRQ1
TC
DRQ2
DACK2#
RESET RD WR IRQ6 TC DRQ DACK
XTAL1/CLK
XTAL2
INDEX DSKCHG DIR STEP WDATA WGATE TRK0 WP RDATA HDSEL DR0 DR1 DR2 DR3 MTR0 MTR1 MTR2 MTR3 DENSEL DRATE0 DRATE1 DRV2 IDENT MFM INVERT
FLPINDX# FLPDCHG FLPDIR# FLPSTEP# FLPWRD# FLPWE# FLPTRK0# FLPWP# FLPRDD# FLPHDS# FLPDS0# FLPDS1# FLPME0# FLPME1# FLPDNSEL FLPDRATE
VCCSYS5
PC8477B
FLP24X2
R130 1M
X2 24MHz
FLP24X1
C92 27PF
C93 27PF
P8
FLPDNSEL FLPDRATE FLPINDX# FLPME0# FLPDS1# FLPDS0# FLPME1# FLPDIR# FLPSTEP# FLPWRD# FLPWE# FLPTRK0# FLPWP# FLPRDD# FLPHDS# FLPDCHG
FDD 10th Cntr 17x2 Berg
AMP 1-102977-7
IDE HDD Connector
Edge of Board
Component side of board
RESDRV
U22E 74HCT04SYS
RESDRV#
We buffer PGP1 & PGP2 to prevent backdrive from the IDE Hard Disk.
VCC1
R165 1K
PGP1
PGP2
U38B 74ACT32
U38C 74ACT32
R169 33
R170 33
IRQ14
IOCS16#
BALE
P9
RESET DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0 GND (VCC) IOW# IOR# (IOCHRY) IRQ SA1 SA0 ADDR1 ADDR0 CS0 HDACC# VCCLGC GND
DATA8 DATA9 DATA10 DATA11 DATA12 DATA13 DATA14 DATA15 GND VCCMTR (ALE) IOCS16# PDIAG ADDR2 CS1 GND TYPE#
SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15
SA2
R129 10K
IDE 10th Cntr 22x2 Berg
AMP 2-102977-2
Super I/O Floppy & IDE Hard Drive
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Title
Floppy & IDE Interface
Size B
Document Number ElanSC300 Local Bus Reference
REV 1.8
Date: January 11, 1996
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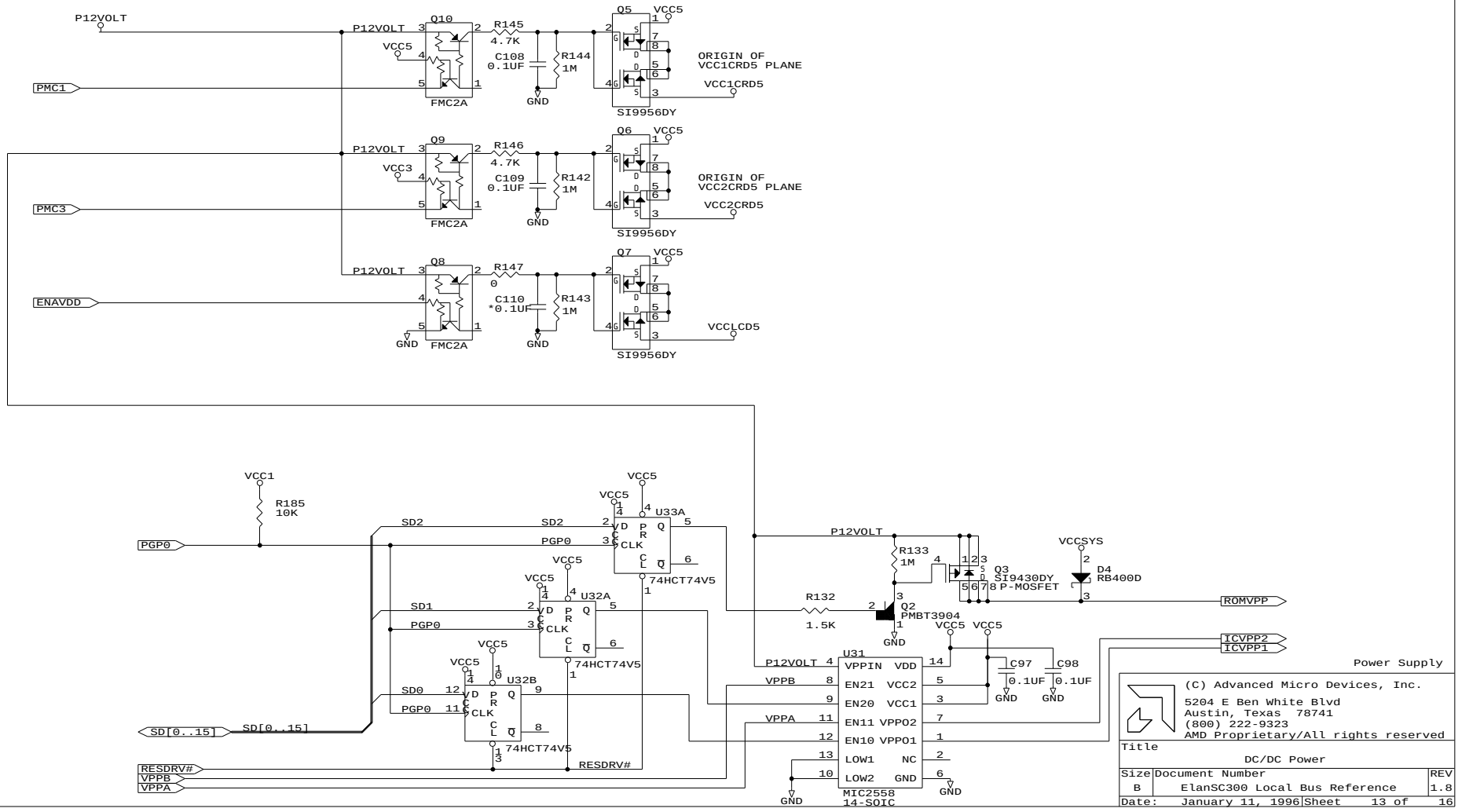

Power Supply

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Title		
DC/DC Power		
Size	Document Number	REV
B	ElanSC300 Local Bus Reference	1.8
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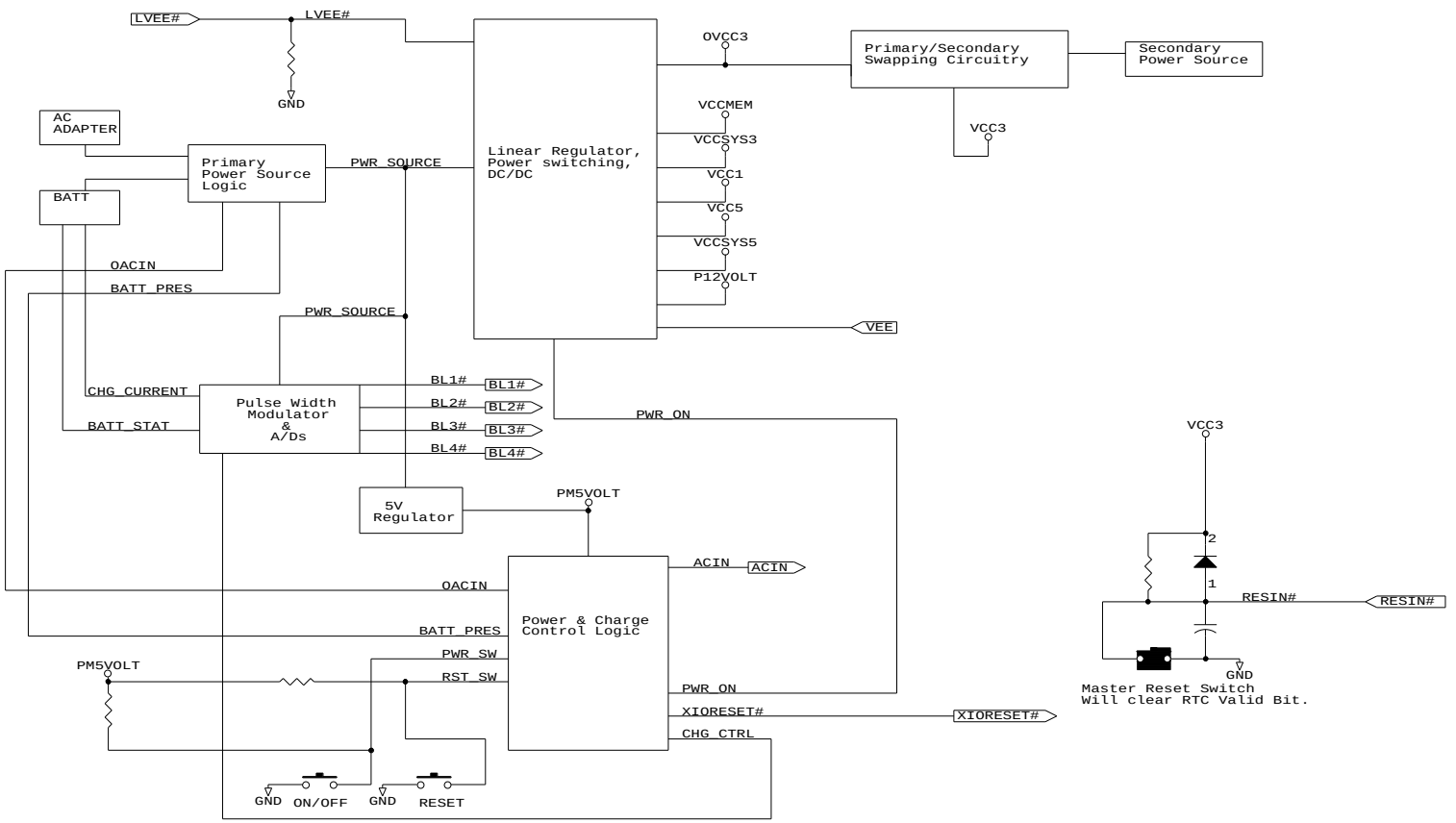

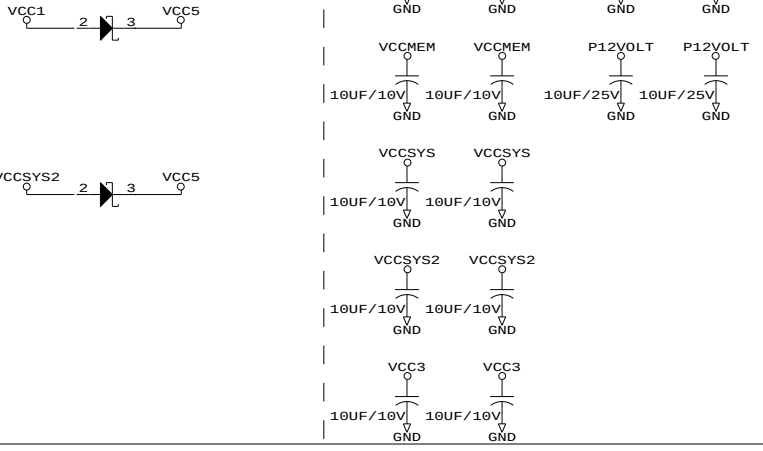

ELAN REV B ONLY
MINIMUM uPower mode configuration

With this implementation the idea is to prevent the RTC RAM from losing its contents while in uPower OFF mode. This is accomplished by allowing the secondary power source to keep the VCC3 plane powered up during uPower OFF mode.

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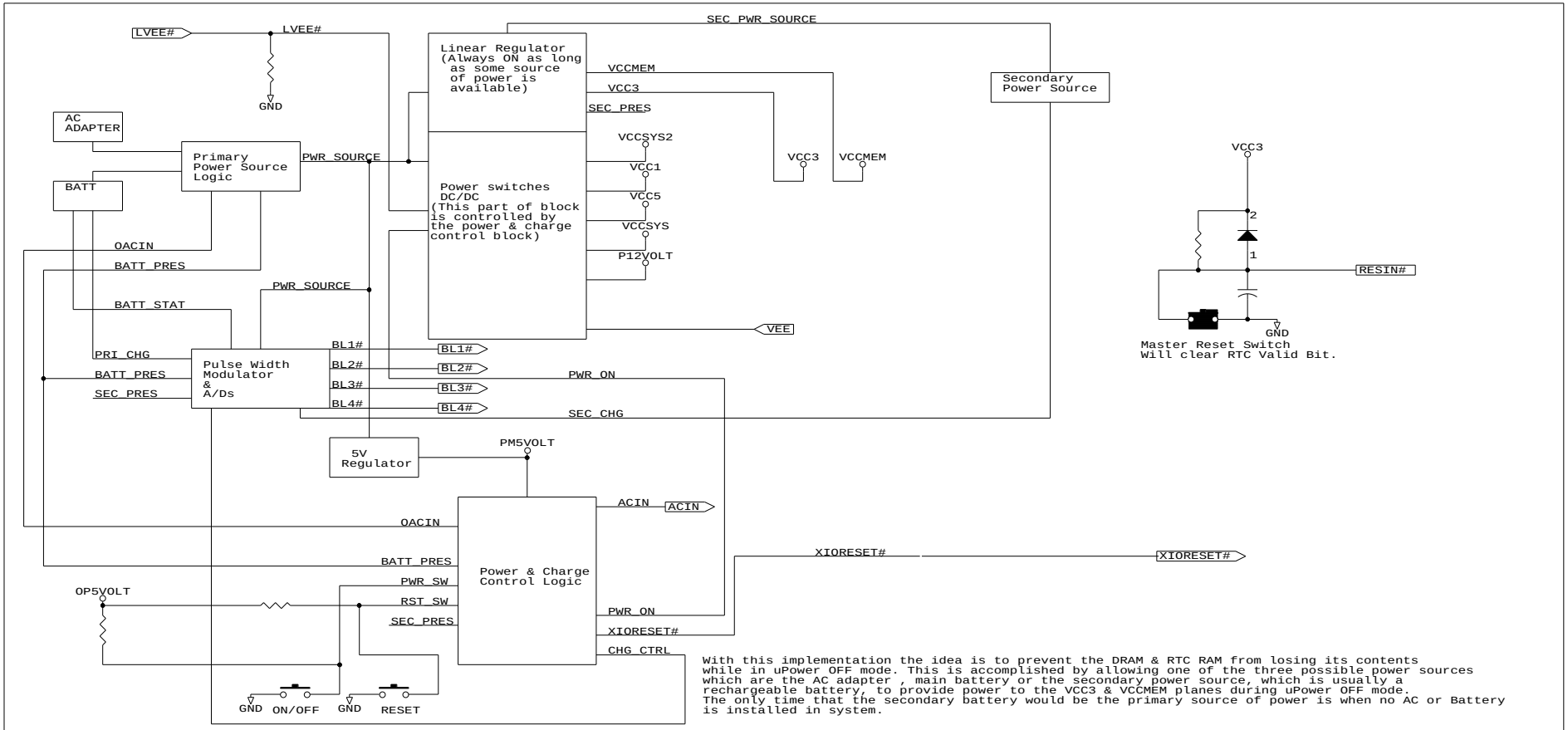
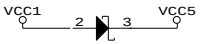
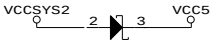
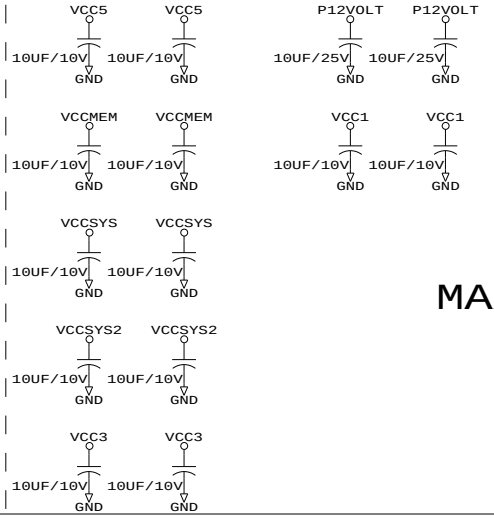
Title: ELAN Rev B uPower mode P/S Block Diagram		
Size: B	Document Number: ElanSC300 Local Bus Reference	REV: 1.8
Date: January 11, 1996	Sheet 14 of 16	



With this implementation the idea is to prevent the DRAM & RTC RAM from losing its contents while in uPower OFF mode. This is accomplished by allowing one of the three possible power sources which are the AC adapter , main battery or the secondary power source, which is usually a rechargeable battery, to provide power to the VCC3 & VCCMEM planes during uPower OFF mode. The only time that the secondary battery would be the primary source of power is when no AC or Battery is installed in system.







ELAN REV B ONLY
MAXIMUM uPower Mode Configuration

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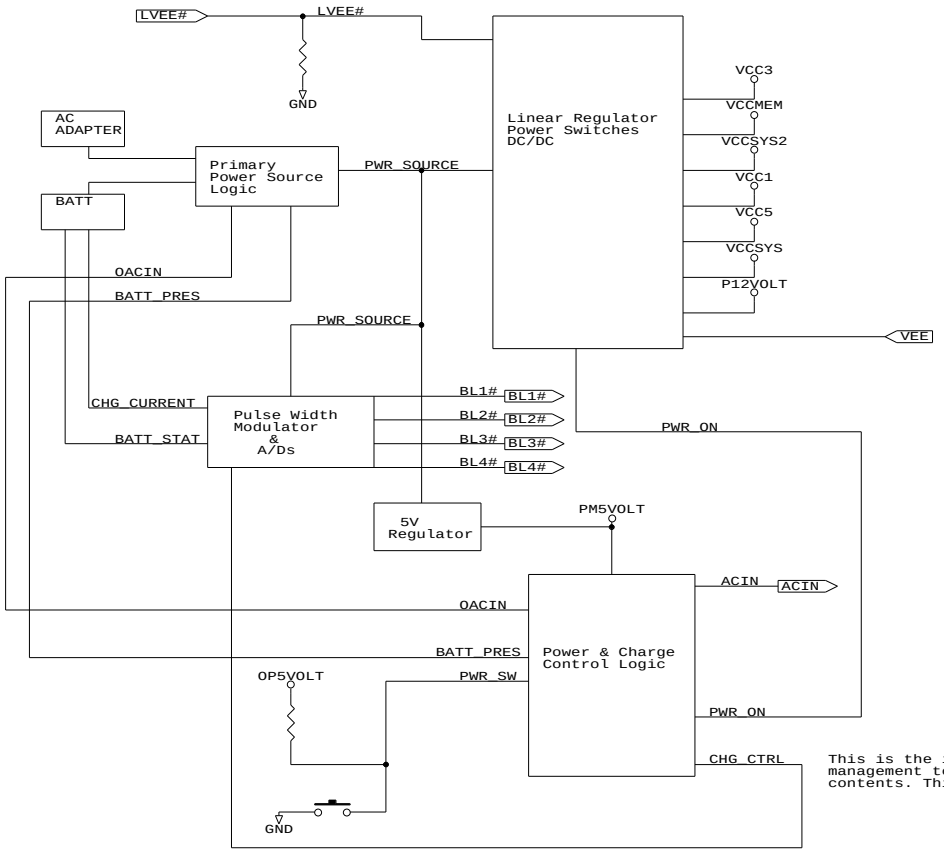
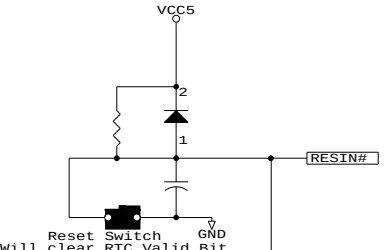
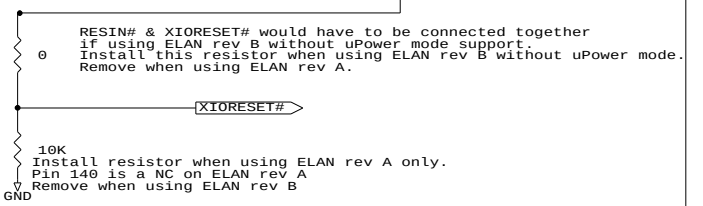
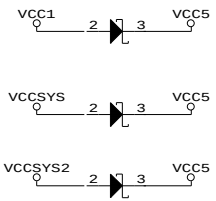
Title: ELAN Rev B uPower mode P/S Block Diagram		
Size: B	Document Number: ElanSC300 Local Bus Reference	REV: 1.8
Date: January 11, 1996	Sheet 15 of 16	



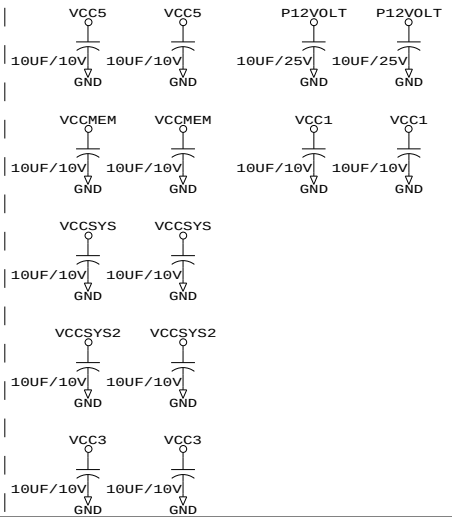




This is the implementation where the system would be normally ON all the time relying on power management to conserve battery power. If the system were to be turned OFF, the RTC RAM would lose its contents. This would also be the implementation if using an ELAN rev B without uPower mode support.



ELAN rev A4



ELAN rev A P/S Block Diagram

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Title		
ELAN Rev A P/S Block Diagram		
Size	Document Number	REV
B	ElanSC300 Local Bus Reference	1.8
Date: January 11, 1996	Sheet 16 of 16	

ElanSC300 Internal Video Reference Design Revision History:

Rev 1.0
Rev 1.1 - 1/24/94 - Added pulldown resistor (R12) to pin 140 of ELAN (page 2).
Rev 1.2 - 1/26/94 - Fixed pinout of ELAN (page 2)

Was: Name - Pin

LF1	- 207
LF2	- 206
LF3	- 205
LF4	- 204

Now: Name - Pin

LF1{HIGHSP PLL}	- 204
LF2{INTERMEDSP PLL}	- 205
LF3{LOWSP PLL}	- 206
LF1{VIDEO PLL}	- 207

- Swapped Intermediate PLL & Low Speed PLL labels on page 3.
- Added this Revision History page.

Rev 1.3 - 3/11/94 - Revisions from debug of Emulation Board.
- Upgraded schematics to OrCad 386+
- Moved this revision page to sheet 1
- Changed signal names for PCMCIA slots:

Old	New	Old	New
MCE1#	MCEHA#	MCE2#	MCEHB#
MCE12#	MCELA#	MCE22#	MCELB#
VPP1	VPPA	VPP2	VPPB
REG1#	REGA#	REG2#	REGB#
1ICRST	RSTA	2ICRST	RSTB
CD1#	CDA#	CD2#	CDB#
RDY1#	RDYA#	RDY2#	RDYB#
WP1	WPA	WP2	WPB
BVD11	BVD1A	BVD21	BVD1B
BVD12	BVD2A	BVD22	BVD2B
		ISA24	PCMSA24
		ISA25	PCMSA25

- sheet 2: renamed LCDD0-3 signals on ELAN (second functions of pins don't change)
- sheet 2: removed REFRESH (REF on pin 148) function from ELAN
- sheet 2: move pullup resistors (R6-9) to VCC3 from VCC5
- sheet 2: add pullup resistors to signals PIRQ0-1
- sheet 2: add better filtering to AVCC (pin 203) of Elan
- sheet 2: add cap to SYSCLK signal for filtering
- sheet 2: run IOCS16# signal off page for IDE HDD on sheet 11
- sheet 2: Elan pin 140 pulldown resistor changed to 1K ohm
- sheet 2: renamed PGPA-D to PGP0-3
- sheet 3: move RESET pullup resistor & diode from VCC3 to VCC5
- sheet 3: move RESUME pullup resistor from VCC3 to VCC5
- sheet 3: fix 32KHz Xtal resistor & cap values, add series resistor to 32KIN signal
- sheet 8: changed series resistor values to 33 ohms
- sheet 8: changed pullup resistor values to 10K ohms
- sheet 8: PCMCIA connector pin changes: pin 7 is MCEHx# & pin 42 is MCELx#
- sheet 10: added inverter to clock line for 80C42
- sheet 10: changed mouse & keyboard clock & data caps to 47pF
- sheet 11: added pullup resistor to PGPB
- sheet 11: added IOCS16# & VCC to IDE connector
- sheet 12: added series resistor to RESIN# signal to power connector
- sheet 13: changed signal name on switch from ACIN to SW_ACIN

Rev 1.4 - 4/19/94 - Revisions from debug of Evaluation Board.
- sheet 2: Change name on ELAN chip pin 183 to PULLUP
- sheet 3: Change DTR# & RTS# pullup & down resistors to 10K ohm
- sheet 3: Fix pinout of 32KHz xtal & component values in circuit
- sheet 5: Add bypass caps to buffers
- sheet 8: fix MCELx# and MCEHx# on connectors
  for the last time:
  CE1# = pin 7 = Even = LOW
  CE2# = pin 42 = Odd = HIGH
- sheet 8: Add OR gates for Card Detect qualification
- sheet 9: Change 74HCT374 to 74HCT373, also change PPCLKR control gate to NOR
- sheet 10: fix way 80C42 connected to keyboard and mouse
- sheet 11: fix floppy connector for 2 drives
- sheet 11: Change PGP0 to PGP3
- sheet 12: Change PGP3 to PGP0
- sheet 12: Tie BAT signal to VCC3 with short
- sheet 13: Change ACIN pullup resistor from VCC3 to VCC5
- sheet 13: Change ACIN series resistor value to 100 ohms
- sheet 13: stronger ACIN pullup, the Elan has internal Pulldown
- sheet 13: Add 10uF/10v caps to power planes

Rev 1.5 - 7-1-94 - SHEET 3: Pulled RTS# down instead of up to select internal video mode.
- SHEET 3: Moved location of R25,series resistor for 32khz xtal.
- SHEET 3: Changed value of R26,parallel resistor on 32khx xtal to 15M to allow faster startup.
- SHEET 3: Changed value of R18, Reset RC resistor, to 390K to allow longer RESET.
- SHEET 3: Changed value of R16, to speed up RESUME# edge, to 100 Ohms.
- SHEET 3: Fixed speaker circuit by installing a .1uF cap and 33 Ohm res in series with spkr.
- SHEET 3: Changed value of PLL caps to .47uF to reduce clock jitter.
- SHEET 4: Changed the DRAM address series resistors to 0 Ohms to compensate for big capacitance.
- SHEET 5: Added a HD151015 translation buffer to convert the SDEN#,SDWRTL,SDWRTH signals to 3V levels.
- SHEET 10: Added KB controller mods to allow functionality in SUSPEND/RESUME states.
- SHEET 11: Gated PGP1 and PGP2 thru an OR gate to the HD conn to fix backdrive issue.
- SHEET 11: Added 1K pullup to VCC3 on PGP1.
- SHEET 12: Added battery to MAX722 to fix 3V powerup issue.
- SHEET 12: Pulled up SHDN# signal on MAX722 to VCC3 instead of VCC5.

Rev 1.6 - 9-5-94 - - This revision of the schematic includes rev C & D reworks
SHEET 2: Changed MEMR# & MEMW# signal labels to EMEMR# & EMEMW#.
SHEET 2: Changed R12 from 1K to 10K.
SHEET 2: Added 10K pullup to IRQ1.
SHEET 3: Modified values & locations of Loop Filter Caps & Resistors.
SHEET 3: Changed RTS# & DTR# pulldown values to 10K.
SHEET 5: Connected DIR pin on U6 & U7 to VCCMEM53 instead of VCCSYS5.
SHEET 6: Changed U13 type from HCT to ACT.
SHEET 7: Added series terminating resistors to video SRAM data lines.
SHEET 8: Added logic (U36 & U37) to gate off MEMR# & MEMW# to the ISA bus during PCMCIA cycles.
SHEET 8: Added resistors to prevent floating PCMCIA signals.
SHEET 8: Pulled PCMCIA resets down instead of up.
SHEET 9: Made corrections to RS232 symbol. Pin 27 is now C2+ & pin 26 is C2-.
SHEET 12: Deleted RESIN# signal from P/S.

Rev 1.7 12-15-94 Added rev B support
-Sheet 2: Pulled up IOCS16#,MCS16#,IRQ14,IOCHRDY to VCC1 instead of VCC3.
Sheet 2: Pin 140 on ELAN is now XIORESET#.
Sheet 2: Seperated VCC core & VCC1 pins on ELAN.
Sheet 2: Added decoupling capacitors to VCC1 plane.
Sheet 2: Deleted R12 pulldown on pin 140 of ELAN.
Sheet 2: Filtered the VCC core and AVCC plane.
Sheet 3: Changed C24 & C25 values to 22pF.
Sheet 3: Added 0 ohm option on BAUDOUT & AFDT# signals for ELAN rev B.
Sheet 3: Added option to support XIORESET# for ELAN rev B.
Sheet 3: Moved reset circuit to power supply block diagram sheet
Sheet 3: Changed R26 from 15M to 10M.
Sheet 4: Added SA12 (MA11 in asymmetrical DRAM mode) to memory interface
to support asymmetrical DRAM devices when using ELAN rev B.
Sheet 6: Added DOSROM Flash support.
Sheet 6: Added DOSROM Address Decode support.
Sheet 7: Changed BAUDOUT label to SBAUDOUT.
Sheet 7: Changed C39-C45 values from 330pF to 100pF.
Sheet 7: Deleted serial I/R circuit.
or to allow Parallel port redefinition option in ELAN rev B.
Sheet 8: Added option to allow gating of ISA MEMR# & MEMW# when using ELAN rev A
Sheet 9: Added option to allow EMEMR# or SLCTIN# as source for PCMCIA PMEMR#.
Sheet 9: Added option to allow EMEMW# or INIT# as source for PCMCIA PMEMW#.
Sheet 10: Removed KB controller suspend erratta fix.
Made a note specifying the type of device we recommend.
Sheet 11: PGPA pulled up to VCC1 instead of VCC3.
Sheet 12: Added 10K pullup to PGP0.
Sheet 13-15: Created Power supply block diagrams showing uPower mode support.

NOTE: See "ALTERNATE PIN FUNCTIONS" section in 386SC300 DATA MANUAL for description of PIN definition differences between Internal Video & Full ISA mode.

Note: pages 13-15 have to be unlinked from schematic before attempting to generate a netlist or BOM. Pages 12-14 are block diagrams.

|LINK
p 1 revision
p 2 |elanchip.sch
p 3 |elanmisc.sch
p 4 |dram.sch
p 5 |buffs.sch
p 6 |biosdos.sch
p 7 |cgavideo.sch
p 8 |pcmnbcon.sch
p 9 |serpar.sch
p 10|keybrd.sch
p 11|flopide.sch
p 12|power.sch
p 13|psblock1.sch
p 14|psblock2.sch
p 15|psblock3.sch

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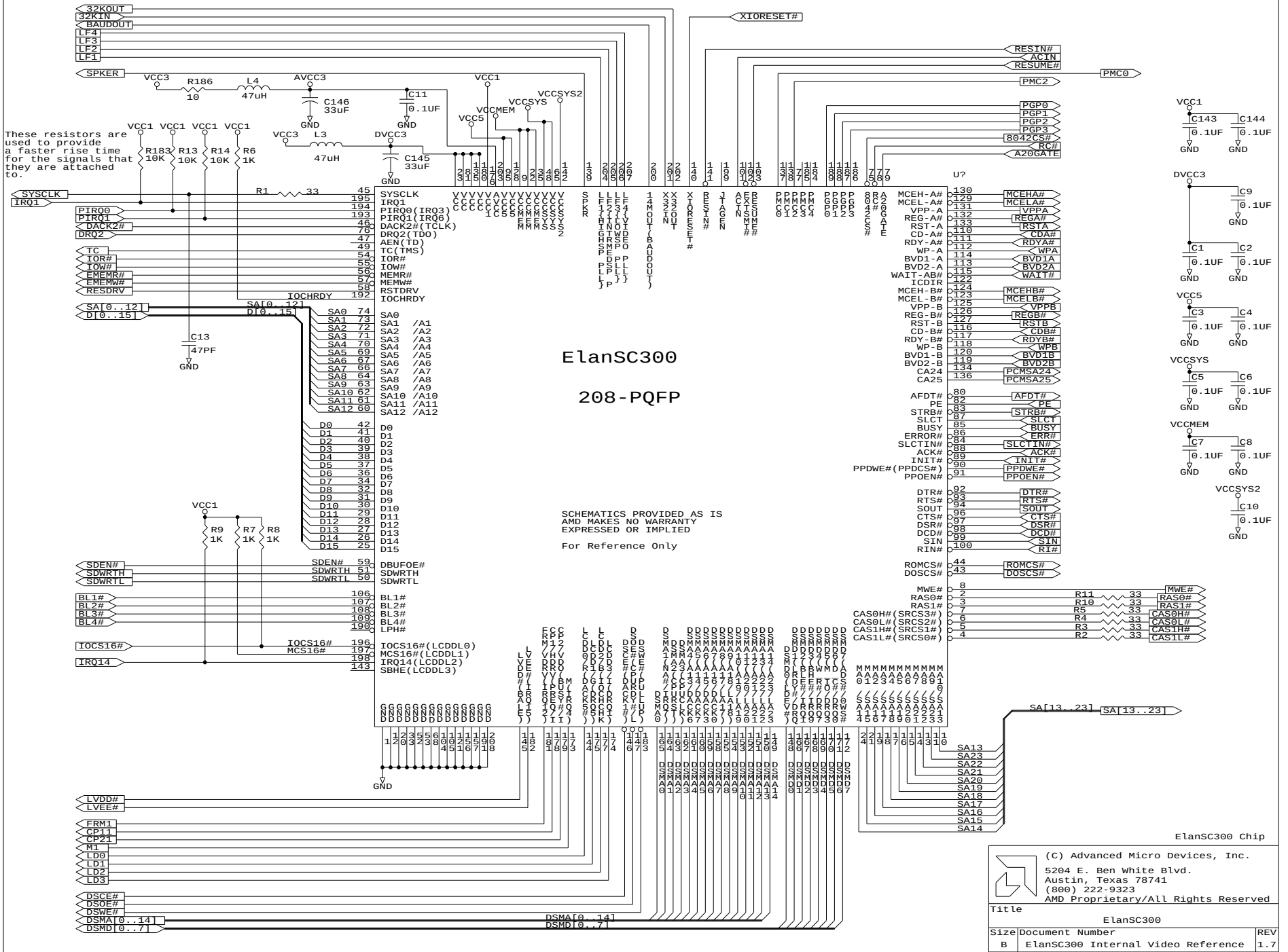
Title: Revision History

Size	Document Number	REV
B	ElanSC300 Internal Video Reference	1.7

Date: January 11, 1996 | Sheet 1 of 15


ElanSC300
208-PQFP
SCHEMATICS PROVIDED AS IS
AMD MAKES NO WARRANTY
EXPRESSED OR IMPLIED
For Reference Only
These resistors are used to provide a faster rise time for the signals that they are attached to.
U?
32KOUT
32KIN
BAUDOUT
LF4
LF3
LF2
LF1
SPKER
XIORESET#
RESIN#
ACIN
RESUME#
PMC2
PMC0
PGP0
PGP1
PGP2
PGP3
8042CS#
RC#
A20GATE
SYSCLK
IRQ1
PIRQ0
PIRQ1
DACK2#
DRQ2
TC
IOR#
IOW#
EMEMR#
EMEMW#
RESDRV
IOCHRDY
SA[0..12]
D[0..15]
SDEN#
SDWRTH
SDWRTL
BL1#
BL2#
BL3#
BL4#
IOCS16#
MCS16#
IRQ14
SBHE
LVDD#
LVEE#
FRM1
CP11
CP21
M1
LD0
LD1
LD2
LD3
DSCE#
DSOE#
DSWE#
DSMA[0..14]
DSMD[0..7]
SA[13..23]
MCEH-A#
MCEL-A#
VPP-A
REG-A#
RST-A
CD-A#
RDY-A#
WP-A
BVD1-A
BVD2-A
WAIT-AB#
ICDIR
MCEH-B#
MCEL-B#
VPP-B
REG-B#
RST-B
CD-B#
RDY-B#
WP-B
BVD1-B
BVD2-B
CA24
CA25
AFDT#
PE
STRB#
SLCT
BUSY
ERROR#
SLCTIN#
ACK#
INIT#
PPDWE#(PPDCS#)
PPOEN#
DTR#
RTS#
SOUT
CTS#
DSR#
DCD#
SIN
RIN#
ROMCS#
DOSCS#
MWE#
RAS0#
RAS1#
CAS0H#(SRCS3#)
CAS0L#(SRCS2#)
CAS1H#(SRCS1#)
CAS1L#(SRCS0#)
VCC1
VCC3
AVCC3
DVCC3
VCCMEM
VCCSYS
VCCSYS2
VCC5
GND
R186 10
L4 47uH
L3 47uH
C146 33uF
C145 33uF
C11 0.1UF
C13 47PF
R1 33
R183 10K
R13 10K
R14 10K
R6 1K
R9 1K
R7 1K
R8 1K
C143 0.1UF
C144 0.1UF
C9 0.1UF
C1 0.1UF
C2 0.1UF
C3 0.1UF
C4 0.1UF
C5 0.1UF
C6 0.1UF
C7 0.1UF
C8 0.1UF
C10 0.1UF
R11 33
R10 33
R5 33
R4 33
R3 33
R2 33
ElanSC300 Chip
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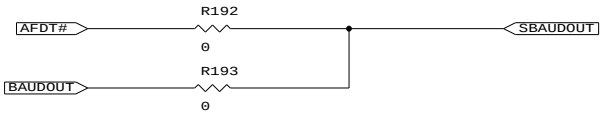
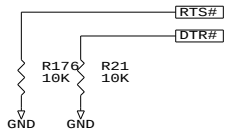
Title
ElanSC300
Size B
Document Number ElanSC300 Internal Video Reference
REV 1.7
Date: January 11, 1996
Sheet 2 of 15

Install when using ELAN rev B with the parallel port signal redefinition option enabled.
Do not install for ELAN rev A
or when using ELAN rev B in a system that requires ELAN parallel port

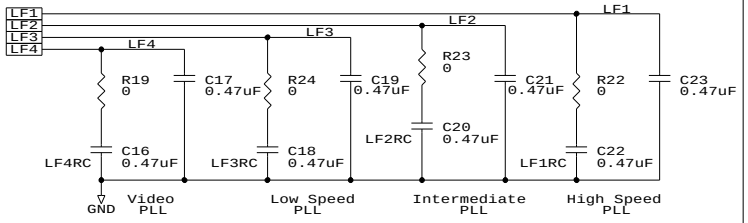


Install for ELAN rev A
or when using ELAN rev B in a system that requires ELAN parallel port
Do not install when using ELAN rev B with the parallel port signal
redefinition option enabled.



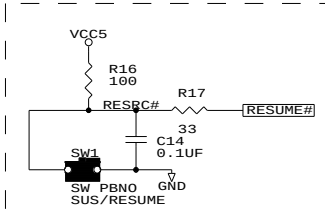
Mode	DTR#	RTS#
Internal CGA	0	0
Local Bus	1	0
Full ISA Bus	X	1

C17,C19,C21 & C23 should not be installed.
Footprints should still be put on board as placeholders
for future revisions of the chip.

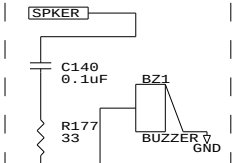


ElanSC300 Chip Loop Filters

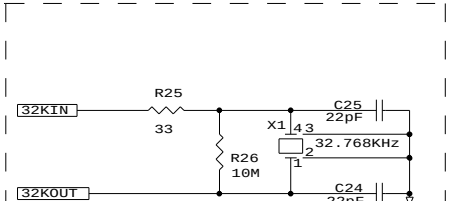
NOTE
Place these componments close to the
ElanSC300 pins to minimize trace length.



Suspend/Resume Switch



System Speaker



32KHz Crystal

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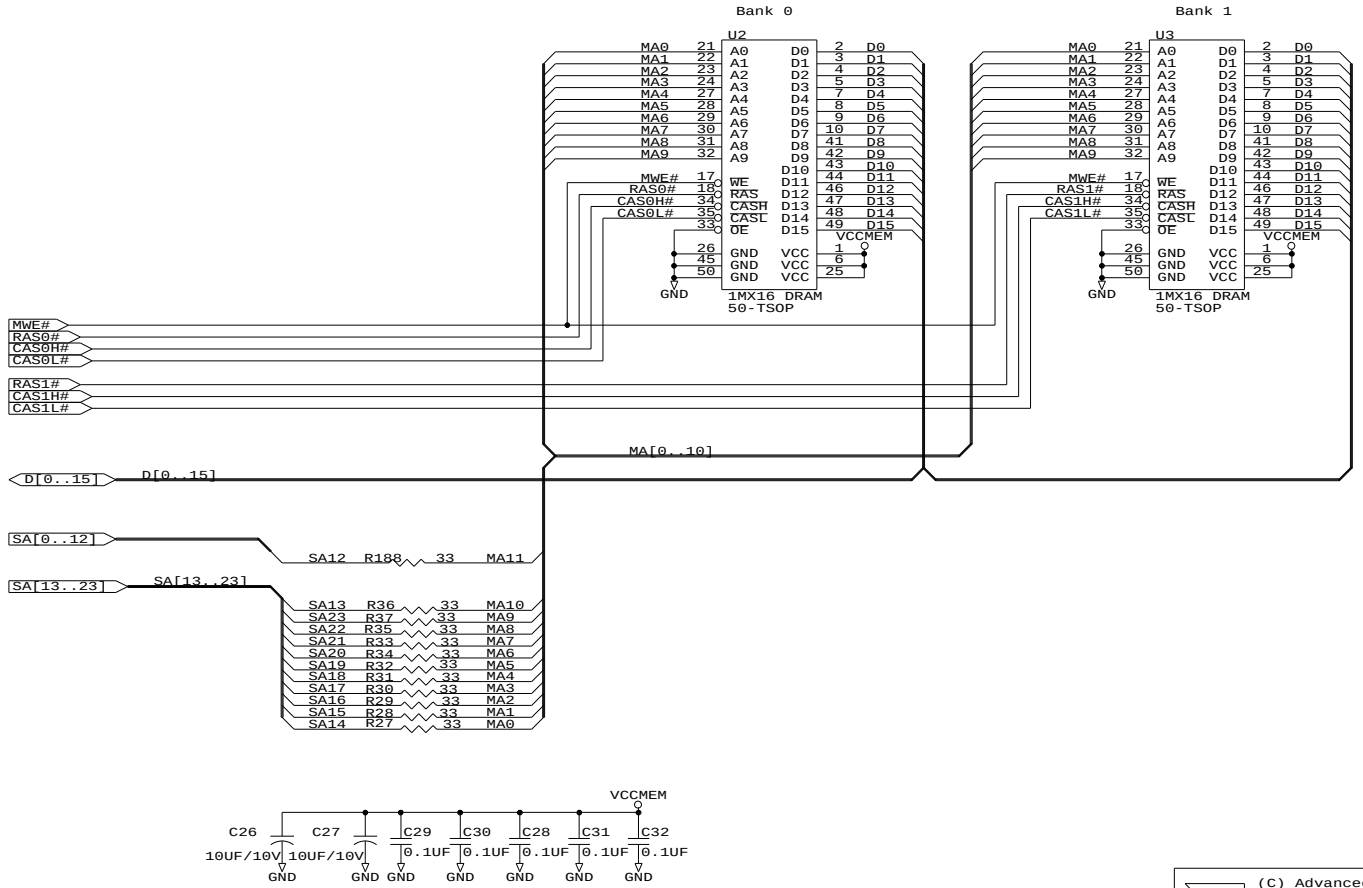
Title
Xtal, Loop Filters, Switches

Size	Document Number	REV
B	ElanSC300 Internal Video Reference	1.7

Date: January 11, 1996 Sheet 3 of 15



Main DRAM System Memory

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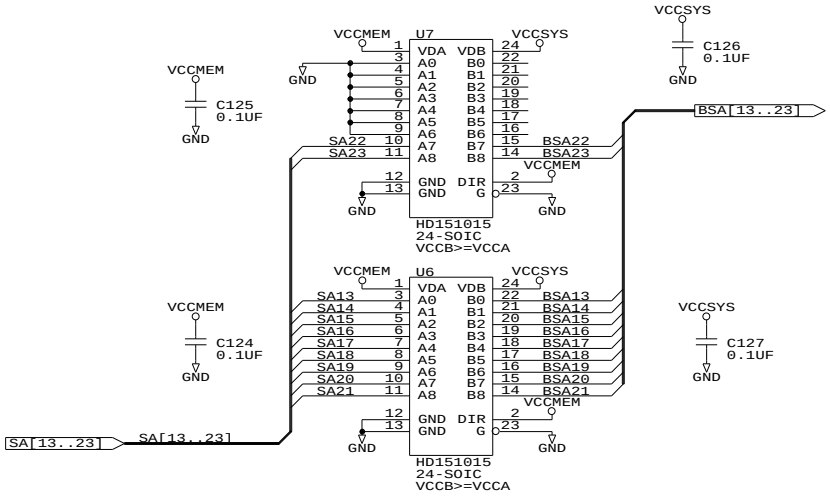
Title		
DRAM Main Memory		
Size	Document Number	REV
B	ElanSC300 Internal Video Reference	1.7
Date: January 11, 1996	Sheet 4 of 15	

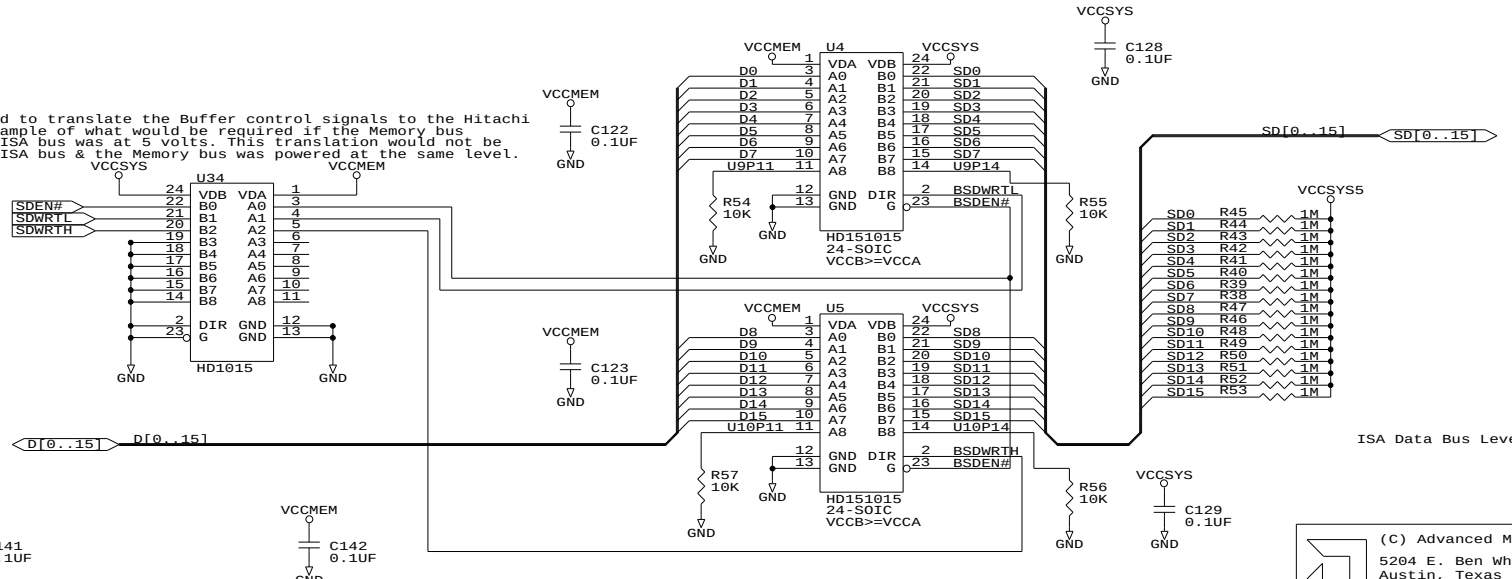
These Hitachi HD151015 devices require that the "B" side always
be greater then or equal to the "A" side.



System Address Bus Buffers

NOTE
Need to translate address signals because memory
may be at 3.3v and ISA bus may be at 5v. This would not
be required if the ISA bus & the Memory bus
were both powered at the same level.

U34 is being used to translate the Buffer control signals to the Hitachi devices as an example of what would be required if the Memory bus was 3.3 volts & ISA bus was at 5 volts. This translation would not be required if the ISA bus & the Memory bus was powered at the same level.



ISA Data Bus Level Translating Buffers

NOTE
Need to translate data signals because memory
bus could be on 3.3v and ISA bus at 5v.
If ISA bus (VCCSYS) & Memory were powered at the same level the translation wouldn't be needed.

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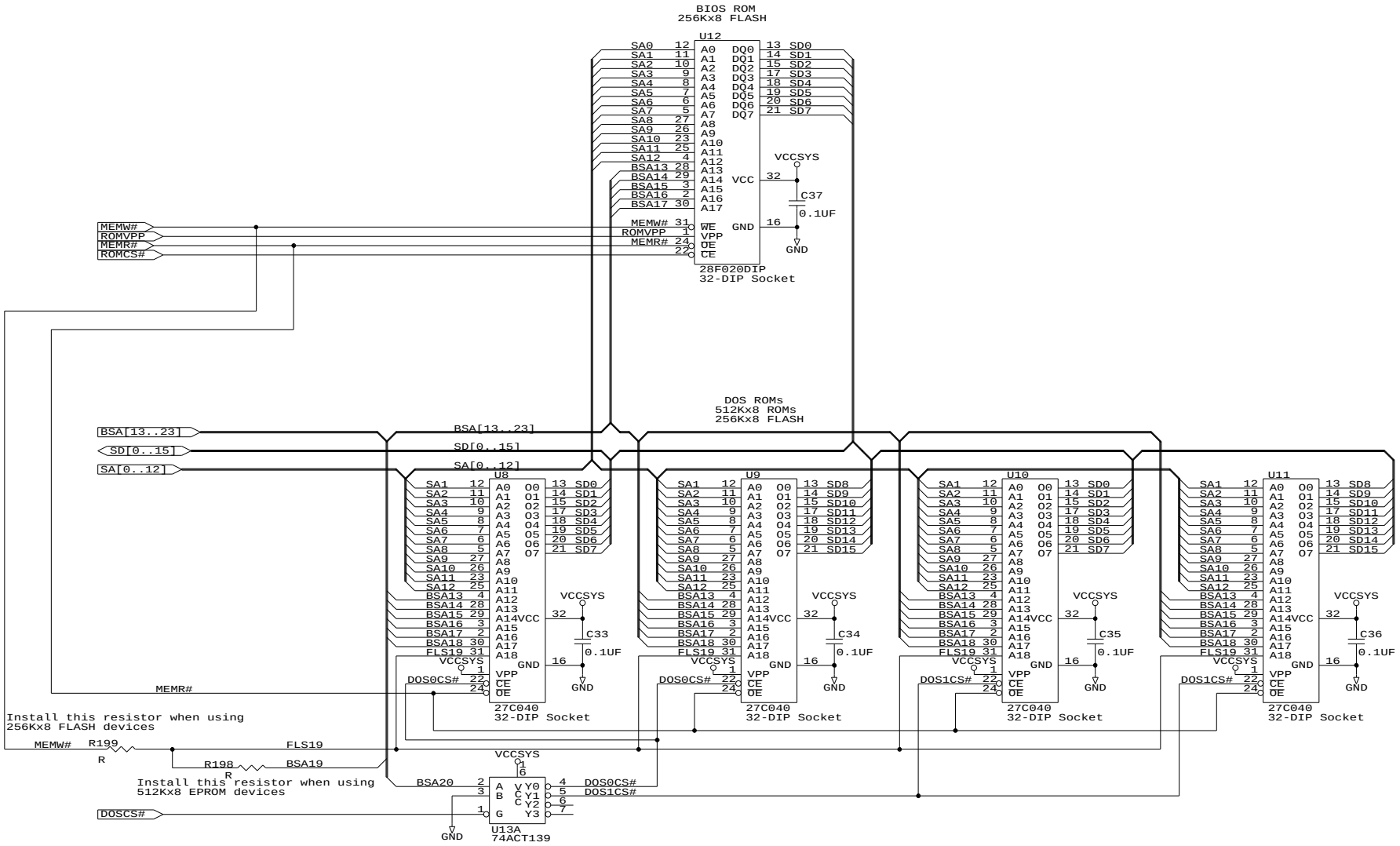
Title		
Address & Data Buffering		
Size	Document Number	REV
B	ElanSC300 Internal Video Reference	1.7
Date: January 11, 1996	Sheet 5 of 15	



BIOS & DOS ROMs

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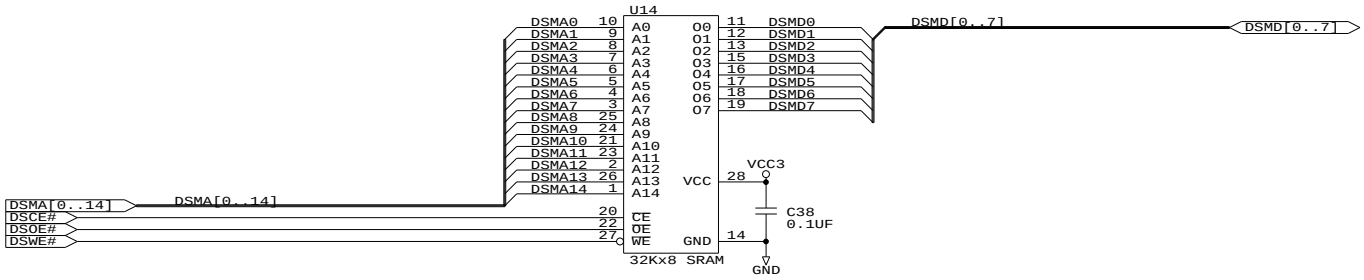
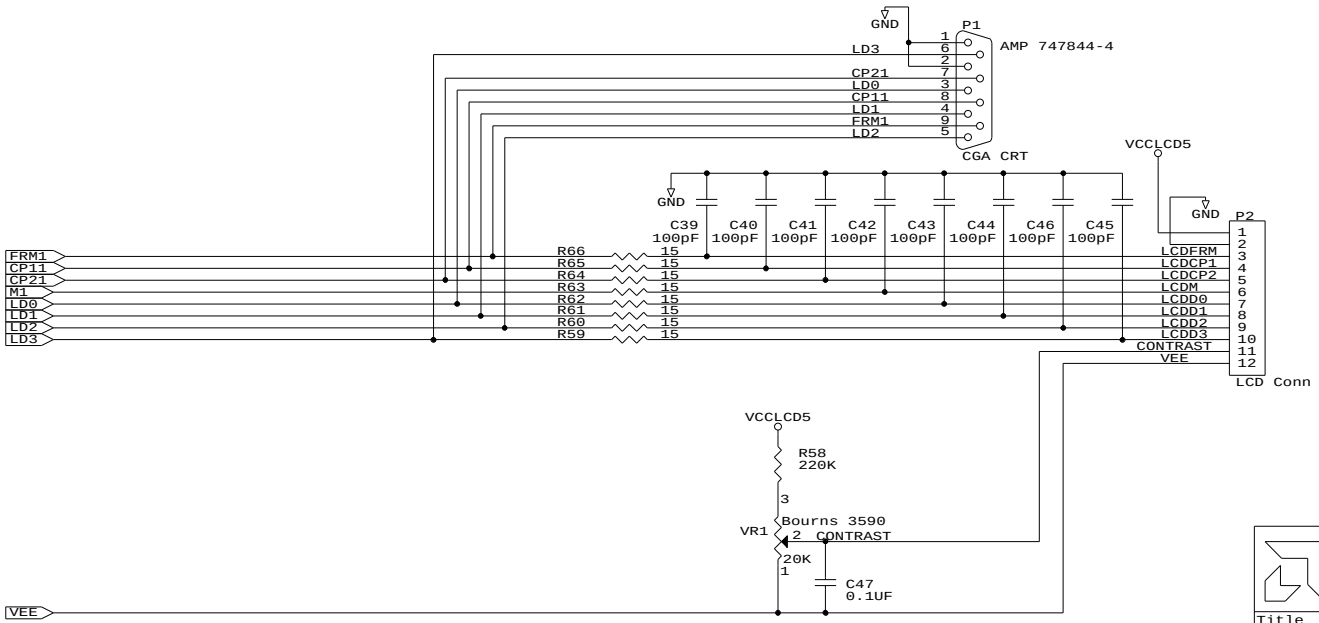
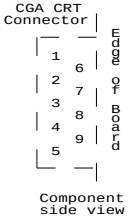
Title		
BIOS & DOS ROMs		
Size	Document Number	REV
B	ElanSC300 Internal Video Reference	1.7
Date: January 11, 1996	Sheet 6 of 15	



Internal Video RAM





Internal Video LCD & CRT Connectors

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Title		
Display SRAM & CRT & LCD Connectors		
Size	Document Number	REV
B	ElanSC300 Internal Video Reference	1.7
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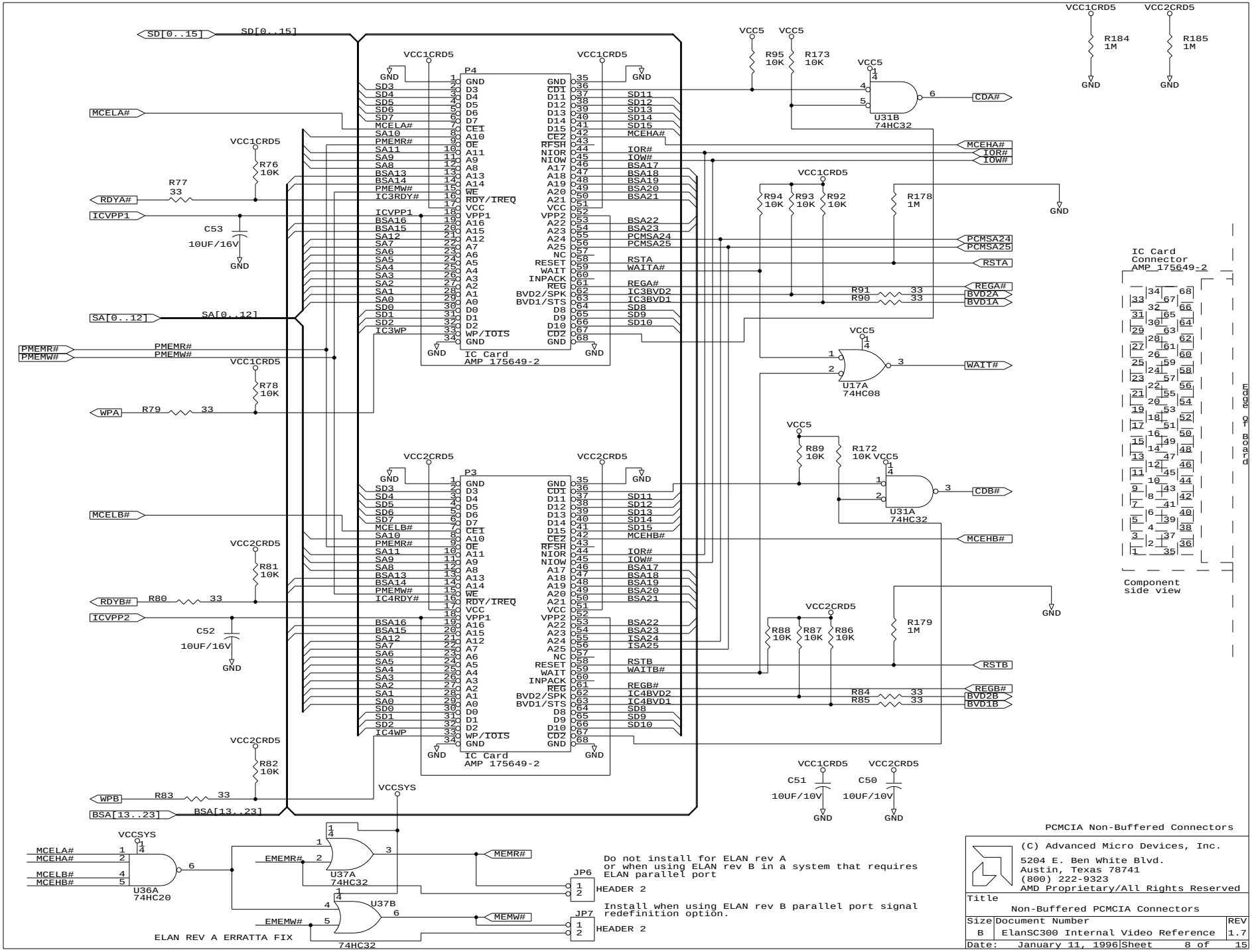
SD[0..15]
SD[0..15]
P4
P3
IC Card
AMP 175649-2
MCELA#
MCELB#
MCEHA#
MCEHB#
SA[0..12]
SA[0..12]
BSA[13..23]
BSA[13..23]
PMEMR#
PMEMW#
RDYA#
RDYB#
WPA
WPB
ICVPP1
ICVPP2
IC3WP
IC4WP
IC3RDY#
IC4RDY#
VCC1CRD5
VCC2CRD5
VCC5
VCCSYS
R76 10K
R77 33
R78 10K
R79 33
R80 33
R81 10K
R82 10K
R83 33
C53 10UF/16V
C52 10UF/16V
C51 10UF/10V
C50 10UF/10V
R95 10K
R173 10K
R94 10K
R93 10K
R92 10K
R178 1M
R91 33
R90 33
R89 10K
R172 10K
R88 10K
R87 10K
R86 10K
R179 1M
R184 1M
R185 1M
U31B 74HC32
U31A 74HC32
U17A 74HC08
U36A 74HC20
U37A 74HC32
U37B 74HC32
CDA#
CDB#
WAIT#
RSTA
RSTB
REGA#
REGB#
BVD2A
BVD1A
BVD2B
BVD1B
PCMSA24
PCMSA25
IOR#
IOW#
MEMR#
MEMW#
EMEMR#
EMEMW#
JP6
JP7
HEADER 2
Do not install for ELAN rev A
or when using ELAN rev B in a system that requires
ELAN parallel port
Install when using ELAN rev B parallel port signal
redefinition option.
ELAN REV A ERRATTA FIX
IC Card
Connector
AMP 175649-2
Component
side view
Edge of Board
PCMCIA Non-Buffered Connectors
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Title
Non-Buffered PCMCIA Connectors
Size B
Document Number ElanSC300 Internal Video Reference
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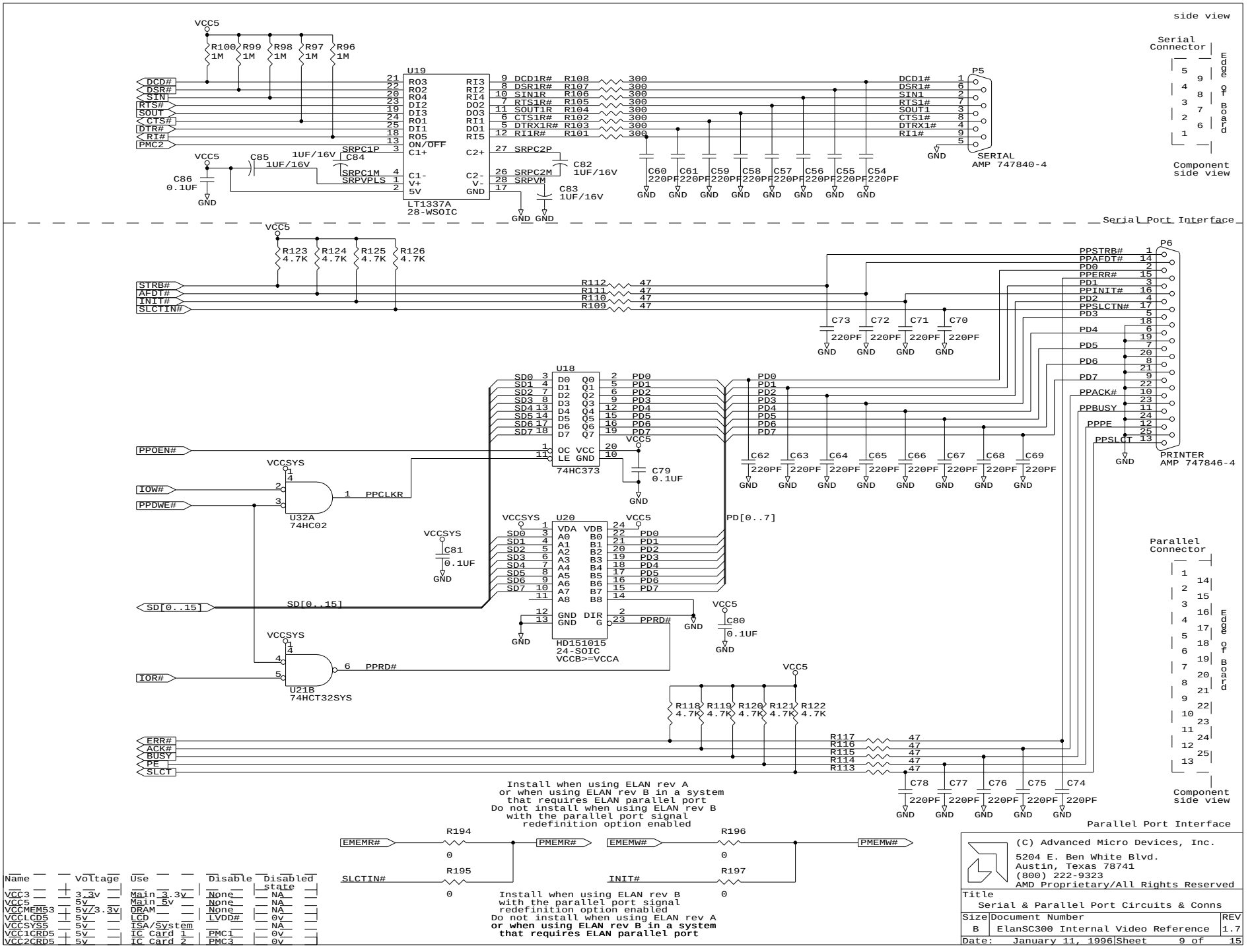

Name	Voltage	Use	Disable	Disabled state
VCC3	3.3v	Main 3.3v	None	NA
VCC5	5v	Main 5v	None	NA
VCCMEM53	5v/3.3v	DRAM	None	NA
VCCLCD5	5v	LCD	LVDD#	0v
VCCSYS5	5v	ISA/System		NA
VCC1CRD5	5v	IC Card 1	PMC1	0v
VCC2CRD5	5v	IC Card 2	PMC3	0v

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Title: Serial & Parallel Port Circuits & Conns

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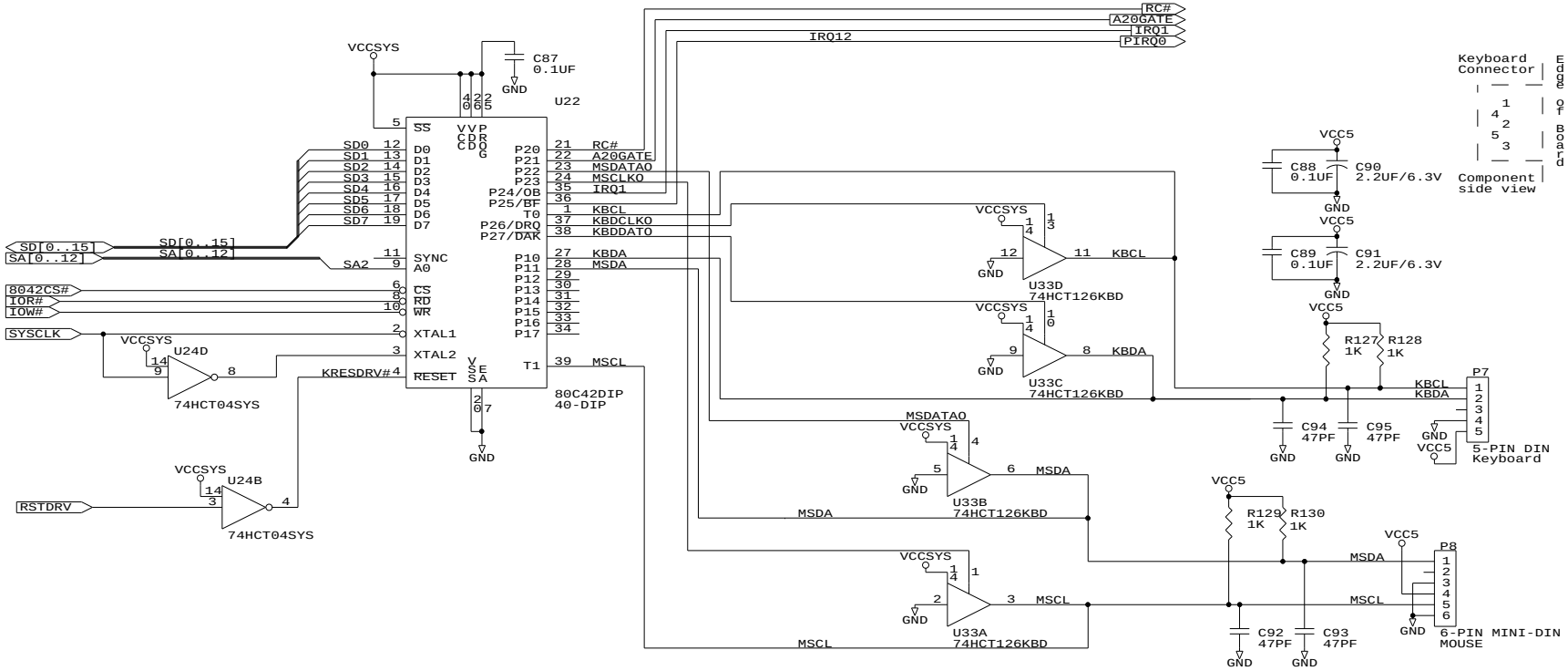

The recommended keyboard controller to use should be a device that supports power mamagement capabilities.
This is neccesary to avoid issues that may arise when suspending the system.

Keyboard & Mouse Processor & Connectors

In this example we are assuming that VCCSYS is 5 volts.
This is the reason for pulling up the outputs of U33 to VCC5.

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Title		
SCP, Keyboard, & Mouse		
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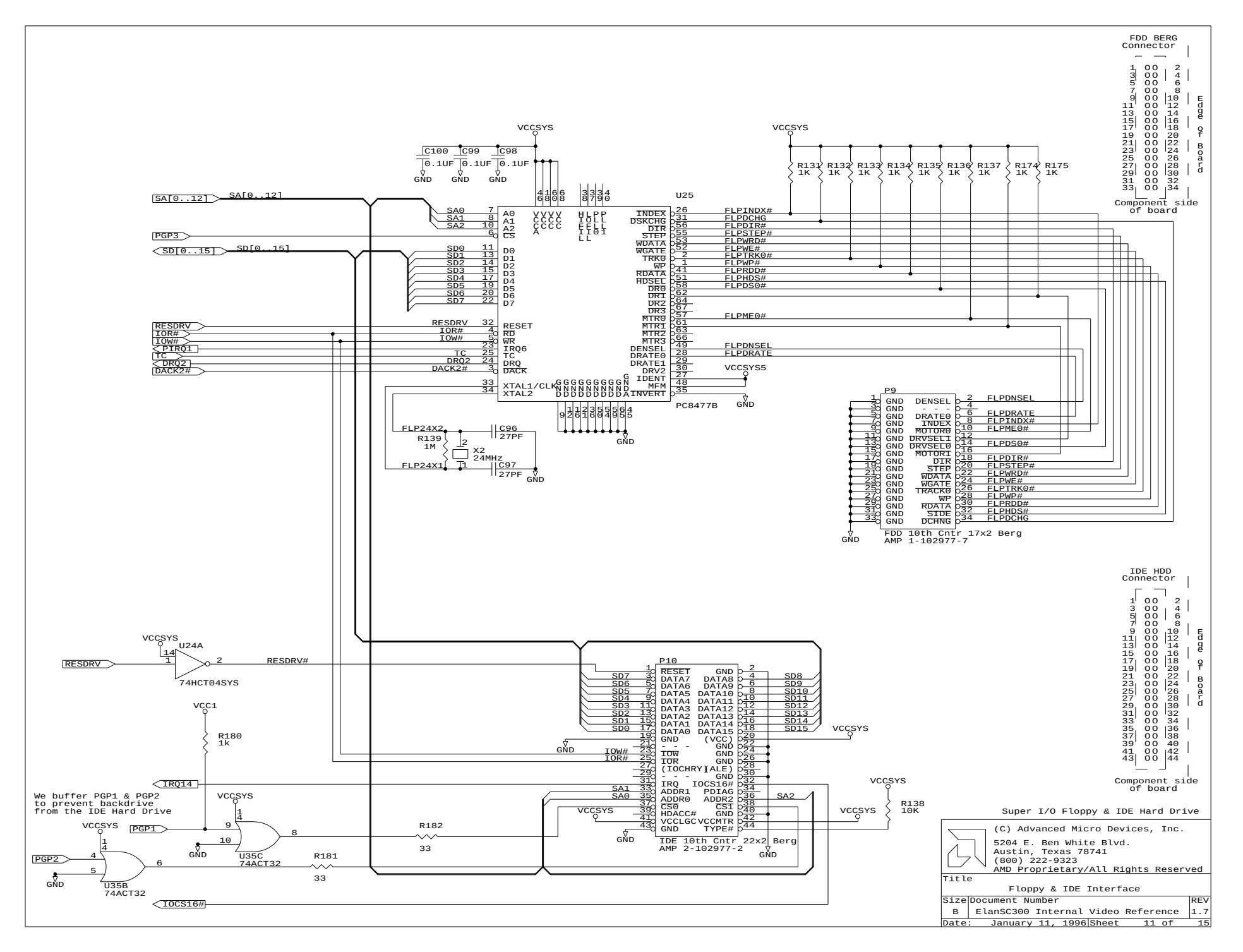
FDD BERG Connector
Edge of Board
Component side of board
IDE HDD Connector
Edge of Board
Component side of board
VCCSYS
C100 0.1UF
C99 0.1UF
C98 0.1UF
GND
R131 1K
R132 1K
R133 1K
R134 1K
R135 1K
R136 1K
R137 1K
R174 1K
R175 1K
U25
PC8477B
SA[0..12]
SD[0..15]
PGP3
RESDRV
IOR#
IOW#
PIRQ1
TC
DRQ2
DACK2#
FLP24X2
FLP24X1
R139 1M
X2 24MHz
C96 27PF
C97 27PF
P9
FDD 10th Cntr 17x2 Berg
AMP 1-102977-7
U24A
74HCT04SYS
RESDRV#
VCC1
R180 1k
IRQ14
We buffer PGP1 & PGP2 to prevent backdrive from the IDE Hard Drive
PGP1
PGP2
U35C 74ACT32
U35B 74ACT32
R182 33
R181 33
IOCS16#
P10
IDE 10th Cntr 22x2 Berg
AMP 2-102977-2
SA2
R138 10K
Super I/O Floppy & IDE Hard Drive
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Floppy & IDE Interface
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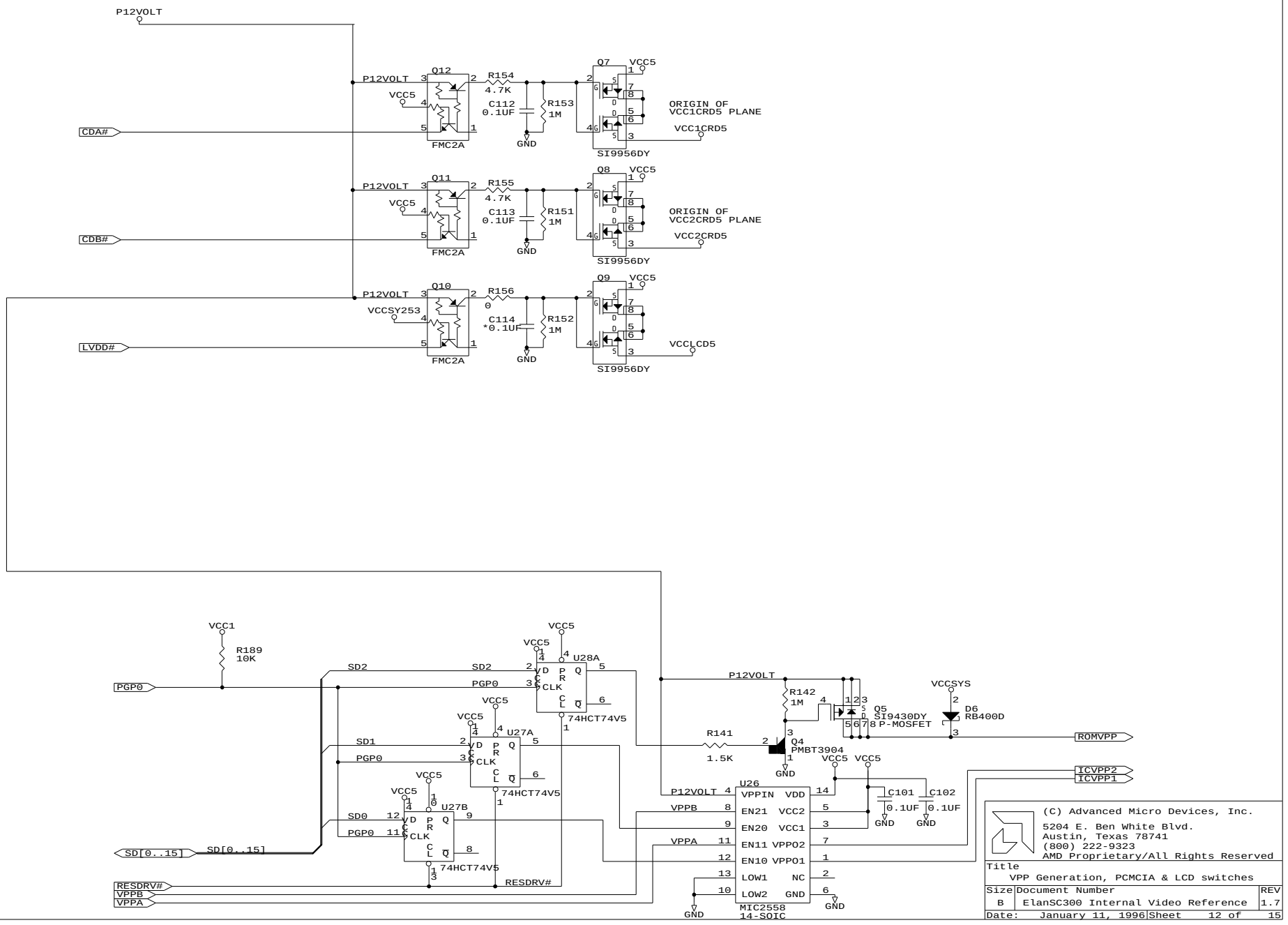

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Title
VPP Generation, PCMCIA & LCD switches

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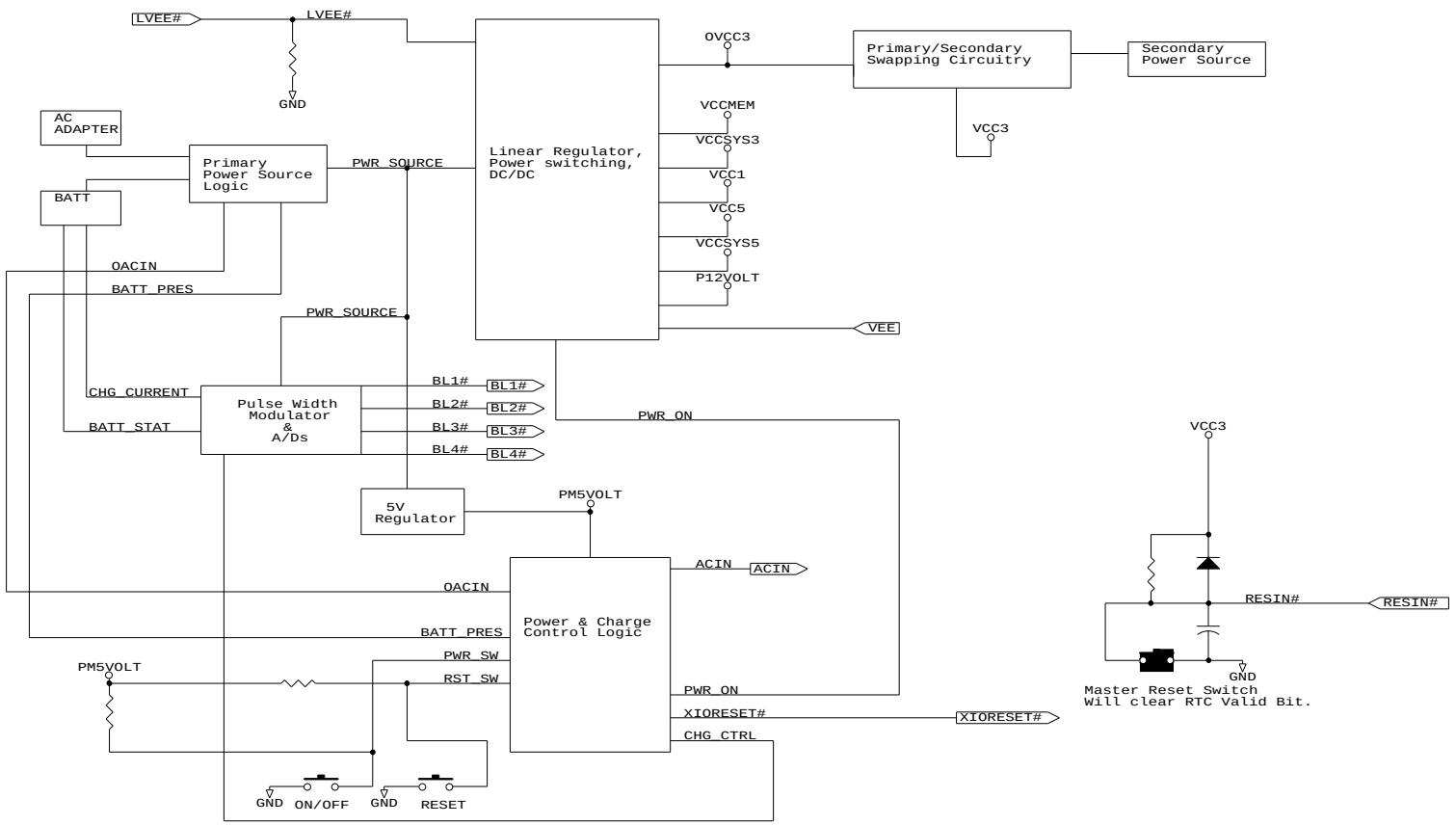

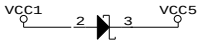

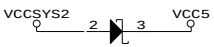

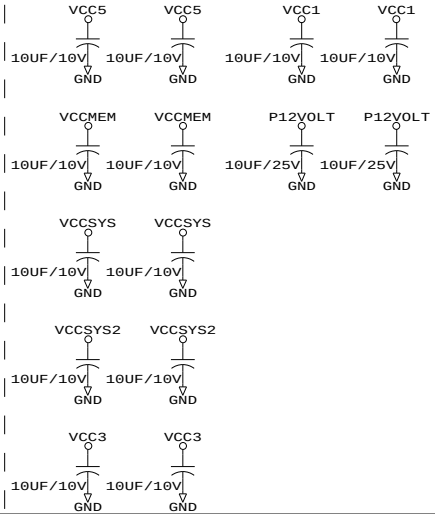

ELAN REV B ONLY
MINIMUM uPower mode configuration

With this implementation the idea is to prevent the RTC RAM from losing its contents while in uPower OFF mode. This is accomplished by allowing the secondary power source to keep the VCC3 plane powered up during uPower OFF mode.

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Title		
ELAN Rev B uPower mode P/S Block Diagram		
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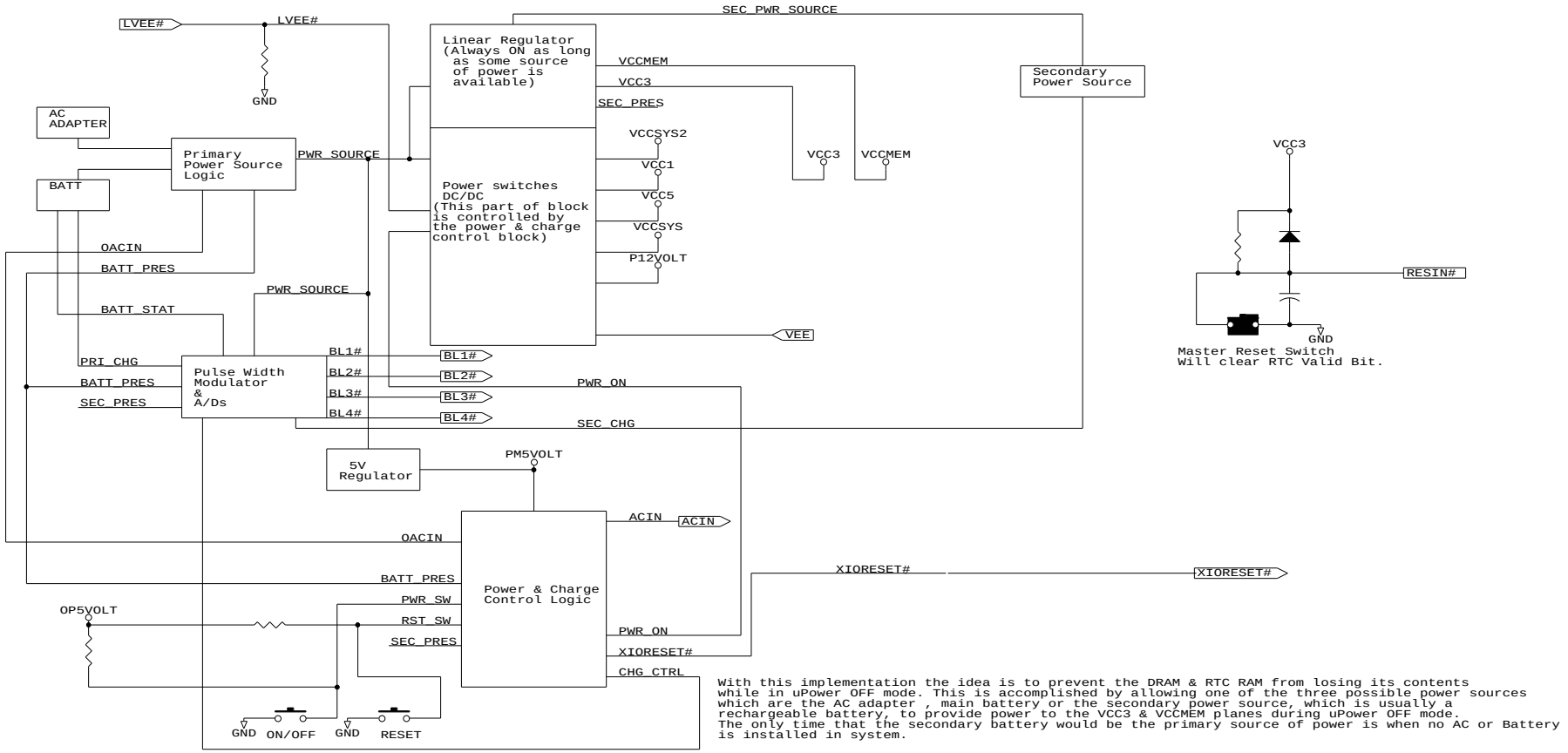
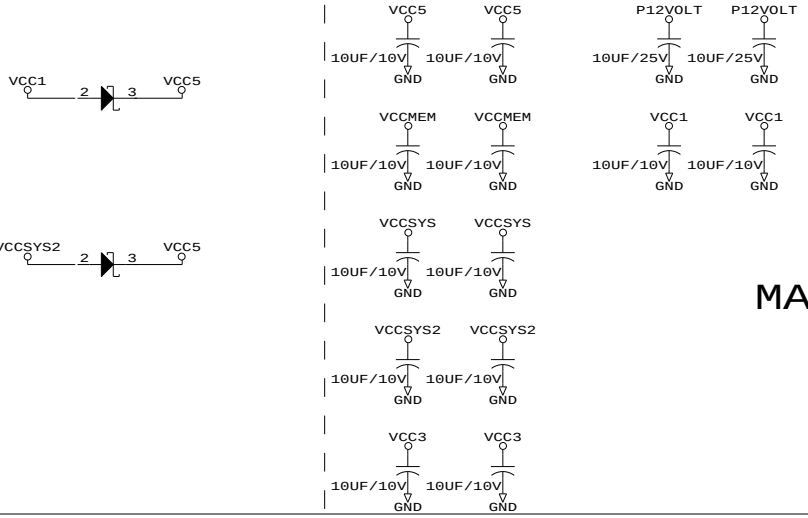


With this implementation the idea is to prevent the DRAM & RTC RAM from losing its contents while in uPower OFF mode. This is accomplished by allowing one of the three possible power sources which are the AC adapter , main battery or the secondary power source, which is usually a rechargeable battery, to provide power to the VCC3 & VCCMEM planes during uPower OFF mode. The only time that the secondary battery would be the primary source of power is when no AC or Battery is installed in system.



ELAN REV B ONLY
MAXIMUM uPower Mode Configuration

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Title		
ELAN Rev B uPower mode P/S Block Diagram		
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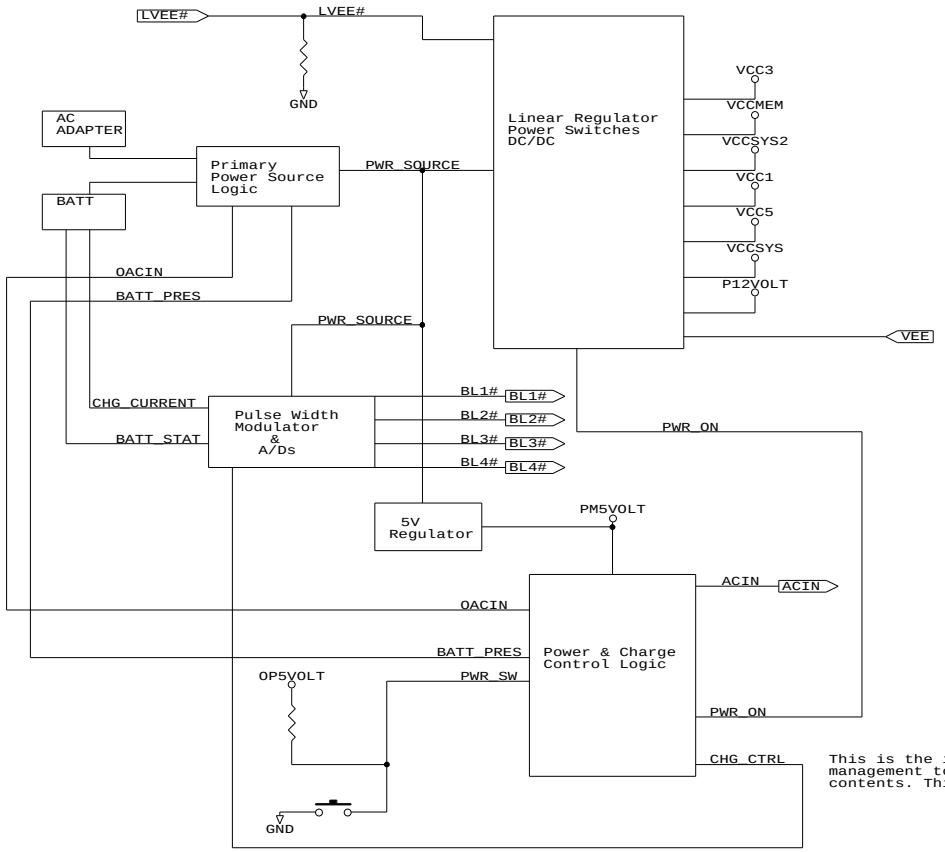
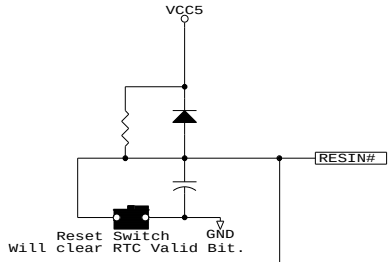
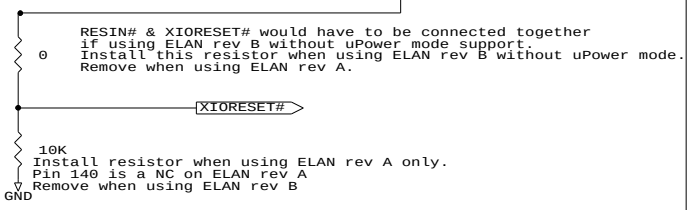
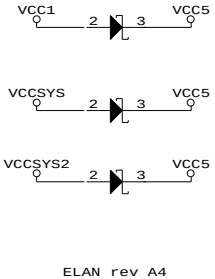
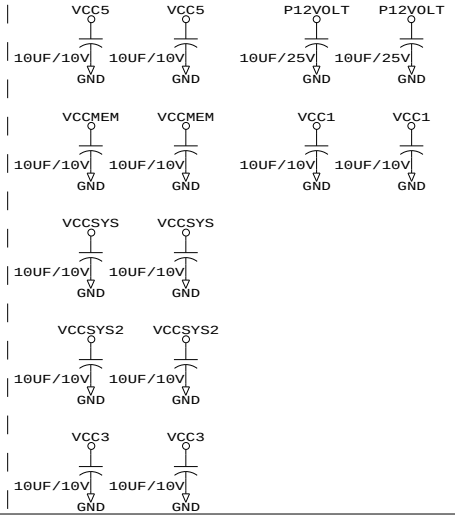






This is the implementation where the system would be normally ON all the time relying on power management to conserve battery power. If the system were to be turned OFF, the RTC RAM would lose its contents. This would also be the implementation if using an ELAN rev B without uPower mode support.





ELAN rev A P/S Block Diagram

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