Élan[™]SC400 Microcontroller Register Set

Reference Manual

Rev. A, December 1996



© 1996 Advanced Micro Devices, Inc.

Advanced Micro Devices reserves the right to make changes in its products without notice in order to improve design or performance characteristics.

The information in this publication is believed to be accurate at the time of publication, but AMD makes no representations or warranties with respect to accuracy or completeness of the contents of this publication or the information contained herein, and reserves the right to make changes at an time, without any notice. AMD disclaims responsibility for any consequences resulting from the use of the information included in this publication.

This publication neither states nor implies any representations or warranties of any kind, including but not limited to, any implied warranty of merchantability or fitness for a particular purpose. AMD products are not authorized for use as critical components in life support devices or systems without AMD's written approval. AMD assumes no liability whatsoever for claims associated with the sale or use (including the use of engineering samples) of AMD product except as provided in AMD's Terms and Conditions of Sale for such product.

Trademarks

AMD, the AMD logo and combinations thereof are trademarks of Advanced Micro Devices, Inc.

Am386 and Am486 are registered trademarks, and Am186, Am188, E86, K86, Élan, Systems in Silicon, and AMD Facts-On-Demand are trademarks of Advanced Micro Devices, Inc. Microsoft and Windows are registered trademarks of Microsoft Corp. Product names used in this publication are for identification purposes and may be trademarks of their respective companies.

FusionE86 is a service mark of Advanced Micro Devices, Inc.

TABLE OF CONTENTS

PREFACE	INTRODUCTION	viii
		XIII viii
		XIII viii
		 viii
	Related Documents	
	Documentation Conventions	XIV XV
CHAPTER 1	OVERVIEW	
	Configuration Registers	1-1
	Direct-Mapped Configuration Registers	1-1
	Internal I/O Port Address Map Summary	1-2
	Indexed Configuration Registers.	1-2
CHAPTER 2	PC/AT-COMPATIBLE DIRECT-MAPPED REGISTERS	
•••••		2-1
	PC/AT-Compatible Direct-Mapped Register Map	2-1
	Register Descriptions	2-5
	Slave DMA Channel 0 Memory Address Register	2-6
	Slave DMA Channel 0 Transfer Count Register	2-7
	Slave DMA Channel 1 Memory Address Register	2-8
	Slave DMA Channel 1 Transfer Count Register	2-9
	Slave DMA Channel 2 Memory Address Register	2-10
	Slave DMA Channel 2 Transfer Count Register	2-11
	Slave DMA Channel 3 Memory Address Register	2-12
	Slave DMA Channel 3 Transfer Count Register	2-13
	Slave DMA Status Register for Channels 0–3	2-14
	Slave DMA Control Register for Channels 0–3	2-15
	Slave Software DRQ(n) Request Register	2-17
	Slave DMA Mask Register Channels 0–3	2-18
	Slave DMA Mode Register Channels 0–3	2-19
	Slave DMA Clear Byte Pointer Register	2-20
	Slave DMA Controller Reset Register	2-21
	Slave DMA Controller Temporary Register	2-22
	Slave DMA Reset Mask Register	2-23
	Slave DMA General Mask Register	2-24
	Master 8259 Interrupt Request Register	2-25
	Master 8259 In-Service Register	2-26
	Master 8259 Initialization Control Word 1 Register	2-27
	Master 8259 Operation Control Word 2 Register	2-28
	Master 8259 Operation Control Word 3 Register	2-29
	Master 8259 Initialization Control Word 2 Register	2-30
	Master 8259 Initialization Control Word 3 Register	2-31
	Master 8259 Initialization Control Word 4 Register	2-32
	Master 8259 Interrupt Mask Register	2-33
	ElanSC400 Microcontroller Chip Setup and Control	
	(CSC) Index Register	2-34
	ElanSC400 Microcontroller Chip Setup and Control	
	(CSC) Data Port	2-35

Programmable Interval Timer #1 Channel 0 Count Register (System Timer/Timer Tick) 2-36
Programmable Interval Timer #1 Channel 1 Count
Register (Refresh Timer)2-37
Programmable Interval Timer #1 Channel 2 Count
Register (Speaker Timer)2-38
Programmable Interval Timer #1 Status Register2-39
Counter Mode Status Bits 3–12-40
Programmable Interval Timer #1 Mode Control Register2-41
Programmable Interval Timer #1 Counter Latch Command Register 2-43
Programmable Interval Timer #1 Read-back Command Register2-44
Keyboard/Mouse Interface Output Buffer2-45
PC/AT Keyboard Interface Data Register
PC/XT Keyboard Data Register2-4/
System Control Port B/NMI Status Register
PC/AT Keyboard/Mouse Interface Status Register
Reyboard/Mouse Interface Command Register
RTC/CMOS RAM Index Register
Concrel Degister
DMA Chappel 2 Dage Degister 255
DMA Channel 2 Page Register 2-56
DMA Channel 1 Page Register 2-57
General Register 2-58
General Register 2-50
General Register 2-60
DMA Channel 0 Page Register 2-61
General Register
DMA Channel 6 Page Register
DMA Channel 7 Page Register
DMA Channel 5 Page Register
General Register
General Register
General Register
General Register
System Control Port A Register (PS/2 Compatibility Port)2-70
Slave 8259 Interrupt Request Register
Slave 8259 In-Service Register
Slave 8259 Initialization Control Word 1 Register
Slave 8259 Operation Control Word 2 Register2-75
Slave 8259 Operation Control Word 3 Register
Slave 8259 Initialization Control Word 2 Register
Slave 8259 Initialization Control Word 3 Register
Slave 8259 Initialization Control Word 4 Register2-79
Slave 8259 Interrupt Mask Register (also known as
Operation Control Word 1)
Master DMA Channel 4 Memory Address Register
Master DMA Channel & Manary Address Pagister
Master DMA Channel 5 Transfer Count Register
Master DMA Channel 6 Memory Address Register 2-85
Master DMA Channel 6 Transfer Count Register
Master DMA Channel 7 Memory Address Register 2-87
Master DMA Channel 7 Transfer Count Register 2-88
Master DMA Status Register for Channels 4–7 2-89
Master DMA Control Register for Channels 4–7
Master Software DRQ(n) Request Register

Master DMA Mask Register Channels 4–7	2-93
Master DMA Mode Register Channels 4–7	2-94
Master DMA Clear Byte Pointer Register	2-95
Master DMA Controller Reset Register	2-96
Master DMA Controller Temporary Register	2-97
Master DMA Reset Mask Register	
Master DMA General Mask Register	
Alternate Gate A20 Control Port	2-100
Alternate CPU Reset Control Port	2-101
Parallel Port 2 Data Register (DC/AT Compatible Mode)	2-102
Parallel Port 2 Status Register (PC/AT Compatible Mode)	2 104
Parallel Port 2 Status Register (EDP Mode)	2 104
Parallel Port 2 Control Register	2-106
Parallel Port 2 EPP Address Register	2-107
Parallel Port 2 EPP 32-bit Data Register	2-108
COM2 Transmit Holding Register	2-109
COM2 Receive Buffer Register	2-110
COM2 Baud Clock Divisor Latch LSB.	2-111
COM2 Baud Clock Divisor Latch MSB	2-112
COM2 Interrupt Enable Register	2-113
COM2 Interrupt ID Register	2-114
COM2 FIFO Control Register	2-116
COM2 Line Control Register	2-117
COM2 Modem Control Register	2-118
COM2 Line Status Register	2-119
COM2 Modem Status Register	2-121
COM2 Scratch Pad Register	2-122
Parallel Port 1 Data Register	2-123
Parallel Port 1 Status Register (PC/AT Compatible Mode)	2-124
Parallel Port 1 Status Register (Bidirectional Mode)	2-125
Parallel Port 1 Status Register (EPP Mode)	2-126
Parallel Port 1 Control Register	2-127
Parallel Port 1 EPP Address Register	2-128
Parallel Port 1 EPP 32-bit Data Register	2-129
MDA/HGA Index Register	2-130
MDA/HGA Data Register	2-131
MDA/HGA Mode Control Register	2-132
MDA/INGA Status Register	2 124
	2-135
CGA Data Port	2-136
CGA Mode Control Register	2-137
CGA Color Select Register 03D	
CGA Status Register	
Primary 82365-Compatible PC Card Controller Index Register	2-140
Primary 82365-Compatible PC Card Controller Data Port	2-141
COM1 Transmit Holding Register	2-142
COM1 Receive Buffer Register	2-143
COM1 Baud Clock Divisor Latch LSB.	2-144
COM1 Baud Clock Divisor Latch MSB	2-145
COM1 Interrupt Enable Register	2-146
COM1 Interrupt ID Register	2-147
COM1 FIFO Control Register	2-148
COM1 Line Control Register	2-149
COM1 Modem Control Register	
	2-150
COM1 Line Status Register	2-150 2-151

	COM1 Scratch Pad Register	2-154
CHAPTER 3	CHIP SETUP AND CONTROL (CSC) INDEXED REGISTERS	
	Overview	3-1
	Chip Setup and Control (CSC) Index Register Map	3-1
	Register Descriptions	3-7
	ElanSC400 Microcontroller Chip Setup and Control	
	(CSC) Index Register	3-8
	ElanSC400 Microcontroller Chip Setup and Control	
	(CSC) Data Port	
	DRAM Bank 1 Configuration	
	DRAM Bank 2 Configuration	
	DRAM Control Register	
	DRAW Reflesh Control Register	2 17
	Drive Strength Control Pegister R	2 10
	Non Cashaabla Window 0 Address Pagister	2 10
	Non-Cacheable Window 0 Address Register	3-20
	Non-Cacheable Window 1 Address Register	3-21
	Non-Cacheable Window 1 Address/Attributes Register	3-22
	Cache and VI Miscellaneous Register	3-23
	Pin Stran Status Register	3-25
	Linear ROMCS0/Shadow Register	
	Linear ROMCS0 Attributes Register	3-28
	ROMCS0 Configuration Register A	
	ROMCS0 Configuration Register B	
	ROMCS1 Configuration Register A	
	ROMCS1 Configuration Register B	
	ROMCS2 Configuration Register A	3-35
	ROMCS2 Configuration Register B	3-37
	MMS Window C–F Attributes Register	3-38
	MMS Window C–F Device Select Register	3-39
	MMS Window A Destination Register	3-40
	MMS Window A Destination/Attributes Register	3-41
	MMS Window B Destination Register	3-42
	MMS Window B Destination/Attributes Register	3-43
	Pin Mux Register A	3-44
	Pin Mux Register B	3-45
	Pin Mux Register C	3-46
	GPIO Termination Control Register A.	3-47
	GPIO Termination Control Register B	3-48
	GPIO Termination Control Register C	3-49
	GPIO Termination Control Register D	3-50
	PMU Force Mode Register	
	PMU Present and Last Mode Register	
	Hyper/High-Speed Mode Timers	
	Low-Speed/Standby Mode Timers Register	
	Suspend/Temporary Low-Speed Mode Timers Register	
	Wake-Up Pause/High-Speed Clock Timers Register	
	SUS_KES PIN CONTIGURATION REGISTER	
	wake-up Source Enable Register A.	
	wake-up Source Enable Register B.	
	Wake Up Source Enable Register C	
	Wake Up Source Enable Register D	
	Wake Up Source Status Register P	
	wake-op ource status register D	

Wake-Up Source Status Register C	3-65
Wake-Up Source Status Register D	3-66
GPIO as a Wake-Up or Activity Source Status Register A	3-67
GPIO as a Wake-I In or Activity Source Status Register B	3-68
CP CS Activity Enable Projector	3-60
	2 70
GP_CS Activity Status Register	3-70
	3-71
Activity Source Enable Register B	3-72
Activity Source Enable Register C	3-73
Activity Source Enable Register D	3-74
Activity Source Status Register A	3-75
Activity Source Status Register B	3-76
Activity Source Status Register C	3-77
Activity Source Status Register D	3-78
Activity Closeffication Register A	2 70
	3-79
	3-80
Activity Classification Register C	3-81
Activity Classification Register D	3-82
Battery/AC Pin Configuration Register A	3-83
Battery/AC Pin Configuration Register B	3-85
Battery/AC Pin State Register	3-86
CPU Clock Speed Register	3-87
CPU Clock Auto Slowdown Register	3-88
Clock Control Register	2 00
	3-90
	3-91
Factory Debug Register A	3-92
Factory Debug Register B	3-93
Miscellaneous SMI/NMI Enable Register	3-94
PC Card and Keyboard SMI/NMI Enable Register	3-95
Mode Timer SMI/NMI Enable Register	3-96
Battery Low and ACIN SMI/NMI Enable Register	3-97
Miscellaneous SMI/NMI Status Register	3-99
PC Card and Keyboard SMI/NMI Status Persister	2_100
Mode Timer SMI/NMI Status Degister	> 100
	5-101
Battery Low and ACIN SMI/NMI Status Register	3-102
SMI/NMI Select Register	3-104
I/O Access SMI Enable Register A	3-105
I/O Access SMI Enable Register B	3-106
I/O Access SMI Status Register A	3-107
I/O Access SMI Status Register B	3-108
XMI Control Register	3-109
GPIO CS Function Select Register A	3-110
GPIO CS Function Select Register B	2-111
CDIO_CS Function Select Register C	2 1 1 2
OPIO_CS Function Select Register C	
GPIO_CS Function Select Register D	3-113
GPIO Function Select Register E	3-114
GPIO Function Select Register F	3-115
GPIO Read-Back/Write Register A	3-116
GPIO Read-Back/Write Register B	3-117
GPIO Read-Back/Write Register C	3-118
GPIO Read-Back/Write Register D	3-119
GPIO_PMUA Mode Change Register	3-120
GPIO PMUB Mode Change Register	3-122
CPIO PMUC Mode Change Pogister	2-101
CDIO_INUOU Mode Change Register	> 100
	J-1∠0
	5-128
GPIO_PMU to GPIO_CS Map Register B	3-129
GPIO_XMI to GPIO_CS Map Register	3-130

Otan dand Daarda ta ODIO, OO Man Daniatan	0 4 0 4
Standard Decode to GPIO_CS Map Register	. 3-131
GP_CS to GPIO_CS Map Register A	. 3-132
GP_CS to GPIO_CS Map Register B	. 3-133
GP_CSA I/O Address Decode Register	. 3-134
GP_CSA I/O Address Decode and Mask Register	. 3-135
GP_CSB I/O Address Decode Register	. 3-136
GP_CSB I/O Address Decode and Mask Register	. 3-137
GP_CSA/B I/O Command Qualification Register	. 3-138
GP_CSC Memory Address Decode Register	. 3-140
GP_CSC Memory Address Decode and Mask Register	. 3-141
GP_CSD Memory Address Decode Register	. 3-142
GP CSD Memory Address Decode and Mask Register	. 3-143
GP CSC/D Memory Command Qualification Register	. 3-144
Keyboard Configuration Register A	3-146
Keyboard Configuration Register B	3-149
Keyboard Input Buffer Read-Back Register	3-151
Keyboard Output Buffer Write Register	3-152
Mouse Output Buffer Write Degister	3-152
Kouboard Status Degister Write Degister	2 153
Keyboard Status Register Wille Register	0 15F
Keyboard Timer Register	. 3-155
	. 3-150
	. 3-158
	. 3-160
Keyboard Column Termination Control Register	. 3-162
Internal I/O Device Disable/Echo Z-Bus Configuration Register	. 3-164
Parallel/Serial Port Configuration Register	. 3-167
Parallel Port Configuration Register	. 3-168
UART FIFO Control Shadow Register	. 3-169
Interrupt Configuration Register A	. 3-170
Interrupt Configuration Register B	. 3-171
Interrupt Configuration Register C	. 3-172
Interrupt Configuration Register D	. 3-173
Interrupt Configuration Register E	. 3-174
DMA Channel 0–3 Extended Page Register	. 3-175
DMA Channel 5–7 Extended Page Register	. 3-176
DMA Resource Channel Map Register A	. 3-177
DMA Resource Channel Map Register B	. 3-178
Internal Graphics Control Register A	.3-179
Internal Graphics Control Register B	3-180
Write-protected System Memory (DRAM)	
Window/Overlapping ISA Window Enable Register	3-181
Overlanning ISA Window Start Address Register	3-182
Overlapping ISA Window Size Register	3-183
Suspend Din State Register A	3-18/
Suspend Pin State Register R	2 104
Suspend Mode Din State Override Degister	2 100
	2 4 0 0
	. 3-188
	. 3-190
	. 3-192
IrDA Own Address Register	. 3-193
IrDA Frame Length Register A	3-194
IrDA Frame Length Register B	. 3-195
PC Card Extended Features Register	. 3-196
PC Card Mode and DMA Control Register	. 3-198
PC Card Socket A/B Input Pull-Up Control Register.	. 3-200
ElanSC400 Microcontroller Povision ID Pagister	3-201

CHAPTER 4	RTC AND CMOS RAM INDEXED REGISTERS	
		-1
		-1 - 1
	Register Descriptions	-2
	RTC/CMOS RAM Index Register	-3 ⊢⊿
	RTC Current Second Register	·-4
	RTC Alarm Second Register 4	5 1-6
	RTC Current Minute Register	-7
	RTC Alarm Minute Register	-8
	RTC Current Hour Register4	-9
	RTC Alarm Hour Register	10
	RTC Current Day of the Week Register4-	11
	RTC Current Day of the Month Register4-	12
	RTC Current Month Register	13
	RTC Current Year Register4-	14
	General Purpose CMOS RAM (114 bytes)4-	15
	Register A	10
	Register C	10 10
	Register D 4-	19 20
		20
CHAPTER 5		
	Overview)-1 - 4
)-1 - 0
	Register Descriptions	-3
	CGA/MDA Index Register)-4 :_5
	Cursor Start Register 5	5-6
	Cursor End Register	;-7
	Start Address High Register	5-8
	Start Address Low Register	5-9
	Cursor Address High Register	10
	Cursor Address Low Register5-	11
	Light Pen High Register (Read Only)5-	12
	Light Pen Low Register (Read Only)5-	13
	Horizontal Total Register	14
	Horizontal Display End Register	15
	Horizontal Line Pulse Start Register	10
	Non-display Lines Register	17 18
	Vertical Adjust Register 5-	10
	Overflow Register	20
	Vertical Display End Register	21
	Vertical Border End Register	22
	Frame Sync Delay Register	23
	Dual Scan Row Adjust Register 5-2	24
	Dual Scan Offset Address High Register 5-2	25
	Dual Scan Offset Address Low Register. 5-2	26
	Offset Register	27
	Underline Location Register	28
	IVIAXIMUM Scan Line Register	29
	ECD Parter AC Modulation Clock	კე შ₁
	Graphics Controller Gravscale Mode Register	31 32
	Graphics Controller Grayscale Remanning Register	34
	Pixel Clock Control Register	36
	Frame Buffer Base Address	37

	Font Buffer Base Address High Byte	. 5-38
	Frame/Font Buffer Base Address Register Low	5-39
	PMU Control Register 1	. 5-40
	PMU Control Register 2	5-41
	Extended Feature Control Register	. 5-42
CHAPTER 6	PC CARD CONTROLLER INDEXED REGISTERS	
	Overview	6-1
	PC Card Controller Register Map	6-1
	Pagistar Descriptions	61
	Primary 82365-Compatible PC Card Controller Index Register	6-5
	Primary 82365-Compatible PC Card Controller Index Register	6-6
	Identification and Revision Register	6-7
	Interface Status Register	6-8
	Power and RESETDRV/ Control Register	6-9
	Interrunt and General Control Register	6-11
	Card Status Change Register	6-12
	Card Status Change Interrupt Configuration Register	6-13
	Address Window Enable Register	6-15
	PC Card Socket B Memory Window Resources Used for MMS	. 6-15
	I/O Window Control Register	6-16
	I/O Window 0 Start Address I ow Register	6-17
	I/O Window 0 Start Address High Register	6-18
	I/O Window 0 Stop Address I ow Register	6-19
	I/O Window 0 Stop Address High Register	. 6-20
	I/O Window 1 Start Address Low Register	. 6-21
	I/O Window 1 Start Address High Register	. 6-22
	I/O Window 1 Stop Address Low Register	. 6-23
	I/O Window 1 Stop Address High Register	. 6-24
	Memory Window 0 Start Address Low Registe	. 6-25
	Memory Window 0 Start Address High Register	. 6-26
	Memory Window 0 Stop Address Low Register	. 6-27
	Memory Window 0 Stop Address High Register	. 6-28
	Memory Window 0 Address Offset Low Register	. 6-29
	Memory Window 0 Address Offset High Register.	. 6-30
	Memory Window 1 Start Address Low Register	. 6-31
	Memory Window 1 Start Address High Register	. 6-32
	Memory Window 1 Stop Address Low Register	. 6-33
	Memory Window 1 Stop Address High Register	. 6-34
	Memory Window 1 Address Offset Low Register	. 6-35
	Memory Window 2 Stort Address Low Register	6 27
	Memory Window 2 Start Address High Pegister	6-38
	Memory Window 2 Stan Address Low Register	6-30
	Memory Window 2 Stop Address High Register	6-40
	Memory Window 2 Address Offset Low Register	6-41
	Memory Window 2 Address Offset High Register	6-42
	Memory Window 3 Start Address I ow Register	6-43
	Memory Window 3 Start Address High Register.	. 6-44
	Memory Window 3 Stop Address Low Register	. 6-45
	Memory Window 3 Stop Address High Register	. 6-46
	Memory Window 3 Address Offset Low Register	. 6-47
	Memory Window 3 Address Offset High Register	. 6-48
	Memory Window 4 Start Address Low Register	. 6-49
	Memory Window 4 Start Address High Register.	. 6-50
	Memory Window 4 Stop Address Low Register	. 6-51
	Memory Window 4 Stop Address High Register	. 6-52
	Memory Window 4 Address Offset Low Register	. 6-53

Memory Window 4 Address Offset High Register
Command Timing 1 Register6-59
Recovery Timing 1 Register
Setup Timing 2 Register
Command Timing 2 Register
Recovery Timing 2 Register
Setup Timing 3 Register6-64
Command Timing 3 Register6-65
Recovery Timing 3 Register

INDEX

INTRODUCTION

ÉLANSC400 MICROCONTROLLER

The Élan[™]SC400 microcontroller is the latest in a series of E86[™] family microcontrollers using AMD's new Systems-in-Silicon[™] design philosophy, which integrates proven x86 CPU cores with a comprehensive set of on-chip peripherals in an advanced 0.35 micron process.

The ÉlanSC400 microcontroller combines a 32-bit, low-voltage Am486® CPU with a complete set of PC/AT-compatible peripherals, along with the power management features required for battery operation. With its low-voltage Am486 CPU core and ultra-small form factor, the ÉlanSC400 microcontroller is highly optimized for mobile computing applications.

PURPOSE OF THIS MANUAL

This manual includes in reference format the complete set of configuration and control registers required to program the ÉlanSC400 microcontroller.

Intended Audience

This reference manual is intended primarily for programmers who are developing code for the ÉlanSC400 microcontroller. Computer software and hardware architects and system engineers who are designing or are considering designing systems based on the ÉlanSC400 microcontroller may also be interested in the information contained in this document. For more information on using the ÉlanSC400 microcontroller, see the *ÉlanSC400 Microcontroller User's Manual* (order #21030).

Overview of This Manual

This manual is organized into the following chapters.

- Chapter 1 contains an overview of the configuration registers on the ÉlanSC400 microcontroller.
- Chapter 2 includes descriptions for all of the **direct-mapped registers**.
- Chapter 3 includes descriptions for the indexed ÉlanSC400 Chip Setup and Control (CSC) registers
- Chapter 4 includes descriptions for the indexed Real-Time Clock and CMOS RAM registers.
- Chapter 5 includes descriptions for the indexed LCD Graphics Controller registers.
- Chapter 6 includes descriptions for the **indexed PC Card Controller registers**.

Within each chapter, the registers are listed in ascending hexadecimal order.

RELATED DOCUMENTS

AMD Documentation

The following AMD documents provide additional information about the ÉlanSC400 microcontroller.

- The *ÉlanSC400 Microcontroller Data Sheet* (order #21028) includes complete pin lists, pin state tables, timing and thermal characteristics, and package dimensions for the ÉlanSC400 microcontroller.
- The *ÉlanSC400 Microcontroller User's Manual* (order #21030) provides a functional description of the microcontroller for both hardware and software designers.
- The Am486 Microprocessor Software User's Manual (order #18497) includes the Am486 microprocessor instruction set. Appendices provide useful information about programming the base architecture and system level registers, as well as describing segmentation and paging on the Am486 microprocessor. A glossary of terms is also included. Note that this document describes floating-point features not supported on the ÉlanSC400 microcontroller.

Other documents of interest:

- Enhanced Am486 Microprocessor Data Sheet (order #19225)
- Am486DX/DX2 Microprocessor Hardware Reference Manual (order #17965). Note that this document describes floating-point features not supported on the ÉlanSC400 microcontroller.

DOCUMENTATION CONVENTIONS

The following table lists the documentation conventions used throughout this manual.

Documentation Conventions Table

Notation	Meaning		
Register Descriptions			
Default	Power-on reset value or value after master reset asserted		
x in default register value	Non-deterministic or floating; no value is guaranteed		
? in default register value	Determined by sources external to the ÉlanSC400 microcontroller		
Shading in PC Card index register bit description	Deviates from strict 83865SL compliance		
Reference Notation			
CSC index 00h[1]	ÉlanSC400 Chip Setup and Control (CSC) indexed register 00h, bit 1		
Graphics index 00h[1]	Graphics controller indexed register 00h, bit 1		
PC Card index 00h[1]	PC Card controller indexed register 00h, bit 1		
Port 00h[1]	Direct-mapped register 00h, bit 1		
RTC index 00h[1]	RTC and configuration RAM indexed register 00h, bit 1		
Pin Naming			
/	Two functions available on the pin at the same time		
{}	Pin function during hardware reset		
[]	Alternative pin function selected by firmware configuration		
[[]]	Alternative pin function selected by a hardware configuration pin state at power-on reset		
ROMCS2-ROMCS0	All three ROM chip select signals		
ROMCSx	Any of the three ROM chip select signals		
Numbers			
b	Binary number		
d	Decimal number Decimal is the default radix		
h	Hexadecimal number		
x in register address	Any of several legal values; e.g., 3x4h as a graphics index address register can be either 3B4h or 3D4h, depending on the mode selected		

Notation	Meaning		
[X–Y, Z]	The bit field that consists of bits X through Y, and the bit field consisting of the single bit Z. Example: Use CSC index 52h[5–3,1]		
General			
field	Bit field in a register (one or more consecutive and related bits)		
can	It is possible to perform an action if properly configured		
will	A certain action is going to occur		
XMI	SMI or NMI		
Set 29h[1]	Write bit 1 of index 29h to 1. Note: The applicable indexed register space will either be obvious from the surrounding text, or will be stated explicitly. For example, RTC index 0h[1] would be a reference to index 1 in Real-time Clock indexed register space.		
Clear 29h[1]	Write bit 1 of index 29h to 0. Note: The applicable indexed register space will either be obvious from the surrounding text, or will be stated explicitly. For example, RTC index 0h[1] would be a reference to index 1 in Real-time Clock indexed register space.		

CHAPTER

OVERVIEW

This chapter provides an overview of the different types of configuration registers that are documented in this manual.

1.1 CONFIGURATION REGISTERS

Configuration registers are used to read back status or to control various aspects of the ÉlanSC400 microcontroller's on-board cores or peripherals. The internal configuration registers on the ÉlanSC400 microcontroller fall into one of five categories:

- Direct-mapped PC/AT-compatible I/O registers
- ÉlanSC400 Chip Setup and Control (CSC) indexed registers
- Real-Time Clock (RTC) and CMOS RAM indexed registers
- LCD graphics controller indexed registers
- PC Card controller indexed registers

1.1.1 Direct-Mapped Configuration Registers

Direct-mapped PC/AT-compatible I/O registers include those for the typical PC/AT cores, such as the DMA controllers, programmable interval timer, prioritized interrupt controllers, parallel port, and serial port. The registers in this group include the industry-standard list of registers for IBM PC/AT-compatible computers which have been implemented in the ÉlanSC400. A summary listing of these standard I/O port addresses is shown in Table 1-1.

Table 1-1	Internal	I/O Port	Address	Мар	Summary

Internal I/O Device	I/O Address Range			
Slave DMA (DMA1)	0000–000Fh			
Master Programmable Interrupt Controller (PIC)	0020–0021h			
CSC Index, Data	0022h, 0023h			
Programmable Interval Timer (PIT)	0040–0043h			
Keyboard	0060h, 0064h			
System Control Port B/NMI Status	0061h			
RTC Index, Data	0070h, 0071h			
General 8x Registers	0080h, 0084–0086h, 0088h, 008C–008Fh			
DMA Page Registers	0081–0083h, 0087h, 0089–008Bh			
System Control Port A	0092h			
Slave PIC	00A0–00A1h			
Master DMA (DMA0)	00C0–00DEh (even addresses only)			
Alternate A20 Gate Control	00EEh			
Alternate CPU Reset Control	00EFh			
Parallel Port LPT2	0278–027Fh			
Serial Port COM2	02F8–02FFh			
Parallel Port LPT1	0378–037Fh			
MDA Graphics Index, Data	03B4h, 03B5h			
CGA Graphics Index, Data	03D4h, 03D5h			
PC Card Index, Data	03E0h, 03E1h			
Serial Port COM1	03F8–03FFh			

Note: DMA Page register extension bits are found in Chip Setup and Control (CSC) indexed registers D9h and DAh.

1.1.2 Indexed Configuration Registers

Four additional groups of configuration registers are indirectly accessible to the programmer by using pairs of direct-mapped I/O ports. The four additional groups of registers available on the ElanSC400 microcontroller are illustrated in Figure 1-1.

All of the registers accessed through this mechanism are referred to as "indexed." Indexing uses direct-mapped I/O index and data ports to expand the I/O space for reading and writing internal system registers.

- An I/O write to one of the index registers latches the index number of the register to be indirectly accessed.
- A subsequent I/O write to the corresponding data port will write the register indexed by the index register. Similarly, an I/O read from data port will read the register indexed by the index register.
- A read from an index register provides the last index value written to that internal index latch.

An example of using indexing to access the ÉlanSC400 Chip Setup and Control (CSC) registers is shown in Figure 1-2.

Figure 1-1 Indexed Configuration Register Space



Figure 1-2 Using the Index and Data I/O Ports to Access CSC Register Space





1.1.2.1 ÉlanSC400 Chip Setup and Control (CSC) Indexed Registers

ÉlanSC400 Chip Setup and Control (CSC) registers are defined as ÉlanSC400 microcontroller-specific registers which support features beyond standard PC/AT compatibility requirements (i.e., all memory controller and power management registers are CSC indexed registers). These registers are accessed through an indexing scheme to limit the number of direct-mapped I/O ports required.

To access the CSC registers, an I/O write to I/O port 0022h is first performed. The data written is the index of the CSC register. This I/O write is followed by an I/O read or write to port 0023h to access the data from the selected register.

The ÉlanSC400 microcontroller does not implement any locking mechanism for CSC register access. Also, back-to-back access of I/O address 0022h/0023h is not required for access to the CSC indexed registers. For example, the following code fragment:

```
mov al, 90h; force an SMI
out 22h, al
mov al, 1
out 23h, al
:
:
```

has the same result as this code fragment:

mov AX, 0190h; force an SMI. out 22h, AX

1.1.2.2 RTC and CMOS RAM Indexed Registers

Real-Time Clock and CMOS RAM indexed registers are accessed using I/O ports 70h (index) and 71h (data). These registers function as setup, control, and status for the RTC, as well as user CMOS RAM locations.

1.1.2.3 Graphics Controller Indexed Registers

Graphics controller indexed registers are accessed using I/O ports 3D4h (index) and 3D5h (data) for CGA mode and I/O ports 3B4h (index) and 3B5h (data) for MDA mode. These registers function as setup, control, and status for the LCD graphics controller.

1.1.2.4 PC Card Controller Indexed Registers

PC Card controller indexed registers are accessed using I/O ports 3E0h (index) and 3E1h (data). These registers function as setup, control, and status for the PC Card controller.

2 PC/AT-COMPATIBLE DIRECT-MAPPED REGISTERS

2.1 OVERVIEW

This chapter describes the direct-mapped registers on the ÉlanSC400 microcontroller. These registers include those for the typical PC/AT cores, such as the DMA controllers, programmable interval timer, programmable interrupt controllers, parallel port, and serial port. The registers in this group include those PC/AT compatible I/O ports that have been implemented in the ÉlanSC400 microcontroller. They are listed in hexadecimal order in Table 2-1.

The registers in this chapter are all addressed directly; no indexing is required. Other controls that relate to the PC/AT legacy core functions can be found in the Chip Setup and Control (CSC) registers found in Chapter 3.

Table 2-1 PC/AT-Compatible Direct-Mapped Register Map

Register Name	I/O (Port) Address	Page Number
Slave DMA Channel 0 Memory Address Register	0000h	page 2-6
Slave DMA Channel 0 Transfer Count Register	0001h	page 2-7
Slave DMA Channel 1 Memory Address Register	0002h	page 2-8
Slave DMA Channel 1 Transfer Count Register	0003h	page 2-9
Slave DMA Channel 2 Memory Address Register	0004h	page 2-10
Slave DMA Channel 2 Transfer Count Register	0005h	page 2-11
Slave DMA Channel 3 Memory Address Register	0006h	page 2-12
Slave DMA Channel 3 Transfer Count Register	0007h	page 2-13
Slave DMA Status Register for Channels 0–3	0008h	page 2-14
Slave DMA Control Register for Channels 0–3	0008h	page 2-15
Slave Software DRQ(n) Request Register	0009h	page 2-17
Slave DMA Mask Register Channels 0–3	000Ah	page 2-18
Slave DMA Mode Register Channels 0–3	000Bh	page 2-19
Slave DMA Clear Byte Pointer Register	000Ch	page 2-20
Slave DMA Controller Reset Register	000Dh	page 2-21
Slave DMA Controller Temporary Register	000Dh	page 2-22
Slave DMA Reset Mask Register	000Eh	page 2-23
Slave DMA General Mask Register	000Fh	page 2-24
Master 8259 Interrupt Request Register	0020h	page 2-25
Master 8259 In-Service Register	0020h	page 2-26
Master 8259 Initialization Control Word 1 Register	0020h	page 2-27

Register Name	I/O (Port) Address	Page Number	
Master 8259 Operation Control Word 2 Register	0020h	page 2-28	
Master 8259 Operation Control Word 3 Register	0020h	page 2-29	
Master 8259 Initialization Control Word 2 Register	0021h	page 2-30	
Master 8259 Initialization Control Word 3 Register	0021h	page 2-31	
Master 8259 Initialization Control Word 1 Register	0021h	page 2-27	
Master 8259 Interrupt Mask Register (also known as Master 8259 Operation Control Word 1 Register)	0021h	page 2-33	
ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Index Register	0022h	page 2-34	
ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Data Port	0023h	page 2-35	
Programmable Interval Timer #1 Channel 0 Count Register	0040h	page 2-36	
Programmable Interval Timer #1 Channel 1 Count Register	0041h	page 2-37	
Programmable Interval Timer #1 Channel 2 Count Register	0042h	page 2-38	
Programmable Interval Timer #1 Status Byte Format	0040–0042h	page 2-39	
Programmable Interval Timer #1 Mode Control Register (Mode selection)	0043h	page 2-41	
Programmable Interval Timer #1 Mode Control Register (Counter latch)	0043h	page 2-43	
Programmable Interval Timer #1 Mode Control Register (Read-back)	0043h	page 2-44	
Keyboard/Mouse Interface Output Buffer	0060h	page 2-45	
PC/AT Keyboard Interface Data Register	0060h	page 2-46	
XT Keyboard Data Register	0060h	page 2-47	
System Control Port B/ NMI Status Register	0061h	page 2-48	
Keyboard/Mouse Interface Status Register	0064h	page 2-49	
Keyboard/Mouse Interface Command Register	0064h	page 2-51	
RTC/CMOS RAM Index Register	0070h	page 2-52	
RTC/CMOS RAM Data Port	0071h	page 2-53	
General Register	0080h	page 2-54	
DMA Channel 2 Page Register	0081h	page 2-55	
DMA Channel 3 Page Register	0082h	page 2-56	
DMA Channel 1 Page Register	0083h	page 2-57	
General Registers	0084–0086h	page 2-58	
DMA Channel 0 Page Register	0087h	page 2-61	
General Register	0088h	page 2-62	
DMA Channel 6 Page Register	0089h	page 2-63	

Register Name	I/O (Port) Address	Page Number
DMA Channel 7 Page Register	008Ah	page 2-64
DMA Channel 5 Page Register	008Bh	page 2-65
General Registers	008C–008Fh	pages 2-66–2-69
System Control Port A Register (PS/2 compatibility port)	0092h	page 2-70
Slave 8259 Interrupt Request Register	00A0h	page 2-71
Slave 8259 In-Service Register	00A0h	page 2-72
Slave 8259 Initialization Control Word 1 Register	00A0h	page 2-73
Slave 8259 Operation Control Word 2 Register	00A0h	page 2-75
Slave 8259 Operation Control Word 3 Register	00A0h	page 2-76
Slave 8259 Initialization Control Word 2 Register	00A1h	page 2-77
Slave 8259 Initialization Control Word 3 Register	00A1h	page 2-76
Slave 8259 Initialization Control Word 4 Register	00A1h	page 2-79
Slave 8259 Interrupt Mask Register (AKA Operation Control Word 1)	00A1h	page 2-80
Master DMA Channel 4 Memory Address Register	00C0h	page 2-81
Master DMA Channel 4 Transfer Count Register	00C2h	page 2-82
Master DMA Channel 5 Memory Address Register	00C4h	page 2-83
Master DMA Channel 5 Transfer Count Register	00C6h	page 2-84
Master DMA Channel 6 Memory Address Register	00C8h	page 2-85
Master DMA Channel 6 Transfer Count Register	00CAh	page 2-86
Master DMA Channel 7 Memory Address Register	00CCh	page 2-87
Master DMA Channel 7 Transfer Count Register	00CEh	page 2-88
Master DMA Status Register for Channels 4–7	00D0h	page 2-89
Master DMA Control Register for Channels 4–7	00D0h	page 2-90
Master Software DRQ(n) Request Register	00D2h	page 2-92
Master DMA Mask Register Channels 4–7	00D4h	page 2-93
Master DMA Mode Register Channels 4–7	00D6h	page 2-94
Master DMA Clear Byte Pointer Register	00D8h	page 2-95
Master DMA Controller Reset Register	00DAh	page 2-96
Master DMA Controller Temporary Register	00DAh	page 2-97
Master DMA Reset Mask Register	00DCh	page 2-98
Master DMA General Mask Register	00DEh	page 2-99
Alternate Gate A20 Control Port	00EEh	page 2-100
Alternate CPU Reset Control Port	00EFh	page 2-101
Parallel Port 2 Data Register	0278h	page 2-102
Parallel Port 2 Status Register(PC/AT Compatible mode)	0279h	page 2-103

Register Name	I/O (Port) Address	Page Number
Parallel Port 2 Status Register (Bidirectional mode)	0279h	page 2-104
Parallel Port 2 Status Register (EPP mode)	0279h	page 2-105
Parallel Port 2 Control Register	027Ah	page 2-106
Parallel Port 2 EPP Address Register	027Bh	page 2-107
Parallel Port 2 EPP 32-bit Data Register	027C-027Fh	page 2-108
COM2 Transmit Holding Register (When 02FB[7] = 0, (COM2 DLAB=0)	02F8h	page 2-109
COM2 Receive Buffer Register (When 02FB[7] = 0, COM2 DLAB = 0)	02F8h	page 2-110
COM2 Baud Clock Divisor Latch LSB (When 02FB[7] = 1, COM2 DLAB =1)	02F8h	page 2-111
COM2 Baud Clock Divisor Latch MSB (When 02FB[7] = 1, COM2 DLAB =1)	02F9h	page 2-112
COM2 Interrupt Enable Register (When 02FB[7] = 0, COM2 DLAB = 0)	02F9h	page 2-113
COM2 Interrupt ID Register	02FAh	page 2-114
COM2 FIFO Control Register	02FAh	page 2-116
COM2 Line Control Register	02FBh	page 2-117
COM2 Modem Control Register	02FCh	page 2-118
COM2 Line Status Register	02FDh	page 2-119
COM2 Modem Status Register	02FEh	page 2-121
COM2 Scratch Pad Register	02FFh	page 2-122
Parallel Port 1 Data Register	0378h	page 2-123
Parallel Port 1 Status Register (PC/AT Compatible mode)	0379h	page 2-124
Parallel Port 1 Status Register (Bidirectional) mode)	0379h	page 2-125
Parallel Port 1 Status Register (EPP mode)	0379h	page 2-126
Parallel Port 1 Control Register	037Ah	page 2-127
Parallel Port 1 EPP Address Register	037Bh	page 2-128
Parallel Port 1 EPP 32-bit Data Register	037C-037Fh	page 2-129
MDA/HGA Index Register	03B4h	page 2-130
MDA/HGA Data Port	03B5h	page 2-131
MDA/HGA Mode Control Register	03B8h	page 2-132
MDA/HGA Status Register	03BAh	page 2-133
HGA Configuration Register	3BFh	page 2-134
CGA Index Register	03D4h	page 2-135
CGA Data Port	03D5h	page 2-136
CGA Mode Control Register	03D8h	page 2-137
CGA Color Select Register	03D9h	page 2-138

Register Name	I/O (Port) Address	Page Number
CGA Status Register	03DAh	page 2-139
Primary 82365-Compatible PC Card Controller Index Register	03E0h	page 2-140
Primary 82365-Compatible PC Card Controller Data Port	03E1h	page 2-141
COM1 Transmit Holding Register (When 03FB[7] = 0, (COM1 DLAB =0)	03F8h	page 2-142
COM1 Receive Buffer Register (When 03FB[7] = 0, COM1 DLAB = 0)	03F8h	page 2-143
COM1 Baud Clock Divisor Latch LSB (When 03FB[7] =1, COM1 DLAB =1)	03F8h	page 2-144
COM1 Baud Clock Divisor Latch MSB (When 03FB[7] = 1, COM1 DLAB = 1)	03F9h	page 2-145
COM1 Interrupt Enable Register (When 03FB[7] = 0, COM1 DLAB = 0)	03F9h	page 2-146
COM1 Interrupt ID Register	03FAh	page 2-147
COM1 FIFO Control Register	03FAh	page 2-148
COM1 Line Control Register	03FBh	page 2-149
COM1 Modem Control Register	03FCh	page 2-150
COM1 Line Status Register	03FDh	page 2-151
COM1 Modem Status Register	03FDh	page 2-153
COM1 Scratch Pad Register	03FFh	page 2-154

2.2 **REGISTER DESCRIPTIONS**

Each direct-mapped PC/AT Compatible register is described on the following pages. Additional information about using these registers to program the ÉlanSC400 microcontroller can be found in the *ÉlanSC400 User's Manual* (order #21030).

Slave DMA Channel 0 Memory Address Register

I/O Address 0000h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in the indexed ÉlanSC400 microcontroller registers D9h and DAh.



I/O Address 0001h



Programming Notes

Slave DMA Channel 1 Memory Address Register

I/O Address 0002h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in the indexed ÉlanSC400 microcontroller registers D9h and DAh.



I/O Address 0003h



Programming Notes

Slave DMA Channel 2 Memory Address Register

I/O Address 0004h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in the indexed ÉlanSC400 microcontroller registers D9h and DAh.



I/O Address 0005h



Programming Notes

Slave DMA Channel 3 Memory Address Register

I/O Address 0006h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in the indexed ÉlanSC400 microcontroller registers D9h and DAh.

Slave DMA Channel 3 Transfer Count Register

I/O Address 0007h



Programming Notes

Slave DMA Status Register for Channels 0-3

I/O Address 0008h

	7		6	5	4	3	2	1	0	
Bit	DMAF	२३	DMAR2	DMAR1	DMAR0	ТСЗ	TC2	TC1	TC0	
Default	0		0	0	0	0	0	0	0	
R/W	R		R	R	R	R	R	R	R	
	Bit	Na	me	Functio	n					
	7	DN	IAR3	Channe 0 = Char	I 3 DMA Requined 3 DMA re	uest equest not per	nding			
				1 = Chai	nnel 3 DMA re	equest pendin	g			
	6	DN	/IAR2	Channe	I 2 DMA Requ	uest				
				0 = Chai	nnel 2 DMA re	equest not per	nding			
				1 = Chai	nnel 2 DMA re	equest pendin	g			
	5	DN	/IAR1	Channe	Channel 1 DMA Request					
				0 = Chai	nnel 1 DMA re	equest not per	nding			
				1 = Chai	1 = Channel 1 DMA request pending					
	4 DMAR0			Channe	Channel 0 DMA Request					
				0 = Channel 0 DMA request not pending						
				1 = Chai	nnel 0 DMA re	equest pendin	g			
	3 TC3			Channe 0 = Char	Channel 3 Terminal Count 0 = Channel 3 terminal count not detected					
				1 = Chai	1 = Channel 3 terminal count detected					
	2 TC2		Channe	Channel 2 Terminal Count						
				0 = Chai	nnel 2 termina	I count not de	etected			
				1 = Chai	nnel 2 termina	I count detect	ed			
	1	TC	;1	Channe	1 1 Terminal (Count				
				0 = Chai	nnel 1 termina	I count not de	etected			
				1 = Chai	nnel 1 termina	I count detect	ed			
	0	ТС	0	Channe	l 0 Terminal (Count				
				0 = Chai	nnel 0 termina	I count not de	etected			
				1 = Chai	nnel 0 termina	I count detect	ed			

Programming Notes

Bits 3–0 of this register are read/reset. Any read from this direct-mapped port clears bits 3–0.

Slave DMA Control Register for Channels 0-3

I/O Address 0008h

	7		6	5	4	3	2	1	0		
Bit	DAKS	EN	DRQSEN	WRTSEL	PRITYPE	COMPTIM	ENADMA	ADRHEN	MEM2MEM		
Default	0		0	0	0	0	0	0	0		
R/W	W		W	W	W	W	W	W	W		
	Bit	Na	me	Functio	n						
	7 DAKSEN		DACK(n This bit o controlle	DACK(n) Sense This bit controls the polarity of all <u>DACK</u> outputs from the slave DMA controller:							
				0 = Asse	erted Low						
				1 = Asse	erted High						
				System drive act system o	logic ext <u>ernal</u> tive Low DAC	to the DMA co K outputs. Thi	ontroller expension s bit must be	cts the DMA c written to '0b'	controller to for proper		
	6	DR	QSEN	DREQ(n This bit o	 Sense controls the po 	plarity of all DF	REQ inputs to	the slave DM	A controller:		
				0 = Asse	0 = Asserted High						
				1 = Asse	erted Low						
	System logic external to the DMA controller expects the DMA controller to respond to active High DREQ inputs. This bit must be written to '0b' for proper system operation.						controller to 0 '0b' for				
	5	WF	RTSEL	Write Se 0 = Late Any have	Write Selection Control 0 = Late write selection Any DMA channel that is routed to the ÉlanSC400 IrDA controller must have this bit cleared.						
	1 = Extended (early) write selection										
				Enabling violate th	Enabling this feature will result in timing changes on the ISA bus that can violate the ISA specification.						
	4	PR	ITYPE	Priority 0 = Fixe	Type d priority						
				1 = Rota	ting priority						
	3 COMPTIM Compressed Timing 0 = Normal timing										
				1 = Com	pressed timin	g					
	Enabling this feature will result in timing changes on the ISA bus that can violate the ISA specification.						is that can				
	2	EN	IADMA	Enable I 0 = Enat	DMA Control	ler					
				1 = DMA	requests are	ignored but E	MA registers	are available	to the CPU		
				The DM prevent program DMA coi	A controller sh unintended tra ming operatio ntroller is disa	nould be disab ansfers from o n. If an I/O DN ble via this bit	led prior to pr ccurring durir MA initiator as , abnormal sys	ogramming it og the DMA co serts DREQ v stem operatio	in order to ontroller vhile the n can occur.		

Name	Function
ADRHEN	Enable Channel 0 Address Hold Control IF bit 0 = 1, then:
	0 = Disabled, Channel 0 memory address changes for each memory-to-memory transfer
	1 = Enabled, Channel 0 memory address does not change for each memory-to-memory transfer (not supported by the system)
	ELSE this bit does nothing.
	Since bit 0 should always be written to 0, this bit will be a don't care after the DMA controller has been initialized.
MEM2MEM	Enable Memory-to-Memory Transfer 0 = Disabled
	1 = Enabled (not supported by the system)
	Memory-to-memory DMA support is not provided in a PC/AT Compatible system. This bit should always be written to 0.
	Name ADRHEN MEM2MEM

Programming Notes
I/O Address 0009h

Slave Software DRQ(n) Request Register



Slave DMA Mask Register Channels 0-3

I/O Address 000Ah

	7	6	5	4	3	2	1	0		
Bit			Reserved		MSK MSK	SEL1 SEL0				
Default	x x		x	х	х	х	х	х		
R/W						W	W			
	Bit	Name	Functio	n						
	7–3	Reserved	Reserved Software should write these bits to 0.							
	2	CHMASK	DMA Ch 0 = Clea	hannel Mask Ir mask bit for	channel selec	cted by bits 1–	0			
			1 = Set i	mask bit for cl	nannel selecte	ed by bits 1–0				
	1–0	MSKSEL1	DMA Ch	nannel Mask	Select					
		MSKSEL0	Bits 1–0 unmask	the DRQ sigr	DMA channel al into the spe	ecified DMA cl	nternally to i hannel:	mask or		
			0 0 = Ma	ask/unmask D	MA Channel (0 mask per the	e CHMASK bi	t		
			0 1 = Mask/unmask DMA Channel 1 mask per the CHMASK bit							
		1 0 = Mask/unmask DMA Channel 2 mask per the CHMASK								
			1 1 = Mask/unmask DMA Channel 3 mask per the CHMASK bit					t		

Programming Notes

The same DMA channel masks can be controlled via DMA registers 0Ah, 0Eh, and 0Fh.

Slave DMA Mode Register Channels 0-3

I/O Address 000Bh

	7		6	5	4	3	2	1	0				
Bit		TRN	MOD	ADDDEC	AINIT	OP OP	SEL1 SEL0	MOD MOD	SEL1 SEL0				
Default	х		х	х	Х	х	х	х	х				
R/W		V	V	W	W		W	V	V				
	Bit	Na	me	Functio	n								
	7–6	TR	NMOD	Transfer Mode 0 0 = Demand transfer mode									
				0 1 = Sir	ngle transfer n	node							
				1 0 = Blc	ock transfer m	ode							
				1 1 = Ca	1 1 = Cascade mode								
	5 ADDDEC		DDEC	Address 0 = Incre	Address Decrement 0 = Increment the DMA memory address after each transfer								
				1 = Decr	ement the DN	1A memory a	address after e	ach transfer					
	4	AIN	ΝΤ	If enabled, the base address and transfer count registers are restored to the values they contained prior to performing the last DMA transfer. The channel selected by bits 0–1 of this register is then ready to perform another DMA transfer without processor intervention as soon as the next DRQ is detected.									
				0 = Automatic initialization disabled									
				1 = Automatic initialization enabled									
	3–2	OP OP	SEL1 SEL0	Operation Select 0 0 = Verify mode DMA controller acts normally except that no I/O or memory commands are generated, and no data is transferred									
				0 1 =Wr Da me	ite transfer ta will be trans mory	sferred from	a DMA-capabl	e I/O device ir	nto system				
				1 0 = Re Da dev	ad transfer ta will be trans vice	sferred from	system memo	ry to a DMA-ca	apable I/O				
				1 1 = Re	served								
	1–0 M N		DSEL1 DSEL0	DMA Channel Select Bits 7–2 of this register are latched internally for each channel. Bits 0–1 determine which of the channels will be programmed by the write to port 0Bh as follows:									
				0 0 = Se	lect Channel ()							
				0 1 = Se	lect Channel	1							
				1 0 = Se	lect Channel 2	2							
				1 1 = Se	lect Channel 3	3							

Slave DMA Clear Byte Pointer Register

I/O Address 000Ch





I/O Address 000Dh



Slave DMA Controller Temporary Register

I/O Address 000Dh



Programming Notes

The same DMA channel masks can be controlled via DMA registers 0Ah, 0Eh, and 0Fh.



I/O Address 000Eh



Programming Notes

The same DMA channel mask can be controlled via DMA register 0Ah, 0Eh, and 0Fh.

7 6 5 4 3 2 1 0 Bit Reserved DIS3 DIS2 DIS1 DIS0 Default 0 0 0 0 1 1 1 1 W W W W R/W Bit Name Function 7–4 Reserved Reserved Software should write these bits to 0. 3 DIS3 **DMA Channel 3 Mask** 0 = Enable DMA Channel 3 for servicing DMA requests 1 = Disable DMA Channel 3 from servicing DMA requests 2 DIS2 **DMA Channel 2 Mask** 0 = Enable DMA Channel 2 for servicing DMA requests 1 = Disable DMA Channel 2 from servicing DMA requests 1 DIS1 **DMA Channel 1 Mask** 0 = Enable DMA Channel 1 for servicing DMA requests 1 = Disable DMA Channel 1 from servicing DMA requests 0 DIS0 **DMA Channel 0 Mask** 0 = Enable DMA Channel 0 for servicing DMA requests 1 = Disable DMA Channel 0 from servicing DMA requests

I/O Address 000Fh

Slave DMA General Mask Register

Programming Notes

The same DMA channel masks can be controlled via DMA registers 0Ah, 0Eh, and 0Fh.

Master 8259 Interrupt Request Register

I/O Address 0020h

	7		6	5	4	3	2	1	0			
Bit	IR7		IR6	IR5	IR4	IR3	IR2	IR1	IR0			
Default	х		х	х	х	х	х	х	х			
R/W	R		R	R	R	R	R	R	R			
	Bit Name		me	Functio	n							
	7 IR		7	Interrup 0 = IRQ	ot Request 7 7 input to the I	I						
				1 = IRQ	7 is asserted							
	6 IR		6	Interrup 0 = IRQ	ot Request 6 6 input to the I	l						
				1 = IRQ	6 is asserted							
	5 IR5		5	Interrup 0 = IRQ	ot Request 5 5 input to the I	l						
				1 = IRQ	5 is asserted							
	4	IR4	1	Interrupt Request 4 0 = IRQ4 input to the Master 8259 is not asserted								
				1 = IRQ	1 = IRQ4 is asserted							
	3	IR	3	Interrup 0 = IRQ	ot Request 3 3 input to the I	Master 8259 i	s not asserted	l				
				1 = IRQ	1 = IRQ3 is asserted							
	2	IR2	2	Interrup 0 = IRQ	Interrupt Request 2 0 = IRQ2 input to the Master 8259 is not asserted							
				1 = IRQ	2 is asserted							
	1 IR		1	Interrup 0 = IRQ	Interrupt Request 1 0 = IRQ1 input to the Master 8259 is not asserted							
				1 = IRQ	1 is asserted							
	0 IR)	Interrup 0 = IRQ	ot Request 0 0 input to the I	Master 8259 i	s not asserted	I				
				1 = IRQ	0 is asserted							

Programming Notes

This register provides a real-time status of the IRQ (interrupt request) inputs to the Master 8259. The Master Interrupt Request register (IRR) is accessed by first writing a value of 0Ah to port 20h followed by a read-back from port 20h.

Since the Slave 8259 cascades into Channel 2 of the Master 8259, IR2 is a real-time status indication that one of the slave IRQ inputs is asserted.

Master 8259 In-Service Register

I/O Address 0020h

	7		6	5	4	3	2	1	0		
Bit	IS7		IS6	IS5	IS4	IS3	IS2	IS1	IS0		
Default	х		Х	х	х	Х	Х	Х	х		
R/W	R		R	R	R	R	R	R	R		
	Bit Name		Functio	Function							
	7 IS7		,	IRQ7 In 0 = IRQ	IRQ7 In-Service 0 = IRQ7 is not being serviced						
				1 = IRQ	7 is being serv	viced					
	6 IS6		IRQ6 In ∙ 0 = IRQ€	IRQ6 In-Service 0 = IRQ6 is not being serviced							
				1 = IRQ6	1 = IRQ6 is being serviced						
	5	5 IS5		IRQ5 In 0 = IRQ	IRQ5 In-Service 0 = IRQ5 is not being serviced						
				1 = IRQ	5 is being serv	viced					
	4	IS4	Ļ	IRQ4 In-Service 0 = IRQ4 is not being serviced							
				1 = IRQ4	4 is being serv	viced					
	3	IS3	3	IRQ3 In - 0 = IRQ3	- Service 3 is not being	serviced					
				1 = IRQ3	3 is being serv	viced					
	2	IS2	2	IRQ2 In 0 = IRQ2	-Service 2 is not being	serviced					
				1 = IRQ2	2 is being serv	viced					
	1	1 IS1		IRQ1 In 0 = IRQ ²	- Service 1 is not being	serviced					
				1 = IRQ	1 is being serv	viced					
	0	ISC)	IRQ0 In 0 = IRQ0	- Service D is not being	serviced					
				1 = IRQ() is being serv	viced					

Programming Notes

The Master In-Service register (ISR) is accessed by first writing a value of 0Bh to port 20h followed by a read-back from port 20h.

Since the Slave 8259 cascades into Channel 2 of the Master 8259, IS2 will be asserted if any slave IRQ level is asserted.

Master 8259 Initialization Control Word 1 Register

I/O Address 0020h

AMDЛ

	7	6	5	4	3	2	1	0				
Bit		Reserved		SLCT_ICW1	LTIM	ADI	SNGL	IC4				
Default	x	х	х	х	х	х	х	х				
R/W		W		W	W	W	W	W				
	Bit	Name	Functio	Function								
	7–5	Reserved	Reserve Must all	ed be written to ().							
	4	SLCT_ICW1	Select I Must be Initializa	Select ICW1 Must be written to 1 to access ICW1 (D4 = 1 means the IOW to port 2 Initialization Control Word 1).								
	3	LTIM	Level-T 0 = Edg	Level-Triggered Interrupt Mode 0 = Edge-sensitive IRQ detection								
			1 = Leve	el-sensitive IR	Q detection							
	2	ADI	Address 0 = Inter	s Interval (ha rupt vectors a	s no effect w re separated	hen the 8259 by 8 locations	is used in x8	86 mode)				
			1 = Inter	rupt vectors a	re separated	by 4 locations						
			In the Él internall	anSC400 mic y fixed to '1b'.	rocontroller de	esign, this PC	AT Compatib	le bit is				
	1	SNGL	Single 8 If this bit ICW4 if the expla	3259 is set, then th ICW4 was sele anation for bit	e internal regi ected to be pro 0 of this regis	ster pointer w ogrammed via ter:	ill skip ICW3, a bit 0 of this re	and point to egister. See				
			0 = Cas	cade mode, IC	W3 will be ex	pected						
			1 = Sing	le 8259 in the	system, ICW	3 will not be e	xpected					
			In the Él internall	anSC400 mic y fixed to '0b'.	rocontroller de	esign, this PC	AT Compatib	le bit is				
	0	IC4	word (ICW) re with bit 4 = 1 he PIC's interr 4 are progran W1), the regis d ICW2 must a rogrammed u	egisters 1–4 causes the hal state hmed via ster pointer always be hder certain								
			0 = Initia Wore	lization Contro d 1, ICW4 will	ol Word 4 is cl not be expect	eared by writi ed by the PIC	ng Initializatio	n Control				
			1 = ICW softv	4 is not cleare vare is expect	d by this write ed to initialize	to Initializatio	on Control Wo	rd 1, and				
			This bit or wheth program PIC will	determines wher a value of our of the second	nether ICW4 is 20h will serve ster pointer wi re to provide a	s required to b for ICW4. If IO Il point to ICW an initialization	be explicitly pr CW4 is selecte /4 after ICW3, n value for it.	ogrammed, ed to be , and the				
			In the Él internall	anSC400 mic y fixed to '1b'.	rocontroller de	esign, this PC	AT Compatib	le bit is				

Master 8259 Operation Control Word 2 Register

I/O Address 0020h

	7		6	5	4	3	2	1	0	
Bit			R SL EOI		SLCT_ICW1 IS_OCW3			LS[2-0]		
Default	х		х	х	x	х	х	х	х	
R/W			W		W	W				
	Bit	Nam	ne	R/W	Function					
	7–5	R SI		W	IRQ EOI and Priority Rotation Controls 0 0 0 = Rotate in auto EOI mode (clear)					
		EOL			0 0 1 = Non-s	specific EOI				
		_0.			0 1 0 = No op	peration				
					0 1 1 = Speci	ific EOI				
					1 0 0 = Rotate in auto EOI mode (set)					
					1 0 1 = Rotate on non-specific EOI command					
					1 1 0 = Set p	riority comma	nd			
					1 1 1 = Rotat	e on specific l	EOI command	1		
	4	SLC	CT_ICW1	W	Select Initial Software mus	lization Contu st write this bi	t to 0 to acces	s OCW2 or C	CW3.	
	3	IS_C	DCW3	W	Access is O An I/O write t is to be acces	CW3 to port 20h wit ssed.	h this bit clea	red indicates	that OCW2	
	2–0	LS[2	2–0]	W	Specific EOI Interrupt leve 7–5 of this re	Level Select Which is acte gister):	ed upon when	the SL bit = '	lb' (see bits	
					0 0 0 = IRQ0					
					0 0 1 = IRQ1					
					0 1 0 = IRQ2					
					0 1 1 = IRQ3					
					1 0 0 = IRQ4					
					1 0 1 = IRQ5					
					1 1 0 = IRQ6					
					1 1 1 = IRQ7					

Programming Notes

I/O writes to port 20h access different PIC registers based on bits 4–3 of the data that is written. See the following table:

Bit 4	Bit 3	Register Accessed
0	0	OCW2
0	1	OCW3
1	х	ICW1

Master 8259 Operation Control Word 3 Register

I/O Address 0020h

	7		6	5	4	3	2	1	0			
Bit	Reserv	red	ESMM SMM		SLCT_ICW1	IS_OCW3	Р	RF	8			
Default	х		x	х	х	Х	Х	х	х			
R/W			W		W	W	W	W				
	Rit Name		Functio	n								
			served	Posorva								
	'	/ Reserved		Software should write this bit to 0.								
	6–5	ES SM	MM 1M	Special Mask Mode 0 x = No operation								
				1 0 = Reset special mask								
				1 1 = Set special mask								
				In the Él '1b'.	anSC400 mic	rocontroller de	sign, the ESN	1M bit is interna	ally fixed to			
	4	SL	CT_ICW1	Initializa Software	ation Control e should write	Word 1 Sele this bit to 0 to	ct access OCW	/2 or OCW3.				
	3	IS_	_OCW3	Access is OCW3 An I/O write to port 20h with this bit set indicates that OCW3 is to be accessed.								
	2	Ρ		PIC Poll A system this case interrupt the PIC OCW3 v	PIC Poll Command A system design can choose to use the PIC in a non-interrupting mode. In this case, the interrupt controller can be polled for the status of pending interrupts. In order to support this PC/AT incompatible mode of operation, the PIC supports a special poll command which is invoked by writing OCW3 with this bit set.							
				0 = Not	poll command							
				1 = Poll	command							
	1–0	RR RIS	R S	Status F 0 0 = No	Status Register Select 0 0 = No change from last state							
			-	0 1 = No	change from	last state						
				1 0 = Ne	ext port 20h re	ad will return	Interrupt Requ	uest Register (I	RR)			
				1 1 = Ne	ext port 20h re	ad will return	In-Service Re	gister (ISR)				

Programming Notes

I/O writes to port 20h access different PIC registers based on bits 4–3 of the data that is written. See the following table:

Bit 4	Bit 3	Register Accessed
0	0	OCW2
0	1	OCW3
1	х	ICW1

Master 8259 Initialization Control Word 2 Register

I/O Address 0021h



Master 8259 Initialization Control Word 3 Register

I/O	Address	0021h
-----	---------	-------

	7		6	5	4	3	2	1	0				
Bit	S7		S6	S5	S4	S3	S2	S1	SO				
Default	х		Х	х	х	х	х	х	х				
R/W	W		W	W	W	W	W	W	W				
	Bit Name 7 S7			Functio Channe	n I 7 Slave Cas	cade Select							
					0 = I/O device attached to IRQ7 input 1 = IRQ7 input used for slave cascading								
	6	6 S6			Channel 6 Slave Cascade Select 0 = I/O device attached to IRQ6 input								
	5	S5		1 = IRQ6 Channe 0 = I/O c	Channel 5 Slave Cascade Select 0 = I/O device attached to IRQ5 input								
	4	S4		1 = IRQ Channe 0 = I/O c	 1 = IRQ5 input used for slave cascading Channel 4 Slave Cascade Select 0 = I/O device attached to IRQ4 input 								
	3	S3		1 = IRQ4 Channe 0 = I/O c	 1 = IRQ4 input used for slave cascading Channel 3 Slave Cascade Select 0 = I/O device attached to IRQ3 input 								
	2	S2		1 = IRQ3 Channe 0 = I/O c	1 = IRQ3 input used for slave cascading Channel 2 Slave Cascade Select 0 = I/O device attached to IRQ2 input								
	1	S1		1 = IRQ2 Channe 0 = I/O c	1 = IRQ2 input used for slave cascading Channel 1 Slave Cascade Select 0 = I/O device attached to IRQ1 input								
					 1 = IRQ1 input used for slave cascading In the ÉlanSC400 microcontroller design, this PC/AT Compatible bit is internally fixed to '1b'. 								
	0	S0		Channe 0 = I/O c 1 = IRQ0	Channel 0 Slave Cascade Select 0 = I/O device attached to IRQ0 input 1 = IRQ0 input used for slave cascading								

Programming Notes

Bits 7–3 and 1–0 of ICW3 are internally fixed to '0b' in this design. Bit 2 is internally fixed to '1b'.

Master 8259 Initialization Control Word 4 Register

I/O Address 0021h

	7		6	5	4	3	2	1	0		
Bit		Rese	erved		SFNM	BUF M/S		AEOI	РМ		
Default	х		x	х	х	х	х	х	х		
R/W		١	V		W W W				W		
	Bit	Name		Functio	n						
	7–5	Reserved		Reserved Software should write these bits to 0.							
	4	SFNM		Special Fully Nested Mode Enable 0 = Normal nested mode							
				1 = Spec	cial fully neste	d mode					
	3–2	BUF M/S		Buffered 0 x = No	d Mode and M	Master/Slave	Select				
		141/0		1 0 = Bu	ffered mode/s	slave					
				1 1 = Bu	ffered mode/r	naster					
				In the Él '00b'.	anSC400 mic	rocontroller de	esign, these b	its are interna	lly fixed to		
	1	AEOI		Automatic EOI Mode 0 = Normal EOI Interrupt handler must send an End of Interrupt command to the PIC(s)							
				1 = Auto EOI CPU	EOI is automatical	ly performed a	after the seco	nd INTA signa	I from the		
	0	PM		Micropr 0 = 8080	ocessor Mod)/8085 mode	le					
				1 = 8086	6 mode						
				In the ÉlanSC400 microcontroller design, this PC/AT Compatible bit is internally fixed to '1b'.							

I/O Address 0021h

Master 8259 Interrupt Mask Register (also known as Operation Control Word 1)

	7		6	5	4	3	2	1	0		
Bit	IM7		IM6	IM5	IM4	IM3	IM2	IM1	IMO		
Default	х		х	х	х	х	х	х	х		
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Bit	Na	me	Functio	n						
	7	7 IM7		IRQ7 M a 0 = Unm	IRQ7 Mask 0 = Unmask IRQ7						
				1 = Mas	1 = Mask IRQ7						
	6	6 IM6		IRQ6 M a 0 = Unm	IRQ6 Mask 0 = Unmask IRQ6						
				1 = Mas	k IRQ6						
	5	IM	5	IRQ5 M a 0 = Unm	IRQ5 Mask 0 = Unmask IRQ5						
				1 = Mas	k IRQ5						
	4	IM4	1	IRQ4 M a 0 = Unm	IRQ4 Mask 0 = Unmask IRQ4						
				1 = Mas	k IRQ4						
	3	IM	3	IRQ3 M a 0 = Unm	ask lask IRQ3						
				1 = Mas	k IRQ3						
	2	2 IM2		IRQ2 M a 0 = Unm	ask nask IRQ2						
				1 = Mas	k IRQ2						
	1	1 IM1		IRQ1 M a 0 = Unm	IRQ1 Mask 0 = Unmask IRQ1						
				1 = Mas	k IRQ1						
	0	IM)	IRQ0 M a 0 = Unm	IRQ0 Mask 0 = Unmask IRQ0						
				1 = Mas	k IRQ0						

ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Index Register



ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Data Port

I/O Address 0023h



Programmable Interval Timer #1 Channel 0 Count Register (System Timer/Timer Tick)

I/O Address 0040h



Programming Notes

If a read-back command is issued in which LSTAT = '0b', and the CNT0 bit = '1b', a status byte for this channel, as defined by the Programmable Interval Timer #1 Status Register (see below), will be read back. If a read-back command is issued in which LSTAT = '0b', LCNT = '0b', and the CNT0 bit = '1b', the first read from this register will return the status byte, and the second/third bytes will return the 1 or 2 (low/high) latched count byte(s).

When set up for either BCD or 16-bit binary count operation, the maximum count for Channel 0 is achieved by writing the internal counting element associated with this register to 0000h/d. See direct-mapped register 43h for more detail.

I/O Address 0041h

Programmable Interval Timer #1 Channel 1 Count Register (Refresh Timer)



Programming Notes

If a read-back command is issued in which LSTAT = '0b', and the CNT1 bit = '1b', a status byte for this channel, as defined by the Programmable Interval Timer #1 Status Register (see below), will be read back. If a read-back command is issued in which LSTAT = '0b', LCNT = '0b', and the CNT1 bit = '1b', the first read from this register will return the status byte, and the second/third bytes will return the 1 or 2 (low/high) latched count byte(s).

When set up for either BCD or 16-bit binary count operation, the maximum count for Channel 1 is achieved by writing the internal counting element associated with this register to 0000h/d. See direct-mapped register 43h for more detail.

Programmable Interval Timer #1 Channel 2 Count Register (Speaker Timer)



I/O Address 0042h

Programming Notes

If a read-back command is issued in which LSTAT = '0b', and the CNT2 bit = '1b', a status byte for this channel, as defined by the Programmable Interval Timer #1 Status Register (see below), will be read back. If a read-back command is issued in which LSTAT = '0b', LCNT = '0b', and the CNT2 bit = '1b', the first read from this register will return the status byte, and the second/third bytes will return the 1 or 2 (low/high) latched count byte(s).

When set up for either BCD or 16-bit binary count operation, the maximum count for Channel 2 is achieved by writing the internal counting element associated with this register to 0000h/d. See direct-mapped register 43h for more detail.

Programmable Interval Timer #1 Status Register

I/O Address 0040-0042h

	7	6	5	4	3	2	1	0
Bit	OUTPUT	NULLCNT	RV RV	V1 V0		M2 M1 M0		BCD
Default	0	0	0	0	0	0	0	0
R/W	R	R	F	र		R		R

Bit	Name	Function
7	OUTPUT	Output Pin State Output signal for the current timer channel. Each timer channel has an output pin that is driven high or low based on the current mode. See the brief mode descriptions for bits 3–1 of this register for more detail.
		0 = Current state of OUT(x) signal = logic 0
		1 = Current state of OUT(x) signal = logic 1
6	NULLCNT	Null Count When programming a new count value into one of the timers, the new value does not take effect until it has actually been transferred to the counting element, which can take some time. Thus, when attempting to read back a count value, this bit indicates whether the value read back is valid or not.
		1 = Null count, read back of the counter will be invalid
		0 = Counter is available for reading
5–4	RW1 RW0	Counter Read/Write Operation Control or Counter Latch Command Reflects the last bit setting that was programmed into this field for this counter channel via the Programmable Interval Timer #1 Mode Control Register. See the Programmable Interval Timer #1 Mode Control Register on page 2-41 for more information.
		0 0 = Counter Latch Command
		0 1 = Read/Write LSB only
		1 0 = Read/Write MSB only
		1 1 = Read/Write LSB first followed by MSB
3–1	M2 M1 M0	Counter Mode Status Reflects the last counter mode setting for counters 0, 1, or 2 that was programmed into this channel via the Programmable Interval Timer #1 Mode Control Register. See the Programmable Interval Timer #1 Mode Control Register on page 2-41 for more information.
		Gate = High unless noted
		0 0 0 = Mode 0: Interrupt on terminal count
		0 0 1 = Mode 1: Hardware retriggerable one-shot
		0 1 0 = Mode 2: Rate generator
		0 1 1 = Mode 3: Square wave generator
		1 0 0 = Mode 4: Software retriggerable strobe
		1 0 1 = Mode 5: Hardware retriggerable strobe
		1 1 0 = Alias for mode 2
		1 1 1 = Alias for mode 3
		See the table below for more detail on this register.
0	BCD	Binary Coded Decimal Select Status Reflects the last BCD setting for counters 0, 1, or 2 that was programmed into this channel via the Programmable Interval Timer #1 Mode Control Register. See the Programmable Interval Timer #1 Mode Control Register on page 2-41 for more information.
		0 = 16-bit binary counter with a range of 0–FFFFh
		1 = BCD counter with a range of 0–9999d

Programming Notes

These three registers (at direct-mapped I/O addresses 40h, 41h, and 42h) are separately available only as a result of sending a read-back command with the LSTAT bit = '0b', and the appropriate CNTX bit set (where X is a counter from 0-2). For more detail, see the Read-Back Command Register on page 2-44. Note also that modes 1 and 5 require a rising edge on the gate input for each timer channel. Only Timer 2 has a gate control (see direct-mapped port 61h[0]) so only Channel 2 is capable of running all modes. The gate controls for Timers 0 and 1 are fixed internally to '1b', so they are only capable of operation in modes 0, 2, 3 and 4.

Counter Mode Status Bits 3-1

Settings	Mode Name	Description
0 0 0 = Mode 0	Interrupt on terminal count	When the counter is programmed, the Counter Output Signal transitions to 0. When counter reaches 0, the Counter Output signal transitions to 1 until another count is written.
0 0 1 = Mode 1	Hardware retriggerable one-shot	When mode/counter are programmed, the Counter Output signal transitions to 1. When gate goes 0 transitions to 1, OUT transitions to 0 until the count reaches 0, then OUT transitions to 1 until the next low-high transition on gate.
0 1 0 = Mode 2	Rate generator	Each time the count transitions to 1, OUT transitions to 0, and remains there for 1 cycle of the input clock, and then OUT transitions to 1. The count is automatically reloaded, and the process repeats. Timer 0 uses this mode by default in the PC/AT.
0 1 1 = Mode 3	Square wave generator	When the count is loaded, OUT transitions to 1. When 1/2 of the count has expired, OUT transitions to 0. When count transitions to 0, OUT transitions to 1, and count is automatically reloaded. In the PC/ AT, Timers 1 and 2 use this mode by default to drive DRAM refresh and the speaker respectively.
1 0 0 = Mode 4	Software retriggerable strobe	When the count is loaded, OUT transitions to 1. When counter = 0, OUT transitions to 0 for 1 clock and then OUT transitions to 1.
1 0 1 = Mode 5	Hardware retriggerable strobe	The Counter Output signal behaves just like mode 4 except that the triggering is done by a low to high transition on the gate input. A trigger seen during the count reloads the count to the initial value and then counting continues.
1 1 0 = Alias for mode 2		
1 1 1 = Alias for mode 3		

Programmable Interval Timer #1 Mode Control Register I/O Address 0043h

	7		6	5	4	3	2	1	0		
Ri+		SC1	l	RV	V1	M2					
ы		SCO)	RW0			MO		ВСБ		
Default	0		0	0	0	0	0	0	0		
R/W		W		V	V		W		W		
	Bit	Nam	ie	Function							
	7–6 SC1 SC0			Channe When th redefine Commar	Channel Select or Read-back Command When this register is written to with bits 7–6 = '11b', this register is redefined (for the duration of the current I/O write) as the Read-back Command Register which is described as a separate register below.						
				When th these bit 5–0 appl	When this register is written to with bits 7–6 \neq '11b', and bits 5–4 \neq '00b', these bits specify to which of the three on-chip counters the settings in bits 5–0 apply:						
				0 0 = Se	lect Channel	0					
				0 1 = Se	lect Channel	1					
				1 0 = Select Channel 2							
				1 1 = Read-back Command							
				A read-b comman only the 5–4 will t Register	ack command d. If bits 5–4 a read-back cor take on the m below.	d is a higher p are written to ' mmand will be eanings as de	riority comma 00b', and bits recognized a scribed by the	nd than the co 7–6 are writte is command b e Read-back (ounter latch en to '11b', its, and bits Command		
	5–4	RW1 RW0)	Counter When th this regis Counter register l	Counter Read/Write Operation Control or Counter Latch Command When this register is written to with bits $5-4 = '00b'$, and bits $7-6 \neq '11b'$, this register is redefined (for the duration of the current I/O write) as the Counter Latch Command Register which is described as a separate register below.						
				When th these bit where X count reg write to t the 8 bits explicitly	is register is v s define what is selected by gister will be a he count regis of the assoc written to.	vritten to with can be writter bits 7–6 of th ccessed (i.e., ster (as indica iated internal	bits 7–6 ≠ '11 n to the Chan nis register. N bits 5–4 = '01 ted by bits 7– 16-bit countin	b', and bits 5– nel X Count R ote that if only b' or '10b'), a 6) will automa g element whi	4 ≠ '00b', egister, 8 bits of a subsequent tically clear ch were not		
				0 0 = Co	unter Latch C	ommand					
				0 1 = Re	ad/Write cour	nter bits [7–0]					
				1 0 = Re	ad/Write cour	nter bits [15–8]				
				11 = Re	ad/Write cour	nter bits [7–0]	followed imm	ediately by [15	5–8]		
				A counter takes a s required used to c are ignor count rep not provi	er latch comm snapshot of th obtain it. Once red until all lat gister. Also no de any way to e count registe	and does not e current valu ch command e the count da ched count da ote that the 82 read back the ers.	stop a counte e. When a co or a read-bac been latched ta is read ba 54 Programme original cour	r from running unter's curren k command sl d, further latch ck from the as able Interval t programmed	g, but rather t value is hould be commands sociated Timer does d into any of		

Bit	Name	Function
3–1	M2 M1	Counter Mode When this register is written to with bits $7-6 \neq 11b'$, and bits $5-4 \neq 00b'$, these bits control the counter operation:
	MO	0 0 0 = Mode 0: Interrupt on terminal count
		0 0 1 = Mode 1: Hardware retriggerable one-shot
		0 1 0 = Mode 2: Rate generator
		0 1 1 = Mode 3: Square wave generator
		1 0 0 = Mode 4: Software retriggerable strobe
		1 0 1 = Mode 5: Hardware retriggerable strobe
		1 1 0 = Alias for mode 2
		1 1 1 = Alias for mode 3
0	BCD	Binary Coded Decimal Select When this register is written to with bits $7-6 \neq `11b'$, and bits $5-4 \neq `00b'$, this bit controls whether the counter indicated by bits $7-6$ of this register will count in binary with a range of 0–FFFFh or in binary coded decimal (BCD) with a range of 0–9999d.
		0 = 16-bit binary counter
		1 = BCD counter

Programming Notes

Writing to this register to change the mode for a particular counter resets the control logic and resets the associated counter value and OUT pin.

Programmable Interval Timer #1 Counter Latch Command Register

I/O Address 0043h

	7		6	5	4	3	2	1	0		
Bit	SC1 SC0		RW1 RW0		Reserved						
Default	0 0		0	0	0	0	0	0			
R/W	W			Ŵ				·			
	Bit 7–6	Name SC1 SC0		Functio Counte Specify	Function Counter Select Specify which of the three counter elements to latch for read back from the associated count register. The counter latch command is a subset of the						
				read-back command since only one channel can have its counter latched per counter latch command:							
				0 0 = Select counter 0							
				0 1 = Select counter 1							
				1 0 = Select counter 2							
				1 1 = N/	Ά						
	5–4	RW1		Counte	r Command						
		RW0		0 0 = C 0	ounter Latch C	Command					

Software should write these bits to 0.

Reserved

See Programmable Interval Timer #1 Mode Control Register on page 2-41 for more detail.

Programming Notes

Reserved

3–0

Programmable Interval Timer #1 Read-Back Command Register

	7	6	5	4	3	2	1	0
Bit	SC1 SC0		LCNT	LSTAT	CNT2	CNT1	CNT0	Reserved
Default	0	0	0	0	0	0	0	0
	W		W	W	W	W	W	W

Bit	Name	Function
7–6	SC1 SC0	Counter Select/Read-back Command 1 1 = Read-back Command Values as selected by bits 5–1 of this register are available to be read back from direct-mapped ports 40h–42h immediately following completion of the I/O write that implements this Read-back Command. Latched counts will be read back based on the current mode for each counter (bits 7–0, bits 15–8, or bits 7–0 followed by bits 15–8). For the format of the returned status byte, see the Programmable Interval Timer#1 Status Register bit descriptions above. See the Programmable Interval Timer #1 Mode Control Register on page 2-41 for more detail.
		If both LSTAT and LCNT = '0b', the status byte will be available at the respective count register (direct-mapped 40h, 41h, and 42h) first. When this byte has been read, the latched count byte(s) will be available, and will read back low order byte and then high order byte (if set up to read back all 16-bits of count via the Programmable Interval Timer #1 Mode Control Register).
5	LCNT	Latch Count (low true) 0 = Latch count for counters selected via bits 3–1
		1 = Do not latch count for counters selected via bits 3-1
4	LSTAT	Latch Status (low true) 0 = Latch status for counters selected via bits 3–1
		1 = Do not latch status for counters selected via bits 3–1
3	CNT2	Select Counter 2 0 = Counter 2 not selected for operations specified by bits 5–4
		1 = Counter 2 selected for operations specified by bits 5–4
2	CNT1	Select Counter 1 0 = Counter 1 not selected for operations specified by bits 5–4
		1 = Counter 1 selected for operations specified by bits 5–4
1	CNT0	Select Counter 0 0 = Counter 0 not selected for operations specified by bits 5–4
		1 = Counter 0 selected for operations specified by bits 5–4
0	Reserved	Reserved Software should write this bit to 0.

Keyboard/Mouse Interface Output Buffer

I/O Address 0060h



Programming Notes

This port is typically inside the external processor that is used to implement the SCP (System Control Processor) on a PC/AT Compatible system. Although an entire SCP is not implemented on-board in this design, some SCP registers are available to support the ÉlanSC400 microcontroller's capability of SCP emulation using a matrix keyboard. This PC/AT SCP emulation support register is only available to be read from this location when the ÉlanSC400 microcontroller's SCP emulation feature is enabled via CSC index C1h[3–2].

PC/AT Keyboard Interface Data Register

I/O Address 0060h



Programming Notes

This port is typically inside the external processor that is used to implement the SCP (System Control Processor) on a PC/AT Compatible system. Although an entire SCP is not implemented on-board in this design, some SCP registers are available to support the ÉlanSC400 microcontroller's capability of SCP emulation using a matrix keyboard. This PC/AT SCP emulation support register is only available to be read from this location when the ÉlanSC400 microcontroller's SCP emulation feature is enabled via CSC index register C1h[3–2].

PC/XT Keyboard Data Register

I/O Address 0060h



System Control Port B/NMI Status Register

I/O Address 0061h

	7		6	5	4	3	2	1	0		
Bit	PERF	२	IOCHCK	T2OUT	RFD	Reserved	Reserved	SPKD	T2G		
Default	0		0	х	0	0	0	0	0		
R/W	R/W		R/W	R	R	R/W	R/W	R/W	R/W		
	Bit	Na	me	Fundion DO/AT Desite Fases to the star							
	7	PERR		Not supported (always reads back '0b').							
	6	6 IOCHCK		PC/AT Channel Check Indicator Not supported (always reads back '0b').							
	5	T2	OUT	Timer 2 (Speaker) Output Pin State This status bit directly reflects the state of the output signal of Channel 2 the on-board 8254 Programmable Interval Timer and is sampled before t gate controlled by bit 1 of this register.							
				0 = T2 o	utput is low						
			1 = T2 output is high								
	4	RF	D	DRAM Refresh Indicator This bit changes state each time a refresh is detected. On the original PC/AT, the Programmable Interval Timer Channel 1 output pin was used to generate the refresh signal. As an alternative in this design, the doubled 32 KHz clock can be used as the input to a divider to obtain the refresh clock. This bit tracks the current refresh source, regardless of the refresh generation source.							
	3	Re	served	Reserved On the original PC/AT, this bit was used to enable I/O channel check. Although this read/write register bit has been implemented on this design, it does not control anything. For software using this register to remain PC/AT Compatible, read/modify/write operations should preserve this bit.							
	2	Re	served	Reserved On the original PC/AT, this bit was used to enable RAM parity chec Although this read/write register bit has been implemented on this d does not control anything. For software using this register to remain Compatible, read/modify/write operations should preserve this bit.					check. iis design, it nain PC/AT bit.		
	1	SPKD		Speaker This bit o AND gat	Data Enable controls a sigr e output is the	e hal which is Al en used to driv	NDed with the ve the system	output from T speaker.	imer 2. The		
				0 = Do n	ot propagate	speaker data					
				1 = Prop	agate speake	er data					
	0 T2G		G	Timer 2 GATE Input Control This bit drives the GATE input signal for Channel 2 of the 8254 Programmable Interval Timer which can be used to control the Timer Channel 2 operation depending on the current timer mode. See the Programmable Interval Timer Status Register description at direct-mapp 40–42h for more detail on the function of the gate input.							
				0 = Prog	rammable Int	erval Timer G	ATE input is c	leasserted			
				1 = Prog	rammable Int	erval Timer G	ATE input is a	sserted			

PC/AT Keyboard/Mouse Interface Status Register

I/O Address 0064h

	7	6	5	4	3	2	1	0		
Bit	KEYPAR	KEYRTO	KEYTTO	KEYENB	KEYCMD	KEYSYS	KEYIBF	KEYOBF		
Default	0	0	0	0	0	0	0	0		
R/W	R	R	R	R	R	R	R	R		
	Bit Na 7 KE	ame EYPAR	Functio Keyboa	Function Keyboard Data Transmission Parity Error						
			 1 = Parity error occurred in the serial data transmission between the processor within the keyboard and the SCP 							
			There is providec can cont ÉlanSC4	no real SCP I for software trol this bit via 100 microcont	on-board the l compatibility p the Keyboard roller configur	ÉlanSC400 m purposes only I Status Regis ration index re	icrocontroller. SCP emulati ter Write Reg gister C5h.	This bit is on software ister at		
	6 KE	EYRTO	Keyboa 0 = No re	rd Data Rece	ive Time-out ^{ut}					
			1 = Rece A tra	eive time-out nsmission sta	irted by the ke	yboard did no	t complete.			
			There is providec can cont ÉlanSC4	no real SCP for software rol this bit via 400 microcont	on-board the l compatibility p the Keyboarc roller configur	ÉlanSC400 m ourposes only I Status Regis ation index re	icrocontroller. SCP emulati ter Write Reg gister C5h.	This bit is on software ister at		
	5 KE	ΕΥΤΤΟ	Transm When C output b an emula more de	it Time-out/M SC index C0h uffer full flay. ' ated keyboard tail.	louse Output [0] is set, this When CSC in time-out bit.	Buffer Full bit is a PC/2 r dex C0h[0] is See CSC inde	nouse-compa cleared, this b exes C0h and	tible mouse bit becomes C5h for		
			0 = No k avail	eyboard to S0 able	CP communica	ations time-ou	t or no mouse	e data		
			1 = Keyboard to SCP communications time-out or mouse data available							
			When Co indicates complete set/clear	onfiguration Ir s that a transn ed; the transm ed by AT SCI	ndex Register nission started nit byte was no P emulation so	C0h[0] = 0 (Tr d by the keybo ot clocked out oftware via a 0	ansmit Time-(ard was not p in the time lim CSC index reg	Out), this bit properly it. This bit is jister.		
			When C this bit is in the SC It is clea buffer us set/clear register of this re output b controlle	onfiguration Ir s automatically CP output buff red when AT sing the Output red automatica bit manipulation gister. When uffer. If bit 0 is or (SCP) response	ndex Register y set when AT er using the M SCP emulatio ut Buffer Exter ally by writing on by software bits 0 and 5 a s set and bit 5 onse data is in	C0h[0] = 1 (M SCP emulation louse Output I n software planded Register to CSC index e. This bit work re set, then m is cleared the the buffer.	louse Output on software pl Buffer Extende aces a byte in . In this mode registers, not is in conjunctio ouse device d in keyboard of	Buffer Full), aces a byte ed Register. the output , this bit is by a direct on with bit 0 ata is in the r command		
	4 KE	EYENB	Keyboa 0 = Pass	rd Password sword protecte	Protection S ed	tatus				
			1 = Not	protected						
			There is provided can confi configura	no real SCP for software rol this bit via ation index reg	on-board the l compatibility p the Keyboard gister C5h.	ÉlanSC400 m ourposes only I Status Regis	icrocontroller. SCP emulati ter Write Reg	This bit is on software ister at chip		

KEYCMD	Command/Data 0 = Between the keyboard command and data ports, the data port at direct mapped 60h that was last written to
	1 = Between the keyboard command and data ports, the command port at direct-mapped 64h that was last written to
KEYSYS	System Flag Bit In a PC/AT-compatible system, this bit reads back the state of the system flag bit (bit 2) of the SCP's command byte. This SCP command byte is stored in location 0 of the on-board SCP RAM of a normal PC/AT system. This bit would normally be cleared by the SCP upon system power-up (cold boot) and would remain that way until the system BIOS enabled the keyboard interface. At this time, the result of the SCP's on-board diagnostic would be written to the system flag bit (1 = pass, 0 = fail). Since BIOS must always enable the keyboard interface before the system flag bit can be set, BIOS would read this bit after a reset to know whether the reset was a cold reset, or if the reset was initiated by software.
	0 = A keyboard diagnostic pass indication has not been posted since SCP/ system cold power-up reset
	1 = A keyboard diagnostic pass has been posted since SCP/system cold power-up reset
	There is no real SCP or SCP RAM on-board the ÉlanSC400 microcontroller. This bit is provided for software compatibility purposes only. SCP emulation software can control this bit via the Keyboard Status Register Write Register at chip configuration index register C5h.
KEYIBF	Input Buffer Full (Keyboard Input Buffer Status) 0 = Buffer empty (SCP able to receive next command/data byte)
	1 = Buffer full (SCP has not read the last command/data byte)
KEYOBF	Output Buffer Full (Keyboard Output Buffer Status) 0 = SCP (System Control Processor) has no data available for the system
	1 = SCP has data available for read-back by the system
	When this bit is active, either the keyboard IRQ1 signal to the PIC (master 8259, Channel 1), or the mouse IRQ12 signal to the PIC (slave 8259, Channel 4) is automatically asserted based upon whether the data in the output buffer was from the keyboard or from the mouse. If bit 5 of this register has been defined to be mouse output buffer full, and bits 0 and 5 of this register are set, IRQ12 is being asserted to the slave PIC. If bit 5 is not defined to be mouse output buffer full, then when bit 0 is set IRQ1 is being asserted to the master PIC. Either IRQ1 or IRQ12 are cleared by reading port 60h.
	KEYSYS KEYIBF KEYOBF

Programming Notes

This port is typically inside the external processor that is used to implement the SCP (System Control Processor) on a PC/AT Compatible system. Although an entire SCP is not implemented on-board in this design, some SCP registers are available to support the ÉlanSC400 microcontroller's capability of SCP emulation using a matrix keyboard. This PC/AT SCP Emulation Support Register is only available to be read from this location when the ÉlanSC400 microcontroller's SCP emulation feature is enabled via CSC index register C1h[3–2].

Keyboard/Mouse Interface Command Register

I/O Address 0064h



Programming Notes

This port is typically inside the external processor that is used to implement the SCP (System Control Processor) on a PC/AT Compatible system. Although an entire SCP is not implemented on-board in this design, some SCP registers are available to support the ÉlanSC400 microcontroller's capability of SCP emulation using a matrix keyboard. This PC/AT SCP emulation support register is only available to be read from this location when the ÉlanSC400 microcontroller's SCP emulation feature is enabled via CSC index register C1h[3–2].

RTC/CMOS RAM Index Register



Programming Notes

Bit 7 of this register is the master NMI gate control in a typical PC/AT Compatible system. For various reason, this bit has been made to reside at CSC index 9Dh[2] on the ÉlanSC400 microcontroller. Compatibility issues are minimized since the ÉlanSC400 microcontroller does not support generation of either of the legacy NMI sources (channel check or parity error).
RTC/CMOS RAM Data Port

I/O Address 0071h



General Register



Programming Notes

In the original PC/AT, this register would have been DMA Channel 4 Page Register, but DMA Channel 4 was used for the cascade function, so this register was not used by the DMA subsystem. The I/O address 80h, however, was used to send BIOS Power-on Self Test (POST) codes to the ISA bus where a special card (port 80h card) could display the progress/error codes from BIOS. Because of this legacy use by BIOS, I/O writes to this internal ElanSC400 microcontroller register automatically go to the ISA bus as well as to an internal storage element for this register. I/O reads from port 80h come from the internal register only.

DMA Channel 2 Page Register

I/O Address 0081h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

DMA Channel 3 Page Register



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

DMA Channel 1 Page Register

I/O Address 0083h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

General Register



Programming Notes

Access to this register is not affected by the DMA disable bits in CSC index D0h.

General Register

I/O Address 0085h



Programming Notes

Access to this register is not affected by the DMA disable bits in CSC index D0h.

General Register

I/O Address 0086h



Programming Notes

Access to this register is not affected by the DMA disable bits in CSC index D0h.

DMA Channel 0 Page Register

I/O Address 0087h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

Access to this register is not affected by the DMA disable bits in CSC index D0h.

General Register



Programming Notes

Access to this register is not affected by the DMA disable bits in CSC index D0h.

DMA Channel 6 Page Register

I/O Address 0089h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

DMA Channel 7 Page Register



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

DMA Channel 5 Page Register

I/O Address 008Bh



Programming Notes

General Register



Programming Notes

Access to this register is not affected by the DMA disable bits in CSC index D0h.

General Register

I/O Address 008Dh



Programming Notes

Access to this register is not affected by the DMA disable bits in CSC index D0h.

General Register

I/O Address 008Eh



Programming Notes

Access to this register is not affected by the DMA disable bits in CSC index D0h.

General Register

I/O Address 008Fh



Programming Notes

This general register is slightly different from the other direct-mapped general registers. All I/O accesses to port 8Fh go to the internal register only. Therefore, no VL or ISA bus cycles are generated on I/O writes to this port.

System Control Port A Register (PS/2 Compatibility Port) I/O Address 0092h

	7		6	5	4	3	2	1	0
Bit				Rese	erved			AGA20	ACPURESET
Default	0 0			0	0	0	0	0	0
R/W								R/W	R/W
	Bit	Nar	ne	R/W	Function				
	7–2	Res	served		Reserved Software sho	uld write thes	e bits to 0.		
	1	AG	A20	R/W	Alternate A2 This bit can b CPU A20 sig SCP (System but much fas	0 Gate Contr be used to cau nal that was h o Control Proc ter:	ol ise the same istorically per essor) in a PO	type of maskii formed by an C/AT Compati	ng of the external ble system,
					0 = Deasserts this partic	s the forcing o ular control	f the propaga	tion of the A2	0 signal via
					1 = Forces th	e A20 signal t	o propagate		
					For software compatibility and other reasons, there are sev sources of GateA20 control. These controls are effectively together with the output of the OR gate driving the Enhance Am486 microprocessor A20M input. Therefore, A20 will proj if any of the independent sources are forcing A20 to propage				
	0	ACF	PURESET	R/W	Alternate CF Changing this signal. This we that was histor Control Procee faster. The 48 microcontrolle affected as a will remain set the BIOS as a reset.	PU Core Rese s bit from '0b' vill cause the s prically perform essor) in a PC 86 cache state er indexed or result of this at until softwar an indication t	et Control to '1b' will pul same type of 0 med by an ext AT Compatib e, SMBASE, a direct-mapper soft reset. Fol e clears it. Th hat port 92h v	se the CPU S CPU core reso ernal SCP (S ble system, bu and ElanSC40 d registers wil lowing the reso is feature can vas used to go	RESET et to occur ystem it much 0 I not be set, this bit be used by enerate the
					0 = Do not ge	enerate a soft	reset to the C	PU core	
					1 = Pulse the	SRESET CP	U signal		

Slave 8259 Interrupt Request Register

I/O Address 00A0h

	7		6	5	4	3	2	1	0	
Bit	IR15		IR14	IR13	IR12	IR11	IR10	IR9	IR8	
Default	х		х	х	х	х	х	х	х	
R/W	R		R	R	R	R	R	R	R	
	Bit	Na	me	Functio	n					
	7	IR1	5	Interrup 0 = IRQ	t Request 15 15 is not asse	rted				
				1 = IRQ	15 is asserted					
	6	IR1	4	Interrup 0 = IRQ	t Request 14 14 is not asse	rted				
				1 = IRQ	14 is asserted					
	5	IR1	3	Interrup 0 = IRQ	t Request 13 13 is not asse	rted				
				1 = IRQ	13 is asserted					
	4	4 IR12		Interrup 0 = IRQ	t Request 12 12 is not asse	rted				
				1 = IRQ	12 is asserted					
	3	IR1	1	Interrup 0 = IRQ	t Request 11 11 is not asse	rted				
				1 = IRQ ²	11 is asserted					
	2	2 IR10		Interrup 0 = IRQ	Interrupt Request 10 0 = IRQ10 is not asserted					
				1 = IRQ	10 is asserted					
	1	1 IR9		Interrup 0 = IRQ9	Interrupt Request 9 0 = IRQ9 is not asserted					
				1 = IRQ9	9 is asserted					
	0	IR	3	Interrup 0 = IRQ8	t Request 8 8 is not assert	ed				
				1 = IRQ8	8 is asserted					

Programming Notes

This register provides a real-time status of the IRQ inputs to the Slave 8259. It is accessed by first writing a value of 0Ah to port A0h followed by a read-back of port A0h.

Slave 8259 In-Service Register

I/O Address 00A0h

	7		6	5	4	3	2	1	0
Bit	IS15		IS14	IS13	IS12	IS11	IS10	IS9	IS8
Default	х		х	х	х	х	х	х	х
R/W	R		R	R	R	R	R	R	R
	Bit	Nar	me	Functio	n				
	7	IS1	5	IRQ15 I I 0 = IRQ	n- Service 15 is not being	g serviced			
				1 = IRQ	15 is being se	rviced			
	6	IS1	4	IRQ14 I I 0 = IRQ	n- Service 14 is not being	g serviced			
				1 = IRQ	14 is being se	rviced			
	5	IS1	3	IRQ13 l ı 0 = IRQ	n- Service 13 is not being	g serviced			
				1 = IRQ	13 is being se	rviced			
	4 IS12		2	IRQ12 In-Service 0 = IRQ12 is not being serviced					
	3 IS11			1 = IRQ12 is being serviced					
			IRQ11 l i 0 = IRQ	n- Service 11 is not being	g serviced				
				1 = IRQ	11 is being se	rviced			
	2 IS10		0	IRQ10 l i 0 = IRQ	n- Service 10 is not being	g serviced			
				1 = IRQ	10 is being se	rviced			
	1 IS9			IRQ9 In 0 = IRQ9	- Service 9 is not being	serviced			
				1 = IRQ	9 is being serv	viced			
	0	IS8		IRQ8 In 0 = IRQ8	- Service 8 is not being	serviced			
				1 = IRQ8	B is being serv	viced			

Programming Notes

The Slave In-Service Register (ISR) is accessed by writing a value of 0Bh to port A0h followed by a read-back from port A0h.

Slave 8259 Initialization Control Word 1 Register

I/O Address 00A0h

	7	6	5	4	3	2	1	0				
Bit	Reserved			SLCT_ICW1	LTIM	ADI	SNGL	IC4				
Default	х	x	x	х	х	х	х	x				
R/W		W		W	W	W	W	W				
	Bit	Name	Functio	Function								
	7–5	Reserved	Reserve Must all	ed be written to ().							
	4	SLCT_ICW1	Initializa Must be Initializa	ation Control written to 1 to tion Control W	Word 1 Sele access ICW1 ord 1).	ct │(D4 = 1 mea	ns the IOW to	port A0h is				
	3	LTIM	Level Ti 0 = Edge	riggered Inter e sensitive IRC	Q detection							
			1 = Leve	1 = Level sensitive IRQ detection								
	2	ADI	Address Has no e	Address Interval Has no effect when the 8259 is used in x86 mode:								
			0 = Inter	rupt vectors a	re separated	by 8 locations						
			1 = Inter	rupt vectors a	re separated	by 4 locations						
			In the Él internall	anSC400 mic y fixed to '1b'.	rocontroller de	esign, this PC	AT Compatib	le bit is				
	1 SNGL		Single 8 If this bit ICW4, if the expla	Single 8259 If this bit is set, the internal register pointer will skip ICW3 and point to ICW4, if ICW4 was selected to be programmed via bit 0 of this register. See the explanation for bit 0 of this register:								
			0 = Case	cade mode, IC	W3 will be ex	pected						
			1 = Sing	1 = Single 8259 in the system, ICW3 will not be expected								
	In the ÉlanSC400 microcontro internally fixed to '0b'.					rocontroller design, this PC/AT Compatible bit is						
	0	IC4	Initializa ICW4 is 1–4 are the inter machine A1. Eacl to the ne program circumst explicitly ICW4 is after ICV value for 0 = Initia	ation Control required. The programmed i nal ICW1 Reg and ICW1 Reg and ICW1 Reg and ICW regin time A1h is v ext internal ICV med, but ICW ances. This b programmed selected to be V3, and the Pl r it.	Word 4 8259's initiali n sequence. V ister to be wri ster pointer. S written to (follo W register. IC' 3 and ICW4 n it determines or whether a programmed C will expect	zation control Writing to port tten, and rese Slave ICW2–4 wing ICW1), W1 and ICW2 eed only be p whether ICW4 value of 00h I, the register software to pr eared by writi	word (ICW) F A0h with bit 4 ts the PIC's ir are program the register po must always rogrammed u is required to will serve for pointer will po ovide an initia	Registers = 1 causes internal state inter points be inder certain o be ICW4. If pint to ICW4 alization on Control				
			Word 1 = ICW	Word 1, ICW4 will not be expected by the PIC 1 = ICW4 is not cleared by this write to Initialization Control Word 1, and								
			softv	vare is expecte	ed to initialize							
			In the El	anSC400 mic	rocontroller, th	his bit is interr	ally fixed to '1	ID'.				

Programming Notes

I/O writes to port A0h access different slave PIC registers based on bits 4–3 of the data that is written. See the following table:

Bit 4	Bit 3	Register Accessed
0	0	OCW2
0	1	OCW3
1	х	ICW1

Slave 8259 Operation Control Word 2 Register

I/O Address 00A0h

	7		6	5	4	3	2	1	0		
Bit			R SL EOI		SLCT_ICW1	IS_OCW3		LS[2-0]			
Default	х		х	х	х	х	х	х	х		
R/W			W		W	W		W			
	Bit	Nam	ie	Functio	n Land Priority	Potation Co	atrols				
	7-5	сı		000 = F	Rotate in auto	EOI mode (cl	ear)				
		FOL		0 0 1 = 1	Non-specific E	OI					
		201		010=1	No operation						
				0 1 1 = 5	Specific EOI						
				1 0 0 = F	Rotate in auto	EOI mode (se	et)				
				101=F	Rotate on non-	-specific EOI	command				
				110=\$	Set priority cor	nmand					
				111=F	Rotate on spec	cific EOI comr	nand				
	4	SLC.	T_ICW1	Initializa Software	e should write	Word 1 Select this bit to 0 to	ect to access OCW2 or OCW3. hit set indicates that OCW3 is to be				
	3	IS_C	DCW3	Access An I/O w accesse	is OCW3 vrite to port A0 d.	h with this bit					
	2–0	LS[2	2-0]	Specific Interrupt below:	EOI Level Se level which is	elect acted upon v	vhen the SL b	it = '1b' (see t	oits 7–5]		
				0 0 0 = I	RQ8						
				0 0 1 = I	RQ9						
				0 1 0 = I	RQ10						
				0 1 1 = I	RQ11						
				1 0 0 = l	RQ12						
				1 0 1 = I	RQ13						
				1 1 0 = I	RQ14						
				111=1	RQ15						

Programming Notes

I/O writes to port A0h access different slave PIC registers based on bits 4–3 of the data that is written. See the following table:

Bit 4	Bit 3	Register Accessed
0	0	OCW2
0	1	OCW3
1	х	ICW1

Slave 8259 Operation Control Word 3 Register

I/O Address 00A0h

	7		6	5	4	3	2	1	0				
Bit	Reserv	ed	ES SM	MM MM	SLCT_ICW1 IS_OCW3 P RR RIS								
Default	х		Х	х	x	х	х	х	х				
R/W			١	N	W	W	W	W					
	Bit	Nai	me	Functio	Function								
	7	Res	served	Reserve Software	Reserved Software should write this bit to 0.								
	6–5	ESI SM	MM M	Special 0 x = No	Special Mask Mode 0 x = No operation								
				1 0 = Re	eset special m	ask							
				1 1 = Se	et special mas	k							
				In the Él '1b'.	anSC400 mici	rocontroller de	esign, the ESN	/M bit is interna	lly fixed to				
	4	SLO	CT_ICW1	Initializa Software	Initialization Control Word 1 Select Software must write this bit to 0 to access OCW2 or OCW3.								
	3	IS_	OCW3	Access An I/O v accesse	Access is OCW3 An I/O write to port A0h with this bit set indicates that OCW3 is to be accessed.								
	2	P D RR BIS		PIC Pol A system this case interrupt the PIC OCW3 v	PIC Poll Command A system design can choose to use the PIC in a non-interrupting mode. In this case, the interrupt controller can be polled for the status of pending interrupts. In order to support this PC/AT incompatible mode of operation, the PIC supports a special poll command which is invoked by writing OCW3 with this bit set.								
				0 = Not	poll command								
				1 = Poll	command								
	1–0			Status I 0 0 = No	Register Sele o change from	ct last state							
			-	0 1 = No	o change from	last state							
				1 0 = Ne	ext port A0h re	ad will return	Interrupt Req	uest Register (I	RR)				
				1 1 = Ne	ext port A0h re	ad will return	In-Service Re	gister (ISR)					

Programming Notes

I/O writes to port A0h access different slave PIC registers based on bits 4–3 of the data that is written. See the following table:

Bit 4	Bit 3	Register Accessed
0	0	OCW2
0	1	OCW3
1	x	ICW1

Slave 8259 Initialization Control Word 2 Register

I/O Address 00A1h

x	X	T7–T3 x W	x	x	x	A10–A8 x W	x
x	x	x W	X	X	x	x W	x
		W				W	
Bit Na 7–3 T7- 2–0 A11	t his PIC level. For exa PIC (IRQ0 ge nds to int 70h)	mple, these enerates int) in a PC/AT					
7- 2-	-3 T7· -0 A1	-3 T7–T3 -0 A10–A8	-3 T7–T3 Bits 7–3 Bits 2–0 bits will t 8), and 0 Compati -0 A10–A8 A10–A8 Software	 -3 T7–T3 Bits 7–3 of Base Inter Bits 2–0 are concaten bits will be programme 8), and 01110b for the Compatible system. -0 A10–A8 A10–A8 of Interrupt Software should write 	 -3 T7-T3 Bits 7-3 of Base Interrupt Vector Bits 2-0 are concatenated by PIC b bits will be programmed to 00001b 8), and 01110b for the slave PIC (IF Compatible system. -0 A10-A8 A10-A8 of Interrupt Vector Software should write these to 0 in a 	 -3 T7-T3 Bits 7-3 of Base Interrupt Vector Number for the Bits 2-0 are concatenated by PIC based on IRQ bits will be programmed to 00001b for the master 8), and 01110b for the slave PIC (IRQ8 correspondent Compatible system. -0 A10-A8 A10-A8 of Interrupt Vector Software should write these to 0 in a PC/AT-com 	 -3 T7-T3 Bits 7-3 of Base Interrupt Vector Number for this PIC Bits 2-0 are concatenated by PIC based on IRQ level. For exa bits will be programmed to 00001b for the master PIC (IRQ0 gr 8), and 01110b for the slave PIC (IRQ8 corresponds to int 70h) Compatible system. -0 A10-A8 A10-A8 of Interrupt Vector Software should write these to 0 in a PC/AT-compatible system

Slave 8259 Initialization Control Word 3 Register

I/O Address 00A1h



I/O Address 00A1h

	7	6	5	4	3	2	1	0
--	---	---	---	---	---	---	---	---

Slave 8259 Initialization Control Word 4 Register

			-	-		-			-			
Bit			Reserved		SFNM	BI M	JF /S	AEOI	PM			
Default	х		х	х	x	х	х	x	х			
R/W			W		W	۷	V	W	W			
	Bit 7–5	Na Re	me served	Functio Reserve	n ed	4h h 14 - 4 - 4						
	4	SF	NM	Software Special 0 = Norr 1 = Spec In the Él	Special Fully Nested Mode Enable 0 = Normal nested mode 1 = Special fully nested mode In the ÉlanSC400 microcontroller design, this PC/AT-compatible bit is							
	3–2	BU M/S	F S	Buffere 0 x = No 1 0 = Bu 1 1 = Bu In the Él	Buffered Mode and Master/Slave Select 0 x = Non buffered mode 1 0 = Buffered mode/slave 1 1 = Buffered mode/master In the ÉlanSC400 microcontroller, these PC/AT-compatible bits are internally fixed to '00b'.							
	1 AEOI			Automa 0 = Norn Inter 1 = Auto EOI CPU In the Él internally	tic EOI Mode nal EOI rupt handler n EOI is automatical anSC400 mic y fixed to '0b'.	nust send an I ly performed a rocontroller de	End of Interru	pt command to nd INTA signa /AT-compatibl	o the PIC(s) al from the le bit is			
	0	PN	1	Micropr 0 = 8080 1 = 8080 In the Él internall	ocessor Mod D/8085 mode 6 mode danSC400 mic y fixed to '1b'.	le rocontroller de	esign, this PC	/AT-compatib	le bit is			

Slave 8259 Interrupt Mask Register (also known as Operation Control Word 1)

I/O Address 00A1h

	7	6	5	4	3	2	1	0
Bit	IM15	IM14	IM13	IM12	IM11	IM10	IM9	IM8
Default	Х	х	Х	Х	Х	Х	Х	Х
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	IM15	IRQ15 Mask 0 = Unmask IRQ15
		1 = Mask IRQ15
6	IM14	IRQ14 Mask 0 = Unmask IRQ14
		1 = Mask IRQ14
5	IM13	IRQ13 Mask 0 = Unmask IRQ13
		1 = Mask IRQ13
4	IM12	IRQ12 Mask 0 = Unmask IRQ12
		1 = Mask IRQ12
3	IM11	IRQ11 Mask 0 = Unmask IRQ11
		1 = Mask IRQ11
2	IM10	IRQ10 Mask 0 = Unmask IRQ10
		1 = Mask IRQ10
1	IM9	IRQ9 Mask 0 = Unmask IRQ9
		1 = Mask IRQ9
0	IM8	IRQ8 Mask 0 = Unmask IRQ8
		1 = Mask IRQ8



I/O Address 00C0h



Master DMA Channel 4 Transfer Count Register

I/O Address 00C2h





I/O Address 00C4h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

Master DMA Channel 5 Transfer Count Register

I/O Address 00C6h





I/O Address 00C8h



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

Master DMA Channel 6 Transfer Count Register

I/O Address 00CAh





I/O Address 00CCh



Programming Notes

The ÉlanSC400 microcontroller is capable of performing 26-bit DMA accesses using the extended DMA page registers that reside in CSC index registers D9h and DAh.

Master DMA Channel 7 Transfer Count Register

I/O Address 00CEh


Master DMA Status Register for Channels 4-7

I/O Address 00D0h

	7		6	5	4	3	2	1	0			
Bit	DMAR	87	DMAR6	DMAR5	DMAR4	TC7	TC6	TC5	TC4			
Default	0		0	0	0	0	0	0	0			
R/W	R		R	R	R	R	R	R	R			
	Bit	Na	me	Functio	n							
	7	DN	IAR7	Channe 0 = Not p	I 7 DMA Requestion of the second seco	uest						
				1 = Peno	ding							
	6	DN	IAR6	Channe	I 6 DMA Requ	uest						
				0 = Not p	0 = Not pending							
				1 = Peno	1 = Pending							
	5 DMAR5			Channe 0 = Not p	I 5 DMA Requestion pending	uest						
				1 = Peno	ding							
	4	DN	IAR4	Channe 0 = Not p	Channel 4 DMA Request 0 = Not pending							
				1 = Pending								
	3	тс	7	Channe 0 = Not o	I 7 Terminal (detected	Count						
				1 = Dete	ected							
	2	тс	6	Channe 0 = Not o	I 6 Terminal (detected	Count						
				1 = Dete	ected							
	1	тс	5	Channel 5 Terminal Count 0 = Not detected								
				1 = Dete	ected							
	0 TC4			Channel 4 Terminal Count 0 = Not detected								
				1 = Dete	ected							

Programming Notes

Bits 3–0 of this register are read/reset. Any read from this direct mapped port clears all of these bits.

Master DMA Control Register for Channels 4-7

I/O Address 00D0h

	7		6	5	4	3	2	1	0			
Bit	DAKSE	ΞN	DRQSEN	WRTSEL	PRITYPE	COMPTIM	ENADMA	ADRHEN	MEM2MEM			
Default	0		0	0	0	0	0	0	0			
R/W	W		W	W	W	W	W	W	W			
	Bit	Na	me	Functio	n							
	7	DA	KSEN	DACK(n This bit o controlle) Sense controls the po r:	olarity of all \overline{D}	ACK outputs f	rom the maste	er DMA			
				0 = Asse	erted Low							
				1 = Asse	erted high							
				System I drive act system c	ogic ext <u>ernal</u> ive Low DAC operation.	to the DMA co K outputs. Thi	ontroller expension s bit must be	cts the DMA c written to '0b'	ontroller to for proper			
	6	DR	QSEN	DREQ(n This bit o controlle	DREQ(n) Sense This bit controls the polarity of all DREQ inputs to the master DMA controller:							
				0 = Asse	erted High							
				1 = Asserted Low								
		System logic external to the DMA controller expects the DMA controller to respond to active High DREQ inputs. This bit must be written to '0b' for proper system operation.							ontroller to 0 '0b' for			
	5	WF	RTSEL	Write Se 0 = Late	Write Selection Control 0 = Late write selection							
				1 = Exte	1 = Extended (early) write selection							
				Enabling violate th	this feature when the teature when the teature when the teature of teature	will result in tin cation.	ning changes	on the ISA bu	is that can			
	4	PR	ITYPE	Priority 0 = Fixed	Type d priority							
				1 = Rota	ting priority							
	3	CC	MPTIM	Compre 0 = Norn	ssed Timing nal timing							
				1 = Com	pressed timin	g						
				Enabling violate th	this feature v ne ISA specifi	vill result in tin cation.	ning changes	on the ISA bu	is that can			
	2	EN	ADMA	Enable DMA Controller 0 = Enabled								
				1 = DMA requests are ignored but DMA registers are available to the CPU								
				The DM/ prevent program DMA cor	A controller m unintended tra ming operatio ntroller is disa	ust be disable ansfers from o on. If an I/O DI ble via this bit	ed prior to prog occurring durin MA initiator as , abnormal sys	gramming it in ig the DMA co serts DREQ v stem operatio	order to ontroller vhile the n can occur.			

Bit	Name	Function
1	ADRHEN	Enable Channel 4 Address Hold Control (not supported) IF bit 0 = 1, then:
		0 = Disabled, Channel 0 memory address changes for each memory-to-memory transfer
		1 = Enabled, Channel 0 memory address does not change for each memory-to-memory transfer (not supported by the system)
		ELSE this bit does nothing.
		Since bit 0 should always be written to 0, this bit will be a don't care after the DMA controller has been initialized.
0	MEM2MEM	Enable Memory-to-Memory Transfer 0 = Disabled
		1 = Enabled (not supported by the system)
		Memory-to-memory DMA support is not provided in an AT compatible system. This bit should always be written to 0.

Master Software DRQ(n) Request Register

I/O Address 00D2h

	7	6	5	4	3	2	1	0		
Bit			Reserved			REQDMA REQSEL1 REQSEL0		QSEL1 QSEL0		
Default	0	0	0	0	0	0	0	0		
R/W						W		W		
	Bit	Name	Functio	n						
	7–3	Reserved	Reserved Software should write these bits to 0.							
	2	REQDMA	DMA Request 0 = Reset request bit for channel selected by bits 1–0							
			1 = Set request bit for channel selected by bits 1–0							
	1–0	REQSEL1	DMA CI	nannel Selec	t					
		REQSEL0	Bits 1–0 deasser	select which t a DMA requ	DMA channel est via softwa	will latch bit 2 re:	internally to	assert or		
		0 0 = Mask/unmask DMA Channel 4 mask per the REQDMA bit								
			0 1 = Ma	ask/unmask [MA Channel	5 mask per the	e REQDMA b	bit		
			1 0 = Ma	ask/unmask [MA Channel	6 mask per the	e REQDMA b	oit		
			1 1 = Ma	ask/unmask [MA Channel	7 mask per the	e REQDMA b	bit		

I/O Address 00D4h

Master DMA Mask Register Channels 4-7



Programming Notes

The same DMA channel masks can be controlled via DMA registers D4h, DCh, and DEh.

Master DMA Mode Register Channels 4-7

I/O Address 00D6h

	7 6 5 4 3 2				2	1	0				
Bit		TRNMOD	ADDDEC	AINIT	OPS OPS	EL1 EL0	MOD MOD	SEL1 SEL0			
Default	?	?	?	?	?	?	?	?			
R/W		W	W	W	V	V	V	V			
	Bit	Namo	Function	n							
	7.6		Transfor	n Modo							
	7-0	TRINIVIOD	0.0 = De	mand transfe	r mode						
			0 1 = Sir	ngle transfer n	node						
			1 0 = Blc	ock transfer m	ode						
			1 1 = Ca	scade mode							
	5	ADDDEC	DMA Ad 0 = Incre	Idress Mode ement the DM	Decrement A memory address after each transfer						
			1 = Decr	ement the DM	IA memory ad						
	4	AINIT	Automatic Initialization Control If enabled, the base address and transfer count registers are restored to the values they contained prior to performing the last DMA transfer. The channel selected by bits 0–1 of this register is then ready to perform another DMA transfer without processor intervention as soon as the next DRQ is detected.								
			0 = Auto	0 = Auto initialization disabled							
			1 = Auto initialization enabled								
	3–2	OPSEL1 OPSEL0	Operatio 0 0 = Ver DN cor	Operation Select 0 0 = Verify mode DMA controller acts normally except that no I/O or memory commands are generated, and no data is transferred							
			0 1 =Wr Da me	ite transfer ta will be trans mory	sferred from a	DMA-capabl	e I/O device ir	ito system			
			1 0 = Rea Da dev	ad transfer ta will be trans vice	sferred from s	ystem memoi	y to a DMA-ca	apable I/O			
			1 1 = Re	served							
	1–0	MODSEL1 MODSEL0	DMA Ch Bits 7–2 determin D6h as f	DMA Channel Select Bits 7–2 of this register are latched internally for each channel. Bits 0–1 determine which of the channels will be programmed by the write to port D6h as follows:							
			0 0 = Se	lect Channel	4						
			0 1 = Se	lect Channel	5						
			1 0 = Se	lect Channel (6						
			1 1 = Se	lect Channel	7						

Master DMA Clear Byte Pointer Register

I/O Address 00D8h



Master DMA Controller Reset Register

I/O Address 00DAh



Master DMA Controller Temporary Register

I/O Address 00DAh



Master DMA Reset Mask Register



Programming Notes

The same DMA channel masks can be controlled via DMA registers D4h, DCh, and DEh.

Master DMA General Mask Register

I/O Address 00DEh

	7		6	5	4	3	2	1	0	
Bit			Rese	erved		DIS7	DIS6	DIS5	DIS4	
Default	0		0	0	0	1	1	1	1	
R/W						W	W	W	W	
	Bit	Nam	ne	Functio	n					
	7–4	Rese	erved	Reserve Software	ed e should write	these bits to ().			
	3	DIS7	7	Disable 0 = Enal	DMA Channe ole DMA Char	el 7 Mask nnel 7 for serv	icing DMA red	quests		
	1 = Disable DMA Channel 7 from servicing DMA requests									
	2	DIS	6	Disable 0 = Enal	Disable DMA Channel 6 Mask 0 = Enable DMA Channel 6 for servicing DMA requests					
				1 = Disa	ble DMA Cha	MA Channel 6 from servicing DMA requests				
	1	DIS	5	Disable 0 = Enal	DMA Channe ole DMA Char	el 5 Mask nnel 5 for serv	icing DMA red	quests		
				1 = Disa	ble DMA Cha	nnel 5 from se	ervicing DMA	requests		
	0 DIS4 Disable DMA Channel 4 Mask 0 = Enable DMA Channel 4 for servicing DMA requests, also enables DMA cascading to the slave DMA controller on this channel									
				1 = Disa DMA	ble DMA Chai cascading to	nnel 4 from se the slave DM	rvicing DMA A controller o	requests, also In this channe	enables	

Programming Notes

The same DMA channel masks can be controlled via DMA registers D4h, DCh, and DEh.

Alternate Gate A20 Control Port



Programming Notes

Bits 7–0: For software compatibility and other reasons, there are several sources of GateA20 control. These controls are effectively ORed together with the output of the OR gate driving the Enhanced Am486 microprocessor A20M pin. Therefore, A20 will propagate if ANY of the independent sources are forcing A20 to propagate.

Alternate CPU Reset Control Port

I/O Address 00EFh



Parallel Port 2 Data Register



Programming Notes

There is only one parallel port on the ÉlanSC400 microcontroller, but it can be configured to have a base address of either 378h or 278h (LPT1/LPT2).

Parallel Port 2 Status Register (PC/AT Compatible Mode) I/O Address 0279h

	7		6	5	4	3	2	1	0		
Bit	BUS	Y	ACK	PE	SLCT	ERROR		Reserved			
Default	-		I	-	-	-	-	-	_		
R/W	R		R	R	R	R					
	Bit	Na	me	Functio	n						
	7	BU	SY	Printer I This bit i	Busy is the inverse	of the (BUSY/	WAIT) pin (ac	tive Low):			
				0 = Print	ter busy						
				1 = Print	ter is ready						
	6	AC	К	Printer Acknowledge The printer pulses this line Low when it has received a byte of data. This bi follows the state of the ACK pin (active Low):							
				0 = Print	ter acknowled	ge					
				1 = No p	orinter acknow	/ledge					
	5	PE		Paper E This bit f	nd follows the sta	ate of the PE p	oin:				
				0 = Printer has paper							
				1 = Pape	er end (out of	paper)					
	4	SL	СТ	Printer S This bit f	Selected follows the sta	ate of the SLC	T pin:				
				0 = Print	ter not selecte	ed					
	1 = Printer selected										
	3	ER	ROR	Printer I This bit f	Error follows the sta	ate of ERROR	pin (active Lo	ow):			
				0 = Print	ter error						
				1 = No p	orinter error						
	2–0	Re	served	Reserved							

Programming Notes

The default value for this register depends on the mode. For PC/AT Compatible mode, the default value for this register is ????xxxb. For EPP mode, the default value is ????xxxb.

Parallel Port 2 Status Register (Bidirectional Mode)

I/O Address 0279h

	7		6	5	4	3	2	1	0			
Bit	BUSY	Y	ACK	PE	SLCT	ERROR		Reserved				
Default	-		-	-	-	-	-	-	-			
R/W	R		R	R	R	R						
	Bit	Na	me	Functio	n							
	7	BU	ISY	Printer I This bit i	Busy is the inverse	of the (BUSY/	WAIT) pin (ac	tive Low):				
				0 = Print	ter busy							
				1 = Print	er ready							
	6	AC	K	Printer The prin follows t	Acknowledge ter pulses this he state of the	e line Low whe ACK pin (act	n it has receiv tive Low):	ed a byte of da	ata. This bit			
				0 = Print	ter acknowled	ge						
				1 = No p	orinter acknow	ledge						
	5	PE		Paper End This bit follows the state of the PE pin:								
				0 = Print	0 = Printer has paper							
				1 = Pape	er end (out of	paper)						
	4	SL	СТ	Printer S This bit f	Selected follows the sta	ite of the SLC	T pin:					
				0 = Print	ter not selecte	d						
				1 = Print	ter selected							
	3 ERROR			Printer Error This bit follows the state of ERROR pin (active Low):								
				0 = Printer error								
				1 = No printer error								
	2–0 Reserved			Reserve	ed							

Programming Notes

The default value for this register depends on the mode. For PC/AT Compatible mode, the default value for this register is ????xxxb. For EPP mode, the default value is ????xxxb.

Parallel Port 2 Status Register (EPP Mode)

I/O Address 0279h

	7		6	5	4	3	2	1	0			
Bit	BUS	Y	ACK	PE	SLCT	ERROR	Rese	erved	EPP_TIMEO			
Default	0		0	0	0	0	0	0	0			
R/W	R		R	R	R	R			R			
	Bit	Na	me	Functio	n							
	7	BU	SY	Printer I This bit i	Busy s the inverse	of the (BUSY/	WAIT) pin (ad	tive Low):				
				0 = Print	er busy							
				1 = Print	er ready							
	6	AC	К	Printer The prin follows t	Acknowledge ter pulses this he state of the	e s l <u>ine L</u> ow whe e ACK pin (act	n it has receiv ive Low):	red a byte of c	lata. This bit			
				0 = Print	er acknowled	ge						
				1 = No p	rinter acknow	nowledge						
	5	PE Paper End This bit follows the state of the PE pin:										
				0 = Print	er has paper							
				1 = Pape	er end (out of	paper)						
	4	SL	СТ	Printer : This bit f	Selected follows the sta	ate of the SLC	T pin:					
				0 = Print	er not selecte	ed						
				1 = Print	er selected							
	3	ER	ROR	Printer I This bit f	Error follows the sta	ate of ERROR	pin (active Lo	ow):				
				0 = Print	er error							
				1 = No p	orinter error							
	2–1	Re	served	Reserve	ed							
	0 EPP_TIMEO EPP Time-out Status 0 = No time-out											
				1 = EPP	1 = EPP cycle time-out occurred							
	This bit is set if a time-out occurred only when EPP mode is enabled (bits 1–0 of the Parallel Port Configuration Register in the CSC indexed address space) = '01b'. This bit is reset when either the status register is read, or when EPP mode is enabled. An EPP time-out occurs when the BUSY pin remains inactive (low) for greater than 10s after either SLCTIN or AFDT go active Low in EPP mode.						abled (bits ked address s read, or BUSY pin or AFDT go					

Parallel Port 2 Control Register

	7	6	5	4	3	2	1	0			
Bit		Reserved	DIR	IRQEN	SLCTIN	INIT	AUTOFDXT	STROBE			
Default	0	0	0	0	0	0	0	0			
R/W			R/W	R/W	R/W	R/W	R/W	R/W			
	5:	Nama	Frenchis	_							
	Bit	Name	Functio	n							
	7–6	Reserved	Reserve Software	ed e should write	these bits to ().					
	5	DIR	Bidirect When th mode, th a paralle mode is	ional Parallel e parallel port his bit controls el port data wri selected:	I Port Data Di is set to oper the data direc ite operation v	i rection ate in either B ction between vhere either B	idirectional m host and peri idirectional m	ode or EPP pheral. For ode or EPP			
			0 = Data	written to PD	7–PD0						
			1 = Data	written is late	hed only						
			For a pa EPP mo	rallel port data de is selected	a read operati :	on where eith	er Bidirectiona	al mode or			
			0 = Inter	nal data regis	ter read						
			1 = Data	read from PD	07–PD0						
			This bit is undefined when neither Bidirectional mode nor EPP mode selected.								
	4	IRQEN	Printer I Clearing	RQ Enable this bit clears	any pending	interrupts:					
			0 = Disable printer IRQ								
			1 = Enable printer IRQ								
	3	SLCTIN	Select P This bit i	Printer Signal s the inverse	Control of the SLCTIN	I pin.					
			0 = The	SLCTIN pin is	a logic 1						
			1 = The	SLCTIN pin a	logic 0						
	2	INIT	Printer I 0 = Hold	Reset Signal	Control et						
			1 = Rele	ase printer fro	om reset, this l	bit follows the	INIT pin (activ	ve Low)			
	1	AUTOFDXT	Auto Lir This bit i	ne Feed Sign s the inverse	al Control of the AFDT p	in:					
			0 = AFDT pin is a logic 1								
			 1 = AFDT pin is a logic 0 When connected to a printer, setting this bit causes the printer to automatically insert a line feed when it sees a carriage return (ASCII 13) character. 								
	0	STROBE	Printer I This bit i	Port Strobe S s the inverse	ignal <u>Contr</u>o of the STRB p	l pin:					
			0 = <u>STR</u>	B pin not activ	/e						
			1 = <u>STR</u>	B pin active							



I/O Address 027Bh



Parallel Port 2 EPP 32-bit Data Register

I/O Address 027C-027Fh



Programming Notes

Bits 31–0: A 16-bit I/O write to 27Ch will cause two back-to-back 8-bit bus cycles to occur to the EPP Data Registers 27Ch and 27Dh. Two bytes of data will be presented to the parallel port data lines in succession starting with the data written to 27Ch. An EPP data strobe will be automatically generated for each of the bus cycles.

An 8-bit I/O write to 27Ch will cause a single 8-bit bus cycle to occur to the EPP Data Register at 27Ch. The single byte of data will be presented to the parallel port data lines along with an automatically generated EPP data strobe.

In common practice, all write accesses to the parallel port 2 EPP Data Register (x8, x16, or x32 I/ O instructions) should be directed to port 27Ch.



I/O Address 02F8h



Programming Notes

There is only one serial port on the ÉlanSC400 microcontroller, but it can be configured to have a base address of either 3F8h or 2F8h (COM1/COM2).

COM2 Receive Buffer Register

I/O Address 02F8h





I/O Address 02F8h



COM2 Baud Clock Divisor Latch MSB

I/O Address 02F9h



COM2 Interrupt Enable Register

I/O Address 02F9h

	7		6	5	4	3	2	1	0		
Bit			Res	erved		EMSI	ERLSI	ETHREI	ERDAI		
Default	0		0	0	0	0	0	0	0		
R/W						R/W	R/W	R/W	R/W		
	Bit	Nam	e	Functio	on						
	7–4	Rese	erved	Reserv Softwar	r ed re should write	these bits to ().				
	3	EMS	51	Enable 0 = Dis	Modem Statu able modem st	is Interrupt atus interrupt					
				1 = Ena	atus interrupt						
	2	ERL	SI	Enable 0 = Dis	Enable Receiver Line Status Interrupt 0 = Disable receiver line status interrupt						
				1 = Ena	able receiver lir	ne status inter	rupt				
	1	ETH	REI	Enable 0 = Dis	Enable Transmitter Holding Register Empty Interrupt 0 = Disable transmitter holding register empty interrupt						
				1 = Ena	able transmitter	[,] holding regis	ter empty inte	errupt			
	0	0 ERDAI Enable Received Data Available Interrupt 0 = Disable data available interrupt in 16450-compatible mode; in 16550-compatible mode, this bit also disables time-out interrupts									
				1 = Ena 165	ble received d 50-compatible	ata available i mode, this bit	nterrupt in 16 also enables	450-compatibl time-out inter	le mode; in rupts		
				More de Registe	etail on time-ou er (I/O address	it interrupts ca 2FAh/3FAh) o	n be found in description.	the Interrupt lo	dentification		

COM2 Interrupt ID Register

I/O Address 02FAh

	7	6	5	4	3	2	1	0
Bit	FIFO1 FIFO0		Reserved		ID2 ID1 ID0			IP
Default	0	0	0	0	1	1	1	1
R/W		3				R		R

Bit	Name	Function	Priority	
7–6	FIFO1 FIFO0	FIFO Feature Presence Indication FIFO is only present when 16550-compatible mode is enabled):		
		0 0 = No significance		
		0 1 = No significance		
		1 0 = 16450-compatible mode is enabled		
		1 1 = 16550-compatible mode is enabled		
5–4	Reserved	Reserved These bits always read back '00b'.		
3–1	ID2 ID1	Interrupt Identification Bit Field 0 0 0 = Modem status	Fourth (Lowest)	
	ID0	0 0 1 = Transmitter Holding Register Empty/Transmit FIFO Empty (16550-compatible mode)		
		0 1 0 = Received Data Available/Receiver FIFO trigger (16550-compatible mode)	Second	
		0 1 1 = Receive Line Status	First (Highest)	
		1 0 0 = Not used		
		1 0 1 = Not used		
		1 1 0 = FIFO time-out	Second	
		1 1 1 = Not used		
		In 16450-compatible mode, bit 3 always reads back '0b'. See the Modem Status Register (MSR) and Line Status Register (LSR) for more detail on interrupt events.		
		If two interrupt sources are pending simultaneously, only the highest priority interrupt (as defined by the rightmost column for bits $3-1$) will be indicated by bits 3-1 of the Interrupt Identification Register (IIR). When the interrupt source is cleared, a subsequent read from the Interrupt Identification Register (IIR) will return the next highest priority interrupt source. Bits $3-1$ have no meaning if bit $0 = '1b'$.		
		A FIFO time-out occurs when the receive FIFO is not empty, and more than four continuous character-times have transpired without more data being placed into or read out of the receive FIFO. Reading a character from the receive FIFO clears the time-out interrupt.		

Bit	Name	Function	Priority
0	IP	Serial Port Interrupt Pending (Active Low) 0 = Interrupt pending	
		1 = No interrupt pending	

COM2 FIFO Control Register

I/O Address 02FAh

	7	6	5	4	3	2	1	0		
Bit	RFRT[1–0]		Res	erved	Reserved	TFCLR	RFCLR	FIFOEN		
Default	0	0	0	0	0	0	0	0		
R/W		W			W	W	W	W		
	Di4	Nomo	D M	Function						
	BIT		R/W							
	7-6	KFK1[1–0]	vv	When in 16550-compatible mode, this bit field specifies the trigger level at which the Interrupt Identification Register will report that a received data available interrupt is pending. If received data available interrupts are enabled in the IER, the system will be interrupted when the receive FIFO fills to the trigger level per the following table:						
				0 0 = 1 byte						
				0.1 = 4 bytes						
				1 0 = 8 bytes						
				11 = 14 byte	S					
				the interrupt will be cleared.						
	5–4	Reserved		Reserved Software should write these bits to 0.						
	3	Reserved	W	Reserved Software should write this bit to 1.						
	2	TFCLR	W	Transmitter Writing a '1b' resets the tra Transmitter S the Interrupt Register.	FIFO Buffer (to this bit pos nsmit FIFO co Shift Register. ID Register, o	Clear sition clears th bunter logic. If This bit is cle r by a write to	e transmit FIF does not clea ared by either the Transmit	O and ar the a read of Holding		
	1	RFCLR	W	Receiver FIFO Buffer Clear Writing a '1b' to this bit position clears the receive FIFO and the receive FIFO counter logic. It does not clear the Receiv Register. This bit is self-clearing, and does not need to be 0 under software control.						
	0	FIFOEN	W	 W FIFO Enable (16550-Compatible Mode Enable) 0 = Causes UART to enter 16450-compatible mode Disables accesses to receive and transmit FIFO control bits, except this bit. 						
				1 = Causes L Enables r other FIF	JART to enter eceive and tra O control bits.	16550-compa ansmit FIFOs	atible mode and enables a	accesses to		
				The main difference between a 16450-compatible mode and 16550-compatible mode is the addition of transmit and receive FIFOs in the 16550-compatible mode						
				This bit must written to or t clear both FII interface to o	be '1b' when hey will not be FOs. The FIF(perate in High	other FIFO co e programmed Os must be er h-Speed IrDA	ontrol register d. Any mode s nabled for the mode.	bits are witch will IrDA		

Programming Notes

The contents of this write-only register can be read back via the Chip Setup and Control (CSC) indexed register D3h. The on-board UART can be mapped to only one of COM1 or COM2 at any time, and the Shadow register at CSC index D3h serves either configuration.

COM2 Line Control Register

I/O Address 02FBh

	7		6	5	4	3	2	1	0				
Bit	DLAB		SB	SP	EPS	PE	STP	WLB WLB	0 1				
Default	0		0	0	0	0	0	0	0				
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	1				
	BitName7DLAB6SB			Function Divisor L Set this bi Clear this	Function Divisor Latch Access Bit Set this bit to gain access to the baud rate divisor latches for this COM port. Clear this bit to mux in the Transmit Holding Register and Receive Buffer								
				Register a Set Breal Setting th UART.	Register at port XF8h, and the Interrupt Enable Register at port XF9h. Set Break Enable Setting this bit causes a break condition to be transmitted to the receiving UART.								
				0 = Disabi 1 = Force transn	 0 = Disable set break 1 = Force serial output to spacing state (logic '0') regardless of other transmitter activity 								
				The break transmitte	The break control acts on the SOUT pin only and has no other effect on the transmitter logic.								
	5 SP			Stick Par Forces the that there bit is 0, th the parity = 0, the p	Stick Parity Enable Forces the parity bit to always be 0 or 1 versus dynamically changing it so that there are an odd or even number of 1 bits in the transmitted data. If this bit is 0, then normal parity is used if parity is enabled. If bits 5,4, and $3 = 1$, the parity bit is generated/checked as a logical 1. If bits 5 and $3 = 1$ and bit $4 = 0$, the parity bit is generated/checked as a logical 0.								
	4	EP	S	Even Par Parity mu	Even Parity Select Parity must be enabled via bit 3 for this bit to have meaning:								
				0 = Odd p The pa transn receiv 1 = Even p The pa transn	 0 = Odd parity The parity bit will be manipulated to force an odd number of 1 bits in the transmitted data and the same condition will be checked for in the received data. 1 = Even parity The parity bit will be manipulated to force an even number of 1 bits in the transmitted data and the same condition will be checked for in the 								
				receiv Start/stop	ed data. bits are not ir	ncluded in the	narity genera	tion/checking s	cheme				
	3	PE		Asynchro Causes a checked i word bit a	Asynchronous Data Parity Enable Causes a parity bit to be generated in the transmitted data and to be checked in the received data. The parity bit is located between the last data word bit and the first stop bit in the bit stream.								
	2	ST	Ρ	Stop Bits Based on	Stop Bits Based on character length from bits 1–0 above.								
				If characte	er length = 5:								
				0 = 1 stop	bit								
				1 = 1.5 st	op bits								
				If characte	If character length = 6, 7, or 8:								
				0 = 1 stop	bit								
				1 = 2 stop	bits								
	1–0	WL	.B0 B1	Transmit 0 0 = 5 bit	/Receive Cha ts	aracter Lengt	h						
		۷۷L	ו ש.	0 1 = 6 bit	ts								
				1 0 = 7 bit	ts								
				1 1 = 8 bit	11 = 8 bits								

COM2 Modem Control Register

	7		6	5	4	3	2	1	0			
Bit			Reserved		LOOP	OUT2	OUT1	RTS	DTR			
Default	0		0	0	0	0	0	0	0			
R/W					R/W	R/W	R/W	R/W	R/W			
	Bit	Na	me	Functio	n							
	7–5	ке	served	Software	e should write	these bits to (Э.					
	4	LO	OP	Loopba 1 = Enat The bit: RTS DTR OUT OUT	Loopback (Diagnostic Mode) Enable 1 = Enabled The following internal connections are made by setting this diagnosti bit: RTS is internally connected to CTS DTR is internally connected to DSR OUT1 is internally connected to RI OUT2 is internally connected to DCD							
				0 = Loop	back mode is	disabled						
				In addition, the SOUT bit is driven High, and the SIN input line is blocked. The Transmit Shift Out Register is directly connected to the receive shift in register. In addition, the DTR, RTS, OUT1 and OUT2 signals are forced inactive. Modem control interrupts can be forced by enabling the appropriate bit in the IER, and asserting one of the bits 3–0 in loopback mode								
	3	OL	IT2	Enable This bit COM2 ir Program	Enable COM2 Interrupts This bit controls the OUT2 signal which is used as a master enable for COM2 interrupts. If this bit is not set, no COM port 2 IRQs will be felt at the Programmable Interrupt Controller (PIC).							
	2	OL	IT1	OUT1 C This bit of for PC/A diagnost be used	OUT1 Control This bit controls the OUT1 signal which is not tied to anything. It is provided for PC/AT compatibility and can be used as part of the loopback diagnostics. Other than that, it has no effect on system operation and can be used as a scratch pad during normal system operation.							
	1 RTS			Reques 0 = Deas	Request to Send $0 = Deassert the Request To Send signal (\overline{RTS})$							
			_	1 = Asse	ert the Reques	st To Send sig	inal (RTS)					
	0	DT	R	Data Te 0 = Deas 1 - Assa	Data Terminal Ready 0 = Deassert the Data Terminal Ready signal (DTR)							
				. = 7.330				,				

COM2 Line Status Register

I/O Address 02FDh

	7	6	5	4	3	2	1	0			
Bit	16550_ERR	TEMT	THRE	BI	FE	PE	OE	DR			
Default	0	1	1	0	0	0	0	0			
R/W	R	R	R	R	R	R		R			
	Bit Na 7 16	i me 550_ERR	Function 16550-M In 16450 In 16550 parity en This bit i subsequ	Function 16550-Mode Error In 16450-compatible mode, this bit reads back '0b'. In 16550-compatible mode, when this bit is set it indicates at least one parity error, framing error, or break condition is present in the receive FIFO. This bit is cleared by a read from the Line Status Register if there are no							
	6 TEMT Transmitter Empty Indicator In 16450-compatible mode, this bit is set when both the Transmit Hol Register and the Transmit Shift Register are empty.										
	5 TH	IRE	E Transmitter Holding Register (16450-Compatible Mode) or Transmit								
			In 16450 Register by a writ mode. In 16550 complete cleared Identifica if progra	In 16450-compatible mode, this bit indicates that the Transmit Holding Register is ready to accept a new character. This bit is automatically reset by a write to the Transmit Holding Register when in 16450-compatible mode. In 16550-compatible mode, this bit indicates that the transmit FIFO is completely empty. When in 16550-compatible mode, this interrupt will be cleared when either the transmit FIFO is written to, or when the Interrupt Identification Register is read. This bit can be used to generate an interrupt if programmed to do so via the Interrupt Enable Register							
	4 BI		Break Indicator In 16450-compatible mode, this bit is set when the UART detects that the sending UART is transmitting a break condition for a period longer than the time it takes to receive start, data, parity, and stop bits.								
			In 16550-compatible mode, this bit is set when an entire word (start, data, parity, stop) that has been received with break indication present into the receive FIFO is at the top of the FIFO. Only one break indication will be loaded into the FIFO regardless of the duration of the break condition. A new character will not be loaded into the FIFO until the next valid start bit is detected. This latched status bit is automatically cleared by a read from the Line Status Register.								
	3 FE		Framing Error In 16450-compatible mode, this bit is set to indicate that a received character did not have a valid stop bit.								
			In 16550-compatible mode, this bit is set when a character that has been received with a framing error into the receive FIFO is at the top of the FIFO. This latched status bit is automatically cleared by a read from the Line Status Register.								
	2 PE		Parity E In 16450 parity.	Parity Error In 16450-compatible mode, this bit is set upon receipt of data with incorrect parity.							
			In 16550 received latched s Register)-compatible n with bad pari status bit is au	node, this bit i ty into the rece tomatically clo	s set when a eive FIFO is a eared by a rea	character that t the top of the ad from the Li	has been FIFO. This ne Status			

Bit	Name	Function
1	OE	Overrun Error In 16450-compatible mode, this bit is set if a new character is received into the receiver buffer before a previous character was read, thus resulting in lost data.
		In 16550-compatible mode, this bit is set if a new character is completely received into the Shift Register when the FIFO is already 100% full. Data in the FIFO is not overwritten by this overrun. The data in the Shift Register will be lost when the next character is received. This latched status bit is automatically cleared by a read from the Line Status Register.
0	DR	Data Ready In 16450-compatible mode, when this bit is set, a character has been received and placed in the Receiver Buffer Register. This bit is automatically cleared by reading the Receiver Buffer Register.
		In 16550-compatible mode, when this bit is set, a character has been received and placed in the receive FIFO. This bit is automatically cleared by reading the Receiver FIFO.

Programming Notes

When a receiver line status interrupt is enabled and detected, bits 1 through 4 above will indicate the reason for the interrupt. The status bits are valid even when the receiver line status interrupt is not enabled.

COM2 Modem Status Register

I/O Address 02FEh

	7		6	5	4	3	2	1	0				
Bit	DCD		RI	DSR	стѕ	DDCD	TERI	DDSR	DCTS				
Default	x		х	х	х	0	0	0	0				
R/W	R		R	R	R	R	R	R	R				
	Bit 7	Na DC RI	me :D	Functio Data Ca 0 =DCD 1 = DCD If in I Ring Inc	Function Data Carrier Detect 0 =DCD input signal is deasserted 1 = DCD input signal is asserted If in loopback mode, this bit tracks bit 3 of the Modem Control Register. Ring Indicator								
	5	DS	R	0 =RI inj 1 = RI in If in I Data Se 0 =DSR 1 = DSR	 0 =RI input signal is deasserted 1 = RI input signal is asserted If in loopback mode, this bit tracks bit 2 of the Modem Control Register. Data Set Ready 0 =DSR input signal is deasserted 1 = DSR input signal is asserted 								
	4	СТ	S	If in loopback mode, this bit tracks bit 0 of the Modem Control Register. Clear To Send 0 =CTS input signal is deasserted 1 = CTS input signal is asserted If in loopback mode, this bit tracks bit 1 of the Modem Control Register.									
	3	DD	CD	 Delta Data Carrier Detect 0 = Indicates that the DCD signal has not changed since the Modem Stat Register was last read 1 = Indicates that the DCD signal changed since the Modem Status 									
	2	TE	RI	Trailing 0 = Indic inact 1 = Indic since	 Trailing Edge Ring Indicator 0 = Indicates that the RI signal has not changed from an active to an inactive state since the Modem Status Register was last read 1 = Indicates that the RI signal changed from an active to an inactive state since the Modem Status Register (MSR) was last read 								
	1	DD	PSR	Delta Da 0 = Indic Regi 1 = Indic	 Delta Data Set Ready 0 = Indicates that the DSR signal has not changed since the Modem Status Register was last read 1 = Indicates that the DSR signal changed since the Modem Status 								
	0	DC	TS	Delta Cl 0 = Indic Regi 1 = Indic Regi	 Delta Clear To Send 0 = Indicates that the CTS signal has not changed since the Modem Status Register was last read 1 = Indicates that the CTS signal changed since the Modem Status Register (MSR) was last read 								

Programming Notes

Bits 7-4: Real-time status indicators for the indicated inputs to the UART.

Bits 3–0: Latched status bits that will generate an interrupt if modem status interrupts are unmasked in the Interrupt Enable Register (IER). Reading the Modem Status Register (MSR) clears these bits and their associated interrupt.

COM2 Scratch Pad Register

I/O Address 02FFh



Parallel Port 1 Data Register

I/O Address 0378h



Programming Notes

There is only one parallel port on the ÉlanSC400 microcontroller, but it can be configured to have a base address of either 378h or 278h (LPT1/LPT2).

Parallel Port 1 Status Register (PC/AT Compatible Mode) I/O Address 0379h

	7		6	5	4	3	2	1	0				
Bit	BUSY		ACK	PE	SLCT	ERROR Reserved		Reserved					
Default	0		0	0	0	0	0	0	0				
R/W	R		R	R	R	R							
	Bit Name Function												
	7 BUSY Printer Busy This bit is the inverse of the (BUSY/WAIT) pin (active Low):												
				0 = Print	0 = Printer busy								
				1 = Print	1 = Printer ready								
	6 ACK		ĸ	Printer Acknowledge The printer pulses this line Low when it has received a byte of data. This bit follows the state of the ACK pin (active Low):									
				0 = Printer acknowledge									
				1 = No printer acknowledge									
	5 PE			Paper End This bit follows the state of the PE pin:									
				0 = Printer has paper									
				1 = Pape	er end (out of	paper)							
	4	SL	СТ	Printer S This bit f	Printer Selected This bit follows the state of the SLCT pin:								
				0 = Printer not selected									
				1 = Print	er selected								
	3 EF		ROR	Printer I This bit f	Printer Error This bit follows the state of ERROR pin (active Low):								
				0 = Print	er error								
				1 = No p	orinter error								
	2–0	Re	served	Reserve	ed								
Parallel Port 1 Status Register (Bidirectional Mode)

I/O Address 0379h

	7		6	5	4	3	2	1	0		
Bit	BUS	Y	ACK	PE	SLCT	ERROR		Reserved			
Default	-		-	-	-	_	-	_	_		
R/W	R		R	R	R	R					
	Bit Na		me	Functio	n						
	7 Bl		SY	Printer I This bit i	Printer Busy This bit is the inverse of the (BUSY/WAIT) pin (active Low):						
				0 = Print	0 = Printer busy						
				1 = Print	1 = Printer ready						
	6 ACK		K	Printer Acknowledge The printer pulses this line Low when it has received a byte of data. This b follows the state of the ACK pin (active Low):							
				0 = Printer acknowledge							
				1 = No p	rinter acknow	ledge					
	5	PE		Paper End This bit follows the state of the PE pin:							
				0 = Print	0 = Printer has paper						
				1 = Pape	er end (out of	paper)					
	4	SL	СТ	Printer : This bit f	Selected follows the sta	te of the SLC	T pin:				
				0 = Print	er not selecte	d					
				1 = Print	er selected						
	3 ERF		ROR	Printer I This bit f	Error follows the sta	te of ERROR	pin (active Lo	ow):			
				0 = Print	er error						
				1 = No p	orinter error						
	2–0	Re	served	Reserve	ed						

Programming Notes

The default value for this register depends on the mode. For PC/AT Compatible mode, the default value for this register is ????xxxb. For EPP mode, the default value is ????xxxb.

Parallel Port 1 Status Register (EPP Mode)

I/O Address 0379h

	7		6	5	4	3	2	1	0				
Bit	BUSY	Y	ACK	PE	SLCT	ERROR	Rese	erved	EPP_TIMEO				
Default	-		-	-	-	-	-	-	-				
R/W	R		R	R	R	R			R				
	Bit	Na	me	Functio	n								
	7	BU	ISY	Printer I This bit i	Busy s the inverse	of the (BUSY/	WAIT) pin (ad	ctive Low):					
				0 = Print	er busy								
				1 = Print	1 = Printer ready								
	6	AC	K	Printer The prin follows the	Acknowledge ter pulses this he state of the	e line Low whe ACK pin (act	n it has receiv ive Low):	ved a byte of o	data. This bit				
				0 = Print	0 = Printer acknowledge								
				1 = No p	1 = No printer acknowledge								
	5	PE		Paper E This bit f	nd ollows the sta	ite of the PE p	oin:						
				0 = Print	er has paper								
				1 = Pape	er end (out of	paper)							
	4	SL	СТ	Printer S This bit f	Printer Selected This bit follows the state of the SLCT pin:								
				0 = Print	0 = Printer not selected								
				1 = Print	1 = Printer selected								
	3	ER	ROR	Printer I This bit f	E rror follows the sta	te of ERROR	pin (active Lo	ow):					
				0 = Print	er error								
				1 = No p	rinter error								
	2–1	Re	served	Reserve	ed								
	0	EP	P_TIMEO	EPP Tin 0 = No ti	ne-out Status me-out	5							
				1 = EPP	cycle time-ou	it occurred							
				This bit i 1–0 of th microcor when eit EPP time than 10µ	This bit is set if a time-out occurred only when EPP mode is enabled (bits 1–0 of the Parallel Port Configuration Register in the ÉlanSC400 microcontroller-specific indexed address space) = '01b'. This bit is reset when either the status register is read, or when EPP mode is enabled. An EPP time-out occurs when the BUSY pin remains inactive (Low) for greater than 10 μ s after either SLCTIN or AFDT go active (Low) in EPP mode.								

Programming Notes

The default value for this register depends on the mode. For PC/AT Compatible mode, the default value for this register is ????xxxb. For EPP mode, the default value is ????xxxb.

Parallel Port 1 Control Register

I/O Address 037Ah

	7		6	5	4	3	2	1	0				
Bit		Reserv	red	DIR	IRQEN	SLCTIN	INIT	AUTOFDXT	STROBE				
Default	0		0	0	0	0	0	0	0				
R/W				R/W	R/W	R/W	R/W	R/W	R/W				
	Bit	Nam	e	Functio	n								
	7–6	Rese	erved	Reserve Software	ed e should write	these bits to ().						
	5	DIR		Bidirect When th mode, th a paralle mode is	ional Parallel e parallel port his bit controls el port data wri selected:	Port Data Di is set to oper the data direc te operation v	i rection ate in either B ction between vhere either B	idirectional m host and peri idirectional m	ode or EPP pheral. For ode or EPP				
				0 = Data written to PD7–PD0									
				1 = Data	1 = Data written is latched only								
				For a pa EPP mo	For a parallel port data read operation where either Bidirectional mode or EPP mode is selected:								
				0 =Interr	0 =Internal data register read								
				1 = Data	read from PD	07–PD0]							
				This bit i selected	s undefined w	hen neither B	idirectional m	ode nor EPP i	node is				
	4	IRQE	EN	Printer I Clearing	Printer IRQ Enable Clearing this bit clears any pending interrupts.								
				0 = Disable printer IRQ									
				1 = Enable printer IRQ									
	3	SLC	TIN	Select P This bit i	Select Printer Signal Control This bit is the inverse of the SLCTIN pin.								
				0 = The	SLCTIN pin is	a logic 1							
				1 = The	SLCTIN pin a	logic 0							
	2	INIT		Printer I 0 = Hold	Reset Signal printer in rese	Control et							
				1 = Rele	ase printer fro	om reset, this l	bit follows the	INIT pin (activ	ve Low)				
	1	AUT	OFDXT	Auto Lir This bit i	ne Feed Signa s the inverse	al Control of the AFDT p	vin:						
				$0 = \overline{AFD}$	T pin is a logic	:1							
				1 = AFD Whe autor 13) c	1 = AFDT pin is a logic 0 When connected to a printer, setting this bit causes the printer to automatically insert a line feed when it sees a carriage return (ASCII 13) characters.								
	0 STROBE			Printer Port Strobe Signal Control This bit is the inverse of the STRB pin:									
				$0 = \overline{\text{STRB}}$ pin not active									
				1 = <u>STR</u>	B pin active								

Parallel Port 1 EPP Address Register

I/O Address 037Bh





I/O Address 037C-037Fh



Programming Notes

Bits 31–0: A 16-bit I/O write to 37Ch will cause two back-to-back 8-bit bus cycles to occur to the EPP Data Registers 37Ch and 37Dh. Two bytes of data will be presented to the parallel port data lines in succession starting with the data written to 37Ch. An EPP data strobe will be automatically generated for each of the bus cycles.

An 8-bit I/O write to 37Ch will cause a single 8-bit bus cycle to occur to the EPP Data Register at 37Ch. The single byte of data will be presented to the parallel port data lines along with an automatically generated EPP data strobe.

In common practice, all write accesses to the parallel port 1 EPP Data Register (x8, x16, or x32 I/ O instructions) should be directed to port 37Ch.

MDA/HGA Index Register



Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is set (MDA compatibility).

MDA/HGA Data Register

I/O Address 03B5h



Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is set (MDA compatibility). In addition, if the HGA extensions to MDA are required, CRTC index 52h[4] must be set. The B0000h and B8000h pages specified in the description for bit 7 assume that the internal graphics controller has had its display buffer base address set to reside at B0000h. Generally speaking, setting bit 7 of this register when in HGA mode will functionally add 32 K to the shared memory base address (must be configured via graphics index registers 4Dh/4Eh).

MDA/HGA Mode Control Register

I/O Address 03B8h

	7		6	5	4	3	2	1	0				
Bit	HGA_PG_	SEL	Reserved	TXTBLNK	Reserved	VIDCON	Reserved	HGA_GR_EN	TXTCON				
Default	0		0	0	0	0	0	0	0				
R/W	R/W			R/W		R/W		R/W	R/W				
	Bit	Na	me	Function	n								
	7	7 HGA_PG_SEL		HGA Pa 0 = Use	HGA Page Select (HGA Mode Only) 0 = Use B0000h as the start of the display buffer								
				1 = Use	1 = Use B8000h as the start of the display buffer								
	6	6 Reserved		Reserve Software	Reserved Software should write this bit to 0.								
	5	TXTBLNK		Text Bli 0 = Blink	Text Blink Control 0 = Blinking attribute disabled								
				1 = Blinking attribute enabled (attribute byte bit 7 will control blinking)									
	4	Re	served	Reserved Software should write this bit to 0.									
	3	VIE	DCON	Video Blanking Control 0 = Video is blanked									
				1 = Vide	o is not blank	ed							
	2	Re	served	Reserve Software	d should write	this bit to 0.							
	1	HG	A_GR_EN	HGA Gr	aphics Enabl	e (HGA Mode	e Only)						
	0	0 TXTCON		MDA/HG This bit i the colur MDA/HG	MDA/HGA Column Select This bit is provided for compatibility purposes only. It does not actually set the column width. This must be done via the CRTC index registers. The MDA/HGA legacy values for this bit are:								
				0 = 40x2	5 text mode								
				1 = 80x25 text mode									

Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (chip configuration register DDh[0]) is set (MDA compatibility). In addition, if the HGA extensions to MDA are required, CRTC index 52h[4] must be set. Also note that the B0000h and B8000h pages specified in the description for bit 7 assume that the internal graphics controller has had its display buffer base address set up to reside at B0000h. Generally speaking, setting bit 7 of this register when in HGA mode will functionally add 32 Kbytes to the shared memory base address (must be configured via graphics index registers 4Dh/4Eh).

MDA/HGA Status Register

	7	6	5	4	3	2	1	0		
Bit		R	eserved		VERTRET	Rese	erved	DMSTAT		
Default	1	1	1	1	х	0	0	x		
R/W			R		R	I	R	R		
	Bit	Name	Functio	Function						
	7–4	Reserved	Reserve Reads b	ed ack '1111b'.						
	3	VERTRET	Vertical 0 = Rast	Vertical Retrace Status (simulated vertical sync) 0 = Raster is not in vertical retrace						
			1 = Rast	1 = Raster is in vertical retrace						
	2–1	Reserved	Reserve	Reserved						
	0	DMSTAT	Display This bit i meaning never oc	Display-Memory Access Status (Simulated Horizontal Sync) This bit is provided for software compatibility purposes. The legacy meanings for this bit are as shown below. In actuality, screen sparkle will never occur.						
			0 = CPU	0 = CPU access to video buffer RAM will cause screen sparkle						
			1 = CPU	can access	video buffer R	AM without ca	ausing screen	sparkle		

Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is set (MDA compatibility).

HGA Configuration Register



Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is set (MDA compatibility) and the Extended Feature Control Register (graphics index 52h) bit 4 is set, thus enabling HGA mode. Also, bits 1–0 can be read back via the internal graphics controller's Extended Feature Control Register at graphics index 52h in 3x4h/3x5h (internal graphics controller indexed register space).

CGA Index Register

I/O Address 03D4h



Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is cleared (CGA mode).

CGA Data Port

I/O Address 03D5h



Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is cleared (CGA mode).

CGA Mode Control Register

I/O Address 03D8h

	7		6	5	4	3	2	1	0			
Bit		Reserved		TXTBLNK	GRPCON	VIDCON	COLBUR	TGCON	TXTCON			
Default	0		0	0	0	0	0	0	0			
R/W				R/W	R/W	R/W	R/W	R/W	R/W			
	Bit	Name		Functio	n							
	7–6	Reserve	d	Reserve Software	ed e should write	these bits to ().					
	5	TXTBLN	IK	Text Att 0 = Blink	ribute Contro king attribute c	ol lisabled						
				1 = Blink	1 = Blinking attribute enabled (attribute byte bit 7 will control blinking)							
	4	GRPCO	N	CGA Gr 0 = All o	CGA Graphics Control 0 = All other modes							
				1 = 1bpp	high-resoluti	on APA graph	iics mode					
	3	VIDCON	1	Video B 0 = Vide	lanking Cont o is blanked	rol						
				1 = Vide	o is not blank	ed						
	2	COLBUI	२	Color Burst Select (Affects Only Text Modes) 0 = Use color text attributes								
				1 = Norn STN	nal graphics p panels will us	anels will use e monochrom	black and wh	ite text attribu	tes. Color			
	1	TGCON		Text/Gra 0 = Text	aphics Contro mode	ol						
				1 = Grap	hics mode							
	0	TXTCO	N	CGA Column Select This bit is provided for compatibility purposes only. It does not actually set the column width. This must be done via the CRTC index registers. The CGA legacy values for this bit are:								
				0 = 40x25 text mode								
				1 = 80x2	25 text mode							

Programming Notes

Bits 3–0 of this register select the border color for text mode, the background color (C0 = C1 = 0) for 320x200 graphics modes, and the foreground color (C0 = 1) for 640x200 graphics modes. This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is cleared (CGA mode).

CGA Color Select Register

	7		6	5	4	3	2	1	0				
Bit		Rese	erved	ALTPAL	ALTBAK	SBINT	SBRED	SBGREEN	SBBLUE				
Default	0		0	0	0	0	0	0	0				
R/W				R/W	R/W	R/W	R/W	R/W	R/W				
	Bit	Na	me	Functio	n								
	7–6	Re	served	Reserve Software	Reserved Software should write these bits to 0.								
	5 ALTPAL		TPAL	Select A Selects a	Select Alternate Palette Selects an alternate palette for the 320-column graphics mode display:								
				0 = Gree	0 = Green, red, yellow palette								
				1 = Cyan, magenta, white palette									
	4 ALTBAK			Select A 0 = No ir	Select Alternate Background 0 = No intense foreground or background colors								
				1 = Sele text r	1 = Selects intense colors in graphics, and intense background colors in text mode								
	3	SB	INT	Select Intense Border/Background 0 = Border/foreground not intense									
				1 = Inten inten	1 = Intense border in text mode, intense background in 320x200 graphics, intense foreground in 640x200 graphics								
	2	SB	RED	Select R 0 = No re	Select Red Border/Background 0 = No red component								
				1 = Red foreg	border in text pround in 640	mode, red ba 200 graphics	ckground in 3	20x200 graph	ics, red				
	1	SB	GREEN	Select G 0 = No g	Green Border	/Background ent							
				1 = Gree gree	en border in te n foreground i	xt mode, gree in 640x200 gra	n background aphics	l in 320x200 g	raphics,				
	0	SB	BLUE	Select E 0 = No b	Blue Border/E lue componer	Background							
				1 = Blue foreg	border text m pround in 640	ode, blue bac <200 graphics	kground in 32	0x200 graphic	cs, blue				

Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is cleared (CGA mode).

CGA Status Register

	7		6	5	4	3	2	1	0			
Bit			Rese	rved		VERTRET	LPENSW	LPENSTAT	DMSTAT			
Default	1		1	1	1	х	1	х	х			
R/W			R			R	R	R	R			
	Bit	Name		Functio	n							
	7–4	Reserve	ed	Reserve Reads b	ed ack '1111b'.							
	3	VERTR	ET	Vertical 0 = Rast	Retrace Stat	us (Simulate rtical retrace	d Vertical Sy	nc)				
				1 = Rast	1 = Raster is in vertical retrace							
	2	LPENS	N	Light Pe Always r	Light Pen Switch Always reads back logic 1.							
	1	LPENS ⁻	ΤΑΤ	Light Pe This bit accesse accesse	Light Pen Status This bit will read 1 if I/O address 3DC was the most recent previously accessed, or zero if I/O address 3DB was the most recent previously accessed.							
	0	DMSTA	Т	Display This bit i meaning never of	Display-Memory Access Status (Simulated Horizontal Sync) This bit is provided for software compatibility purposes. The legacy meanings for this bit are as shown below. In actuality, screen sparkle will never occur.							
				0 = CPU	CPU access to video buffer RAM will cause screen sparkle							
				1 = CPU can access video buffer RAM without causing screen sparkle								

Programming Notes

This register is visible only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index DDh[0]) is cleared.

Primary 82365-Compatible PC Card Controller Index Register

I/O Address 03E0h



Primary 82365-Compatible PC Card Controller Data Port



COM1 Transmit Holding Register



Programming Notes

There is only one serial port on the ÉlanSC400 microcontroller, but it can be configured to have a base address of either 3F8h or 2F8h (COM1/COM2).

COM1 Receive Buffer Register

I/O Address 03F8h



COM1 Baud Clock Divisor Latch LSB

I/O Address 03F8h





I/O Address 03F9h



COM1 Interrupt Enable Register

I/O Address 03F9h

	7		6	5	4	3	2	1	0			
Bit			Rese	erved		EMSI	ERLSI	ETHREI	ERDAI			
Default	0		0	0	0	0	0	0	0			
R/W						R/W	R/W	R/W	R/W			
	Bit	Na	me	Functio	Function							
	7–4	Re	served	Reserve Software	ed e should write	these bits to ().					
	3	ΕN	ISI	Enable I 0 = Disa	Enable Modem Status Interrupt 0 = Disable modem status interrupt							
				1 = Enat	ole modem sta	atus interrupt						
	2	ER	LSI	Enable I 0 = Disa	Enable Receiver Line Status Interrupt 0 = Disable receiver line status interrupt							
				1 = Enable receiver line status interrupt								
	1	ET	HREI	Enable 0 = Disa	Enable Transmitter Holding Register Empty Interrupt 0 = Disable transmitter holding register empty interrupt							
				1 = Enat	ole transmitter	r holding regis	ter empty inte	rrupt				
	0	ER	DAI	Enable 0 = Disa	Received Dat ble data availa	t a Available l able/16550 tim	nterrupt ne-out interrup	ot				
				1 = Enat 1655	1 = Enable received data available interrupt in 16450-compatible mode; in 16550-compatible mode, this bit also enables time-out interrupts							
				More detail on time-out interrupts can be found in the Interrupt Identification Register description.								

COM1 Interrupt ID Register

I/O Address 03FAh

	7	6	5	4	3	2	1	0
Bit	FIFO1 FIFO0		Reserved		ID2 ID1 ID0			IP
Default	0	0	0	0	1	1	1	1
R/W	R				R			R

Bit	Name	Function	Priority
7–6	FIFO1 FIFO0	FIFO Feature Presence Indication FIFO is only present when 16550-compatible mode is enabled):	
		0 0 = No significance	
		0 1 = No significance	
		1 0 = 16450-compatible mode is enabled	
		1 1 = 16550-compatible mode is enabled	
5–4	Reserved	Reserved These bits always read back '00b'.	
3–1	ID2	Interrupt Identification Bit Field	-
	ID1	0 0 0 = Modem status	Fourth (Lowest)
	ID0	0 0 1 = Transmitter Holding Register Empty/Transmit FIFO Empty (16550-compatible mode)	Third
		0 1 0 = Received Data Available/Receiver FIFO trigger (16550-compatible mode)	Second
		0 1 1 = Receive Line Status	First (Highest)
		1 0 0 = Not used	
		1 0 1 = Not used	
		1 1 0 = FIFO time-out	Second
		1 1 1 = Not used	
		In 16450-compatible mode, bit 3 always reads back '0b'. See the Modem Status Register (MSR) and Line Status Register (LSR) for more detail on interrupt events.	
		If two interrupt sources are pending simultaneously, only the highest priority interrupt (as defined by the rightmost column for bits $3-1$) will be indicated by bits 3-1 of the Interrupt Identification Register (IIR). When the interrupt source is cleared, a subsequent read from the Interrupt Identification Register will return the next highest priority interrupt source. Bits $3-1$ have no meaning if bit $0 = '1b'$.	
		A FIFO time-out occurs when the receive FIFO is not empty, and more than four continuous character-times have transpired without more data being placed into or read out of the receive FIFO. Reading a character from the receive FIFO clears the time-out interrupt.	
0	IP	Serial Port Interrupt Pending (Active Low) 0 = Interrupt pending	
		1 = No interrupt pending	

COM1 FIFO Control Register

I/O Address 03FAh

	7	6	5	4	3	2	1	0				
Bit		RFRT[1–0]	Rese	erved	Reserved	TFCLR	RFCLR	FIFOEN				
Default	0	0	0	0	0	0	0	0				
R/W		Ŵ			W	W	W	W				
	Bit	Name	Functio	n								
	7–6	RFRT[1–0]	Receive When in which th available enabled fills to th	F FIFO Regis 16550-compa e Interrupt Ide interrupt is p in the IER, th e trigger level	ter Trigger B atible mode, th entification Re ending. If rece e system will h per the follow	its his bit field spo gister will repo eived data ava be interrupted ving table:	ecifies the trig ort that a rece ailable interrup when the rec	ger level at ved data ots are eive FIFO				
			$0 \ 0 = 1 \ k$	oyte								
			0 1 = 4 k	oytes								
			10=81	oytes								
			1 1 = 14	bytes								
			When th will be c	When the data in the receive FIFO falls below this trigger level, the interrupt will be cleared.								
	5–4	Reserved	Reserve Software	Reserved Software should write these bits to 0.								
	3	Reserved	Reserve Software	Reserved Software should write this bit to 1.								
	2	TFCLR	Transm Writing a transmit This bit i to the Tr	Transmitter FIFO Buffer Clear Writing a '1b' to this bit position clears the transmit FIFO, and resets the transmit FIFO counter logic. It does not clear the Transmitter Shift Register. This bit is cleared by either a read of the Interrupt ID Register, or by a write to the Transmit Holding Register.								
	1	RFCLR	Receive Writing a receive This bit control.	FIFO Buffe a '1b' to this b FIFO counter is self clearing	r Clear it position clea logic. It does i j, and does no	ars the receive not clear the F at need to be r	e FIFO, and re Receiver Shift eset to 0 unde	sets the Register. er software				
	0	FIFOEN	FIFO Er 0 = Caus Disa bits o	able (16550- ses UART to e bles accesses except this bit	Compatible N enter 16450-co s to receive ar	fode Enable) ompatible mod od transmit FIF	de FOs, and all F	IFO control				
			1 = Caus Enal FIFC	ses UART to e bles receive a control bits.	enter 16550-co nd transmit FI	ompatible mod FOs, and ena	de bles accesses	to other				
			The main difference between 16450-compatible mode and 16550-compatible mode is the addition of transmit and receive FIFOs in 16550-compatible mode.									
			This bit they will FIFOs.	must be '1b' w not be progra	/hen other FIF mmed. Also n	O control reg ote that any m	ister bits are v node switch wi	vritten to or Il clear both				

Programming Notes

The contents of this write-only register can be read back via the shadow register at CSC index D3h. Also note that the on board UART can be mapped to only one of COM1 or COM2 at any time, and CSC index D3h serves either configuration.

COM1 Line Control Register

I/O Address 03FBh

	7		6	5	4	3	2	1	0			
Bit	DLAE	3	SB	SP	EPS	PE	STP	WL WL	B0 B1			
Default	0		0	0	0	0	0	0	0			
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W			
	Dit	Na		Function								
	$7 \text{DLAR} \qquad \qquad \text{Divisor Latch Access Pit}$											
	I	DL	AD	Set this bit to gain access to the baud rate divisor latches for this COM port. C this bit to mux in the Transmit Holding Register and Receive Buffer Register port xF8h, and the Interrupt Enable Register at port xF9h.								
	6	SB		Set Break Enable Setting this bit causes a break condition to be transmitted to the receiving UART.								
				0 = Disable se	t break							
				1 = Force serial output to spacing state (logic '0') regardless of other transmitter activity								
				The break control acts on the SOUT pin only, and has no other effect on the transmitter logic.								
	5	SP		Stick Parity Enable Forces the parity bit to always be 0 or 1 versus dynamically changing it so that there are an odd or even number of 1 bits in the transmitted data. If this bit is 0, then normal parity is used if parity is enabled. If bits 5,4, and $3 = 1$, the parity bit is generated/checked as a logical 1. If bits 5 and $3 = 1$ and bit $4 = 0$, the parity bit is generated/checked as a logical 0.								
	4	EP	S	Even Parity S Parity must be	elect enabled via b	oit 3 for this bi	t to have mea	ning:				
	0 = Odd parity, the parity bit will be manipulated to force an odd number of 1 b in the transmitted data, and the same condition will be checked for in the received data.						per of 1 bits or in the					
				1 = Even parity bits in the received d	y, the parity bi transmitted da ata.	t will be manip ata, and the sa	oulated to forcome condition	e an even nui will be checke	mber of 1 ed for in the			
				Start/stop bits	are not includ	led in the parit	y generation/	checking sche	eme.			
	3	PE		Asynchronous Data Parity Enable Causes a parity bit to be generated in the transmitted data, and to be checked in the received data. The parity bit is located between the last data word bit and the first stop bit in the bit stream.								
	2	ST	Р	Stop Bits Based on character length from bits 1–0 above.								
				If character ler	ngth = 5:							
				0 = 1 stop bit								
				1 = 1.5 stop bi	ts							
				If character length = 6, 7, or 8:								
				0 = 1 stop bit								
				1 = 2 stop bits								
	1–0	WL WL	.B0 .B1	Transmit/Rec 0 0 = 5 bits	eive Charact	er Length						
		_		0 1 = 6 bits								
				1 0 = 7 bits								
				1 1 = 8 bits								

COM1 Modem Control Register

I/O Address 03FCh

	7		6	5	4	3	2	1	0				
Bit			Reserved		LOOP	OUT2	OUT1	RTS	DTR				
Default	0		0	0	0	0	0	0	0				
R/W					R/W	R/W	R/W	R/W	R/W				
	Bit	Na	me	Functio	n								
	7–5	Re	served	Reserve Software	Reserved Software should write these bits to 0.								
	4	LO	ЮР	Loopba 1 = Enat The bit: RTS DTR OUT OUT	Loopback (Diagnostic Mode) Enable 1 = Enabled The following internal connections are made by setting this diagnost bit: RTS is internally connected to CTS DTR is internally connected to DSR OUT1 is internally connected to RI OUT2 is internally connected to DCD								
		0 = Loopback mode is disabled											
				In addition The Tran register. inactive. appropri mode.	In addition, the SOUT bit is driven High, and the SIN input line is blocked. The Transmit Shift Out Register is directly connected to the receive shift in register. In addition, the DTR, RTS, OUT1 and OUT2 signals are forced inactive. Modem control interrupts can be forced by enabling the appropriate bit in the IER, and asserting one of the bits 3–0 in loopback mode.								
	3	OL	JT2	Enable This bit master e IRQs wil	Enable COM2 Interrupts This bit controls the internal OUT2 signal which is used internally as a master enable for COM1 interrupts. If this bit is not set, no COM port 1 IRQs will be felt at the Programmable Interrupt Controller (PIC).								
	2	OL	JT1	OUT1 C This bit internally the loop operatio operatio	T Control bit controls the internal OUT1 signal which is not tied to anything nally. It is provided for PC/AT compatibility, and can be used as part of oopback diagnostics. Other than that, it has no effect on system ration, and can be used for a scratch pad during normal system ration.								
	1	RT	S	Reques 0 = Deas	Request to Send 0 = Deassert the Request To Send signal (RTS)								
				1 = Asse	ert the Reques	st To Send sig	nal (RTS)						
	0	DT	R	Data Te 0 = Deas	rminal Ready ssert the Data	Terminal Rea	ady signal (DT	R)					
				1 = Asse	1 = Assert the Data Terminal Ready signal (DTR)								

COM1 Line Status Register

I/O Address 03FDh

	7	6	5	4	3	2	1	0		
Bit	16550_ERR	TEMT	THRE	BI	FE	PE	OE	DR		
Default	0	1	1	0	0	0	0	0		
R/W	R	R	R	R	R	R	R	R		
	Bit Na 7 16	me 550_ERR	Function 16550-N In 16450 In 16550 parity en This bit i subsequ	Function 16550-Mode Error In 16450-compatible mode, this bit reads back '0b'. In 16550-compatible mode, when this bit is set it indicates at least one parity error, framing error, or break condition is present in the receive FIFO. This bit is cleared by a read from the Line Status Register if there are no subsequent errors in the FIFO.						
	6 TE	MT	Transm In 16450 Register In 16550	Transmitter Empty Indicator In 16450-compatible mode, this bit is set when both the Transmit Holding Register and the Transmit Shift Register are empty.						
	5 TH	IRE	Register Transmi FIFO En In 16450 Register by a writ mode. In 16550 complete cleared Identifica if progra	 Register and transmit FIFO are empty. Transmitter Holding Register (16450-Compatible Mode) or Transmit FIFO Empty (16550-Compatible Mode) In 16450-compatible mode, this bit indicates that the Transmit Holding Register is ready to accept a new character. This bit is automatically reset by a write to the Transmit Holding Register when in 16450-compatible mode. In 16550-compatible mode, this bit indicates that the transmit FIFO is completely empty. When in 16550-compatible mode this interrupt will be cleared when either the transmit FIFO is written to, or when the Interrupt Identification Register is read. This bit can be used to generate an interrupt if programmed to do so via the Interrupt Enable Register. 						
	4 BI		Break Ir In 16450 sending time it ta In 16550 parity, st receive I loaded ir new cha detected Line Sta	 Break indicator In 16450-compatible mode, this bit is set when the UART detects that the sending UART is transmitting a break condition for a period longer than the time it takes to receive start, data, parity, and stop bits. In 16550-compatible mode, this bit is set when an entire word (start, data, parity, stop) that has been received with break indication present into the receive FIFO is at the top of the FIFO. Only one break indication will be loaded into the FIFO regardless of the duration of the break condition. A new character will not be loaded into the FIFO until the next valid start bit i detected. This latched status bit is automatically cleared by a read from th Line Status Register. 						
	3 FE		Framing In 16450 characte In 16550 received This latc Status R	 Framing Error In 16450-compatible mode, this bit is set to indicate that a received character did not have a valid stop bit. In 16550-compatible mode, this bit is set when a character that has been received with a framing error into the receive FIFO is at the top of the FIFO. This latched status bit is automatically cleared by a read from the Line Status Register. 						
	2 PE		Parity E In 16450 parity. In 16550 received latched s Register	 Parity Error In 16450-compatible mode, this bit is set upon receipt of data with incorrect parity. In 16550-compatible mode, this bit is set when a character that has been received with bad parity into the receive FIFO is at the top of the FIFO. This latched status bit is automatically cleared by a read from the Line Status Register. 						

Bit	Name	Function
1	OE	Overrun Error In 16450-compatible mode, this bit is set if a new character is received into the receiver buffer before a previous character was read, thus resulting in lost data.
		In 16550-compatible mode, this bit is set if a new character is completely received into the Shift Register when the FIFO is already 100% full. Data in the FIFO is not overwritten by this overrun. The data in the Shift Register will be lost when the next character is received. This latched status bit is automatically cleared by a read from the Line Status Register.
0	DR	Data Ready In 16450-compatible mode, when this bit is set, a character has been received and placed in the Receiver Buffer Register. This bit is automatically cleared by reading the Receiver Buffer Register.
		In 16550-compatible mode, when this bit is set, a character has been received and placed in the receive FIFO. This bit is automatically cleared by reading the Receiver FIFO.

Programming Notes

When a receiver line status interrupt is enabled and detected, bits 1 through 4 above will indicate the reason for the interrupt. The status bits are valid even when the receiver line status interrupt is not enabled.

COM1 Modem Status Register

I/O Address 03FEh

	7		6	5	4	3	2	1	0
Bit	DCD		RI	DSR	стѕ	DDCD	TERI	DDSR	DCTS
Default	х		х	х	х	0	0	0	0
R/W	R		R	R	R	R	R	R	R
Default R/W	x R Bit 7 6 5 4 3	Nai DC RI DS CT	x R D R S CD	x R Functio Data Ca 0 = DCD 1 = DCD If in I Ring Ind 0 = RI in I = RI in I = RI in I = RI in I = DSR 1 = DSR 1 = DSR I = DSR 1 = DSR I = IN 0 = CTS 1 = CTS If in I Delta Da 0 = Indic Regi 1 = Indic Regi Trailing	x R rrier Detect input signal is oopback mod dicator put signal is d put signal is d oopback mod t Ready input signal is oopback mod t Ready input signal is oopback mod t Ready input signal is oopback mod t Send input signal is oopback mod tate carrier De ates that the E ster was last r ates that the E	0 R s deasserted s asserted e, this bit trac easserted e, this bit trac s deasserted e, this bit trac s deasserted e, this bit trac s deasserted e, this bit trac s deasserted e, this bit trac c deasserted c deassert	0 R ks bit 3 of the ks bit 2 of the ks bit 0 of the ks bit 1 of the s not changed anged since t	0 R Modem Contr Modem Contr Modem Contr Modem Contr d since the Mo he Modem Sta	0 R rol Register. rol Register. rol Register. rol Register. dem Status atus
	1	DD DC	SR TS	 0 = Indicates that the RI signal has not changed from an active to an inactive state since the Modem Status Register was last read 1= Indicates that the RI signal changed from an active to an inactive since the Modem Status Register was last read Delta Data Set Ready 0 = Indicates that the DSR signal has not changed since the Modem Status Register was last read 1 = Indicates that the DSR signal changed since the Modem Status Register was last read 1 = Indicates that the DSR signal changed since the Modem Status Register was last read 0 = Indicates that the CTS signal has not changed since the Modem Status Register was last read 1 = Indicates that the CTS signal has not changed since the Modem Status Register was last read 					

Programming Notes

Bits 3–0 are latched status bits that will generate an interrupt if modem status interrupts are unmasked in the Interrupt Enable Register. Reading the Modem Status Register clears these bits, and their associated interrupt. Bits 7–4 are real time status indicators for the indicated inputs to the UART.

COM1 Scratch Pad Register

I/O Address 03FFh



CHIP SETUP AND CONTROL (CSC) INDEXED REGISTERS

3.1 OVERVIEW

This chapter describes the Chip Setup and Control (CSC) indexed registers available on the ÉlanSC400 microcontroller. Chip Setup and Control indexed registers are defined as ÉlanSC400 microcontroller-specific registers beyond standard PC/AT compatibility requirements. For example, all memory controller and power management registers are included in this group. Also included in this group are all registers that provide extended control features for the on-board peripherals. They are grouped logically by function in hexadecimal order, as listed in Table 3-1.

In addition to the CSC indexed registers, the RTC, graphics controller, and PC Card controller also have their own dedicated groups of indexed registers accessible through different index and data ports. These dedicated register groups are described in following chapters of this manual.

The ÉlanSC400 Chip Setup and Control (CSC) indexed registers are accessed using a two-step process:

- An I/O write to I/O address 22h is first performed. The data written is the index of the CSC register to be accessed.
- This I/O write is followed by an I/O read or write to address 23h. This access causes data to be read from or written to the addressed configuration register.

The ÉlanSC400 microcontroller does not implement any locking mechanism for extended register access. Also, back-to-back access of I/O address 22h/23h is not required for access to the extended index registers. The following code fragment:

```
mov al, 90h; force an SMI
out 22h, al
mov al, 1
out 23h, al
:
:
```

has the same result as this code fragment:

mov AX, 0190h; force an SMI. out 22h, AX

The Chip Setup and Control indexed registers are typically accessed at CPU speeds unless they are being echoed to the ISA bus for debug.

Table 3-1 Chip Setup and Control (CSC) Index Register Map

Register Name	I/O (Port) Address	Index	Page Number
ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Index Register	0022h		page 3-8

Register Name	I/O (Port) Address	Index	Page Number
ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Data Port	0023h		page 3-9
DRAM Setup and Configuration Group		00–07h	
DRAM Bank 0 Configuration Register		00h	page 3-10
DRAM Bank 1 Configuration Register		01h	page 3-11
DRAM Bank 2 Configuration Register		02h	page 3-12
DRAM Bank 3 Configuration Register		03h	page 3-13
DRAM Control Register		04h	page 3-14
DRAM Refresh Control Register		05h	page 3-16
Drive Strength Control Register A		06h	page 3-17
Drive Strength Control Register B		07h	page 3-18
Reserved		08–0Fh	
Cache Control Registers		10–14h	
Non-Cacheable Window 0 Address Register		10h	page 3-19
Non-Cacheable Window 0 Address/Attributes/SMM Register		11h	page 3-20
Non-Cacheable Window 1 Address Register		12h	page 3-21
Non-Cacheable Window 1 Address/Attributes Register		13h	page 3-22
Cache and VL Miscellaneous Register		14h	page 3-23
Reserved		15–1Fh	
ROM Configuration, Setup, and Control Group		20–28h	
Pin Strap Status Register		20h	page 3-25
Linear ROMCS0/Shadow Register		21h	page 3-26
Linear ROMCS0 Attributes Register		22h	page 3-28
ROMCS0 Configuration Register A		23h	page 3-29
ROMCS0 Configuration Register B		24h	page 3-31
ROMCS1 Configuration Register A		25h	page 3-32
ROMCS1 Configuration Register B		26h	page 3-34
ROMCS2 Configuration Register A		27h	page 3-35
ROMCS2 Configuration Register B		28h	page 3-37
Reserved		29–2Fh	
Memory Management System (MMS)		30–35h	
MMS Window C–F Attributes Register		30h	page 3-38
MMS Window C–F Device Select Register		31h	page 3-39
MMS Window A Destination Register		32h	page 3-40

Register Name	I/O (Port) Address	Index	Page Number
MMS Window A Destination/Attributes Register		33h	page 3-41
MMS Window B Destination Register		34h	page 3-42
MMS Window B Destination/Attributes Register		35h	page 3-43
Reserved		36–37h	
GPIO Pin Muxing and Termination Group		38–3Eh	
Pin Mux Register A		38h	page 3-44
Pin Mux Register B		39h	page 3-45
Pin Mux Register C		3Ah	page 3-46
GPIO Termination Control Register A		3Bh	page 3-47
GPIO Termination Control Register B		3Ch	page 3-48
GPIO Termination Control Register C		3Dh	page 3-49
GPIO Termination Control Register D		3Eh	page 3-50
Reserved		3Fh	
PMU Mode Control and Status Group		40–45h	
PMU Force Mode Register		40h	page 3-51
PMU Present and Last Mode Register		41h	page 3-53
Hyper/High-Speed Mode Timers Register		42h	page 3-54
Low-Speed/Standby Mode Timers Register		43h	page 3-55
Suspend/Temporary Low-Speed Mode Timers Register		44h	page 3-56
Wake-Up Pause/High-Speed Clock Timers Register		45h	page 3-57
Reserved		46–4Fh	
PMU Wake-up Control and Status Group		50–5Bh	
SUS_RES Pin Configuration Register		50h	page 3-58
Reserved		51h	
Wake-Up Source Enable Register A		52h	page 3-59
Wake-Up Source Enable Register B		53h	page 3-60
Wake-Up Source Enable Register C		54h	page 3-61
Wake-Up Source Enable Register D		55h	page 3-62
Wake-Up Source Status Register A		56h	page 3-63
Wake-Up Source Status Register B		57h	page 3-64
Wake-Up Source Status Register C		58h	page 3-65
Wake-Up Source Status Register D		59h	page 3-66
GPIO as a Wake-Up or Activity Source Status Register A		5Ah	page 3-67

Register Name	I/O (Port) Address	Index	Page Number
GPIO as a Wake-Up or Activity Source Status Register B		5Bh	page 3-68
Reserved		5C–5Fh	
PMU Activity Control and Status Group		60–6Dh	
GP_CS Activity Enable Register		60h	page 3-69
GP_CS Activity Status Register		61h	page 3-70
Activity Source Enable Register A		62h	page 3-71
Activity Source Enable Register B		63h	page 3-72
Activity Source Enable Register C		64h	page 3-73
Activity Source Enable Register D		65h	page 3-74
Activity Source Status Register A		66h	page 3-75
Activity Source Status Register B		67h	page 3-76
Activity Source Status Register C		68h	page 3-77
Activity Source Status Register D		69h	page 3-78
Activity Classification Register A		6Ah	page 3-79
Activity Classification Register B		6Bh	page 3-80
Activity Classification Register C		6Ch	page 3-81
Activity Classification Register D		6Dh	page 3-82
Reserved		6E–6Fh	
Battery Level BL Pin Control and Status Group		70–72h	
Battery/AC Pin Configuration Register A		70h	page 3-83
Battery/AC Pin Configuration Register B		71h	page 3-85
Battery/AC Pin State Register		72h	page 3-86
Reserved		73–7Fh	
Clock Control and Status Group		80–83h	
CPU Clock Speed Register		80h	page 3-87
CPU Clock Auto Slowdown Register		81h	page 3-88
Clock Control Register		82h	page 3-90
CLK_IO Pin Output Clock Select Register		83h	page 3-91
Reserved		84–87h	
Factory Level Debug Group		88–8Fh	
Factory Debug Register A		88h	page 3-92
Factory Debug Register B		89h	page 3-93
SMI/NMI Generation and Status Group		90–9Dh	
Miscellaneous SMI/NMI Enable Register		90h	page 3-94
PC Card and Keyboard SMI/NMI Enable Register		91h	page 3-95

Register Name	I/O (Port) Address	Index	Page Number
Mode Timer SMI/NMI Enable Register		92h	page 3-96
Battery Low and ACIN SMI/NMI Enable Register		93h	page 3-97
Miscellaneous SMI/NMI Status Register A		94h	page 3-99
PC Card and Keyboard SMI/NMI Status Register		95h	page 3-100
Mode Timer SMI/NMI Status Register		96h	page 3-101
Battery Low and ACIN SMI/NMI Status Register		97h	page 3-102
SMI/NMI Select Register		98h	page 3-104
I/O Access SMI Enable Register A		99h	page 3-105
I/O Access SMI Enable Register B		9Ah	page 3-106
I/O Access SMI Status Register A		9Bh	page 3-107
I/O Access SMI Status Register B		9Ch	page 3-108
XMI Control Register		9Dh	page 3-109
Reserved		9E–9Fh	
GPIO Pin Control, Status, and Muxing Group		A0–BDh	
GPIO_CS Function Select Register A		A0h	page 3-110
GPIO_CS Function Select Register B		A1h	page 3-111
GPIO_CS Function Select Register C		A2h	page 3-112
GPIO_CS Function Select Register D		A3h	page 3-113
GPIO Function Select Register E		A4h	page 3-114
GPIO Function Select Register F		A5h	page 3-115
GPIO Read-Back/Write Register A		A6h	page 3-116
GPIO Read-Back/Write Register B		A7h	page 3-117
GPIO Read-Back/Write Register C		A8h	page 3-118
GPIO Read-Back/Write Register D		A9h	page 3-119
GPIO_PMUA Mode Change Register		AAh	page 3-120
GPIO_PMUB Mode Change Register		ABh	page 3-122
GPIO_PMUC Mode Change Register		ACh	page 3-124
GPIO_PMUD Mode Change Register		ADh	page 3-126
GPIO_PMU to GPIO_CS Map Register A		AEh	page 3-128
GPIO_PMU to GPIO_CS Map Register B		AFh	page 3-129
GPIO_XMI to GPIO_CS Map Register		B0h	page 3-130
Standard Decode To GPIO_CS Map Register		B1h	page 3-131
GP_CS to GPIO_CS Map Register A		B2h	page 3-132
GP_CS to GPIO_CS Map Register B		B3h	page 3-133
GP_CSA I/O Address Decode Register		B4h	page 3-134
GP_CSA I/O Address Decode and Mask Register		B5h	page 3-135

Register Name	I/O (Port) Address	Index	Page Number
GP_CSB I/O Address Decode Register		B6h	page 3-136
GP_CSB I/O Address Decode and Mask Register		B7h	page 3-137
GP_CSA/B I/O Command Qualification Register		B8h	page 3-138
GP_CSC Memory Address Decode Register		B9h	page 3-140
GP_CSC Memory Address Decode and Mask Register		BAh	page 3-141
GP_CSD Memory Address Decode Register		BBh	page 3-142
GP_CSD Memory Address Decode and Mask Register		BCh	page 3-143
GP_CSC/D Memory Command Qualification Register		BDh	page 3-144
Reserved		BE–BFh	
Matrix Keyboard/XT Keyboard Group		C0–CAh	
Keyboard Configuration Register A		C0h	page 3-146
Keyboard Configuration Register B		C1h	page 3-149
Keyboard Input Buffer Read-Back Register		C2h	page 3-151
Keyboard Output Buffer Write Register		C3h	page 3-152
Mouse Output Buffer Write Register		C4h	page 3-153
Keyboard Status Register Write Register		C5h	page 3-154
Keyboard Timer Register		C6h	page 3-155
Keyboard Column Register		C7h	page 3-156
Keyboard Row Register A		C8h	page 3-158
Keyboard Row Register B		C9h	page 3-160
Keyboard Column Termination Register		CAh	page 3-162
Reserved		CB–CFh	
PC/AT-Related Extended Feature Group		D0–DEh	
Internal I/O Device Disable/Echo ZBUS Configuration Register		D0h	page 3-164
Parallel/Serial Port Configuration Register		D1h	page 3-167
Parallel Port Configuration Register		D2h	page 3-168
UART FIFO Control Register Shadow		D3h	page 3-169
Interrupt Configuration Register A		D4h	page 3-170
Interrupt Configuration Register B		D5h	page 3-171
Interrupt Configuration Register C		D6h	page 3-172
Interrupt Configuration Register D		D7h	page 3-173
Interrupt Configuration Register E		D8h	page 3-174
DMA Channel 0–3 Extended Page Register		D9h	page 3-175
Register Name	I/O (Port) Address	Index	Page Number
--	-----------------------	--------	----------------
DMA Channel 5–7 Extended Page Register		DAh	page 3-176
DMA Resource Channel Map Register A		DBh	page 3-177
DMA Resource Channel Map Register B		DCh	page 3-178
Internal Graphics Control Register A		DDh	page 3-179
Internal Graphics Control Register B		DEh	page 3-180
Reserved		DFh	
ISA Bus Configuration Group		E0–E5h	
Write-protected System Memory (DRAM) Window/ Overlapping ISA Window Enable Register		E0h	page 3-181
Overlapping ISA Window Start Address Register		E1h	page 3-182
Overlapping ISA Window Size Register		E2h	page 3-183
Suspend Mode Pin State Register A		E3h	page 3-184
Suspend Mode Pin State Register B		E4h	page 3-185
Suspend Mode Pin State Over-ride Register		E5h	page 3-186
Reserved		E6–E9h	
IrDA Group		EA–EDh	
IrDA Control Register		EAh	page 3-188
IrDA Status Register		EBh	page 3-190
IrDA CRC Status Register		ECh	page 3-192
IrDA Own Address Register		EDh	page 3-193
IrDA Frame Length Register A		EEh	page 3-194
IrDA Frame Length Register B		EFh	page 3-195
PC Card Configuration Group		F0–F2h	
PC Card Extended Features Register		F0h	page 3-196
PC Card Mode and DMA Control Register		F1h	page 3-198
PC Card Socket A/B Input Termination Control Register		F2h	page 3-200
Reserved		F3–F7h	
Miscellaneous		FFh	
ÉlanSC400 Microcontroller Revision ID Register		FFh	page 3-201

3.2 **REGISTER DESCRIPTIONS**

Each CSC indexed register is described on the following pages. Additional information about using these registers to program the ÉlanSC400 microcontroller can be found in the *ÉlanSC400 User's Manual* (order #21030).

ÉlanSC400 Microcontroller Chip Setup and Control (CSC) I/O Address 0022h Index Register



ÉlanSC400 Microcontroller Chip Setup and Control (CSC) I/O Address 0023h Data Port



DRAM Bank 0 Configuration

	7		6	5	4	3	2	1	0					
Bit	BNK_EN	BL0	Reserved	PG_TYPE0	ASYM0	WIDTH0		DEPTH0[20]						
Default	0		х	0	0	0	0	0	0					
R/W	R/W			R/W	R/W	R/W		R/W						
	Bit	Na	me	Functio	n									
	7	BN	K_ENBL0	Bank 0 0 = Bank	Enable < 0 disabled									
				1 = Banl	<pre>0 enabled</pre>									
				If this DF of the sta	RAM bank is d ate of the refre	lisabled, refrestesh enable bit	sh will not be at CSC index	generated to it < 5h[6].	regardless					
	6	Re	served	Reserve During re	Reserved During read/modify/write operations, software must preserve this bit.									
	5	PG	_TYPE0	Bank 0 0 = Fast	Bank 0 DRAM Page Type 0 = Fast page DRAM									
				1 = Hype	1 = Hyper page (Extended Data Out) DRAM									
	4	AS	YM0	Bank 0 I 0 = Sym	Bank 0 DRAM Symmetry 0 = Symmetrical addressing									
				1 = Asyr	nmetrical add	ressing								
				This bit s operate program	should only be in the asymmo med to 256 K	e set when the etrical address bits, bit 4 of th	e bank is popu s mode. If the iis register mu	lated with devi bank depth haust be cleared.	ces which Is been					
	3	WI	DTH0	DRAM E 0 = Bank	DRAM Bank 0 Data Width 0 = Bank uses a 16-bit DRAM data width									
				1 = Bank uses a 32-bit DRAM data width										
				When th and MA ² Keyboar	When this bit is set the CASL3–CASL2, CASH3–CASH2, RAS3–RAS2, and MA12 pins will automatically be enabled. When this bit is set, the Keyboard Row signals (KBD_ROW6–KBD_ROW0I) will be unavailable.									
	2–0 DEPTH0[2–0]		PTH0[2-0]	DRAM E This bit f the DRA should c that are bank) de	Bank 0 Data E ield controls th M devices use onfigure this b used to popula opths are:	Depth ne generation ed to populate bit field accord ate this bank.	of RAS and C DRAM bank ling to the dep The supporte	AS based on the D. System boo oth of the DRAI ad device (and the DRAI	ne depth of t software M devices therefore					
				0 0 0 = 2	256 Kbits (Asy	mmetrical add	dressing is no	t supported for	this depth)					
				0 0 1 = 5	512 Kbits									
				0 1 0 = 1	Mbits									
				0 1 1 = 2	2 Mbits									
				1 0 0 = 4	Mbits									
				101=8	8 Mbits									
				1 1 0 = 1	6 Mbits									
				1 1 1 = F	Reserved									

DRAM Bank 1 Configuration

I/O Address 22h/23h Index 01h

	7		6	5	4	3	2	1	0				
Bit	BNK_ENBL1		Reserved	PG_TYPE1	ASYM1	WIDTH1		DEPTH1[2-0]					
Default	0		х	0	0	0	0	0	0				
R/W	R/W			R/W	R/W	R/W		R/W					
	Bit	Na	me	Functio	n								
	7	BN	K_ENBL1	Bank 1 0 = Bank	Bank 1 Enable 0 = Bank 1 disabled								
				1 = Bank	< 1 enabled								
				If this DF of the sta	RAM bank is d ate of the refre	lisabled, refres esh enable bit	sh will not be at CSC index	generated to it < 5h[6].	regardless				
	6	Re	served	Reserve During re	Reserved During read/modify/write operations, software must preserve this bit.								
	5	PG	_TYPE1	Bank 1 0 = Fast	Bank 1 DRAM Page Type 0 = Fast page DRAM								
				1 = Нуре	1 = Hyper page (Extended Data Out) DRAM								
	4	AS	YM1	Bank 1 0 = Sym	Bank 1 DRAM Symmetry 0 = Symmetrical addressing								
				1 = Asyr	nmetrical add	ressing							
				This bit s operate program	This bit should only be set when the bank is populated with devices which operate in the asymmetrical address mode. If the bank depth has been programmed to 256 Kbits, bit 4 of this register must be cleared.								
	3	WI	DTH1	DRAM E 0 = 16-b	DRAM Bank 1 Data Width 0 = 16-bit DRAM data width								
				1 = 32 - b	1 = 32-bit DRAM data width								
				When th and MA Keyboar	is bit is set the 12 pins will au d Row signals	e CASL3–CAS tomatically be s (KBD_ROW	SL2, CASH3– enabled. Wh 6–KBD_ROW	CASH2, RAS3 en this bit is s /0]) will be una	B–RAS2, et, the wailable.				
	2–0	DE	PTH1[2–0]	DRAM E This bit f the DRA should c that are bank) de	DRAM Bank 1 Data Depth This bit field controls the generation of RAS and CAS based on the depth of the DRAM devices used to populate DRAM Bank 1. System boot software should configure this bit field according to the depth of the DRAM devices that are used to populate this bank. The supported device (and therefore bank) depths are:								
				0 0 0 = 2	256 Kbits (Asy	mmetrical add	dressing is no	t supported fo	r this depth)				
				0 0 1 = 5	512 Kbits								
				0 1 0 = 1	Mbits								
				0 1 1 = 2	2 Mbits								
				1 0 0 = 4	1 Mbits								
				101=8	3 Mbits								
				1 1 0 = 1	6 Mbits								
				1 1 1 = F	Reserved								

DRAM Bank 2 Configuration

	7	6	5	4	3	2	1	0					
Bit	BNK_ENB	L2 Reserved	PG_TYPE2	ASYM2	WIDTH2		DEPTH2[2-0]						
Default	0	x	0	0	0	0	0	0					
R/W	R/W		R/W	R/W	R/W		R/W						
	Bit	Name	Functio	Function									
	7	BNK_ENBL2	Bank 2	Enable									
			0 = Banl	k 2 disabled									
			1 = Banl	k 2 enabled									
			If this DF of the sta when thi MA12 pi (KBD_R	of the state of the refresh enable bit at CSC index 5h[6]. Also note that when this bit is set the CASL3–CASL2, CASH3–CASH2, RAS3–RAS2, and MA12 pins will automatically be enabled, and the Keyboard Row signals (KBD_ROW6–KBD_ROW0) will be unavailable.									
	6	Reserved	Reserve During re	Reserved During read/modify/write operations, software must preserve this bit.									
	5	PG_TYPE2	Bank 2 0 = Fast	Bank 2 DRAM Page Type 0 = Fast page DRAM									
			1 = Hype	1 = Hyper page (Extended Data Out) DRAM									
	4	ASYM2	Bank 2 0 = Sym	DRAM Symm metrical addre	etry essing								
			1 = Asyr	nmetrical add	ressing								
			This bit s operate program	should only be in the asymmo- med to 256 K	e set when the etrical addres bits, bit 4 of th	e bank is popu s mode. If the his register mu	ulated with dev bank depth haust be cleared.	ices which as been					
	3	WIDTH2	DRAM E 0 = 16-b	DRAM Bank 2 Data Width 0 = 16-bit DRAM data width									
			1 = 32-b	it DRAM data	width								
			When th and MA Keyboar	is bit is set the 12 pins will au d Row signals	e CASL3–CAS tomatically be s (KBD_ROW	SL2, CASH3- enabled. Wh 6-KBD_ROW	CASH2, RAS3 nen this bit is so /0]) will be una	B–RAS2, et, the vailable.					
	2–0	DEPTH2[2–0]	DRAM E This bit f the DRA should c that are bank) de	Bank 2 Data D iield controls the M devices used configure this be used to populate the are:	Depth ne generation ed to populate bit field accorc ate this bank.	of RAS and C DRAM Bank ling to the de The supporte	CAS based on t < 2. System bo pth of the DRA ed device (and	the depth of ot software M devices therefore					
			0 0 0 = 2	256 Kbits (Asy	mmetrical add	dressing is no	ot supported fo	r this depth)					
			0 0 1 = 5	512 Kbits									
			0 1 0 = 1	I Mbits									
			0 1 1 = 2	2 Mbits									
			1 0 0 = 4	1 Mbits									
			1 0 1 = 8	3 Mbits									
			1 1 0 = 1	16 Mbits									
			111=F	Reserved									

DRAM Bank 3 Configuration

I/O Address 22h/23h Index 03h

	7		6	5	4	3	2	1	0				
Bit	BNK_ENBL3		Reserved	PG_TYPE3	ASYM3	WIDTH3		DEPTH3[2-0]					
Default	0		х	0	0	0	0	0	0				
R/W	R/W			R/W	R/W	R/W		R/W					
	Bit 7	Na i BN	me K_ENBL3	Function Bank 3 I	Function Bank 3 Enable								
				0 = Bank	3 disabled								
				1 = Bank	3 enabled								
				If this DF of the sta set, the 0 will autor KBD_R0	AM bank is d ate of the refree CASL3–CASL matically be e DW0) will be u	lisabled, refrest esh enable bit 2, CASH3–C nabled and the inavailable.	sh will not be <u>at CSC index</u> ASH2, RAS3- e Keyboard R	generated to it 5 <u>5[6].</u> When RAS2, and M ow signals (KI	t regardless this bit is A12 pins 3D_ROW6–				
	6	Re	served	Reserve During re	Reserved During read/modify/write operations, software must preserve this bit.								
	5	PG	_TYPE3	Bank 3 I 0 = Fast	Bank 3 DRAM Page Type 0 = Fast page DRAM								
				1 = Нуре	1 = Hyper page (Extended Data Out) DRAM								
	4	AS	ҮМЗ	Bank 3 I 0 = Sym	DRAM Symm metrical addre	etry essing							
				1 = Asyn	nmetrical add	ressing							
				This bit s operate i program	This bit should only be set when the bank is populated with devices which operate in the asymmetrical address mode. If the bank depth has been programmed to 256 Kbits, bit 4 of this register must be cleared.								
	3	WI	DTH3	DRAM Bank 3 Data Width 0 = 16-bit DRAM data width									
				1 = 32 - b	it DRAM data	width							
				When th and MA1 signals (is bit is set, th ∣2 pins will au KBD_ROW6-	e CASL3–CA tomatically be -KBD_ROW0)	SL2, CASH3- enabled and will be unava	-CASH2, RAS the Keyboard iilable.	3– <mark>RAS2</mark> , Row				
	2–0	DE	PTH3[2–0]	DRAM E This bit f the DRA should c that are bank) de	Bank 3 Data E ield controls th M devices us onfigure this b used to popul pths are:	Depth ne generation ed to populate bit field accord ate this bank.	of RAS and C DRAM Bank ling to the dep The supporte	AS based on t 3. System bo oth of the DRA d device (and	the depth of ot software M devices therefore				
				0 0 0 = 2	256 Kbits (Asy	mmetrical add	dressing is no	t supported fo	r this depth)				
				0 0 1 = 5	12 Kbits								
				0 1 0 = 1	Mbits								
				0 1 1 = 2	Mbits								
				$1 \ 0 \ 0 = 4 \ \text{Mbits}$									
				1 0 1 = 8	Mbits								
				1 1 0 = 1	6 Mbits								
				1 1 1 = F	Reserved								

DRAM Control Register

	7		6	5	4	3	2 1 0								
Bit	EDO_DET	TECT	TWCS	Reserved	TCAS	TCP	TRCD	INTL	/[1–0]						
Default	0		0	х	1	1	1	0	0						
R/W	R/W	r	R/W		R/W	R/W	R/W	R/	W						
	Bit	Na	me	Functio	n										
	7	ED	O_DETECT	EDO DR This bit i zeros to ns) to ge asserted	EDO DRAM Detection This bit is used for automatic EDO DRAM detection. Setting this bit causes zeros to be driven onto D15–D0] of the DRAM bus for one <u>clock</u> period (15 ns) to get rid of data held on the bus. In addition, it inhibits <u>CAS</u> from being asserted for the following DRAM read.										
	6	ΤW	/CS	MWE Se Defines period) a	MWE Setup Time Defines MWE setup time to CAS active (where t = the memory clock period) as follows:										
				0 = 1t											
				1 = 2t											
				When th before a accomm that the DRAM w delayed TRCS pa	is bit is set, th sserting CAS odate system TWCS param vrite, with no a one memory arameter, for	e DRAM Con on write page s with a heavi eter is met on rbitration. This clock period o the same reas	troller delays hit cycles. Th ly loaded MW DRAM read f s will also cau n read page h son.	one memory on his function is the signal, to ground ollowed imme se assertion on hits, to accomm	clock period provided to uarantee diately by a f CAS to be modate the						
	5	Re	served	Reserve During re	ed ead/modify/wr	ite operations	, software mu	st preserve th	is bit.						
	4	тс	AS	CAS Pu Defines	lse Width CAS pulse wi	dth (where t =	the memory	clock period) a	as follows:						
				For bank	s configured	as fast page [DRAM:								
				0 = 3t minimum for CPU/DMA accesses, and 2t for Graphics controller reads											
				1 = 4t minimum for CPU/DMA accesses, and 3t for Graphics controller reads											
				For bank	s configured	as Hyper Pag	e (EDO) DRA	M:							
				0 = 2t m	inimum for all	cycles									
		1 = 3t minimum for all cycles													

Bit	Name	Function
3	ТСР	CAS Precharge Delay Defines CAS precharge delay (where t = the memory clock period) as follows.
		0 = 1t
		1 = 2t
2	TRCD	RAS to CAS Delay Defines RAS to CAS delay (where t = the memory clock period) as follows:
		0 = 3t
		1 = 4t
1–0	INTLV[1–0]	DRAM Interleave Control Defines DRAM interleave options as follows:
		0 0 = Banks 0-3 non-interleaved
		0 1 = Banks 0-1 two-way interleaved, Banks 2-3 non-interleaved
		1 0 = Banks 2-3 two-way interleaved, Banks 0-1 non-interleaved
		1 1 = Banks 0-1 two-way interleaved, Banks 2-3 two-way interleaved
		Only Fast-Page DRAM banks of the same DRAM data bus width (16/32), depth, and symmetry can be interleaved. The DRAM Controller will not permit banks which have been configured as EDO page type to be interleaved, nor will it allow banks having different data widths, depths, or symmetry to be interleaved. Due to the 64 Mbyte maximum DRAM support, interleaving banks programmed as 16 Mbyte x 4 is not supported.

DRAM Refresh Control Register

	7		6	5	4	3	2	1	0		
Bit	Reserve	ed	RFEN	RTOLEN	RTODIS	REFCLK_SEL	SELF_RFSH	RFSH	_SPD		
Default	х		0	0	0	0	0	0	0		
			R/W	R/W	R/W	R/W	R/W	R/	W		
	Bit	Na	me	Function							
	7	Re	served	Reserved During read,	/modify/write	operations, so	ftware must p	reserve this b	it.		
	6	RF	EN	Refresh En 0 = DRAM r	able efresh is disal	oled					
				1 = DRAM r	efresh is enat	bled					
				This bit is pr bank is disa global refres	ovided for tes bled, refresh v sh enable bit.	ting and EDO will not be ger	DRAM detec erated to it re	tion. Note tha gardless of th	t if a DRAM e state of this		
	5	RT	OLEN	N RAS Time-Out Value $0 = RAS$ time-out occurs after 10 μ S							
		1 = \overline{RAS} time-out occurs after 100 μS									
	4	RT	ODIS	RAS Time- 0 = RAS tim	Out Disable e-outs are en	abled					
				1 = RAS tim	e-outs are dis	abled					
				This bit caus time (see bit	ses all RAS si t 5) to guarant	gnals to be pr ee the DRAM	echarged afte TRAS param	er a programm leter.	able length of		
	3	RE	FCLK_SEL	Refresh Cld This bit dete except Susp generate ref is used to ge required for KHz clock in disabled in t	ock Select ermines the inject mode. W resh requests enerate refres extended refr put is always his mode.	out source of t hen this bit is When this bit h requests. Thesh rates, acc used during S	the Refresh T cleared, the 3 t is set, the 82 ne selected cl cording to bits Suspend mode	imer during al 2 KHz clock ir 254 PIT (Time ock will be div 1–0 of this re e, because the	I PMU modes uput is used to r 1, counter 1) rided as gister.The 32 e 8254 PIT is		
	2	SE	LF_RFSH	DRAM Self When set, th bit should or support this	Refresh his bit enables hly be set whe feature.	the Self Refr n the devices	esh option in t which are po	the refresh co pulated in the	ntroller. This DRAM array		
	1–0	RF	SH_SPD	DRAM Refr Determines	esh Request DRAM refres	Speed h request peri	od as follows:				
				0 0 = Refres	sh clock sourc	e divided by 1					
				0 1 = Refres	sh clock sourc	e divided by 2	2				
				1 0 = Refres	sh clock sourc	e divided by 4					
				1 1 = Refres	sh clock sourc	e divided by 8	5				
				When the 32 KHz clock is used as the refresh clock source (controlled by bit this register), both edges (rising and falling) are used. This results in a refres rate of 64,000 per second. Thus, selecting the divide by 1 option results in a refresh interval of 15.6 mS. For the divide by 2, 4, and 8 selections, the refre intervals are 31.2 mS, 62.5 mS, and 125 mS respectively.							
				When the P clock source equal the PI	rogrammable e, only a single T Channel 1 r	Interval Time e edge is used ate when the	[.] (PIT), Chanr I. Therefore, t divide by 1 op	nel 1 is used a he DRAM refr otion is selecte	s the refresh esh rate will d.		

Drive Strength Control Register A

I/O Address	22h/23h
l I	ndex 06h

	7 6		5		4	3	2	1	0				
Bit	D_H	HI_DF	RIVE[1-0]	MA_	_HI_D	RIVE[1–0]	MWE_HI_	DRIVE[1-0]	RAS_HI_E	DRIVE[1-0]			
Default	0		0	0	0		0	0	0	0			
R/W		R	/W		R/	W	R/W R/W						
	Bit	Na	me		Fun	ction							
	7–6	D_	HI_DRIVE[1-	0]	I/O Pad Drive Strength for D15–D0 Selects drive strength of I/O pads for D15–D0 pins, as follows:								
					00	= 24 mA pads	selected						
					0 1 = 12 mA pads selected								
					10 = 18 mA pads selected								
					11:	= Pads are th	ree-stated						
	5–4	5–4 MA_HI_DRIVE[1–0]				Pad Drive Streets drive streets	r ength for M ngth of I/O pa	A12–MA0 ads for MA12–	MA0 pins, as	follows:			
					0 0 :	= 24 mA pads	selected						
					01	= 12 mA pads	selected						
					1 0 = 18 mA pads selected								
					1 1 = Pads are three-stated								
	3–2	M۷	VE_HI_DRIVE	E[1—0]	I/O I Sele	Pad Drive Streects drive stre	r ength for M ngth of I/O pa	WE ads for <u>MWE</u> p	in, as follows:				
					0 0 :	= 24 mA pads	selected						
					01	= 12 mA pads	selected						
					10	= 18 mA pads	selected						
					11:	= Pads are th	ree-stated						
	1–0	1–0 RAS_HI_DRIVE[1-				Pad Drive Streets drive stre	r ength for R angth of I/O pa	AS3–R<u>AS0</u> ads for RAS3–	RAS0 pins, as	s follows:			
					00	= 24 mA pads	selected						
					01	= 12 mA pads	selected						
					1 0 = 18 mA pads selected								
					11:	= Pads are th	ree-stated						

Stren	gth C	ontrol Regis	ster B			I/O	Address Ir	22h/ 1dex
	7	6	5	4	3	2	1	0
Bit		Reser	ved		SA_HI_DI	RIVE[1-0]	SD_HI_D	RIVE[1-(
Default	х	x	х	х	0	0	0	0
R/W					R/	W	R	/W
	3–2	SA_HI_DRIVE[1-	0] I/O Pa Select	g read/modify/v d Drive Stren s drive strengt	vrite operation gth for SA23 - h of I/O pads t	is, software m -SA0 for SA23–SA(nust preserve) pins, as follo	these bi ws:
			$0 \ 0 = 2$ $0 \ 1 = 2$	24 mA pads se 12 mA pads se	lected			
			1 0 = 1	18 mA pads se	elected			
			11=1	Pads are three	-stated			
	1–0	SD_HI_DRIVE[1-	-0] I/O Pa Select	d Drive Stren s drive strengt	gth for SD15- h of I/O pads f	-SD0 for SD15–SD(0 pins, as follo	ows:
			0 0 = 2	24 mA pads se	elected			
			0 1 = 1	12 mA pads se	elected			
			1 0 = 1	18 mA pads se	elected			

1 1 = Pads are three-stated

Programming Notes

Non-Cacheable Window 0 Address Register

I/O Address 022h/023h Index 10h



Non-Cacheable Window 0 Address/Attributes/SMM Register

-

I/O Address 022h/023h Index 11h

_	1		6	5	4	3	1 0					
Bit	Reserv	ed	CACHE_ SMM_EN	FLUSH_ ENTRY_DIS	N	NCWIN0_SIZE[2-0]			ART[25–24]			
Default	0		0	0	0	0	0	0	0			
R/W			R/W	R/W	R/W			R/W				
	Bit	Na	me		Function							
	7	Re	served		Reserved During read/modify/write operations, software must preserve this bit.							
	6	CA	CHE_SMM_E	ΞN	Enable Cachi 0 = Caching is	i ng in SMM disabled in S	MM					
					1 = Caching is	enabled in S	MM					
	5	FL	USH_ENTRY	_DIS	Disable Auto-Flush on SMM Entry 0 = Automatic cache flushing upon SMM entry is enabled							
					1 = Automatic cache flushing upon SMM entry is disabled							
	4–2	NCWIN0_SIZE[2-0]			Window Size Selection Bits Selects one of the five possible window sizes for non-cacheable window 0.							
					0 0 0 = Window Disabled							
				0 0 1 = 64 Kbytes								
					0 1 0 = 128 Kbytes							
					0 1 1 = 256 Kbytes							

1 0 0 = 512 Kbytes 1 0 1 = 1 Mbytes

000000h.

1 1 0 = Window Disabled 1 1 1 = Window Disabled

Start Address Bits SA25–SA24

Contains bits 25–24 of the start address for Non-cacheable Window 0. There are 1024 possible start addresses which reside on 64 Kbytes boundaries in the destination address space. If all ten bits are cleared, the window start address SA25–SA0 would be

~

Programming Notes

NCWIN0_START[25-24]

1–0

Non-Cacheable Window 1 Address Register

I/O Address 022h/023h Index 12h



Non-Cacheable Window 1 Address/Attributes Register I/O Address 022h/023h Index 13h

	7		6	5	4	3	2	1	0	
Bit			Reserved		NCWIN1_SIZE[2–0] NCWIN1_START[25–24]				ART[25–24]	
Default	х		х	х	0	0	0	0	0	
R/W						R/W		R/	W	
	Bit	Na	me		Function					
	7–5 Reserved			Reserved During read/m bits.	odify/write op	erations, softv	vare must pres	serve these		
	4–2	NCWIN1_SIZE[2-0]		2–0]	Window Size Selection Bits Selects one of the five possible window sizes for Non-Cacheable Window 1.					
					0 0 0 = Windo	w Disabled				
					0 0 1 = 64 Kby	/tes				
					0 1 0 = 128 Kb	oytes				
					0 1 1 = 256 Kb	oytes				
					1 0 0 = 512 Kb	oytes				
					1 0 1 = 1 Mbyt	es				
					1 1 0 = Windo	w Disabled				
					1 1 1 = Windo	w Disabled				
	1–0	NC	WIN1_STAR	T[25–24]	Start Address Contains bits 2 1. There are 1 Kbytes bounda are cleared, th be 0000000h.	s Bits SA25-5 25–24 of the s 024 possible s aries in the de le translated w	SA24 tart address for start addresse stination addr vindow start a	or non-cachea es which resid ess space. If ddress SA25-	ble window e on 64 all ten bits -SA0 would	

Cache and VL Miscellaneous Register

I/O Address 22h/23h Index 14h

	7	6	5	4	3	2	1	0
Bit	VIDCACHE	SHUTDN_DET	MMU_DLY	VL_RESET	VL_EN	SW_FLUSH	SW_WB	WBACK
Default	0	0	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W

Bit Name

Function

7	VIDCACHE	Graphics Memory Write-through Caching This bit controls the write-through caching of the graphics memory regions.
		0 = Graphics controller memory areas are not write-through cached
		1 = Graphics controller memory areas are write-through cached
		With this bit set while the graphics controller is configured for any CGA compatible text mode, the fixed size (16 Kbytes) refresh and font buffers will be cached. With this bit set in graphics mode, the variable size refresh buffer (determined by the current graphics mode) will be cached. No font buffer is available in graphics mode. The unified memory architecture allows relocation of these cached areas as defined by indexes 4Dh, 4Eh, and 4Fh in the graphics controller indexed address space (3x4h/3x5h). Except as explained below, the region that is cached is the same size as the buffer.
		For CGA graphics mode, the refresh buffer is 16 Kbytes in size. For paged, non-CGA graphics, although the buffer is 64 Kbytes (with a base address fixed at B8000h in this case), the cached region size depends on the number of bits per pixel that are configured. For 1 BPP, the cached area is 64 Kbytes wide, for 2 or 4 BPP, the cached area is 128 Kbytes wide. For non-paged, non-CGA graphics, the cached region and the buffer sizes are equal. For 1 BPP, the cached area is 64 Kbytes wide, for 2 or 4 BPP, the cached area is 128 Kbytes wide.
6	SHUTDN_DET	CPU Shut Down Cycle Status Bit If the CPU core performs a shutdown cycle, this bit will be set. Software should write this bit to '0b' to clear. This bit is automatically cleared when the master reset is asserted.
5	MMU_DLY	MMU DRAM Access Delay When the ÉlanSC400 microcontroller is operated at 2.7 volts, a wait state must be added to MMU generated DRAM hits.
		0 = Operation at 3.3 volts, no extra wait state required for MMU DRAM hits
		1 = Operation at 2.7 volts, extra wait state automatically inserted for MMU DRAM hits
4	VL_RESET	Vesa Local Bus Reset 0 = VL_RESET deasserted
		1 = VL_RESET asserted
3	VL_EN	Vesa Local Bus Interface Enable 0 = Disabled
		1 = Enabled
		The VL_RESET bit in this register should be asserted during modifications of VL_EN to ensure that changes in the states of the VL-Bus interface pins do not adversely effect VL-Target device(s).
2	SW_FLUSH	S/W Flush Status 0 = Flush special bus cycle not detected
		1 = Flush special bus cycle detected
		This bit is cleared when read. Note that this bit will not be set when the CPU FLUSH signal is asserted. This bit will be set only as a result of detection of the Am486 CPU's bus cycle that accompanies execution of the Am486 CPU's INVD opcode.

Bit	Name	Function
1	SW_WB	S/W Write-back Status 0 = Write-back special bus cycle not detected
		1 = Write-back special bus cycle detected
		This bit is cleared when read. Note that this bit will not be set when the CPU FLUSH signal is asserted. This bit will be set only as a result of detection of the Am486 CPU's bus cycle that accompanies execution of the Am486 CPU's WBINVD opcode.
0	WBACK	CPU Cache Policy Select 0 = Write-through
		1 = Write-back
		This bit is cleared on CPU reset assertions in addition to system resets. Immediately after clearing this bit, the programmer should perform a WBINVD instruction to maintain cache coherency.

Pin Strap Status Register

I/O Address 022h/023h Index 20h

7	6	5	4	3	2	1	0
	Reserved			ENEXTBUF	PCC_BOOT	ROMCSO	CFG[1-0]
х	x	х	х	?	?	?	?
				R	R/W	R/\	N
Bit	Name	Functio	n				
7 <u>4</u>	Reserved	Reserv	ed				
		During	read/modify/w	rite operation	s, software m	ust preserve th	iese bits.
3	ENEXTBUF	Enable Determ pins:	External Buf ines the availa	fer Controls ability of the e	xternal buffer	control signal	on external
		0 = <mark>DBU</mark> GPI	JFOE, DBUFF O_CS4, GPIC	RDH, and DBI D_CS3, and G	JFRDL are no PIO_CS2 pins	t available on s respectively	the
		1 = <mark>DB</mark> U GPI	JFOE, DBUFF O_CS3, and (RDH, and DBI GPIO_CS2 pi	JFRDL are av	ailable on the	GPIO_CS4,
		This bit deasse	is initialized b rtion of the RE	y latching the SET pin.	state of the M	1A3{CFG3} pir	at the
2	PCC_BOOT	Redired Determ decode	ct ROMCS0 to ines which int :	o PC Card So erface will be	ocket A driven with the	e <mark>ROMCS0</mark> (b	oot vector)
		0 = ROM	MCS0 chip sel	ect pin			
		1 =PC (Card Socket A	١			
		This bit deasse control PC Car purpose cause u	is initialized b rtion of the RE the redirectior d interfaces a es or specializ inexpected re	y latching the SET pin. Soft of ROMCSO t run time. The ed application sults.	state of the N ware can writ cycles betwee e ability to writ ns. Improper n	IA2{CFG2} pir e this bit to dy en the ROMCS te this bit is pro- nanipulation of	at the namically 50 pin and the ovided for test this bit will
1–0	ROMCS0CFG[1-0]	ROMCS	50 Data Bus bits configure	Width Status the data bus v the R32BEO	and Control vidth for the d	evices connec	ted to
			ROMCS0CF0	3			
		{CFC	G1} {C	CFG0}	ROMCS0 Wi	dth R32B	FOE Available
		0		0	8-bit		No
		0		1	8-bit		No
		1		0	16-bit		No
		1		1	32-bit		Yes
		These b MA1{CI can dyr these b interfac ROMCS for low m microcc Caution	bits are initializ FG1} pins at the namically char its. If the 32-b e is always fo 50 interface for word of 32-bit portroller and b n: The ability to	zed by latching he deassertion nge the width it interface is rced into Fast or 32-bit opera ROM0 data b e asserted du to write these	g the state of t of the RESE of the ROMCS configured for ROM mode. I tion enables t ous) signal to g ring accesses bits is provide	the MA0{CFG T pin. In addit 50 interface by ROMCS0, the In addition, col he R32BFOE go off the Élan to ROMCS0. d for test purp)} and ion, software writing to ⇒ ROMCS0 ∩figuring the (buffer enable SC400 oses or
	7 x Bit 7-4 3	7 6 Reserved x x Bit Name 74 Reserved 3 ENEXTBUF 2 PCC_BOOT 1-0 ROMCS0CFG[1-0]	7 6 5 Reserved x x x 7-4 Reserved Reserved 7-4 Reserved Reserved 3 ENEXTBUF Enable Determ pins: 0 = DBI GPI 1 1 = DBI GPI 1 1 = DBI GPI 1 2 PCC_BOOT Redired Determ decode 0 = ROM 1 2 PCC_BOOT Redired Determ decode 0 = ROM 1 1 = PCC_BOOT Redired Determ decode 0 = ROM = RED 1 = PCC_BOOT Redired Determ decode 0 = ROM = PC O 1 = PC O This bit deasse 2 = PCC_BOOT ROMCSOCFG[1-0] 1 = PC O These H 0 = ROMCSOCFG[1-0] ROMCSOCFG[1-0] 1 = ROMCSOCFG[1-0] These H MA1{C = ROMCSOCFG[1-0] These H MA1{C = ROMCSOCFG[1-0] E <t< th=""><th>7 6 5 4 Reserved x x x x 3 ENEXTBUF Function 3 ENEXTBUF Enable External But Determines the availa pins: 0 DBUFOE, DBUFF GPIO_CS3, and Q 1 DBUFOE, DBUFF GPIO_CS3, and Q 2 PCC_BOOT Redirect ROMCS0 the Determines which int decode: 2 PCC_BOOT Redirect ROMCS0 the Determines which int decode: 1 = C Card Socket A This bit is initialized b deassertion of the RE control the redirector PC Card interfaces a purposes or specializ cause unexpected re 1-0 ROMCS0CFG[1-0] ROMCS0 Data Bus These bits configure ROMCS0 and enable 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</th><th>7 6 5 4 3 Reserved ENEXTBUF x x x x ? R Bit Name Function 7-4 Reserved Reserved Colspan="2">During read/modify/write operation: 3 ENEXTBUF Support Support Support Colspan="2">Reserved DUFOE, DBUFRDH, and DBU GPIO_CS4, GPIO_CS3, and GPIO_CS2 pin This bit is initialized by latching the deassertion of the RESET pin. Redirect ROMCS0 FO C Card Socket A This bit is initialized by latching the deassertion of the RESET pin. Soft control the redirection of ROMCS0 PCC_BOOT Redirect ROMCS0 Data Bus Width Status This bit is initialized by latching the deassertion of the RESET pin. Soft control the redirection of ROMCS0 PCC_BOOT ROMCS0 Data Bus Width Status Thosoft control</th><th>7 6 5 4 3 2 Reserved ENEXTBUF PCC_BOOT x x x 7 7 R R/W Bit Name Function 7-4 Reserved Reserved During read/modify/write operations, software m 3 ENEXTBUF Enable External Buffer Controls Determines the availability of the external buffer pins: 0 DBUFOE, DBUFRDH, and DBUFRDL are nor GPIO_CS3, and GPIO_CS2 pins respectively. This bit is initialized by latching the state of the N deassertion of the RESET pin. 2 PCC_BOOT Redirect ROMCS0 to PC Card Socket A Determines which interface will be driven with the decode: 0 =ROMCS0 to pselect pin 1 =PC Card Socket A 1=0 ROMCS0CFG[1=0] ROMCS0 cols palect pin 1=0 ROMCS0CFG[1=0] ROMCS0 and enable for signal on ar ROMCS0 cole palect signal on ar ROMCS0 and enable the R32BFOE signal on ar ROMCS0 and enable the R32BFOE signal on ar ROMCS0 with Status and Control These bits are initialized by latching the state of the M deassertion of the data bus width for the d ROMCS0 with NA1(CFG0) pins at the deassertion of the RESET pin. 1=0 ROMCS0CFG[1=0] ROMCS0 Data Bus Width Status and Control These bits configure the data bus width for the d ROMCS0 with A</th><th>7 6 5 4 3 2 1 Reserved ENEXTBUF PCC_BOOT ROMCSOC x PUC_BOT Redirect ROMCS0 to PC Card Socket A Determines which interface will be driven with the ROMCS0 (be 2 PCC_BOOT Redirect ROMCS0 to PC Card Socket A Determines which interface will be driven with the ROMCS0 (be Cerdirect colspan="2">x PCC_BOOT Redirect ROMCS0 to PC Card Socket A This bit is initialized by latching the state of the MA2(CFG2) pin detecode: <td colspan="</th></th></t<>	7 6 5 4 Reserved x x x x 3 ENEXTBUF Function 3 ENEXTBUF Enable External But Determines the availa pins: 0 DBUFOE, DBUFF GPIO_CS3, and Q 1 DBUFOE, DBUFF GPIO_CS3, and Q 2 PCC_BOOT Redirect ROMCS0 the Determines which int decode: 2 PCC_BOOT Redirect ROMCS0 the Determines which int decode: 1 = C Card Socket A This bit is initialized b deassertion of the RE control the redirector PC Card interfaces a purposes or specializ cause unexpected re 1-0 ROMCS0CFG[1-0] ROMCS0 Data Bus These bits configure ROMCS0 and enable 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	7 6 5 4 3 Reserved ENEXTBUF x x x x ? R Bit Name Function 7-4 Reserved Reserved Colspan="2">During read/modify/write operation: 3 ENEXTBUF Support Support Support Colspan="2">Reserved DUFOE, DBUFRDH, and DBU GPIO_CS4, GPIO_CS3, and GPIO_CS2 pin This bit is initialized by latching the deassertion of the RESET pin. Redirect ROMCS0 FO C Card Socket A This bit is initialized by latching the deassertion of the RESET pin. Soft control the redirection of ROMCS0 PCC_BOOT Redirect ROMCS0 Data Bus Width Status This bit is initialized by latching the deassertion of the RESET pin. Soft control the redirection of ROMCS0 PCC_BOOT ROMCS0 Data Bus Width Status Thosoft control	7 6 5 4 3 2 Reserved ENEXTBUF PCC_BOOT x x x 7 7 R R/W Bit Name Function 7-4 Reserved Reserved During read/modify/write operations, software m 3 ENEXTBUF Enable External Buffer Controls Determines the availability of the external buffer pins: 0 DBUFOE, DBUFRDH, and DBUFRDL are nor GPIO_CS3, and GPIO_CS2 pins respectively. This bit is initialized by latching the state of the N deassertion of the RESET pin. 2 PCC_BOOT Redirect ROMCS0 to PC Card Socket A Determines which interface will be driven with the decode: 0 =ROMCS0 to pselect pin 1 =PC Card Socket A 1=0 ROMCS0CFG[1=0] ROMCS0 cols palect pin 1=0 ROMCS0CFG[1=0] ROMCS0 and enable for signal on ar ROMCS0 cole palect signal on ar ROMCS0 and enable the R32BFOE signal on ar ROMCS0 and enable the R32BFOE signal on ar ROMCS0 with Status and Control These bits are initialized by latching the state of the M deassertion of the data bus width for the d ROMCS0 with NA1(CFG0) pins at the deassertion of the RESET pin. 1=0 ROMCS0CFG[1=0] ROMCS0 Data Bus Width Status and Control These bits configure the data bus width for the d ROMCS0 with A	7 6 5 4 3 2 1 Reserved ENEXTBUF PCC_BOOT ROMCSOC x PUC_BOT Redirect ROMCS0 to PC Card Socket A Determines which interface will be driven with the ROMCS0 (be 2 PCC_BOOT Redirect ROMCS0 to PC Card Socket A Determines which interface will be driven with the ROMCS0 (be Cerdirect colspan="2">x PCC_BOOT Redirect ROMCS0 to PC Card Socket A This bit is initialized by latching the state of the MA2(CFG2) pin detecode: <td colspan="</th>

Caution: The ability to write these bits is provided for test purposes or specialized applications, and special external system logic can be required to support this. Improper manipulation of these bits will cause unexpected results.

Linear ROMCSO/Shadow Register

I/O Address 022h/023h Index 21h

	7	6	5	4	3	2	1	0
Bit	BOOT_ CACHE_EN	PCC_ROM1_ EN	SHADOW_EN	ALIASEDBVEC _DIS	BOOTVEC_DIS	CSEG_EN	DSEG_EN	ESEG_EN
Default	х	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	BOOT_CACHE_EN	Boot ROM Region (3FF0000–3FFFFFFh) Cache Control 0 = Disable caching of linear accesses to the boot ROM region
		1 = Enable caching of linear accesses to the boot ROM region
		This bit has no effect if the boot ROM is disabled (CSC index 21h[3] = '1b').
6	PCC_ROM1_EN	Redirect ROMCS1 to PC Card Socket A When this bit is set, all accesses to ROM1 space get redirected to PC Card Socket A (ROMCS1 is disabled). When this bit is cleared, all accesses to ROMCS1 space result in the generation of ROMCS1.
5	SHADOW_EN	Enable Shadowing When this bit is set, linear accesses to any segments that are enabled for linear ROMCS0 decode (see bits 4 and 2–0 of this register) are redirected to DRAM at the same address. When this bit is cleared, linear accesses to any segments that are enable for ROMCS0 decode (see bits 4 and 2–0 of this register) are directed to ROMCS0 at the same address.
4	ALIASEDBVEC_DIS	Disable 00F0000–00FFFFh for Linear ROM0 Decode 0 = Linear accesses to this region cause either ROMCS0 to be generated or a DRAM cycle to be generated based on bit 5 of this register.
		1 = Linear accesses to this region will be directed to the ISA bus or to the target device and address pointed to by one of MMS Windows C–F if such window is located in this region of CPU address space
		If in SMM mode, linear accesses to this region will go to DRAM regardless. Also note that linear accesses to this region generate ROMCS0 by default at power-on reset. This bit functions similarly to bits 2–0 of this register, but the sense of the control bit is inverted.
3	BOOTVEC_DIS	Disable 3FF0000–3FFFFFh for Linear ROM0 Decode 0 = Linear accesses to this region cause ROMCS0 to be generated even if ROM shadowing is enabled via bit 5 of this register
		1 = Linear accesses to this region do not generate ROMCSO Accesses to this region will go to system DRAM, or to the target device and address pointed to by one of MMS Windows C-F if such window is located in this region of CPU address space.
		This bit will be cleared whenever an SRESET of the CPU core is generated (i.e., slow reset, via port EEh, or via port 92h).
2	CSEG_EN	Enable 00C0000–00CFFFFh for Linear ROM0 Decode 0 = Linear accesses to this region will be directed to the ISA bus or to the target device and address pointed to by one of MMS Windows C–F if such window is located in this region of CPU address space
		1 = Linear accesses to this region cause either ROMCS0 to be generated or a DRAM cycle to be generated based on bit 5 of this register

Bit	Name	Function
1	DSEG_EN	Enable 00D0000–00DFFFFh for Linear ROMCS0 Decode 0 = Linear accesses to this region will be directed to the ISA bus or to the target device and address pointed to by one of MMS Windows C–F if such window is located in this region of CPU address space
		1 = Linear accesses to this region cause either ROMCS0 to be generated or a DRAM cycle to be generated based on bit 5 of this register
0	ESEG_EN	Enable 00E0000-00EFFFFh for Linear ROMCS0 Decode 0 = Linear accesses to this region will be directed to the ISA bus or to the target device and address pointed to by one of MMS Windows C–F if such window is located in this region of CPU address space
		1 = Linear accesses to this region cause either ROMCS0 to be generated or a DRAM cycle to be generated based on bit 5 of this register

Programming Notes

MMS Windows may not be located in any segment that is enabled for linear ROMCS0 decode.

Linear ROMCSO Attributes Register

I/O Address 022h/023h Index 22h

	7	6	5	4	3	2	1	0
Bit	CSEG_ CACHE_EN	DSEG_ CACHE_EN	ESEG_ CACHE_EN	FSEG_ CACHE_EN	CSEG_WP	DSEG_WP	ESEG_WP	FSEG_WP
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	CSEG_CACHE_EN	Enable Caching for 00C0000–00CFFFFh Linear Accesses 0 = Caching is disabled for this region
		1 = This region is cacheable
6	DSEG_CACHE_EN	Enable Caching for 00D0000–00DFFFFh Linear Accesses 0 = Caching is disabled for this region
		1 = This region is cacheable
5	ESEG_CACHE_EN	Enable Caching for 00E0000–00EFFFFh Linear Accesses 0 = Caching is disabled for this region
		1 = This region is cacheable
4	FSEG_CACHE_EN	Enable Caching for 00F0000–00FFFFFh Linear Accesses 0 = Caching is disabled for this region
		1 = This region is cacheable
3	CSEG_WP	Write Protect 00C0000–00CFFFFh Linear Accesses 0 = Linear writes to this shadow-able region are enabled
		1 = Linear writes to this shadow-able region are inhibited
2	DSEG_WP	Write Protect 00D0000–00DFFFFh Linear Accesses 0 = Linear writes to this shadow-able region are enabled
		1 = Linear writes to this shadow-able region are inhibited
1	ESEG_WP	Write Protect 00E0000–00EFFFFh Linear Accesses 0 = Linear writes to this shadow-able region are enabled
		1 = Linear writes to this shadow-able region are inhibited
0	FSEG_WP	Write Protect 00F0000–00FFFFFh Linear Accesses 0 = Linear writes to this shadow-able region are enabled
		1 = Linear writes to this shadow-able region are inhibited

Programming Notes

Individual bits in the above register become don't cares if the segment(s) that they refer to are not enabled for linear decode via CSC index 21h.

Use caution when write-protecting a cached region of memory. Doing so can result in cache incoherency since the write protection applies to the external memory device only. Therefore, a write to a cached, write-protected region will result in only the cached copy of the data being updated, but not the copy stored in an external memory device. Caching should be disabled for regions where write protection is enabled.

ROMCSO Configuration Register A

I/O Address 22h/23h Index 23h

	7	6	5	4	3	2	1	0
Bit	Res	erved	CS_EARLY0	FAST_ ROMCS0	ROMCS0_ WS_SLCT	DSIZE	0[1-0]	Reserved
Default	х	x	0	0	0	?	?	х
R/W			R/W	R/W	R/W	F	र	

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	CS_EARLY0	Early Chip Select This bit enables an early chip select for the ROMCS0 interface when set.
		0 = In Fast ROMCS0 mode, ROMCS0 is asserted when the ROMCS0 address decode is true and is synchronized with the ROM controller clock edge. When Fast_ROMCS0 mode is not enabled, ROMCS0 is additionally qualified with the ROM command signal.
		1 = The ROMCS0 signal is generated as a simple, unqualified address decode thus causing the chip select to be generated earlier in the cycle
		For a write cycle where FAST_ROMCS0 = 0, this bit must always be '1b'. For all other cases, this bit can be either '0b' or '1b'.
4	FAST_ROMCS0	ROMCS0 Access Speed This bit selects the speed of the ROMCS0 interface. Fast ROMCS0 mode must be selected in order to enable burst mode ROM operation. In addition, if the x32 interface is configured, the ROM controller is forced into Fast ROM mode always, and this bit becomes a don't care for either read or write access.
		0 = Normal speed (ISA timings) Wait states can be added to the ROM cycles by deasserting the ISA IOCHRDY signal.
		1 = Fast speed Cycles run at the CPU 1x clock rate up to a maximum of <u>33 MHz.</u> Wait states are controlled by bit 3 of this register and the ROMCS0 Configuration Register B.

Bit	Name	Function
3	ROMCS0_WS_SLCT	Select ROMCS0 Wait State Control New "burst mode" ROM devices support faster access times when performing transfers on paragraph boundaries. The first 32-bit access of the transfer occurs using the same timings as a non-burst access, but the subsequent accesses (7 or 3 respectively) that make up a paragraph occur using faster timings. Support for Burst mode ROM devices requires special ROMCS0 wait state handling which is enabled by this bit.
		This bit selects how CPU wait states will be inserted for ROMCS0 accesses. By default, the ROM controller does not use Burst mode ROM timings. All of the following must be true for the ÉlanSC400 ROM controller to use Burst mode ROM timings:
		 This bit must be set.
		 The CPU is requesting a burst transfer to support a cache line fill, etc. Thus, the burst mode ROM access will occur on a paragraph boundary only.
		 Caching is enabled for the ROM access.
		 The Fast_ROMCS0 bit is set.
		This bit has no effect if FAST_ ROMCS0 = '0b'. Assuming FAST_ROMCS0 = '1b':
		0 = Use wait states as defined by CSC index 24h[2–0] for all ROMCS0 accesses.
		1 = Use wait states as defined by CSC index 24h[2–0] for all non-burst ROMCS0 accesses. For burst ROMCS0 accesses, use the wait states as defined by CSC index 24h[2-0] for the first access of the burst, and then use the wait states defined by CSC index 24h[4-3] for the other accesses which make up the burst.
2–1	DSIZE0[1-0]	ROMCSO Data Bus Width Status These two bits can be read back to determine the \overline{ROMCSO} data bus width which is set via pin strapping options, and latched at power-on reset.
		0 x = 8-bit device
		1 0 = 16-bit device
		1 1 = 32-bit device
		If the x32 interface is configured, the ROM controller is forced into Fast ROM mode always. See bits 1–0 of the Pin Strap Status Register (CSC index register 20h) for more detail on ROMCS0 width control.
0	Reserved	Reserved During read/modify/write operations, software must preserve this bit.

ROMCSO Configuration Register B

I/O Address 22h/23h Index 24h

<u> </u>	7	6	5	4	3	2	1	0		
Bit		Reserved		WAIT_BR	ST0[1–0]	W	AIT_NBRST0[2-	-0]		
Default	х	x	х	0	0	0	0	1		
R/W				R/W R/W						
	Bit	Name	Funct	tion						
	7–5	Reserved	Rese During	 Reserved During read/modify/write operations, software must preserve these bits Wait States for Burst Access When Fast ROM mode for ROMCS0 is enabled, these two bits program the ROMCS0 interface wait states for all cycles of a burst access that occur after the initial cycle. The wait state starts at the transition of SA3–SA0 during burst cycles. When Fast ROM mode for ROMCS0 is disabled, these bits have no effect. 						
	4–3	WAIT_BRST0[1-	-0] Wait S When the Ro occur SA3 disabl							
			0 0 =	0 wait states						
			0 1 =	1 wait states						
			1 0 =	2 wait states						
			11=	3 wait states						
	2–0	WAIT_NBRST0[2–0] Wait : When progra additio these acces have	Wait States for Non-burst Mode When Fast ROM mode for ROMCS0 is enabled, these three bits program the ROMCS0 interface wait states for non-burst mode. In addition, if Fast ROM mode and burst mode for ROMCS0 is enabled, these three bits select the number of wait states generated for the initial access of burst sequence. When FAST_ROMCS0 is disabled, these bits have no effect.						
			000	= 0 wait states	;					
			001	= 1 wait states	i					
			 1 1 1 1	= 7 wait states	i					

Programming Notes

The value programmed for the WAIT_NBRST0 parameter must be greater than or equal to the value programmed for the WAIT_BRST0 parameter. Failure to do this will result in incorrect ROM controller operation.

ROMCS1 Configuration Register A

I/O Address 22h/23h Index 25h

	7	6	5	4	3	2	1	0
Bit	Res	served	CS_EARLY1	FAST_ ROMCS1	ROMCS1_ WS_SLCT	DSIZE1[1-0]		Reserved
Default	х	х	0	0	0	0	0	х
R/W			R/W	R/W	R/W	R	/W	

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	CS_EARLY1	Early Chip Select This bit enables an early chip select for the $\overline{\text{ROMCS1}}$ interface when set.
		0 = In Fast ROMCS1 mode, ROMCS1 is asserted when the ROMCS1 address decode is true and is synchronized with the ROM controller clock edge. When Fast_ROMCS1 mode is not enabled, ROMCS1 is additionally qualified with the ROM command signal.
		1 = The ROMCS1 signal is generated as a simple, unqualified address decode thus causing the chip select to be generated earlier in the cycle
		For a write cycle where FAST_ROMCS1 = 0, this bit must always be '1b'. For all other cases, this bit can be either '0b' or '1b'.
4	FAST_ROMCS1	ROMCS1 Access Speed This bit selects the speed of the ROMCS1 interface. Fast ROMCS1 mode must be selected in order to enable burst mode ROM operation. In addition, if the x32 interface is configured, the ROM controller is forced into Fast ROMCS1 mode always, and this bit becomes a don't care for either read or write access.
		0 = Normal speed (ISA timings) Wait states can be added to the ROM cycles by deasserting the ISA IOCHRDY signal.
		1 = Fast speed Cycles run at the CPU 1X clock rate up to a maximum of <u>33 MHz.</u> Wait states are controlled by bit 3 of this register and the ROMCS1 Configuration Register B.

Bit	Name	Function
3	ROMCS1_WS_SLCT	Select ROMCS1 Wait State Control New "burst mode" ROM devices support faster access times when performing transfers on paragraph boundaries. The first 32-bit access of the transfer occurs using the same timings as a non-burst access, but the subsequent accesses (7 or 3 respectively) that make up a paragraph occur using faster timings. Support for Burst mode ROM devices requires special ROMCS1 wait state handling which is enabled by this bit.
		This bit selects how CPU wait states will be inserted for ROMCS1 accesses. By default, the ROM controller does not use Burst mode ROM timings. All of the following must be true for the ÉlanSC400 ROM controller to use Burst mode ROM timings:
		 This bit must be set.
		 The CPU is requesting a burst transfer to support a cache line fill, etc. Thus, the burst mode ROM access will occur on a paragraph boundary only.
		 Caching is enabled for the ROM access.
		 The Fast_ROMCS1 bit is set.
		This bit has no effect if FAST_ROMCS1 = '0b'. Assuming FAST_ROMCS1 = '1b':
		0 = Use wait states as defined by CSC index 24h[2–0] for all ROMCS1 accesses.
		1 = Use wait states as defined by CSC index 24h[2–0] for all non-burst ROMCS1 accesses. For burst ROMCS1 accesses, use the wait states as defined by CSC index 24h[2-0] for the first access of the burst, and then use the wait states defined by CSC index 24h[4-3] for the other accesses which make up the burst.
2–1	DSIZE1[1-0]	ROMCS1 Data Bus Width Status and Control These two bits can be read back to determine the ROMCS1 data bus width which is set via pin strapping options, and latched at power-on reset.
		0 = 8-bit device
		1 0 = 16-bit device
		1 = 32-bit device
		If the 32-bit interface is configured for ROMCS1, the ROMCS1 interface is always forced into Fast ROM mode. Also note that configuring the ROMCS1 or ROMCS2 interfaces for 32-bit operation does not enable the R32BFOE signal. This signal will be driven from the ÉlanSC400 microcontroller only if the ROMCS0 interface is enabled for 32-bit operation, and only then for accesses to the ROMCS0 interface.
0	Reserved	Reserved During read/modify/write operations, software must preserve this bit.

ROMCS1 Configuration Register B

I/O Address 22h/23h Index 26h

	7		6	5	4	3	2	1	0		
Bit			Reserved		WAIT_BR	ST1[1–0]	W	AIT_NBRST1[2-	-0]		
Default	x x		х	0	0	0	0	0			
R/W					R/W R/W						
	Bit	Nan	ne	Fu	Inction						
	7–5	Res	erved	Re Du	Reserved During read/modify/write operations, software must preserve these bits. Wait States for Burst Access When Fast ROM mode for ROMCS1 is enabled, these two bits program the ROMCS1 interface wait states for all cycles of a burst access that occur after the initial cycle. The wait state starts at the transition of SA3–SA0 during burst cycles. When Fast ROM mode for ROMCS1 is disabled, these bits have no effect.						
	4–3	WA	IT_BRST1[1-	-0] W W the oc S <i>A</i> dis							
				0 (0 = 0 wait states						
				0	1 = 1 wait states						
				1 (0 = 2 wait states						
				1	1 = 3 wait states						
	2–0	WA	IT_NBRST1[2–0] W W pro ad the ac bit	Wait States for Non-burst Access When Fast ROM mode for ROMCS1 is enabled, these three bits program the ROMCS1 interface wait states for non-burst mode. In addition, if Fast ROM mode and burst mode for ROMCS1 is enabled, these three bits select the number of wait states generated for the initial access of burst sequence. When FAST_ROMCS1 is disabled, these bits have no effect.						
				0	0 0 = 0 wait state	es					
				0	0 1 = 1 wait state	es					
				 1	 1 1 = 7 wait state	es					

Programming Notes

The value programmed for the WAIT_NBRST1 parameter must be greater than or equal to the value programmed for the WAIT_BRST1 parameter. Failure to do this will result in incorrect ROM controller operation.

ROMCS2 Configuration Register A

I/O Address 22h/23h Index 27h

	7	6	5	4	3	2	1	0
Bit	Res	erved	CS_EARLY2	FAST_ ROMCS2	ROMCS2_ WS_SLCT	DSIZE	2[1–0]	Reserved
Default	х	х	0	0	0	0	0	х
R/W			R/W	R/W	R/W	R	/W	

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	CS_EARLY2	Early Chip Select This bit enables an early chip select for the ROMCS2 interface when set.
		0 = In Fast ROMCS2 mode, ROMCS2 is asserted when the ROMCS2 address decode is true and is synchronized with the ROM controller clock edge. When Fast_ROMCS2 mode is not enabled, ROMCS2 is additionally qualified with the ROM command signal.
		1 = The ROMCS2 signal is generated as a simple, unqualified address decode thus causing the chip select to be generated earlier in the cycle.
		For a write cycle where FAST_ROMCS2 = 0, this bit must always be '1b'. For all other cases, this bit can be either '0b' or '1b'.
4	FAST_ROMCS2	ROMCS2 Access Speed This bit selects the speed of the ROMCS2 interface. Fast ROMCS2 mode must be selected in order to enable burst mode ROM operation. In addition, if the x32 interface is configured, the ROM controller is forced into Fast ROMCS2 mode always, and this bit becomes a don't care for either read or write access.
		0 = Normal speed (ISA timings) Wait states can be added to the ROM cycles by deasserting the ISA IOCHRDY signal.
		1 = Fast speed Cycles run at the CPU 1X clock rate up to a maximum of <u>33 MHz</u> . Wait states are controlled by bit 3 of this register and the ROMCS2 Configuration Register B.

Bit	Name	Function
3	ROMCS2_WS_SLCT	Select ROMCS2 Wait State Control New "burst mode" ROM devices support faster access times when performing transfers on paragraph boundaries. The first 32-bit access of the transfer occurs using the same timings as a non-burst access, but the subsequent accesses (7 or 3 respectively) that make up a paragraph occur using faster timings. Support for Burst mode ROM devices requires special ROMCS2 wait state handling which is enabled by this bit.
		This bit selects how CPU wait states will be inserted for ROMCS2 accesses. By default, the ROM controller does not use Burst mode ROM timings. All of the following must be true for the ÉlanSC400 ROM controller to use Burst mode ROM timings:
		 This bit must be set.
		 The CPU is requesting a burst transfer to support a cache line fill, etc. Thus, the burst mode ROM access will occur on a paragraph boundary only.
		 Caching is enabled for the ROM access.
		 The Fast_ROMCS2 bit is set.
		This bit has no effect if FAST_ROMCS2 = '0b'. Assuming FAST_ROMCS2 = '1b':
		0 = Use wait states as defined by CSC index 24h[2–0] for all ROMCS2 accesses.
		1 = Use wait states as defined by CSC index 24h[2–0] for all non-burst ROMCS2 accesses. For burst ROMCS2 accesses, use the wait states as defined by CSC index 24h[2-0] for the first access of the burst, and then use the wait states defined by CSC index 24h[4-3] for the other accesses which make up the burst.
2–1	DSIZE2[1-0]	ROMCS2 Data Bus Width Status and Control These two bits can be read back to determine the ROMCS2 data bus width which is set via pin strapping options, and latched at power-on reset.
		0 x = 8-bit device
		1 0 = 16-bit device
		1 1 = 32-bit device
		If the 32-bit interface is configured for ROMCS2, the ROMCS2 interface is always forced into Fast ROMCS2 mode. Also note that configuring the ROMCS1 or ROMCS2 interfaces for 32-bit operation does not enable the R32BFOE signal. This signal will be driven from the ElanSC400 microcontroller only if the ROMCS0 interface is enabled for 32-bit operation, and only then for accesses to the ROMCS0 interface.
0	Reserved	Reserved During read/modify/write operations, software must preserve this bit.

ROMCS2 Configuration Register B

I/O Address 22h/23h Index 28h

	7	6	5	4	3	2	1	0		
Bit		Reserved		WAIT_BRST2[1-0]		WAIT_NBRST2[2-0]				
Default	х	x	х	0	0	0	0	0		
R/W	·			R/	N	R/W				
	Bit	Name	Funct	ion						
	7–5	Reserved	Reser During	r ved g read/modify/\	write operatio	ns, software r	nust preserve	these bits.		
	4–3 WAIT_BRST2[1–0] Wait States for Burst Mode When Fast ROM mode for ROMCS2 is enabled, these two bits progra the ROMCS2 interface wait states for all cycles of a burst access that occur after the initial cycle. The wait state starts at the transition of SA3–SA0 during burst cycles. When Fast ROM mode for ROMCS2 is disabled, these bits have no effect.							its program cess that ion of MCS2 is		
			0 0 = 0	0 0 = 0 wait states						
			0 1 = 1	0 1 = 1 wait states 1 0 = 2 wait states						
			1 0 = 2							
			11=3	3 wait states						
	2–0	WAIT_NBRST2[Wait States for Non-burst Mode When Fast ROM mode for ROMCS2 is enabled, these three bits program the ROMCS2 interface wait states for non-burst mode. In addition, if Fast ROM mode and burst mode for ROMCS2 is enabled, these three bits select the number of wait states generated for the initial access of burst sequence. When FAST_ROMCS2 is disabled, these bits have no effect. 0 0 0 = 0 wait states 							
			001=	= 1 wait states						
			111:	= 7 wait states						

Programming Notes

The value programmed for the WAIT_NBRST2 parameter must be greater than or equal to the value programmed for the WAIT_BRST2 parameter. Failure to do this will result in incorrect ROM controller operation.

DSIZEx[1-0]	ROMCSx Data Bus Width	ROMCS0_ WS_SLCT	FAST_ ROMCSx	ROMCSx Configuration Summary
0 x	8-bit	don't care	0	8-bit, Normal Speed, Non-Burst
0 x	8-bit	don't care	1	8-bit, Fast Speed, Non-Burst
1 0	16-bit	don't care	0	16-bit, Normal Speed, Non-Burst
1 0	16-bit	0	1	16-bit, Fast Speed, Non-Burst
1 0	16-bit	1	1	16-bit, Fast Speed, Burst Capable
1 1	32-bit	0	don't care	32-bit, Fast Speed, Non-Burst
1 1	32-bit	1	don't care	32-bit, Fast Speed, Burst Capable

Non-burst = Not capable of Burst mode ROM interface timings

Burst capable = Capable of Burst mode ROM interface timings under conditions specified in bit 3 of registers 23h, 25h, and 27h.

MMS Window C-F Attributes Register

I/O Address 022h/023h Index 30h

	7	6	5	4	3	2	1	0
Bit	MMSF_ CACHE_EN	MMSE_ CACHE_EN	MMSD_ CACHE_EN	MMSC_ CACHE_EN	MMSF_WP	MMSE_WP	MMSD_WP	MMSC_WP
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function			
7	MMSF_CACHE_EN	Cache Enable Control for MMS Window F 0 = MMS Window F is non-cacheable			
		1 = MMS Window F is cacheable			
6	MMSE_CACHE_EN	Cache Enable Control for MMS Window E 0 = MMS Window E is non-cacheable			
		1 = MMS Window E is cacheable			
5	MMSD_CACHE_EN	Cache Enable Control for MMS Window D 0 = MMS Window D is non-cacheable			
		1 = MMS Window D is cacheable			
4	MMSC_CACHE_EN	Cache Enable Control for MMS Window C 0 = MMS Window C is non-cacheable			
		1 = MMS Window C is cacheable			
3	MMSF_WP	Write Protect Control for MMS Window F 0 = MMS Window F is not write-protected			
		1 = MMS Window F is write-protected			
2	MMSE_WP	Write Protect Control for MMS Window E 0 = MMS Window E is not write-protected			
		1 = MMS Window E is write-protected			
1	MMSD_WP	Write Protect Control for MMS Window D 0 = MMS Window D is not write-protected			
		1 = MMS Window D is write-protected			
0	MMSC_WP	Write Protect Control for MMS Window C 0 = MMS Window C is not write-protected			
		1 = MMS Window C is write-protected			

Programming Notes

To enable the set up of MMS Windows C–F, the internal PC Card controller must be enabled (D0h[1] = 1), and operating in standard mode (F1h[0] = 0). Once any of MMS Windows C–F are opened (via 3E0/3E1h index space), disabling the internal PC Card controller does not disable the MMS window(s), but disallows re-configuration of them until the internal PC Card controller is re-enabled. MMS Windows C–F are not restricted from being opened in system address space below 64 Kbytes as are the PC Card Socket B Windows 1–4 (which share resources with MMS Windows C–F).

MMS Window C-F Device Select Register

I/O Address 022h/023h Index 31h

	7	6	5	4	3	2	1	0
Bit	MMSF_DEVICE[1-0]		MMSE_DEVICE[1-0]		MMSD_DEVICE[1-0]		MMSC_DEVICE[1-0]	
Default	0	0	0	0	0	0	0	0
R/W	R/W		R/W		R/W		R/W	

Bit	Name	Function				
7–6	MMSF_DEVICE[1-0]	Physical Device Selection Bits for MMS Window F Selects one of the four devices that MMS Window F can be pointed to.				
		0 0 = ROMCS0				
		$0.1 = \overline{\text{ROMCS1}}$				
		$1 0 = \overline{\text{ROMCS2}}$				
		1 1 = System memory (DRAM)				
		MMS Windows C–F are only available if the Mode bit of the PC Card Mode and DMA Control Register (CSC index F1h[0]) is cleared.				
5–4	MMSE_DEVICE[1-0]	Physical Device Selection Bits for MMS Window E Selects one of the four devices that MMS Window E can be pointed to.				
		$0 0 = \overline{\text{ROMCS0}}$				
		$0.1 = \overline{\text{ROMCS1}}$				
		$1 0 = \overline{\text{ROMCS2}}$				
		1 1 = System memory (DRAM)				
		MMS Windows C–F are only available if the Mode bit of the PC Card Mode and DMA Control Register (CSC index F1h[0]) is cleared.				
3–2	MMSD_DEVICE[1-0]	Physical Device Selection Bits for MMS Window D Selects one of the four devices that MMS Window D can be pointed to.				
		$0 0 = \overline{\text{ROMCS0}}$				
		$0 1 = \overline{\text{ROMCS1}}$				
		$1 0 = \overline{\text{ROMCS2}}$				
		1 1 = System memory (DRAM)				
		MMS Windows C–F are only available if the Mode bit of the PC Card Mode and DMA Control Register (CSC index F1h[0]) is cleared.				
1–0	MMSC_DEVICE[1-0]	Physical Device Selection Bits for MMS Window C Selects one of the four devices that MMS Window C can be pointed to.				
		$0 0 = \overline{\text{ROMCS0}}$				
		$0.1 = \overline{\text{ROMCS1}}$				
		$1 0 = \overline{\text{ROMCS2}}$				
		1 1 = System memory (DRAM)				
		MMS Windows C–F are only available if the Mode bit of the PC Card Mode and DMA Control Register (CSC index F1h[0]) is cleared.				

Programming Notes

To enable the set up of MMS Windows C–F, the internal PC Card controller must be enabled (D0h[1] = 1), and operating in standard mode (F1h[0] = 0). Once any of MMS Windows C–F are opened (via 3E0h/3E1h index space), disabling the internal PC Card controller does not disable the MMS window(s), but disallows re-configuration of them until the internal PC Card controller is re-enabled.

MMS Window A Destination Register

I/O Address 022h/023h Index 32h



Programming Notes

MMS Window A is 32 Kbytes wide with a fixed address CPU address range of B0000–B7FFFh.

MMS Window A Destination/Attributes Register

I/O Address 022h/023h Index 33h

	7		6	5	4	3	2	1	0		
Bit	MMSA_DEVICE[1-0]		MMSA_WP	MMSA_ CACHE_EN	MMSA_EN	MMSA_DEST_START[25-23		[25–23]			
Default	0	0 0		0	0	0	0	0	0		
R/W	R/W			R/W	R/W	R/W	R/W				
	Bit Name Function										
	7–6 MMSA_DEVICE[1–0]				Physical Selects or pointed to	Physical Device Selection Bits for MMS Window A Selects one of the four devices that MMS Window A can be pointed to:					
					0.0 = ROI	0 0 = ROMCS0					
					0.1 = ROI	0 1 = ROMCS1					
					1 0 = ROI	1 0 = ROMCS2					
					1 1 = Sys ⁻	1 1 = System memory (DRAM)					
	5 MMSA_WP			Write Pro 0 = MMS	Write Protect bit for MMS Window A 0 = MMS Window A is not write-protected						
					1 = MMS	1 = MMS Window A is write-protected					
	4 MMSA_CACHE_EN			Cache Er 0 = MMS	Cache Enable Bit for MMS Window A 0 = MMS Window A is non-cacheable						
	3 MMSA_EN				1 = MMS	1 = MMS Window A is cacheable					
					Enable B 0 = MMS	Enable Bit for MMS Window A 0 = MMS Window A is disabled					
					1 = MMS	1 = MMS Window A is enabled					
	2–0	MN	/ISA_DEST_S	TART[25–23]	MMSA De Contains Kbytes M addressed destinatio destinatio address S	estination Sta bits 25–23 of 1 MS Window A s which reside n address spa n bits are clea SA25–SA0 wo	art Address Bits SA25–SA23 the destination start address for the 32 A. There are 2048 possible start on 32 Kbytes boundaries in the ace. If all eleven MMS Window A ared, the translated destination start buld be 0000000h.				

MMS Window B Destination Register

I/O Address 022h/023h Index 34h



Programming Notes

MMS Window B is 64 Kbytes wide with a fixed address CPU address range of 100000–10FFFh. This memory region is known as the High Memory Area (HMA). It is mappable in target address space on 32 Kbytes boundaries. The 32 Kbytes boundary support allows access of all target address space even when operating in x86 real mode where the top 16 bytes of the HMA are not available due to CPU addressing limitations.
MMS Window B Destination/Attributes Register

I/O Address 022h/023h Index 35h

	7		6	5	4	3	2	1	0	
Bit	MMS	B_DE	VICE[1-0]	MMSB_WP	MMSB_ CACHE_EN	MMSB_EN	MMSB_	_DEST_START	[25–23]	
Default	0		0	0	0	0	0	0	0	
R/W		R/	Ŵ	R/W	R/W	R/W	R/W			
	Bit	Na	me		Function					
	7–6 MMSB_DEVICE[1–0]				Physical Device Selection Bits for MMS Window B Selects one of the four devices that MMS Window B can be pointed to.					
					0 0 = ROM	MCS0				
					0 1 = RO	MCS1				

		$1 0 = \overline{\text{ROMCS2}}$
		1 1 = System memory (DRAM)
5	MMSB_WP	Write Protect Bit for MMS Window B 0 = MMS Window B is not write-protected
		1 = MMS Window B is write-protected
4	MMSB_CACHE_EN	Cache Enable Bit for MMS Window B 0 = MMS Window B is non-cacheable
		1 = MMS Window B is cacheable
3	MMSB_EN	Enable Bit for MMS Window B 0 = MMS Window B is disabled
		1 = MMS Window B is enabled
2–0	MMSB_DEST_START[25-23]	MMSB Destination Start Address Bits SA25–SA23 Contains bits 25–23 of the destination start address for the 64 Kbytes MMS Window B. There are 2048 possible start addresses which reside on 32 Kbytes boundaries in the

Pin Mux Register A

	7	6	5	4	3	2	1	0
Bit	BL0_CLKIO_SLCT[1-0]		Reserved	GP_EQU_ IOCS16	GP_EQU_ IOCHRDY	GP_EQU_ PIRQ1	GP_EQU_ PIRQ0	GP_EQU_ DMA
Default	0	0	0	0	0	0	0	0
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	BL0_CLKIO_SLCT[1-0]	Select BL0 or CLK_IO Signal If CLK_IO is selected as an input, be sure the pin has a stable 1.19318 MHz frequency on it as it will immediately be switched in as the 8254 timer clock. If CLK_IO is selected as an output, program the frequency to output in the clock control registers of the PMU.
		0 0 = Pin disabled
		$0.1 = \overline{BL0}$ input is available
		1 0 = CLK_IO is available as an output
		1 1 = CLK_IO is available as the timer clock input
5	Reserved	Reserved
4	GP_EQU_IOCS16	Select GPIO_CS5 Signal or ISA IOCS16 0 = GPIO_CS signal is available on this pin
		1 = ISA signal is available on this pin
3	GP_EQU_IOCHRDY	Select GPIO_CS6 Signal or ISA IOCHRDY 0 = GPIO_CS signal is available on this pin
		1 = ISA signal is available on this pin
2	GP_EQU_PIRQ1	Select GPIO_CS7 Signal or ISA PIRQ1 0 = GPIO_CS signal is available on this pin
		1 = ISA signal is available on this pin
1	GP_EQU_PIRQ0	Select GPIO_CS8 Signal or ISA PIRQ0 0 = GPIO_CS signal is available on this pin
		1 = ISA signal is available on this pin
0	GP_EQU_DMA	Select GPIO_CS12-GPIO_CS9 Signals or ISA DMA Signals: PDRQ0, PDACK0, AEN, TC 0 = GPIO_CS signals are available on these pins 1 = ISA signals are available on these pins

Pin Mux Register B

I/O Address 22h/23h Index 39h

	7	6	5	4	3	2	1	0
Bit	Reserved	GPIO_PCPWR _SLCTB	GPIO_PCPWR _SLCTA	GPIO_LBL2 _SLCT	GPIO_KBDCOL _SLCT	ISA_KBDROW _SLCT	PP_PCMB_	_SLCT[1-0]
Default	Х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/	W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	GPIO_PCPWR_SLCTB	Select PC Card Socket B VCC and VPP Control Signals or GPIO Signals
		0 = GPIO18–GPIO16 signals available on these pins
		1 = PC Card PCMB_VPP2, PCMB_VPP1, PCMB_VCC (PC Card Socket B VCC/VPP control signals) available on these pins
5	GPIO_PCPWR_SLCTA	Select PC Card Socket A VCC and VPP Control Signals or GPIO/ GPIO_CS Signals 0 = GPIO15, GPIO_CS14–GPIO_CS13 signals available on these pins
		1 = PC Card PCMA_VPP2, PCMA_VPP1, PCMA_VCC (PC Card Socket A VCC/VPP control signals) available on these pins
4	GPIO_LBL2_SLCT	Select GPIO19 Signal or LBL2 Signal 0 = GPIO19 signal available on this pin
		1 = <u>LBL2</u> signal available on this pin LBL2 is simply an indicator that the PMU is currently in Critical Suspend mode.
3	GPIO_KBDCOL_SLCT	Select Keyboard Column Signals or XT Keyboard Signals 0 = Keyboard Column signals KBD_COL0–KBD_COL1 are available on the pins
		1 = XT keyboard signals XT_CLK, XT_DATA are available on the pins
2	ISA_KBDROW_SLCT	Select Keyboard Row Signals: KBD_ROW12–KBD_ROW7 or Additional ISA Controls: MCS16, SBHE, BALE, PIRQ2, PDRQ1, PDACK1
		1 = Additional ISA controls available
1–0	PP_PCMB_SLCT[1-0]	Select Parallel Port Signals, PC Card Socket B Signals, or GPIOs 0 0 = GPIO 21–GPIO31 signals available on the pins
		0 1 = <u>PC Card Socket B signals WP_B,BVD2_B, BVD1_B, RDY_B,</u> CD_B, REG_B, RST_B, MCEH_B, MCEL_B are available on the pins
		1 0 = Parallel Port signals <u>PPDWE</u> , <u>PPOEN</u> , <u>SL</u> CT, BUSY, <u>ACK</u> , PE, ERROR, INIT, <u>SLCTIN</u> , <u>AFDT</u> , and <u>STRB</u> are available on the pins
		1 1 = Reserved
		The pins used for GPIO21 and GPIO22 are three stated if this option is selected.

Pin Mux Register C

I/O Address 22h/23h Index 3Ah

	7	6	5	4	3	2	1	0
Bit				Rese	erved		WIRED_PIRQ	GPIO_ PCACD_SLCT
Default	Х	х	Х	х	х	Х	0	0
R/W							R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5–2	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
1	WIRED_PIRQ	Wired for PIRQ Inputs Indicator to the ElanSC400 microcontroller that the system is wired to use the PIRQ pins as programmable IRQ inputs versus the matrix keyboard column signals. This allows the hardware to switch in the proper pin termination during suspend when the ISA interface (Power Down Group C) signals are powered won via CSC index E3h[2]. System firmware should initialize this bit at boot time to reflect the pin usage as follows:
		0 = KBD_COL6–KBD_COL2 selected (pull-up used when ISA interface is powered down during suspend)
		1 = PIRQ7–PIRQ3 selected (pull-down used when ISA interface is powered down during suspend)
		This allows the hardware to switch in the proper pin termination during suspend when the ISA interface (Power Down Group C) signals are powered down via CSC index E3h[2].
0	GPIO_PCACD_SLCT	Enable PC Card Socket A Second Card Detect Input or GPIO Signal 0 = GPIO 20 signal available on this pin
		1 = PC Card Socket A second card detect input CD_A2 available

GPIO Termination Control Register A

	7		6	5	4	3	2	1	0			
Bit	CS7_PU	EN	CS6_PUEN	CS5_PUEN	CS4_PUEN	CS3_PUEN	CS2_PUEN	CS1_PUEN	CS0_PUEN			
Default	1		1	1	1	1	1	1	1			
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W			
	Bit	Na	me	Functio	Function							
	7	CS	7_PUEN	GPIO_C 0 = Disa	S7 Pull-up E abled							
				1 = Ena	bled							
	6	CS	6_PUEN	GPIO_C 0 = Disa	S6 Pull-up E abled	nable/Disable	9					
				1 = Ena	1 = Enabled							
	5	CS	5_PUEN	GPIO_C 0 = Disa	GPIO_CS5 Pull-up Enable/Disable 0 = Disabled							
				1 = Ena	1 = Enabled							
	4	CS	4_PUEN	GPIO_C 0 = Disa	GPIO_CS4 Pull-up Enable/Disable 0 = Disabled							
				1 = Ena	bled							
	3	CS	3_PUEN	GPIO_C 0 = Disa	S3 Pull-up E abled	nable/Disable	9					
				1 = Ena	bled							
	2	CS	2_PUEN	GPIO_C 0 = Disa	S2 Pull-up E abled	nable/Disable	9					
				1 = Ena	bled							
	1	CS	1_PUEN	GPIO_C 0 = Disa	S1 Pull-up E	nable/Disable	9					
				1 = Ena	bled							
	0	CS	0_PUEN	GPIO_C 0 = Disa	S0 Pull-up E abled	nable/Disable	9					
				1 = Ena	bled							

Programming Notes

Bits 7–0: The termination state that is specified using bits 7–0 is not actually felt at the pins until the Pin Termination Latch Command bit at CSC index E5[0] is set.

GPIO Termination Control Register B

I/O Address 22h/23h Index 3Ch

	7	6	5	4	3	2	1	0
Bit	GPIO15_ PDEN	CS14_PDEN	CS13_PDEN	CS12_PDEN	CS11_PUEN	CS10_PUEN	CS9_PUEN	CS8_PUEN
Default	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	GPIO15_PDEN	GPIO15 Pull-down Enable/Disable 0 = Disabled
		1 = Enabled
6	CS14_PDEN	GPIO_CS14 Pull-down Enable/Disable 0 = Disabled
		1 = Enabled
5	CS13_PDEN	GPIO_CS13 Pull-down Enable/Disable 0 = Disabled
		1 = Enabled
4	CS12_PDEN	GPIO_CS12 Pull-down Enable/Disable 0 = Disabled
		1 = Enabled
3	CS11_PUEN	GPIO_CS11 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
2	CS10_PUEN	GPIO_CS10 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
1	CS9_PUEN	GPIO_CS9 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
0	CS8_PUEN	GPIO_CS8 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled

Programming Notes

Bits 7–0: The termination state that is specified using bits 7–0 is not actually felt at the pins until the Pin Termination Latch Command bit at CSC index E5[0] is set.

GPIO Termination Control Register C

I/O Address 22h/23h Index 3Dh

	7	6	5	4	3	2	1	0
Bit	GPIO23_ PUEN	GPIO22_ PUEN	GPIO21_ PUEN	GPIO20_ PUEN	GPIO19_ PUEN	GPIO18_ PDEN	GPIO17_ PDEN	GPIO16_ PDEN
Default	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	GPIO23_PUEN	GPIO23 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
6	GPIO22_PUEN	GPIO22 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
5	GPIO21_PUEN	GPIO21 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
4	GPIO20_PUEN	GPIO20 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
3	GPIO19_PUEN	GPIO19 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
2	GPIO18_PDEN	GPIO18 Pull-down Enable/Disable 0 = Disabled
		1 = Enabled
1	GPIO17_PDEN	GPIO17 Pull-down Enable/Disable 0 = Disabled
		1 = Enabled
0	GPIO16_PDEN	GPIO16 Pull-down Enable/Disable 0 = Disabled
		1 = Enabled

Programming Notes

Bits 7–0: The termination state that is specified using bits 7–0 is not actually felt at the pins until the Pin Termination Latch Command bit at CSC index E5h[0] is set.

GPIO Termination Control Register D

I/O Address 22h/23h Index 3Eh

	7	6	5	4	3	2	1	0
Bit	GPIO31_ PUEN	GPIO30_ PUEN	GPIO29_ PUEN	GPIO28_ PUEN	GPIO27_ PUEN	GPIO26_ PUEN	GPIO25_ PUEN	GPIO24_ PUEN
Default	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	GPIO31_PUEN	GPIO31 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
6	GPIO30_PUEN	GPIO30 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
5	GPIO29_PUEN	GPIO29 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
4	GPIO28_PUEN	GPIO28 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
3	GPIO27_PUEN	GPIO27 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
2	GPIO26_PUEN	GPIO26 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
1	GPIO25_PUEN	GPIO25 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled
0	GPIO24_PUEN	GPIO24 Pull-up Enable/Disable 0 = Disabled
		1 = Enabled

Programming Notes

Additional pin termination controls can be found in the keyboard section. See CSC index CAh for more information.

Bits 7–0: The termination state that is specified using bits 7–0 is not actually felt at the pins until the Pin Termination Latch Command bit at CSC index E5h[0] is set.

PMU Force Mode Register

I/O Address 22h/23h Index 40h

	7	6	5	4	3	2	1	0
Bit	LS_TIMER_ CNT	EN_HYPER	EN_SB_LCD	FAST_TIMEO	HS_COUNTING	PMU_FORCE[2-0]		
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R/W		

Bit	Name	Function
7	LS_TIMER_CNT	Low-Speed Timer Count Reset Enable a secondary activity received in Low-Speed mode to reset the Low-Speed Timer.
		0 = Timer not reset
		1 = Timer is reset and count starts over
6	EN_HYPER	Enable Hyper-Speed Mode Enable Hyper-Speed mode to be entered as a result of wake-ups or activity:
		0 = The highest PMU mode that can be entered as a result of wake-ups or activities is High-Speed mode. When this bit is cleared, Hyper-Speed mode can be entered only by writing to the PMU mode force bits in 2–0 of this register.
		1 = Hyper-Speed mode entry as a result of wake-ups or activity is enabled. If this bit is set, and the PMU mode is forced to High Speed mode via bits 2–0 of this register, the PMU mode will jump to High Speed mode momentarily, and will then immediately transition to Hyper-Speed mode.
5	EN_SB_LCD	Enable Graphics Operation in Standby Mode 0 = Graphics controller is disabled when system enters Standby mode
		 1 = Graphics controller is still enabled when system enters Standby mode (only if the Graphics mode was enabled before the PMU enters Standby mode)
4	FAST_TIMEO	Speed Up Suspend and Standby Mode Timers for PMU Code Debug 0 = Use normal PMU mode timer time-outs
		1 = Speed up PMU mode timer time-outs
		Setting this bit speeds up (only) the PMU mode timer time-outs to aid software debug for routines that use the mode timers. When this bit is set, the new delay can be calculated from the following formula: log2(OldValue/30.5) * 30.5
		Where OldValue = the time-out value (in micro seconds) that would be in effect if FAST_TIMEO = 0.

Bit	Name	Function
3	HS_COUNTING	High-Speed Clock Delay Timer Status 0 = Timer has expired, and high speed clock is being used
		1 = Timer is counting, and intermediate clock is being used
		Refer to CSC index 45h[5–3] for more detail.
2–0	PMU_FORCE[2-0]	Force Mode of PMU When written, these bits will force the system into selected PMU mode. When read, these bits return the last value written.
		000 = High-Speed mode
		001 = Hyper-Speed mode
		010 = Low-Speed mode
		011 = Reserved
		100 = Standby mode
		101 = Suspend mode
		110–111 = Reserved
		After writing to CSC index 40h for any reason, at least two falling edges of the 32 KHz clock (as monitored at CSC index 82h[3]) must transpire before subsequent forced PMU mode changes will be recognized.

Programming Notes

Use caution when performing read/modify/write operations to this register. Since the PMU_FORCE bits retain the value of what was last written (as opposed to the current PMU mode), a read/modify/ write operation targeted at changing some other bit in this register may force the ElanSC400 microcontroller into an unexpected PMU mode. After reading and modifying the desired bits, either explicitly set the PMU mode bits to a new desired value or read the current mode from CSC index 41h[1–0] and use this value to program the mode force bits.

PMU Present and Last Mode Register

I/O Address 22h/23h Index 41h

	7		6	5		4	3	2	1	0			
Bit	Reserv	ved	TIME0_NOW		LA	AST_MODE[2-	0]	Reserved	PRES_M	DDE[1-0]			
Default	Х		0	1		1	0	х	0	0			
R/W			W			R			F	8			
	Bit	Na	ame		Func	tion							
	7	Re	eserved		Reserved During read/modify/write operations, software must preserve this bit.								
	6	ТІІ	ME0_NOW		Time Out Now Set this bit to immediately time out the current mode timer. This bit does not need to be cleared and is not read back. Software should not invoke this feature for at least 15 microseconds after a wake-up from Suspend mode. Software can read the last mode from bits 5–3 of this register and delay 15 microseconds if the last mode was Suspend mode before setting this bit.								
	5–3	LA	ST_MODE[2-	-0]	Read Last Mode of PMU When Read will indicate which mode the PMU state machine was in before the present mode.								
					000	= High-Speed	d mode						
					0 0 1 = Hyper-Speed mode								
					010	= Low-Speed	l mode						
					011	= Temporary	Low-Speed n	node					
					100	= Standby me	ode						
					101	= Suspend or	Critical Susp	end mode					
					110	-1 1 1 = Rese	erved						
					Powe of the	r-on reset wil first PMU mo	I set these bits de change to	s to '110b'. Th occur.	is will change	as a result			
	2	Re	eserved		Rese Durin	rved g read/modify	/write operation	ons, software	must preserve	e this bit.			
	1–0	PF	RES_MODE[1-	-0]	Read When	Present Moon Read will income	de of PMU licate which m	node the PMU	state machin	e is in.			
					0 0 =	High-Speed I	node						
					0 1 = Hyper-Speed mode								
					1 0 =	Low-Speed n	node						
					1 1 = Temporary Low-Speed mode								

Hyper/High-Speed Mode Timers

I/O Address 22h/23h Index 42h

	7		6	5	4	3	2	1	0				
Bit		Rese	erved		HS_TIM[2-0]		F	IYPER_TIM[2-()]				
Default	х		х	0	0	0	0	0	0				
R/W					R/W		R/W						
	Bit	Na	me served	Functio	n								
	10	T(C)		During r	During read/modify/write operations, software must preserve these bits.								
	5–3	HS	_TIM[2–0]	High-Si Timer va Low-Sp	High-Speed Timer Value Timer value to count down in High-Speed mode before dropping to Low-Speed mode. Read returns the last value written:								
				0 0 0 = 1	Disabled								
				0 1 0 = 0	0.10 = 0.25 seconds								
				011 = 0	0.0 = 1 second								
				100 =	i second								
				101 = 4	+ Seconds								
				1 1 0 = 0	16 seconds								
	2–0	ΗY	PER_TIM[2-0)] Hyper-\$ Timer va High-Sp	Speed Timer V alue to count of eed mode. Re	/alue lown in Hyper ead returns the	-Speed mode e last value w	e before dropp ritten:	ing to				
				000=	Disabled								
				0 0 1 = 0	0.125 seconds	;							
				0 1 0 = 0	0.25 seconds								
				0 1 1 = 0.5 seconds									
				100 = 100	1 second								
				101 = 4	4 seconds								
				110 = 0	seconas								
				1 1 1 =	1 1 1 = 16 seconds								

Low-Speed/Standby Mode Timers Register

I/O Address 22h/23h Index 43h

	7		6	5	4	3	2	1	0			
Bit		Rese	erved	SB_TIM[2–0]			LS_TIM[2–0]					
Default	х		х	0	0	0	0	0	0			
R/W				R/W R/W								
	Rit	Na	mo	Functio	n							
	7–6	Re	served	Reserve During r	Reserved During read/modify/write operations, software must preserve these bits.							
	5–3	SB	_TIM[2–0]	Standby Timer Value Timer value to count down in Standby mode before dropping to Suspend mode. Read returns the last value written.								
				0 0 0 = 1	Disabled							
				0 0 1 = 1	I minute							
				0 1 0 = 2 minutes								
				0 1 1 = 4 minutes								
				100=8	1 0 0 = 8 minutes							
				101=1	16 minutes							
				110=3	32 minutes							
				111=6	60 minutes							
	2–0	LS <u>.</u>	_TIM[2–0]	Low-Sp Timer va mode. R	eed Timer Va alue to count d lead returns th	alue own in Low-S ne last value w	peed mode be vritten.	efore dropping	to Standby			
				0 0 0 = 1	Disabled							
				0 0 1 = 8	3 seconds							
				0 1 0 = 7	16 seconds							
				011=3	32 seconds							
				100=	I minute							
				101=4	1 minutes							
				1 1 0 = 8	3 minutes							
				111=1	16 minutes							

Suspend/Temporary Low-Speed Mode Timers Register I/O Address 22h/23h Index 44h

	7	6	5	4	3	2	1	0					
Bit		Reserved		SUS_TIM[2-0]			TLS_TIM[2-0]						
Default	х	х	0	0	0	0	0	0					
R/W				R/W			R/W						
	Di4	Nome	Functio	_									
	BIC	Name	Functio	n									
	7-0	Reserved	During r	ead/modify/wr	ite operations	, software m	ust preserve the	ese bits.					
	5–3	SUS_TIM[2-0]	Suspen Timer va cause a written. 0 0 0 = I	Timer value to count down in Suspend mode. On a time-out the timer can cause a wake- up, an SMI/NMI, or nothing. Read returns the last value written. 0 0 0 = Disabled									
			0 0 1 = 1	I minute									
			0 1 0 = 8	3 minutes									
			011=1	$0 \ 1 \ 1 = 16 \ minutes$									
			100=3	32 minutes									
			101=1	l hour									
			1 1 0 = 2	2 hours									
			1 1 1 = 4	1 hours									
	2–0	TLS_TIM[2-0]	Return t Timer va returning	from Tempora alue to count d g to the mode	ary Low-Spectory own in Tempo called by. Rea	ed Mode Tin orary Low-Sp ad returns the	her beed mode befo e last value writ	ore tten.					
			000 = 3	0 µseconds									
			001 = 6	1 µseconds									
			010 = 1	22 µseconds									
			011 = 2	44 µseconds									
			100 = 4	88 µseconds									
			101 = 9	76 µseconds									
			110 = 1	.95 millisecon	ds								
			111 = 3.9 milliseconds										
			When temporary low-speed PMU mode is entered for the purpose of allowing an unmasked NMI or SMI to be serviced, the temporary low-spe mode timer begins counting down. The PMU will not return to its previou mode until the temporary low-speed timer times out. You must clear all pending NMIs before the temporary low-speed time-out will be felt by the PMU. Thus, if you gate off NMIs via port 70h while further NMIs are still pending, the PMU will remain in temporary low-speed mode past the po where the temporary low speed mode timer timed-out.										

Wake-Up Pause/High-Speed Clock Timers Register

I/O	Address	S	22h	23h
	I	n	dex	45h

	7	6	5	4	3	2	1	0					
Bit		Reserved	I	HSCLKSTEP[2-	0]	, v	WAKE_DLY[2-0]					
Default	х	x	0	0	0	0	0	0					
R/W				R/W			R/W						
	Bit	Name	Functio	on									
	7–6	Reserved	Reserv During	r ed read/modify/wr	ite operations	s, software mu	ust preserve th	ese bits.					
	5–3	HSCLKSTEP[2-0] High-S When e mode, t clock w	peed Clock St entering High-S the clock will de ill switch to the	epping peed mode fr efault to 8 MH programmed	rom Suspend z. When this speed if it is	mode or from Timer times ou higher than 8	Standby ut the CPU MHz.					
			If this T speed.	ïmer is disable Read returns tl	d the CPU clo ne last value v	ock will restart written.	at the program	mmed					
			0 0 0 =	0 0 0 = Disabled									
			001=	0 0 1 = 0.125 seconds									
			0 1 0 =	0 1 0 = 0.25 seconds									
			011=	0 1 1 = 0.5 seconds									
			100=	$1 \ 0 \ 0 = 1$ seconds									
			101=	1 0 1 = 2 seconds									
			110=	1 1 0 = 4 seconds									
			111=	1 1 1 = Reserved									
			CSC in (interm	CSC index 40h[3] allows software to determine if this timer is still running (intermediate 8 MHz clock in effect) or whether this timer has expired.									
	2–0	WAKE_DLY[2–0]	Wake-U Timer v started High-S are pro supplie outputs	Wake-Up Timer Delay Timer value to count down after a wake up is sensed and the PLLs are started up (if necessary) and the GPIO_CSx signals are switched to High-Speed (or Low-Speed) mode levels (for those GPIO_CSx signals that are programmed to change based on PMU mode) to allow the power supplies to stabilize before the ElanSC400 microcontroller starts driving its outputs or using its inputs. Read returns the last value written.									
			0 0 0 =	Disabled									
			001=	0.125 seconds									
			010=	0.25 seconds									
			011=	0.5 seconds									
			100=	1 seconds									
			101=	2 seconds									
			110=	4 seconds									
			111=	Reserved									

SUS_RES Pin Configuration Register

I/O Address 22h/23h Index 50h

	7	6	5	4	3	2	1	0		
Bit		Rese	erved		SUS_RES	SUS_RES_CFG[1-0]		_RES[1–0]		
Default	х	х	х	х	0	0	0	0		
R/W	N				R	R/	W			
	Bit	Name		Function						
	7–4	Reserved		Reserved During read/modify/write operations, software must preserve these b						
	3–2	SUS_RES_CFG	6[1–0]	SUS_RES Pin Trigger Configuration 0 0 = Rising edge Suspend/Resume						
				0 1 = Falling edge	Suspend/Res	sume				
				1 0 = Rising edge	Suspend, falli	ng edge Resu	ime			
				1 1 = Rising edge	Resume, fallir	ng edge Suspe	end			
	1–0	EN_SUS_RES[1	1–0]	Enable SUS_RES Pin to Cause Suspend/Resume Function 0 0 = Disabled						
				0 1 = Enabled to c	ause Suspend	b				
				1 0 = Enabled to c	ause Resume	;				
				1 1 = Enabled to c	ause both Sus	spend and Re	sume			

Wake-Up Source Enable Register A

I/O Address 22h/23h Index 52h

	7	6	5	4	3	2	1	0
Bit	Reserved	MKYPRS_ WAKE	SUS_TIMR_ WAKE	SIN_WAKE	Reserved	RIN_WAKE	RTC_WAKE	Reserved
Default	х	0	0	0	0	0	0	Х
R/W		R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	MKYPRS_WAKE	Matrix Keyboard Key Pressed Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
		If this option is enabled, and the system is awakened due to a keypress, no further keypressed wake up will be possible until all matrix keys are released, and a key is again pressed, even after the keypressed wake up status bit has been cleared.
5	SUS_TIMR_WAKE	Suspend Mode Timer Time-Out Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
4	SIN_WAKE	Falling Edge on the Internal UART's Serial Input Pin (SIN) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
3	Reserved	Reserved
2	RIN_WAKE	Falling Edge on the Internal UART's Ring Indicate Pin (RIN) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
1	RTC_WAKE	RTC Alarm (IRQ8) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
0	Reserved	Reserved During read/modify/write operations, software must preserve this bit.

Wake-Up Source Enable Register B

I/O Address 22h/23h Index 53h

	7	6	5	4	3	2	1	0	
Bit	ACIN_WAKE[1-0] BL2_WAKE[1-0]		BL1_WAKE[1-0]		BL0_WAKE[1–0]				
Default	0	0	0	0	0 0		0 0		
R/W	R/	W	R/	R/W		R/W		R/w	

Bit	Name	Function
7–6	ACIN_WAKE[1-0]	ACIN Rising or Falling Edge Wake-Up Control 0 0 = Do not wake up system
		0 1 = Falling edge wake up system
		1 0 = Rising edge wake up system
		1 1 = Either edge wake up system
5–4	BL2_WAKE[1-0]	BL2 Rising or Falling Edge Wake-Up Control 0 0 = Do not wake up system
		0 1 = Falling edge wake up system
		1 0 = Rising edge wake up system
		1 1 = Either edge wake up system
3–2	BL1_WAKE[1-0]	BL1 Rising or Falling Edge Wake-Up Control 0 0 = Do not wake up system
		0 1 = Falling edge wake up system
		1 0 = Rising edge wake up system
		1 1 = Either edge wake up system
1–0	BL0_WAKE[1-0]	BL0 Rising or Falling Edge Wake-Up Control 0 0 = Do not wake up system
		0 1 = Falling edge wake up system
		1 0 = Rising edge wake up system
		1 1 = Either edge wake up system

Wake-Up Source Enable Register C

	7	6	5	4	3	2	1	0
Bit	PDRQ1_WAKE	PDRQ0_WAKE	PIRQ5_WAKE	PIRQ4_WAKE	PIRQ3_WAKE	PIRQ2_WAKE	PIRQ1_WAKE	PIRQ0_WAKE
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	PDRQ1_WAKE	Programmable DMA Request 1 (PDRQ1) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
6	PDRQ0_WAKE	Programmable DMA Request 0 (PDRQ0) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
5	PIRQ5_WAKE	Programmable Interrupt Request 5 (PIRQ5) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
4	PIRQ4_WAKE	Programmable Interrupt Request 4 (PIRQ4) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
3	PIRQ3_WAKE	Programmable Interrupt Request 3 (PIRQ3) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
2	PIRQ2_WAKE	Programmable Interrupt Request 2 (PIRQ2) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
1	PIRQ1_WAKE	Programmable Interrupt Request 1 (PIRQ1) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
0	PIRQ0_WAKE	Programmable Interrupt Request 0 (PIRQ0) Wake-Up Control 0 = Do not wake up system
		1 = Wake up system

Wake-Up Source Enable Register D

	7	6	5	4	3	2	1	0
Bit	Reserved	PCMB_SC_ WAKE	PCMA_SC_ WAKE	PCMB_CD_ WAKE	PCMA_CD_ WAKE	PCMB_INT_ WAKE	PCMA_INT_ WAKE	RI_WAKE
Default	х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit
6	PCMB_SC_WAKE	PC Card Socket B Status Change Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
5	PCMA_SC_WAKE	PC Card Socket A Status Change Wake-Up-up Control 0 = Do not wake up system
		1 = Wake up system
4	PCMB_CD_WAKE	PC Card Socket B Card Detect Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
3	PCMA_CD_WAKE	PC Card Socket A Card Detect Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
2	PCMB_INT_WAKE	PC Card Socket B Interrupt Request Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
1	PCMA_INT_WAKE	PC Card Socket A Interrupt Request Wake-Up Control 0 = Do not wake up system
		1 = Wake up system
0	RI_WAKE	PC Card Ring Indicate Wake-Up Control 0 = Do not wake up system
		1 = Wake up system

Wake-Up Source Status Register A

I/O Address 22h/23h Index 56h

	7	6	5	4	3	2	1	0
Bit	Reserved	MKYPRS_ WOKE	SUS_TIMR_ WOKE	SIN_WOKE	Reserved	RIN_WOKE	RTC_WOKE	SUS_RES_ WOKE
Default	х	0	x	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit
6	MKYPRS_WOKE	Matrix Keyboard Key Pressed Wake-Up Status Write to '0b' to clear wake up status.
		0 = Did not wake up system
		1 = Awakened system
5	SUS_TIMR_WOKE	Suspend Mode Timer Time-Out Wake-Up Status 0 = Did not wake up system
		1 = Awakened system
4	SIN_WOKE	Internal UART Receive Signal Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
3	Reserved	Reserved
2	RIN_WOKE	Internal UART Ring Indicate Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
1	RTC_WOKE	RTC Alarm (IRQ8) Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
0	SUS_RES_WOKE	SUS_RES Pin Wake-Up Status (Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system

Wake-Up Source Status Register B

7	6	5	4	3	2	1	0
ACIN_WOKE		BL2_WOKE		BL1_WOKE		BL0_WOKE	
0	0	0	0	0	0	0	0
R/\	N	R	Ŵ	R/	Ŵ	R/	W
	ACIN_V 0	7 6 ACIN_WOKE 0 0 R/W	7 6 5 ACIN_WOKE BL2_V 0 0 0 R/W R.	7 6 5 4 ACIN_WOKE BL2_WOKE 0 0 0 R/W R/W	7 6 5 4 3 ACIN_WOKE BL2_WOKE BL1_V 0 0 0 0 R/W R/W R/W	7 6 5 4 3 2 ACIN_WOKE BL2_WOKE BL1_WOKE 0 0 0 0 0 R/W R/W R/W R/W	7 6 5 4 3 2 1 ACIN_WOKE BL2_WOKE BL1_WOKE BL0_W 0 0 0 0 0 R/W R/W R/W R/W

Bit	Name	Function
7–6	ACIN_WOKE	ACIN Rising or Falling Edge Wake-Up Status Write to '00b' to clear.
		0 0 = Did not wake up system
		0 1 = Falling edge awakened system
		1 0 = Rising edge awakened system
		1 1 = Reserved
5–4	BL2_WOKE	BL2 Rising or Falling Edge Wake-Up Status Write to '00b' to clear.
		0 0 = Did not wake up system
		0 1 = Falling edge awakened system
		1 0 = Rising edge awakened system
		1 1 = Reserved
3–2	BL1_WOKE	BL1 Rising or Falling Edge Wake-Up Status Write to '00b' to clear.
		0 0 = Did not wake up system
		0 1 = Falling edge awakened system
		1 0 = rising Edge awakened system
		1 1 = Reserved
1–0	BL0_WOKE	BL0 Rising or Falling Edge Wake-Up Status Write to '00b' to clear.
		0 0 = Did not wake up system
		0 1 = Falling edge awakened system
		1 0 = Rising edge awakened system
		1 1 = Reserved

Wake-Up Source Status Register C

I/O Address 22h/23h Index 58h

	7	6	5	4	3	2	1	0
Bit	PDRQ1_ WOKE	PDRQ0_ WOKE	PIRQ5_ WOKE	PIRQ4_ WOKE	PIRQ3_ WOKE	PIRQ2_ WOKE	PIRQ1_ WOKE	PIRQ0_ WOKE
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	PDRQ1_WOKE	Programmable DMA Request 1 (PDRQ1) Wake-Up Status Write to '0b to clear.
		0 = Did not wake up system
		1 = Awakened system
6	PDRQ0_WOKE	Programmable DMA Request 0 (PDRQ0) Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
5	PIRQ5_WOKE	Programmable Interrupt Request 5 (PIRQ5) Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
4	PIRQ4_WOKE	Programmable Interrupt Request 4 (PIRQ4) Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
3	PIRQ3_WOKE	Programmable Interrupt Request 3 (PIRQ3) Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
2	PIRQ2_WOKE	Programmable Interrupt Request 2 (PIRQ2) Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
1	PIRQ1_WOKE	Programmable Interrupt Request 1 (PIRQ1) Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
0	PIRQ0_WOKE	Programmable Interrupt Request 0 (PIRQ0) Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system

Wake-Up Source Status Register D

I/O Address 22h/23h Index 59h

	7	6	5	4	3	2	1	0
Bit	Reserved	PCMB_SC_ WOKE	PCMA_SC_ WOKE	PCMB_CD_ WOKE	PCMA_CD_ WOKE	PCMB_INT_ WOKE	PCMA_INT_ WOKE	RI_WOKE
Default	х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	PCMB_SC_WOKE	PC Card Socket B Status Change Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
5	PCMA_SC_WOKE	PC Card Socket A Status Change Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
4	PCMB_CD_WOKE	PC Card Socket B Card Detect Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
3	PCMA_CD_WOKE	PC Card Socket A Card Detect Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
2	PCMB_INT_WOKE	PC Card Socket B Interrupt Request Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
1	PCMA_INT_WOKE	PC Card Socket A Interrupt Request Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system
0	RI_WOKE	PC Card Ring Indicate Wake-Up Status Write to '0b' to clear.
		0 = Did not wake up system
		1 = Awakened system

GPIO as a Wake-Up or Activity Source Status Register A

I/O Address 22h/23h Index 5Ah

	7	6	5	4	3	2	1	0		
Bit	GP7_WOKE	GP6_WOKE	GP5_WOKE	GP4_WOKE	GP3_WOKE	GP2_WOKE	GP1_WOKE	GP0_WOKE		
Default	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Bit Name		Function	Function						
	7 0	I /_WORL	Write to	'0b' to clear.	u System or		ity			
			0 = Did r	not wake up s	ystem or caus	e activity				
			1 = Awa	kened system	or caused ac	tivity				
	6 G	P6_WOKE	GPIO_C Write to	S6 Awakene '0b' to clear.	d System or	Caused Activ	vity			
			0 = Did r	not wake up s	ystem or caus	e activity				
			1 = Awa	kened system	or caused ac	tivity				
	5 G	P5_WOKE	GPIO_C Write to	S5 Awakene '0b' to clear.	d System or	Caused Activ	rity			
			0 = Did r	not wake up s	ystem or caus	e activity				
			1 = Awa	kened system	or caused ac	tivity				
	4 G	P4_WOKE	GPIO_C Write to	S4 Awakene '0b' to clear.	d System or	Caused Activ	vity			
			0 = Did not wake up system or cause activity							
			1 = Awa							
	3 G	P3_WOKE	GPIO_C Write to	S3 Awakene '0b' to clear.	d System or	Caused Activ	vity			
			0 = Did r	not wake up s	ystem or caus	e activity				
			1 = Awa	kened system	or caused ac	tivity				
	2 G	P2_WOKE	GPIO_C Write to	S2 Awakene '0b' to clear.	d System or	Caused Activ	vity			
			0 = Did not wake up system or cause activity							
			1 = Awa	kened system	or caused ac	tivity				
	1 G	P1_WOKE	GPIO_CS1 Awakened System or Caused Activity Write to '0b' to clear.							
			0 = Did not wake up system or cause activity							
			1 = Awa	kened system	or caused ac	tivity				
	0 G	P0_WOKE	GPIO_C Write to	S0 Awakene '0b' to clear.	d System or	Caused Activ	vity			
			0 = Did r	not wake up s	ystem or caus	e activity				
			1 = Awa	kened system	or caused ac	tivity				

GPIO as a Wake-Up or Activity Source Status Register B

I/O Address 22h/23h Index 5Bh

	7	6	5	4	3	2	1	0
Bit	Reserved	GP14_WOKE	GP13_WOKE	GP12_WOKE	GP11_WOKE	GP10_WOKE	GP9_WOKE	GP8_WOKE
Default	х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	GP14_WOKE	GPIO_CS14 Awakened System or Caused Activity Write to '0b' to clear.
		0 = Did not wake up system or cause activity
		1 = Awakened system or caused activity
5	GP13_WOKE	GPIO_CS13 Awakened System or Caused Activity Write to '0b' to clear.
		0 = Did not wake up system or cause activity
		1 = Awakened system or caused activity
4	GP12_WOKE	GPIO_CS12 Awakened System or Caused Activity Write to '0b' to clear.
		0 = Did not wake up system or cause activity
		1 = Awakened system or caused activity
3	GP11_WOKE	GPIO_CS11 Awakened System or Caused Activity Write to '0b' to clear.
		0 = Did not wake up system or cause activity
		1 = Awakened system or caused activity
2	GP10_WOKE	GPIO_CS10 Awakened System or Caused Activity Write to '0b' to clear.
		0 = Did not wake up system or cause activity
		1 = Awakened system or caused activity
1	GP9_WOKE	GPIO_CS9 Awakened System or Caused Activity Write to '0b' to clear.
		0 = Did not wake up system or cause activity
		1 = Awakened system or caused activity
0	GP8_WOKE	GPIO_CS8 Awakened System or Caused Activity Write to '0b' to clear.
		0 = Did not wake up system or cause activity
		1 = Awakened system or caused activity

GP_CS Activity Enable Register

I/O Address 22h/23h Index 60h

	7	6	5	4	3	2	1	0
Bit	CSD_PRI_ ACT	CSC_PRI_ ACT	CSB_PRI_ ACT	CSA_PRI_ ACT	CSD_IS_ACT	CSC_IS_ACT	CSB_IS_ACT	CSA_IS_ACT
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	CSD_PRI_ACT	GP_CSD Activity Level 0 = Secondary activity
		1 = Primary activity
6	CSC_PRI_ACT	GP_CSC Activity Level 0 = Secondary activity
		1 = Primary activity
5	CSB_PRI_ACT	GP_CSB Activity Level 0 = Secondary activity
		1 = Primary activity
4	CSA_PRI_ACT	GP_CSA Activity Level 0 = Secondary activity
		1 = Primary activity
3	CSD_IS_ACT	GP_CSD Activity Enable 0 = Not activity
		1 = Cause activity
2	CSC_IS_ACT	GP_CSC Activity Enable 0 = Not activity
		1 = Cause activity
1	CSB_IS_ACT	GP_CSB Activity Enable 0 = Not activity
		1 = Cause activity
0	CSA_IS_ACT	GP_CSA Activity Enable 0 = Not activity
		1 = Cause activity

Programming Notes

GP_CSA–GP_CSD are logical concepts with two main functional capabilities that are separately configurable, and in no way dependent upon each other. The GP_CSA–GP_CSD features allow CPU accesses to user defined address ranges to:

- 1. Serve as stimulus to the PMU. GP_CS hits can result in the generation of a PMU primary or secondary activity, or they can cause the PMU to generate an SMI.
- 2. Cause a chip select to be driven off chip. The actual pin that the chip select signal will appear on is user mappable by programming index registers B2h and B3h. GP_CSA and GP_CSB refer primarily to I/O accesses while GP_CSC and GP_CSD refer primarily to memory accesses.

GP_CS Activity Status Register

I/O Address 22h/23h Index 61h

	7	6	5	4	3	2	1	0
Bit		Rese	erved		CSD_WAS_ ACT	CSC_WAS_ ACT	CSB_WAS_ ACT	CSA_WAS_ ACT
Default	Х	х	х	х	0	0	0	0
R/W					R	R	R/W	R/W

Bit	Name	Function
7–4	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
3	CSD_WAS_ACT	GP_CSD Activity State Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
2	CSC_WAS_ACT	GP_CSC Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
1	CSB_WAS_ACT	GP_CSB Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
0	CSA_WAS_ACT	GP_CSA Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity

Activity Source Enable Register A

I/O Address 22h/23h Index 62h

	7	6	5	4	3	2	1	0
Bit	Reserved	VL_IS_ACT	CS1-2_IS_ ACT	CS0_IS_ACT	VID_RAM_ IS_ACT	VID_IO_IS_ ACT	UART2_IO_ IS_ACT	UART1_IO_ IS_ACT
Default	Х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	VL_IS_ACT	Any VL Bus Cycle (memory and I/O) Will Be Activity 0 = Not an activity
		1 = Will be activity
5	CS1-2_IS_ACT	CPU Access to ROMCS2–ROMCS1 Will Be Activity 0 = Not an activity
		1 = Will be activity
4	CS0_IS_ACT	CPU Access to ROMCS0 Will Be Activity 0 = Not an activity
		1 = Will be activity
3	VID_RAM_IS_ACT	CPU Access to Internal Graphics Memory Will Be Activity 0 = Not an activity
		1 = Will be activity
2	VID_IO_IS_ACT	CPU Access to Internal Graphics I/O Will Be Activity 0 = Not an activity
		1 = Will be activity
1	UART2_IO_IS_ACT	CPU Access to UART at COM2 Will Be Activity 0 = Not an activity
		1 = Will be activity
0	UART1_IO_IS_ACT	CPU Access to UART at COM1 Will Be Activity 0 = Not an activity
		1 = Will be activity

Activity Source Enable Register B

	7	6	5	4	3	2	1	0
Bit	Res	erved	KYIO_IS_ ACT	KYTIM_IS_ ACT	TICK_IS_ ACT	IRQ_IS_ACT	DRAM_IS_ ACT	MKYPRS_ IS_ACT
Default	х	x	0	0	0	0	0	0
R/W			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	KYIO_IS_ACT	CPU Access to Keyboard Registers (60h and 64h) Will Be Activity 0 = Not an activity
		1 = Will be activity
4	KYTIM_IS_ACT	Keyboard Timer Time-Out Will Be Activity 0 = Not an activity
		1 = Will be activity
3	TICK_IS_ACT	Timer Tick Interrupt Active (IRQ0) Will Be Activity 0 = Not an activity
		1 = Will be activity
2	IRQ_IS_ACT	Interrupt Active (Not Timer Tick) Will Be Activity 0 = Not an activity
		1 = Will be activity
1	DRAM_IS_ACT	CPU Access to DRAM (Non-Graphics Section Access) Will Be Activity 0 = Not an activity
		1 = Will be activity
0	MKYPRS_IS_AC T	Matrix Keyboard Key Pressed Will Be Activity 0 = Not an activity
		1 = Will be activity
		If this option is enabled, and PMU activity is generated due to a key press, no further keypressed PMU activity will be possible until all matrix keys are released, and a key is again pressed, even after the keypressed activity status bit has been cleared.

Activity Source Enable Register C

I/O Address	; 22h	/23h
l.	ndex	64h

	7		6	5	4	3	2	1	0
Bit	ACIN_IS ACT	S_	DRQ_IS_ACT	IDEIO_IS_ ACT	FDDIO_IS_ ACT	XVGARAM_ IS_ACT	XVGAIO_IS_ ACT	SIN_IS_ACT	RIN_IS_ACT
Default	0		0	0	0	0	0	0	0
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W
	\								
	Bit	Na	me	Fund	ction				
	7	AC	CIN_IS_ACT	ACIN 0 = N	I Signal Will I lot an activity	Be Activity			
				1 = V	Vill be activity				
	6	DR	RQ_IS_ACT	DMA 0 = N	Request Will Not an activity	I Be Activity			
				1 = V	Vill be activity				
	5	ID	EIO_IS_ACT	CPU 0 = N	Access to ID lot an activity	E Hard Drive	e Registers W	ill Be Activit	y
				1 = V	Vill be activity				
	4	FD	DIO_IS_ACT	CPU 0 = N	Access to Fl lot an activity	oppy Contro	ller Registers	s Will Be Acti	vity
				1 = V	Vill be activity				
	3	XV	GARAM_IS_A	ACT CPU 0 = N	Access to Ex lot an activity	xternal VGA	Controller Me	emory Will Be	Activity
				1 = V	Vill be activity				
	2	XV	GAIO_IS_AC	T CPU 0 = N	Access to Ex lot an activity	xternal VGA	Controller I/O	Will Be Acti	vity
				1 = V	Vill be activity				
	1	SI	N_IS_ACT	A Fa Activ 0 = N	Iling Edge on /ity lot an activity	the Internal	UART's Seria	al Input Pin (S	SIN) Will Be
				1 = V	Vill be activity				
	0	RI	N_IS_ACT	A Fa Be A 0 = N	Iling Edge or ctivity lot an activity	the Internal	UART's Ring	Indicate Pin	(RIN) Will
				1 = V	Vill be activity				

Activity Source Enable Register D

I/O Address 22h/23h Index 65h

	7	6	5	4	3	2	1	0
Bit	INTREG_ WAS_ACT	PCINTR_IS_ ACT	PCMRI_IS_ ACT	PCMB_IO_ IS_ACT	PCMB_RAM_ IS_ACT	PCMA_IO_ IS_ACT	PCMA_RAM_ IS_ACT	PP_IO_IS_ ACT
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	INTREG_WAS_ACT	CPU Access to Internal System Registers Will Be Activity 0 = Not an activity
		1 = Will be activity
6	PCINTR_IS_ACT	PMU's PC Card Status Change Interrupt Will Be Activity 0 = Not an activity
		1 = Will be activity
5	PCMRI_IS_ACT	PC Card Ring Indicate Will Be Activity 0 = Not an activity
		1 = Will be activity
4	PCMB_IO_IS_ACT	CPU I/O Access to PC Card Socket B Will Be Activity 0 = Not an activity
		1 = Will be activity
3	PCMB_RAM_IS_ACT	CPU Memory Access to PC Card Socket B Will Be Activity 0 = Not an activity
		1 = Will be activity
2	PCMA_IO_IS_ACT	CPU I/O Access to PC Card Socket A Will Be Activity 0 = Not an activity
		1 = Will be activity
1	PCMA_RAM_IS_ACT	CPU Memory Access to PC Card Socket A Will Be Activity 0 = Not an activity
		1 = Will be activity
0	PP_IO_IS_ACT	CPU Access to Parallel Port Will Be Activity 0 = Not an activity
		1 = Will be activity

Activity Source Status Register A

I/O Address 22h/23h Index 66h

	7	6	5	4	3	2	1	0
Bit	Reserved	VL_WAS_ACT	2_WAS_ACT	CS0_WAS_ ACT	VID_RAM_ WAS_ACT	VID_IO_ WAS_ACT	UART2_IO_ WAS_ACT	UART1_IO_ WAS_ACT
Default	Х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit
6	VL_WAS_ACT	Any VL Bus Cycle (Memory and I/O) Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
5	CS1-2_WAS_ACT	CPU Access to ROMCS2–ROMCS1 Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
4	CS0_WAS_ACT	CPU Access to ROMCS0 Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
3	VID_RAM_WAS_ACT	CPU Access to Internal Graphics Memory Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
2	VID_IO_WAS_ACT	CPU Access to Internal Graphics I/O Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
1	UART2_IO_WAS_ACT	CPU Access to UART at COM2 Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
0	UART1_IO_WAS_ACT	CPU Access to UART at COM1 Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity

Activity Source Status Register B

I/O Address 22h/23h Index 67h

	7	6	5	4	3	2	1	0
Bit	Res	erved	KYIO_WAS_ ACT	KYTIM_ WAS_ACT	TICK_WAS_ ACT	IRQ_WAS_ ACT	DRAM_ WAS_ACT	MKYPRS_ WAS_ACT
Default	х	x	0	0	0	0	0	0
			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	KYIO_WAS_ACT	CPU Access to Keyboard Registers Active (60h and 64h) Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
4	KYTIM_WAS_ACT	Keyboard Timer Time-Out Active Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
3	TICK_WAS_ACT	Timer Tick Interrupt Active (IRQ0) Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
2	IRQ_WAS_ACT	Interrupt Active (Not Timer Tick) Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
1	DRAM_WAS_ACT	CPU Access to DRAM (Non-Graphics Section Access) Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity
0	MKYPRS_WAS_ACT	Matrix Keyboard Key Pressed Activity Status Write to '0b' to clear.
		0 = Not detected as activity
		1 = Detected as activity

Activity Source Status Register C

I/O Address	22h/23h
In	dex 68h

	7		6	5	4	3	2	1	0		
Bit	ACIN_WA ACT	S_	DRQ_WAS_ ACT	IDEIO_WAS_ ACT	FDDIO_ WAS_ACT	XVGARAM_ WAS_ACT	XVGAIO_ WAS_ACT	SIN_WAS_ ACT	RIN_WAS_ ACT		
Default	0		0	0	0	0	0	0	0		
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Bit 7	Nam ACIN	ne N_WAS_AC`	Fu T A (W	Inction CIN Signal Ac rite to '0b' to c	tivity Status lear.					
				0 :	= Not detected	l as activity					
				1 :	= Detected as	activity					
	6	DRG	Q_WAS_ACT	CT DMA Request Activity Status Write to '0b' to clear.							
					= Not detected	l as activity					
					= Detected as	activity					
	5	IDEIO_WAS_ACT CPU Access to IDE Hard Drive Registers Activity Status Write to '0b' to clear.						us			
					0 = Not detected as activity						
					1 = Detected as activity						
	4 FDDIO_WAS_ACT			CT CI W	CPU Access to Floppy Controller Registers Activity Status Write to '0b' to clear.						
				0 :	0 = Not detected as activity						
					1 = Detected as activity						
	3 XVGARAM_WAS_ACT			S_ACT CI W	CPU Access to External VGA Controller Memory Activity Status Write to '0b' to clear.						
					0 = Not detected as activity						
					1 = Detected as activity						
	2 XVGAIO_WAS_ACT			ACT CI W	CPU Access to External VGA Controller I/O Activity Status Write to '0b' to clear.						
					0 = Not detected as activity						
				1 :	1 = Detected as activity						
	1	SIN_	_WAS_ACT	ln W	Internal UART Receive Toggle Activity Status Write to '0b' to clear.						
					0 = Not detected as activity						
	1 = Detected as activity										
	0	RIN_	_WAS_ACT	ln W	Internal UART Ring Indicate Activity Status Write to '0b' to clear.						
				0 :	0 = Not detected as activity						
				1 :	= Detected as	activity					

Activity Source Status Register D

I/O Address 22h/23h Index 69h

	7	6	5	. 4	3	2	1	0		
Bit	INTREG_ WAS_ACT	PCMINTR_ WAS_ACT	PCMRI_ WAS_ACT	PCMB_IO_ WAS_ACT	PCMB_RAM_ WAS_ACT	PCMA_IO_ WAS_ACT	PCMA_RAM_ WAS_ACT	PP_IO_ WAS_ACT		
Default	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Bit Na	ame		Function						
	7 IN	IIREG_WAS_/	ACT	CPU Access to Internal System Registers Activity Status Write to '0b' to clear.						
					0 = Not detected as activity					
				1 = Detected as activity						
	6 P0	CMINTR_WAS	_ACT	PMU's PC Card Status Change Interrupt Activity Status Write to '0b' to clear.						
				0 = Not detected as activity						
				1 = Detected as activity						
	5 P0	CMRI_WAS _A	ACT .	PC Card Ring Indicate Activity Status Write to '0b' to clear.						
				0 = Not detected as activity						
				1 = Detected as activity						
	4 P0	CMB_IO_WAS	_ACT	CPU I/O Access to PC Card Socket B Activity Status Write to '0b' to clear.						
				0 = Not detected as activity						
				1 = Detected as activity						
	3 P	CMB_RAM_W	AS_ACT	CPU Memory Access to PC Card Socket B Activity Status Write to '0b' to clear.						
				0 = Not detected as activity						
				1 = Detected as activity						
	2 PCMA_IO_WAS_ACT			CPU I/O Access to PC Card Socket A Activity Status Write to '0b' to clear.						
				0 = Not detected as activity						
				1 = Detected as activity						
	1 P(CMA_RAM_W	AS_ACT	CPU Memory Access to PC Card Socket A Activity Status Write to '0b' to clear.						
				0 = Not detected as activity 1 = Detected as activity						
	0 PI	P_IO_WAS_A	СТ	CPU Access to Parallel Port Activity Status Write to '0b' to clear.						
				0 = Not detected as activity						
				1 = Detected as activity						
					-					
Activity Classification Register A

I/O Address 22h/23h Index 6Ah

	7	6	5	4	3	2	1	0
Bit	Reserved	VL_SEC_ACT	CS1 - 2_ SEC_ACT	CS0_SEC_ ACT	VID_RAM_ SEC_ACT	VID_IO_ SEC_ACT	UART2_IO_ SEC_ACT	UART1_IO_ SEC_ACT
Default	Х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
6	VL_SEC_ACT	Any VL Bus Cycle (Memory and I/O) Activity Class 0 = Primary activity
		1 = Secondary activity
5	CS1-2_SEC_ACT	CPU Access to ROMCS2–ROMCS1 Activity Class 0 = Primary activity
		1 = Secondary activity
4	CS0_SEC_ACT	CPU Access to ROMCS0 Activity Class 0 = Primary activity
		1 = Secondary activity
3	VID_RAM_SEC_ACT	CPU Access to Internal Graphics Memory Activity Class 0 = Primary activity
		1 = Secondary activity
2	VID_IO_SEC_ACT	CPU Access to Internal Graphics I/O Activity Class 0 = Primary activity
		1 = Secondary activity
1	UART2_IO_SEC_ACT	CPU Access to UART at COM 2 Activity Class 0 = Primary activity
		1 = Secondary activity
0	UART1_IO_SEC_ACT	CPU Access to UART at COM1 Activity Class 0 = Primary activity
		1 = Secondary activity

Activity Classification Register B

I/O Address 22h/23h Index 6Bh

	7 6		5	4	3	2	1	0
Bit	Reserved		KYIO_SEC_ ACT	KYTIM_SEC_ ACT	IRQ0_SEC_ ACT	IRQ_SEC_ ACT	DRAM_SEC_ ACT	MKYPRS_ SEC_ACT
Default	x x		0	0	0	0	0	0
			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	KYIO_SEC_ACT	CPU Access to Keyboard Registers (60h and 64h) Activity Class 0 = Primary activity
		1 = Secondary activity
4	KYTIM_SEC_ACT	Keyboard Timer Time-Out Activity Class 0 = Primary activity
		1 = Secondary activity
3	IRQ0_SEC_ACT	Timer Tick Interrupt Active (IRQ0) Activity Class 0 = Primary activity
		1 = Secondary activity
2	IRQ_SEC_ACT	Interrupt Active (Not Timer Tick) Activity Class 0 = Primary activity
		1 = Secondary activity
1	DRAM_SEC_ACT	CPU Access to DRAM (Non-Graphics Section Access) Activity Class 0 = Primary activity
		1 = Secondary activity
0	MKYPRS_SEC_ACT	Matrix Keyboard Key Pressed Activity Class 0 = Primary activity
		1 = Secondary activity

Activity Classification Register C

I/O Address 22h/23h Index 6Ch

	7	6	5	4	3	2	1	0
Bit	ACIN_SEC_ ACT	DRQ_SEC_ ACT	IDEIO_SEC_ ACT	FDDIO_ SEC_ACT	XVGARAM_ SEC_ACT	XVGAIO_ SEC_ACT	SIN_SEC_ ACT	RIN_SEC_ ACT
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	ACIN_SEC_ACT	ACIN Signal Activity Class 0 = Primary activity
		1 = Secondary activity
6	DRQ_SEC_ACT	DMA Request Activity Class 0 = Primary activity
		1 = Secondary activity
5	IDEIO_SEC_ACT	CPU Access to IDE Hard Drive Registers Activity Class 0 = Primary activity
		1 = Secondary activity
4	FDDIO_SEC_ACT	CPU Access to Floppy Controller Registers Activity Class 0 = Primary activity
		1 = Secondary activity
3	XVGARAM_SEC_ACT	CPU Access to External VGA Controller Memory Activity Class 0 = Primary activity
		1 = Secondary activity
2	XVGAIO_SEC_ACT	CPU Access to External VGA Controller I/O Activity Class 0 = Primary activity
		1 = Secondary activity
1	SIN_SEC_ACT	Falling Edge on Internal UART Serial Input Pin Activity Class 0 = Primary activity
		1 = Secondary activity
0	RIN_SEC_ACT	Falling Edge on Internal UART Ring Indicate Pin Activity Class 0 = Primary activity
		1 = Secondary activity

Activity Classification Register D

I/O Address 22h/23h Index 6Dh

	7	6	5	4	3	2	1	0
Bit	INTREG_ SEC_ACT	PCINTR_ SEC_ACT	PCRI_ SEC _ACT	PCMB_IO_ SEC_ACT	PCMB_RAM_ SEC_ACT	PCMA_IO_ SEC_ACT	PCMA_RAM_ SEC_ACT	PP_IO_SEC_ ACT
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	INTREG_SEC_ACT	CPU Access to Internal System Registers Activity Class 0 = Primary activity
		1 = Secondary activity
6	PCINTR_SEC_ACT	PMU's PC Card Status Change Interrupt Activity Class 0 = Primary activity
		1 = Secondary activity
5	PCRI_SEC _ACT	PC Card Ring Indicate Activity Class 0 = Primary activity
		1 = Secondary activity
4	PCMB_IO_SEC_ACT	CPU I/O Access to PC Card Socket B Activity Class 0 = Primary activity
		1 = Secondary activity
3	PCMB_RAM_SEC_ACT	CPU Memory Access to PC Card Socket A Activity Class 0 = Primary activity
		1 = Secondary activity
2	PCMA_IO_SEC_ACT	CPU I/O Access to PC Card Socket B Activity Class 0 = Primary activity
		1 = Secondary activity
1	PCMA_RAM_SEC_ACT	CPU Memory Access to PC Card Socket A Activity Class 0 = Primary activity
		1 = Secondary activity
0	PP_IO_SEC_ACT	CPU Access to Parallel Port Activity Class 0 = Primary activity
		1 = Secondary activity

Battery/AC Pin Configuration Register A

I/O Address 22h/23h Index 70h

	7	6	5	4	3 2		1	0
Bit	WAS_ SUSPEND	WAS_CRIT_ SUS	SW_ACIN	BL2_CRIT_ SUS	BL1_CFG[1-0]		BL0_CFG[1-0]	
Default	0	0	0	0	0 0		0	0
R/W	R/W	R/W	R/W	R/W	R/W		R/W	

Bit	Name	R/W	Function
7	WAS_SUSPEND	R/W	Suspend Status System has been in Suspend indication. Cleared by writing a 0.
			0 = The system has not been in Suspend mode
			1 = The system has been in Suspend mode since the last time this bit was cleared
6	WAS_CRIT_SUS	R/W	Resumed from Critical Suspend Indication Cleared by writing a 0.
			0 = The system was not forced to Critical Suspend mode by $\overline{BL2}$
			1 = The system has been forced to Critical Suspend mode by $\overline{\text{BL2}}$ since the last time this bit was cleared
5	SW_ACIN	R/W	Software ACIN 0 = Do not force software ACIN
			1 = Force software ACIN
4	BL2_CRIT_SUS	R/W	BL2 Forces Critical Suspend Mode BL2 pin forces PMU Mode to Critical Suspend when BL2 is low
			0 = Disabled, does not force mode change
			1 = Force PMU to Critical Suspend mode when $\overline{BL2}$ is low
			If BL2 is configured to generate an XMI by setting CSC index 93h[5–4] to either 01b or 11b, and BL2 is also configured to go in to Critical Suspend mode when it is low by setting this bit, then Critical Suspend mode will be entered immediately if BL2 occurs. Upon exit from Critical Suspend mode, the XMI will automatically occur.
			Since LBL2 is really a Critical Suspend mode indication, it will never go active if this bit is cleared.

E	Bit	Name	R/W	Function
3.	-2	BL1_CFG[1–0]	R/W	$\label{eq:BL1} \begin{array}{ c c c } \hline \textbf{BL1} \ \textbf{Configuration} \\ \hline \textbf{BL1} \ \textbf{pin} \ \textbf{disables} \ \textbf{Hyper-Speed} \ \textbf{mode} \ \textbf{and} \ \textbf{forces} \ \textbf{High-Speed} \\ \hline \textbf{clock} \ to \ 8.29 \ \textbf{MHz} \ \textbf{when} \ \textbf{BL1} \ \textbf{is} \ \textbf{active} \ \textbf{or} \ \textbf{BL1} \ \textbf{pin} \ \textbf{forces} \ \textbf{PMU} \ \textbf{to} \\ \hline \textbf{disable} \ \textbf{High-Speed} \ \textbf{mode} \ \textbf{when} \ \textbf{active}. \ \textbf{If} \ \textbf{these} \ \textbf{bits} = `01b' \ \textbf{or} \\ `10b' \ \textbf{to} \ \textbf{limit} \ \textbf{the} \ \textbf{PMU} \ \textbf{mode} \ \textbf{to} \ \textbf{High-Speed} \ \textbf{modes} \\ \hline \textbf{respectively} \ \textbf{(via} \ \textbf{CSC} \ \textbf{index} \ 40h[2-0]) \ \textbf{will} \ \textbf{result} \ \textbf{in} \ \textbf{a} \ \textbf{momentary} \\ \hline \textbf{change to} \ \textbf{the} \ \textbf{higher power} \ \textbf{PMU} \ \textbf{mode} \ \textbf{followed} \ \textbf{by} \ \textbf{an immediate} \\ \hline \textbf{drop-back to} \ \textbf{High-Speed} \ \textbf{or} \ \textbf{Low-Speed} \ \textbf{mode} \ \textbf{respectively}. \\ \hline \textbf{Activities} \ \textbf{and} \ \textbf{wake-ups} \ \textbf{will only} \ \textbf{go to} \ \textbf{Low-Speed} \ \textbf{mode}. \end{array}$
				0 0 = Disabled, does not force anything
				0 1 = Force CPU clock to 8MHz in High-Speed mode
				1 0 = Force PMU to Low-Speed as highest mode, disable High-Speed
				1 1 = Reserved
1.	-0	BL0_CFG[1-0]	R/W	BLO Configuration BLO pin disables Hyper-Speed mode and forces High-Speed clock to 8.29MHz when BLO is active or BLO pin forces PMU to disable High-Speed mode when active. If these bits = '01b' or '10b' to limit the PMU mode to High speed or High-Speed modes respectively (via CSC index 40h[2–0]) will result in a momentary change to the higher power PMU mode followed by an immediate drop-back to High-Speed or Low-Speed mode respectively. Activities and wake ups will only go to Low-Speed mode.
				0 0 = Disabled, does not force anything
				0 1 = Force CPU clock to 8 MHz in High-Speed mode
				1 0 = Force PMU to Low-Speed as highest mode, disable High-Speed
				1 1 =Reserved

Battery/AC Pin Configuration Register B

	7	6	5	4	3	2	1	0
Bit		Rese	erved		NOBL1_CS_ LOCK	NOBL2_CS_ LOCK	ACIN_CS_ LOCK	ACIN_KILL_ PMU
Default	Х	х	Х	х	0	0	0	0
R/W					R/W	R/W	R/W	R/W

Bit	Name	Function
7–4	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
3	NOBL1_CS_LOCK	BLx Critical Suspend Unlock Control to force the PMU mode from Critical Suspend to Suspend mode when both BL2 and BL1 are inactive.
		0 = Will change to Suspend mode
		1 = Will stay in Critical Suspend mode
2	NOBL2_CS_LOCK	Inactive BL2 Critical Suspend Unlock Control to allow BL2 being inactive to force the PMU mode from Critical Suspend mode to Suspend mode.
		0 = Will change to Suspend mode
		1 = Will stay in Critical Suspend mode
1	ACIN_CS_LOCK	ACIN Signal Critical Suspend Unlock Disallow ACIN transitioning active from unlocking Critical Suspend mode. Assuming that the PMU is in Critical Suspend mode due to the BL0 pin being driven low, and that this bit is cleared, a transition of the ACIN pin from inactive to active will unlock the PMU from Critical Suspend mode, and cause it to transition into Suspend mode. If BL0 is still active when the ACIN pin transitions active, the PMU will return immediately to Critical Susupend mode. If CSC index 71h[0] is set, this bit will have no effect.
		0 = Will change to Suspend mode
		1 = Will stay in Critical Suspend mode
0	ACIN_KILL_PMU	ACIN Signal Disable PMU Functions Control to allow the assertion of ACIN to disable PMU functions
		0 = Disabled
		1 = Enabled
		If this bit is set, and either the ACIN pin or the software ACIN bit is set (see CSC index 70h[5]), forcing the PMU mode to any mode other than Suspend mode (forcing is done via CSC index 40h[2–0]) will result in the PMU going to the forced mode, and then immediately jumping back to Hyper-Speed or High-Speed PMU mode, whichever is the highest allowed (via CSC index 40h[6]). Forcing the PMU to Suspend mode when this bit is set will cause the PMU to enter Suspend mode.8

Battery/AC Pin State Register

I/O Address 22h/23h Index 72h

	7	6	5	4	3	2	1	0
Bit		Reserved		SUS_RES_ STATE	ACIN_STATE	BL2_STATE	BL1_STATE	BL0_STATE
Default	x	x	Х	0	0	0	0	0
R/W				R	R	R	R	R

Bit	Name	Function
7–5	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
4	SUS_RES_STATE	SUS_RES Pin State
3	ACIN_STATE	ACIN Pin State
2	BL2_STATE	BL2 Pin State
1	BL1_STATE	BL1 Pin State
0	BL0_STATE	BL0 Pin State

CPU Clock Speed Register

7

0

6

CPUCLK_PRES_SP[2-0]

1

R

5

1

0

HYS_CPUCLK

R/W

I/O Address 22h/23h Index 80h

1

0

2

0

HS_CPUCLK[1-0]

R/W

Bit Default R/W

Name	Function
CPUCLK_PRES_SP[2-0]	Present Speed of the CPU Clock For all bit patterns except '110b', the 1x CPU clock is referenced. For bit pattern '110b', refer to bit 0 of this register to determine whether the 2x (66 MHz) is being used. A write to these bits has no effect.
	0 0 0 = 1 MHz
	0 0 1 = 2 MHz
	0 1 0 = 4 MHz
	0 1 1 = 8 MHz
	1 0 0 = 16 MHz
	1 0 1 = 33 MHz
	1 1 0 = Clock-multiplied mode enabled
	1 1 1 = Reserved
LS_CPUCLK[1-0]	CPU Clock Speed in Low-Speed Mode 0 0 = 8.29 MHz
	0 1 = 4.15 MHz
	1 0 = 2.07 MHz
	1 1 = 1.04 MHz
HS_CPUCLK[1-0]	CPU Clock Speed in High-Speed Mode 0 0 = 8.29 MHz
	0 1 = 16.59 MHz
	1 0 = 33.18 MHz
	1 1 = Reserved
HYS_CPUCLK	CPU Clock Speed in Hyper-Speed Mode 0 = Clock doubled (66 MHz)
	1 = Clock tripled (99 MHz)
	The ÉlanSC400 microcontroller may require special packaging to safely support clock-tripled mode. Selection of clock-tripled mode results in much higher heat generation by the device. Selecting clock-tripled mode for an ÉlanSC400 microcontroller device which uses a package that is not specifically approved by AMD for use at clock-tripled speed may result in erratic system operation, loss of data, or damage to the ÉlanSC400 microcontroller device.
	Name CPUCLK_PRES_SP[2-0] LS_CPUCLK[1-0] HS_CPUCLK[1-0] HYS_CPUCLK

4

0

LS_CPUCLK[1-0]

R/W

3

0

CPU Clock Auto Slowdown Register

3–2

SLOW_PERIOD[1-0]

I/O Address 22h/23h Index 81h

	7		6	5	4	3	2	1	0	
Bit	Reserved		ACIN_X	AUTO_ SLOWDOWN	SLOW_PERIOD[1-0]		FAST_PERIOD[1-0]			
Default	х		Х	0	0	0	0	0	0	
R/W				R/W	R/W	R	Ŵ	R/	W	
	Bit 7–6	Na Re:	me served		Function Reserved					
					During read/modify/write operations, software must preserve these bits.					
	5	ACIN_X			Override ACIN for Auto Slowdown Enable auto slowdown to occur even if ACIN is enabled and active. This is a thermal protection measure.					
					0 = Disabled					
					1 = Enabled, u	se bits 4–0 to	o control perio	d		
	4	4 AUTO_SLOWDOWN			Enable Auto Slowdown The PMU modes or states provide a way to trade off performance for processing power in discrete steps. The auto slowdown feature allows the (average power/average performance) to be fine tuned when the PMU is operating in the highest available PMU mode. This can be either be Hyper-Speed mode or High-Speed mode, depending on whether or not Hyper-Speed mode is disabled. Enabling this feature causes the CPU clock to switch between the fast speed and slow speed operating frequencies as defined by the FAST_PERIOD and SLOW_PERIOD bit fields.					
					0 = Auto slowd	own disabled	ł			

1 = Auto slowdown enabled, use bits 3-0 to control period

Slow Clock Duration

When Auto Slowdown is enabled, these bits define how long the CPU clock runs at the slow clock frequency before switching up to run at the fast clock frequency. When the Hyper-Speed PMU mode is enabled, the slow clock frequency will be the High-Speed mode clock frequency. When the Hyper-Speed PMU mode is disabled, the slow clock will equal the Low-Speed mode clock frequency. See the FAST_PERIOD field for further explanation.

- 0 0 = 0.25 seconds
- 0 1 = 0.5 seconds
- 1 0 = 1 seconds
- 11 = 2 seconds

|--|

Bit	Name	Function
1–0	FAST_PERIOD[1–0]	Fast Clock Duration When Auto Slowdown is enabled, these bits define how long the CPU clock runs at the fast clock frequency before switching down to run at the slow clock frequency. When the Hyper-Speed PMU mode is enabled, the fast clock frequency will be the Hyper-Speed mode clock frequency. When the Hyper-Speed PMU mode is disabled, the fast clock will equal the High-Speed mode clock frequency. See the SLOW_PERIOD field for further explanation.
		0 0 = 4 seconds
		0 1 = 8 seconds
		1 0 = 16 seconds
		1 1 = 32 seconds

Clock Control Register

I/O Address 22h/23h Index 82h

	7	6	5	4	3	2	1	0
Bit	Reserved	DMA_C	SLK[1–0]	STB_HS _PLL_DIS	RD_32KHZ	PLL_D	LY[1–0]	SUS_PLL_EN
Default	0	0	1	0	0	0	0	1
R/W	R/W	R/W		R/W	R	R	W	R/W

Bit	Name	Function
7	Reserved	Reserved
6–5	DMA_CLK[1-0]	DMA Controller Clock Frequency Select 0 0 = DC
		0.1 = 4 MHz or CPUCLK, whichever is slower
		1 0 = 8 MHz or CPUCLK, whichever is slower
		1 1 = 16 MHz or CPUCLK, whichever is slower
		8 and 16 MHz operation of the DMA controller is intended for high speed IrDA operation only. This higher speed DMA operation for IrDA transactions may or may not be required depending on overall system latency issues. Timing for ISA and PC Card DMA cycles at DMA controller clock speeds higher than 4 MHz is not specified or guaranteed. Since CPUCLK can run at 2 MHz or 1 MHz, the possible DMA clock speeds are 16, 8, 4, 2, and 1 MHz.
4	STB_HS_PLL_DIS	Disable the High-Speed PLL in Standby mode 0 = High-Speed PLL is enabled
		1 = High-Speed PLL is disabled in Standby mode
3	RD_32KHZ	State of the 32 KHz Clock Read high or low depending on the 32 KHz clock. Writing this bit has no effect.
2–1	PLL_DLY[1-0]	System PLL Restart Delay Time (not the CPU PLL) 0 0 = 32 milliseconds
		0 1 = 16 milliseconds
		1 0 = 8 milliseconds
		1 1 = 4 milliseconds
0	SUS_PLL_EN	All System PLLs enable/disable in Suspend mode (not the CPU
		O = PLLs are disabled in Suspend mode
		1 = PLLs are enabled in Suspend mode

CLK_IO Pin Output Clock Select Register

I/O Address 22h/23h Index 83h

	7	6	5	4	3	2	1	0
Bit		Res	erved			CLK_IO_	SEL[3-0]	
Default	х	x	х	х	1	0	0	0
R/W						R	/W	
	Bit	Name	Fun	ction				
	7–4	Reserved	Res Duri	erved ng read/modify	/write operati	ons, software	must preserve	e these bits
	3–0	CLK_IO_ SEL[3	–0] CLI_ Whe sele	IO Pin Select in the CLK_IO ct the internal	pin is selecte clock that will	d as an outpu be multiplexe	t clock source d out onto this	, these bits pin.
			000	0 0 =UART clo	ck (18.432 MI	Hz)		
			000	01=Reserved				
			0.0	l 0 =Graphics Graphics	dot clock (20. controller mod	736 MHz to 3 de)	6.864 MHz de	pending on
			0.0	1 1 =CPU cloc MHz, 1.04	k (33.18 MHz) 1 MHz)	,16.59 MHz, 8	8.29 MHz, 4.15	6 MHz, 2.07
			010	0 0 =System cl	ock (8.29 MH	z, 4.15 MHz,	2.07 MHz, 1.0	4 Mhz)
			010	01=2x system	n clock			
			01	1 0 =DMA cloc MHz)	k (16.59 MHz	, 8.29 MHz, 4	.15 MHz, 2.07	MHz, 1.04
			01	1 1 =2x DMA c	lock			
			1 X .	X X =DC				
			The sour sele clea	CLK_IO outpu ce is DC. Durin ction is change nly.	t signal will be ng operation, ed, the output	e DC wheneve when the CLk clock signal is	er the selected <_IO clock souse not guarantee	l clock irce ed to switch

Factory Debug Register A

I/O Address 22h/23h Index 88h



Factory Debug Register B

I/O Address 22h/23h Index 89h



Miscellaneous SMI/NMI Enable Register

I/O Address 22h/23h Index 90h

	7	6	5	4	3	2	1	0
Bit	WAKE_ WIL_XMI	SIN_WILL_XMI	RIN_WILL_XMI	RTC_WILL_XMI	SUS_RE	ES_CFG	SW_NMI	SW_SMI
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/	W	W	W

Dit	Name	FUNCTION
7	WAKE_WILL_XMI	Wake-Up XMI Enable 0 = Do not cause XMI 1 = Cause SMI/NMI
6	SIN_WILL_XMI	Falling Edge on the Internal UART's Serial Input Pin (SIN) XMI Enable 0 = Do not cause XMI 1 = Cause SMI/NMI
5	RIN_WILL_XMI	Falling Edge on the Internal UART's Ring Indicate Pin (RIN) Enable 0 = Do not cause XMI 1 = Cause SMI/NMI
4	RTC_WILL_XMI	RTC Alarm XMI Enable 0 = Do not cause XMI 1 = Cause SMI/NMI
3	SR_RISE_WILL_XMI	Rising Edge on SUS_RES Pin XMI Enable 0 = Do not cause SMI/NMI 1 = Cause SMI/NMI
2	SR_FALL_WILL_XMI	Rising Edge on SUS_RES Pin XMI Enable 0 = Do not cause SMI/NMI 1 = Cause SMI/NMI
1	SW_NMI	Force NMI 0 = Do not cause NMI 1 = Cause NMI Refer to CSC index 9Dh[1] for a related bit.
0	SW_SMI	Force SMI 0 = Do not cause SMI 1 = Cause SMI

Programming Notes

Bits 6–2: If, when an XMI is enabled, the signal that is being used to generate the XMI is already in the state where it would have been after the enabled edge occurred, an XMI will be generated immediately, without need for another edge. For example, if SIN is low, and then SIN is configured to XMI on a falling edge, the SMI will occur immediately as a result of enabling it. To avoid unwanted XMIs, follow these steps:

- 1. Disable the SMI at its master control.
- 2. Enable the XMI.
- 3. Clear the XMI status bit.
- 4. Re-enable the SMI at its master source (port 70h[7] for NMIs, CSC index 9Dh[0] for SMIs).

Bits 1–0: These bits behave as if they were self-clearing. When generating an SMI via bit 0 of this register, be sure to clear CSC index 94h[0] while inside the SMI handler prior to exiting SMM mode (by executing a resume instruction) or another SMI will be generated as soon as the resume instruction is executed.

PC Card and Keyboard SMI/NMI Enable Register

I/O Address 22h/23h Index 91h

	7		6	5	4	3	2	1	0		
Bit	KYOBR WILL_X	R MI	KYIBW_ WILL_XMI	KYTIM_ WILL_XM	MKYPRS_ WILL_XMI	PCM_INT_ WILL_XMI	PCM_RI_ WILL_XMI	PCMB_CD_ WILL_XMI	PCMA_CD_ WILL_XMI		
Default	0		0	0	0	0	0	0	0		
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Bit 7	Name KYOBR_WILL_XMI		Function Keyboard Output Buffer Read XMI Enable							
				() = Do not cause	e XMI					
					I = Cause SMI/N						
	6	ΚY	IBW_WILL_X	MI I	(eyboard Input) = Do not cause	e XMI	en XMI Enabl	e			
				-	I = Cause SMI/N	NMI					
	5	ΚY	YTIM_WILL_XMI		Keyboard Timer XMI Enable 0 = Do not cause XMI						
					1 = Cause SMI/NMI						
	4	MK	YPRS_WILL	_XMI I	Matrix Keyboard Key Pressed/XT Keyboard XMI Enable 0 = Do not cause XMI						
					1 = Cause SMI/NMI						
				H f i i i	Keyboard row 14 rom causing an s enabled, and a press XMI will be s again pressed cleared.	is shared wit XMI by defau an XMI occurs possible unti , even after th	h the SUS_R It. See CSC ir due to a key I all matrix key e keypressed	ES pin, and is ndex C0h[3]. I press, no furt ys are release XMI status bi	excluded f this option her key d and a key t has been		
					If XT keyboard interface mode is enabled and is configured to generate XMIs (see CSC index C1h[5–4]), the resultant XMI will only be properly cleared once CSC index C1h[1] has been toggled. See CSC index C1h[1–0] for more detail.						
	3	PC	M_INT_WILL	_XMI I	PMU's PC Card Status Change Interrupt XMI Enable 0 = Do not cause XMI						
					1 = Cause SMI/NMI						
	2	PCM_RI_WILL_XMI		XMI I	PC Card Ring Indicate XMI Enable 0 = Do not cause XMI						
					1 = Cause SMI/NMI						
	1	PC	MB_CD_WIL	L_XMI I	PC Card Socke) = Do not cause	t B Card Dete e XMI	ect XMI Enab	le			
					1 = Cause SMI/NMI						

Programming Notes

PCMA_CD_WILL_XMI

0

0 = Do not cause XMI 1 = Cause SMI/NMI

PC Card Socket A Card Detect XMI Enable

Mode Timer SMI/NMI Enable Register

	7	6	5	4	3	2	1	0
Bit		Reserved		SUSTO_ WILL_XMI	SBTO_WILL_ XMI	LOTO_WILL_ XMI	HITO_WILL_ XMI	HYTO_WILL_ XMI
Default	Х	x	Х	0	0	0	0	0
R/W				R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–5	Reserved	Reserved During read/modify/write operations, software must preserve these bits
4	SUSTO_WILL_XMI	Suspend Mode Timer Time-Out XMI Enable 0 = Do not cause XMI
		1 = Cause SMI/NMI
3	SBTO_WILL_XMI	Standby Mode Timer Time-Out XMI Enable 0 = Do not cause XMI
		1 = Cause SMI/NMI
2	LOTO_WILL_XMI	Low-Speed Mode Timer Time-Out XMI Enable 0 = Do not cause XMI
		1 = Cause SMI/NMI
1	HITO_WILL_XMI	High-Speed Mode Timer Time-Out XMI Enable 0 = Do not cause XMI
		1 = Cause SMI/NMI
0	HYTO_WILL_XMI	Hyper-Speed Mode Timer Time-Out XMI Enable 0 = Do not cause XMI
		i = Cause SMI/NMI

Battery Low and ACIN SMI/NMI Enable Register

I/O Address 22h/23h Index 93h

	7	6	5	4	3	2	1	0
Bit	ACIN_RISE_ WAS_XMI	ACIN_FALL_ WAS_XMI	BL2_RISE_ WAS_XMI	BL2_FALL_ WAS_XMI	BL1_RISE_ WAS_XMI	BL1_FALL_ WAS_XMI	BL0_RISE_ WAS_XMI	BL0_FALL_ WAS_XMI
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	ACIN_RISE_WAS_XMI	ACIN Pin Edge XMI Enable A Rising Edge on ACIN
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
6	ACIN_FALL_WAS_XMI	ACIN Pin Edge XMI Enable A Falling Edge on ACIN
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
5	BL2_RISE_WAS_XMI	BL2 Pin Edge XMI Enable A Rising Edge on BL2
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
4	BL2_FALL_WAS_XMI	BL2 Pin Edge XMI Enable A Falling Edge on BL2
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
3	BL1_RISE_WAS_XMI	BL1 Pin Edge XMI Enable A Rising Edge on BL1
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
2	BL1_FALL_WAS_XMI	BL1 Pin Edge XMI Enable A Falling Edge on BL1
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
1	BL0_RISE_WAS_XMI	BLO Pin Edge XMI Enable A Rising Edge on BLO
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
0	BL0_FALL_WAS_XMI	BLO Pin Edge XMI Enable A Falling Edge on BLO
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI

Programming Notes

For all bit fields in this register, if, when an XMI is enabled, the signal that is being used to generate the XMI (BLx, ACIN) is already in the state where it would have been after the enabled edge occurred, an XMI will be generated immediately, without need for another edge. For example, if BL0 is low,

and then BL0 is configured to XMI on a falling edge, the SMI will occur immediately as a result of enabling it. To avoid unwanted XMIs, follow these steps:

- 1. Disable the SMI at its master control.
- 2. Enable the XMI.
- 3. Clear the XMI status bit.
- 4. Re-enable the SMI at its master source (port 70h[7] for NMIs, CSC index 9Dh[0] for SMIs).

Miscellaneous SMI/NMI Status Register

I/O Address 22h/23h Index 94h

	7	6	5	4	3	2	1	0
Bit	WAKE_WAS_ XMI	SIN_WAS_ XMI	RIN_WAS_ XMI	RTC_WAS_ XMI	SUS_RISE_ WAS_XMI	SUS_FALL_ WAS_XMI	SW_NMI	SW_SMI
Default	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	WAKE_WAS_XMI	Wake-Up XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
6	SIN_WAS_XMI	UART Receive XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
5	RIN_WAS_XMI	UART Ring Indicate XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
4	RTC_WAS_XMI	RTC Alarm (IRQ8) XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
3	SUS_RISE_WAS_XMI	SUS_RES Pin XMI Status Rising Edge on SUS_RES caused XMI
		0 = Did not cause SMI /NMI
		1 = Caused SMI/NMI
2	SUS_FALL_WAS_XMI	SUS_RES Pin XMI Status Falling Edge on SUS_RES caused XMI
		0 = Did not cause SMI /NMI
		1 = Caused SMI/NMI
1	SW_NMI	Force NMI XMI Status Write to '0b' to clear.
		0 = Did not cause NMI
		1 = Caused NMI
0	SW_SMI	Force SMI XMI Status Write to '0b' to clear.
		0 = Did not cause SMI
		1 = Caused SMI

Programming Notes

Although bits 3 and 2 are shown above as separate bits, the XMI that is associated with either event will be cleared only when both of these bits are written to '00b'.

PC Card and Keyboard SMI/NMI Status Register

I/O Address 22h/23h Index 95h

	7	6	5	4	3	2	1	0			
Bit	KYOBR_ WAS_XMI	KYIBW_ WAS_XMI	KYTIM_ WAS_XMI	MKYPRS_ WAS_XMI	PCM_INT_ WAS_XMI	PCM_RI_ WAS_XMI	PCMB_CD_ WAS_XMI	PCMA_CD_ WAS_XMI			
Default	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
	Bit Name 7 KYOBR_WAS_XMI 6 KYIBW_WAS_XMI 5 KYTIM_WAS_XMI		Fu (MI Ke Wi 0 = 1 = MI Ke Wi 0 = 1 = MI Ke Wi 0 = 1 = 1 =	Function Keyboard Output Buffer Read XMI Status Write to '0b' to clear. 0 = Did not cause SMI/NMI 1 = Caused SMI/NMI Keyboard Input Buffer Written XMI Status Write to '0b' to clear. 0 = Did not cause SMI/NMI 1 = Caused SMI/NMI Keyboard Timer XMI Status Write to '0b' to clear. 0 = Did not cause SMI/NMI 1 = Caused SMI/NMI 1 = Caused SMI/NMI							
	4 M	MKYPRS_WAS_XMI		Matrix Reyboard Key Pressed/XT Reyboard XMI Status 0 = Did not cause SMI/NMI 1 = Caused SMI/NMI If XT keyboard interface mode is enabled and is configured to generate XMIs (see CSC index C1h[5–4]), the resultant XMI will only be properly cleared once CSC index C1h[1] has been toggled. See CSC index C1h[1–0] for more details.							
	3 P(CM_INT_WAS	_XMI PN 0 = 1 =	PMU's PC Card Status Change XMI Status 0 = Did not cause SMI/NMI 1 = Caused SMI/NMI							
	2 P(CM_RI_WAS_	XMI PC 0 =	PC Card Ring Indicate XMI Status 0 = Did not cause SMI/NMI							
	1 P(CMB_CD_WA	1 = S_XMI PC Wi 0 = 1 =	 Caused SMI, Card Socket ite to '0b' to cl Did not caus Caused SMI, 	i B Card Dete ear. e SMI/NMI /NMI	ct XMI Statu	S				
	0 P(CMA_CD_WAS	S_XMI PC Wi 0 = 1 =	Card Socket ite to '0b' to cl Did not caus Caused SMI,	t A Card Dete lear. e SMI/NMI /NMI	ct XMI Statu	S				

Mode Timer SMI/NMI Status Register

I/O Address 22h/23h Index 96h

	7	6	5	4	3	2	1	0
Bit	Res	erved	GPIO_WAS_ XMI	SUSTO_ WAS_XMI	SBTO_WAS_ XMI	LOTO_WAS_ XMI	HITO_WAS_ XMI	HYTO_WAS_ XMI
Default	х	х	0	0	0	0	0	0
R/W			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits
5	GPIO_WAS_XMI	GPIO_XMI XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
4	SUSTO_WAS_XMI	Suspend Mode Timer Time-Out XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
3	SBTO_WAS_XMI	Stand-by Mode Timer Time-Out XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
2	LOTO_WAS_XMI	Low-Speed Mode Timer Time-Out XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
1	HITO_WAS_XMI	High-Speed Mode Timer Time-Out XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
0	HYTO_WAS_XMI	Hyper-Speed Mode Timer Time-Out XMI Status Write to '0b' to clear.
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI

Battery Low and ACIN SMI/NMI Status Register

I/O Address 22h/23h Index 97h

	7	6	5	4	3	2	1	0
Bit	ACIN_RISE_ WAS_XMI	ACIN_FALL_ WAS_XMI	BL2_RISE_ WAS_XMI	BL2_FALL_ WAS_XMI	BL1_RISE_ WAS_XMI	BL1_FALL_ WAS_XMI	BL0_RISE_ WAS_XMI	BL0_FALL_ WAS_XMI
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	ACIN_RISE_WAS_XMI	ACIN Pin Edge XMI Status Rising Edge on ACIN caused XMI
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
6	ACIN_FALL_WAS_XMI	ACIN Pin Edge XMI Status Falling Edge on ACIN caused XMI
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
5	BL2_RISE_WAS_XMI	BL2 Pin Edge XMI Status Rising Edge on BL2 caused XMI
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
4	BL2_FALL_WAS_XMI	BL2 Pin Edge XMI Status Falling Edge on BL2 caused XMI
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
3	BL1_RISE_WAS_XMI	BL1 Pin Edge XMI Status Rising Edge on BL1 caused XMI
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
2	BL1_FALL_WAS_XMI	BL1 Pin Edge XMI Status Falling Edge on BL1 caused XMI
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
1	BL0_RISE_WAS_XMI	BL0 Pin Edge XMI Status Rising Edge on BL0 caused XMI
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI
0	BL0_FALL_WAS_XMI	BL0 Pin Edge XMI Status Falling Edge on BL0 caused XMI
		0 = Did not cause SMI/NMI
		1 = Caused SMI/NMI

Programming Notes

Although all bits in this register are shown above as separate bits, they must be treated as four pairs of bits when clearing an XMI. The ACIN bits are grouped as a pair and the BLx bits are grouped as three additional pairs. The XMI that is associated with either the rising or falling edge event associated with a pair will be cleared only when both of the bits in the pair are written to '00b'.

For all bit fields in this register, if, when an XMI is enabled, the signal that's being used to generate the XMI (BLx, ACIN) is already in the state where it would have been after the enabled edge occurred, an XMI will be generated immediately, without requiring another edge. For example, if BL0 is low, and then BL0 is configured to XMI on a falling edge, the XMI will occur immediately as a result of enabling it. To avoid unwanted XMIs, perform the following steps:

- 1. Disable the XMI at its master control.
- 2. Enable the XMI.
- 3. Clear the XMI status bit.
- 4. Re-enable the XMI at its master control (CSC index 9Dh[2] for NMIs, CSC index 9Dh[0] for SMIs).

SMI/NMI Select Register

7

RTC_XMI_

SEL

0

R/W

6

UART_XMI_

SEL

0

R/W

5

PCM_INT_

XMI_SEL

0

R/W

4

WAKE_XMI_

SEL

0

R/W

3

KEYINT_

XMI_SEL

0

R/W

2

SUS_RES_

XMI_SEL

0

R/W

I/O Address 22h/23h Index 98h

0

MODTIM_

XMI_SEL

0

R/W

1

BLX_ACIN_

XMI_SEL

0

R/W

Bit
Default
R/W

Bit	Name	Function
7	RTC_XMI_SEL	RTC Alarm XMI Select 0 = SMI/NMI interrupts are SMI
		1 = SMI/NMI interrupts are NMI
6	UART_XMI_SEL	Falling Edge on Either UART Ring Indicate/UART Receive XMI Select 0 = SMI/NMI interrupts are SMI
		1 = SMI/NMI interrupts are NMI
5	PCM_INT_XMI_SEL	PC Card XMI Select 0 = SMI/NMI interrupts are SMI
		1 = SMI/NMI interrupts are NMI
4	WAKE_XMI_SEL	Wake-Ups XMI Select 0 = SMI/NMI interrupts are SMI
		1 = SMI/NMI interrupts are NMI
3	KEYINT_XMI_SEL	Internal Keyboard XMI Select Internally generated keyboard interrupts due to keyboard timer time-out, input buffer written, output buffer read, matrix key pressed, or XT keyboard byte received. Each of these can have individual enables. See the keyboard index registers for more detail.
		0 = SMI/NMI interrupts are SMI
		1 = SMI/NMI interrupts are NMI
2	SUS_RES_XMI_SEL	SUS_RES Signal XMI Select 0 = SMI/NMI interrupts are SMI
		1 = SMI/NMI interrupts are NMI
1	BLX_ACIN_XMI_SEL	Battery Management (BL0, BL1, BL2, and ACIN) XMI Select 0 = SMI/NMI interrupts are SMI
		1 = SMI/NMI interrupts are NMI
0	MODTIM_XMI_SEL	High-Speed, Low-Speed, Standby, and Suspend Mode Timer XMI Select 0 = SMI/NMI interrupts are SMI 1 = SMI/NMI interrupts are NMI

Programming Notes

NMI handlers will need to set the NMI_DONE bit at CSC index 9Dh[1] prior to returning control to the interrupted routine.

I/O Access SMI Enable Register A

I/O Address 22h/23h Index 99h

	7		6	5	4	3	2	1	0			
Bit			Reserved		KEYIOTRAP	INTVIDTRAP	PPTRAP	UART2TRAP	UART1TRAP			
Default	х		х	х	0	0	0	0	0			
R/W					R/W	R/W	R/W	R/W	R/W			
	Bit	Na	me	Functio	n							
	7–5	Re	served	Reserved During read/modify/write operations, software must preserve these b								
	4	KE	YIOTRAP	Keyboard Access SMI Enable 0 = Do not cause an SMI due to an access to this I/O device								
				1 = Cau	1 = Cause an SMI due to an access to this I/O device							
				When the XT keyboard interface is enabled, accesses to port 60h can be configured to generate an SMI. When the PC/AT keyboard interface is enabled, accesses to either port 60h or 64h can be configured to gener an SMI.								
	3	INT	IVIDTRAP	Internal 0 = Do n	Graphics I/O not cause an S	SMI Enable MI due to an	access to this	is I/O device				
				1 = Cau	1 = Cause an SMI due to an access to this I/O device							
				The add graphics	The address range that will generate the SMI is based on the internal graphics mode that is currently enabled.							
	2	PP	TRAP	LPT1/LF 0 = Do n	LPT1/LPT2 Parallel Port I/O SMI Enable 0 = Do not cause an SMI due to an access to either LPT1 or LPT2							
				1 = Cau	se an SMI due	e to an access	to either LPT	1 or LPT2				
	1 UART2TRAP			UART C 0 = Do n	UART COM2 SMI Enable 0 = Do not cause an SMI due to an I/O access to UART COM2							
				1 = Cau	1 = Cause an SMI due to an I/O access to UART COM2							
	0	UA	RT1TRAP	UART C 0 = Do n	OM1 SMI Ena not cause an S	a ble SMI due to an	I/O access to	UART COM1				
				1 = Cau	1 = Cause an SMI due to an I/O access to UART COM1							

I/O Access SMI Enable Register B

I/O Address 22h/23h Index 9Ah

	7	6	5	4	3	2	1	0
Bit	Reserved	GPCSB_ TRAP	GPCSA_ TRAP	PCMB_ IOTRAP	PCMA_ IOTRAP	XVGA_ IOTRAP	HDD_IOTRAP	FDD_IOTRAP
Default	х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	GPCSB_TRAP	GP_CSB SMI Enable 0 = Do not cause an SMI due to an access to this I/O range
		1 = Cause an SMI due to an access to this I/O range
5	GPCSA_TRAP	GP_CSA SMI Enable 0 = Do not cause an SMI due to an access to this I/O range
		1 = Cause an SMI due to an access to this I/O range
4	PCMB_IOTRAP	PC Card Socket B I/O Access SMI Enable 0 = Do not cause an SMI due to an access to any enabled I/O windows supported by PC Card Socket B
		1 = Cause an SMI due to an access to any enabled I/O windows supported by PC Card Socket B
3	PCMA_IOTRAP	PC Card Socket A I/O Access SMI Enable 0 = Do not cause an SMI due to an access to any enabled I/O windows supported by PC Card Socket A
		1 = Cause an SMI due to an access to any enabled I/O windows supported by PC Card Socket A
2	XVGA_IOTRAP	External VGA Graphics I/O Access SMI Enable 0 = Do not cause an SMI due to an I/O access to an External VGA Graphics controller
		1 = Cause an SMI due to an I/O access to an External VGA Graphics controller
1	HDD_IOTRAP	IDE Hard Drive Access SMI Enable 0 = Do not cause an SMI due to an I/O access to the primary fixed disk controller
		1 = Cause an SMI due to an I/O access to the primary fixed disk controller
0	FDD_IOTRAP	Floppy Disk Controller Access SMI Enable 0 = Do not cause an SMI due to an I/O access to the primary floppy disk controller
		1 = Cause an SMI due to an I/O access to the primary floppy controller

I/O Access SMI Status Register A

	7	6	5	4	3	2	1	0
Bit	Reserved			KEYIOTRAP- PED	INTVIDTRA- PPED	PPTRAPPED	UART2TRAP- PED	UART1TRAP- PED
Default	х	x	х	0	0	0	0	0
R/W				R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–5	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
4	KEYIOTRAPPED	Keyboard Access SMI Status Write to '0b' to clear.
		0 = Did not cause an SMI due to an access to this I/O device
		1 = Caused an SMI due to an access to this I/O device
3	INTVIDTRAPPED	Internal Graphics I/O SMI Status Write to '0b' to clear.
		0 = Did not cause an SMI due to an access to this I/O device
		1 = Caused an SMI due to an access to this I/O device
		The address range that will generate the SMI is based on the internal graphics mode that is currently enabled.
2	PPTRAPPED	LPT1/LPT2 Parallel Port I/O SMI Status Write to '0b' to clear.
		0 = Did not cause an SMI due to an access to LPT1 or LPT2
		1 = Caused an SMI due to an access to LPT1 or LPT2
1	UART2TRAPPED	UART COM2 SMI Status Write to '0b' to clear.
		0 = Did not cause an SMI due to an I/O access to UART COM2
		1 = Caused an SMI due to an I/O access to UART COM2
0	UART1TRAPPED	UART COM1 SMI Status Write to '0b' to clear.
		0 = Did not cause an SMI due to an I/O access to UART COM1
		1 = Caused an SMI due to an I/O access to UART COM1

I/O Access SMI Status Register B

I/O Address 22h/23h Index 9Ch

	7	6	5	4	3	2	1	0
Bit	Reserved	GPCSB_ TRAPPED	GPCSA_ TRAPPED	PCMB_ IOTRAPPED	PCMA_ IOTRAPPED	XVGA_ IOTRAPPED	HDD_ IOTRAPPED	FDD_ IOTRAPPED
Default	x	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	R/W	Function
7	Reserved		Reserved During read/modify/write operations, software must preserve this bit.
6	GPCSB_TRAPPED	R/W	GP_CSB SMI Status Write to '0b' to clear.
			0 =Did not cause an SMI due to an access to this I/O range
			1 =Caused an SMI due to an access to this I/O range
5	GPCSA_TRAPPED	R/W	GP_CSA SMI Status Write to '0b' to clear.
			0 =Did not cause an SMI due to an access to this I/O range
			1 =Caused an SMI due to an access to this I/O range
4	PCMB_IOTRAPPED	R/W	PC Card Socket B I/O Access SMI Status Write to '0b' to clear.
			0 = Did not cause an SMI due to an access to any enabled I/O windows supported by PC Card Socket B
			1 = Caused an SMI due to an access to any enabled I/O windows supported by PC Card Socket B
3	PCMA_IOTRAPPED	R/W	PC Card Socket A I/O Access SMI Status Write to '0b' to clear.
			0 = Did not cause an SMI due to an access to any enabled I/O windows supported by PC Card Socket A
			1 = Caused an SMI due to an access to any enabled I/O windows supported by PC Card Socket A
2	XVGA_IOTRAPPED	R/W	External VGA Graphics I/O Access SMI Status Write to '0b' to clear.
			0 = Did not cause an SMI due to an I/O access to an external VGA graphics controller
			1 = Caused an SMI due to an I/O access to an external VGA graphics controller
1	HDD_IOTRAPPED	R/W	IDE Hard Drive Access SMI Status Write to '0b' to clear.
			0 = Did not cause an SMI due to an I/O access to the primary fixed disk controller
			1 = Caused an SMI due to an I/O access to the primary fixed disk controller
0	FDD_IOTRAPPED	R/W	Floppy Disk Controller Access SMI Status Write to '0b' to clear.
			0 = Did not cause an SMI due to an I/O access to the primary floppy disk controller
			1 = Caused an SMI due to an I/O access to the primary floppy disk controller

XMI Control Register

I/O Address 22h/23h Index 9Dh

	7	6	5	4	3	2	1	0		
Bit			Reserved			NMI_GATE	NMI_DONE	SMI_GATE		
Default	х	х	х	х	х	х	0	0		
R/W							W	R/W		
	Bit	Name	Functio	n						
	7–3	Reserved	Reserved During read/modify/write operations, software must preserve these bits							
	2	NMI GATE	Master	NMI Enable						

		1 = NMI events will propagate to the CPU core
		This bit is a read/write version of the NMI Gate bit which typically resides at direct-mapped port 70h[7] on a PC/AT Compatible system. It has been moved here to facilitate internal design integration with the ElanSC400 microcontroller PMU.
1	NMI_DONE	NMI Routine Done Write a '1b' to this bit to indicate to the PMU that the NMI routine is done. This bit is used by, and cleared automatically by, the PMU state machine. After setting NMI_DONE, at least three cycles of the 32 KHz clock (as monitored at CSC index 82h[3]) must transpire before a subsequent pending NMI will be felt at the CPU.
0	SMI_GATE	Master SMI Enable 0 = SMI events are gated off from reaching the CPU core
		1 = SMI events will propagate to the CPU core
		This bit will be automatically cleared whenever the internal master reset is asserted. This occurs during a power-on reset and as a result of the CPU executing a shutdown cycle during SMM mode. Clearing this bit does not disable operation of the SMI status bits in CSC indexes 94–97h.

0 = NMI events are gated off from reaching the core

GPIO_CS Function Select Register A

	7		6	5	4	2	2 1 0						
Bit	CS3_F	PRI	CS3_DIR	CS2_PRI	CS2_DIR	CS1_PRI	CS1_DIR	CSO_PRI	CS0_DIR				
Default	0		0	0	0	0	0	0	0				
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W				
	Dit	Na	ma	<u> </u>									
		INd		Functio									
	7 CS3_PRI		3_PRI	GPIO_C53 Signal is a Primary Activity and wake-up (Falling Edge) Enable 0 = Not activity or wake up									
				1 = Cau	se activity or v	vake up							
	6 CS3_DIR			GPIO_C 0 = Inpu	S3 Signal is	an Input/Out	out						
				1 = Outp	out								
	5 CS2_PRI			GPIO_CS2 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up									
				1 = Cause activity or wake up									
	4	CS	2_DIR	GPIO_CS2 Signal is an Input/Output 0 = Input									
				1 = Output									
	3	CS	61_PRI	GPIO_CS1 Signal is a Primary Activity and Wake-up (Falling E Enable 0 = Not activity or wake up									
				1 = Cau	se activity or v	vake up							
	2	CS	61_DIR	GPIO_CS1 Signal is an Input/Output 0 = Input									
				1 = Outp	out								
	1 CSO_PRI			GPIO_CS0 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up									
				1 = Cau	se activity or v	vake up							
	0	CS	60_DIR	GPIO_C 0 = Inpu	S0 Signal is	an Input/Outj	out						
				1 = Output									

GPIO_CS Function Select Register B

I/O Address 22h/23h Index A1h

	7		6	5	4	3	2	1	0			
Bit	CS7_PRI		CS7_DIR	CS6_PRI	CS6_DIR	CS5_PRI	CS5_DIR	CS4_PRI	CS4_DIR			
Default	0		0	0	0	0	0	0	0			
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W			
	Bit Name		Function									
	7 CS7_PRI		S7_PRI	GPIO_CS7 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up								
				1 = Cause activity or wake up								
	6 CS7		S7_DIR	GPIO_C 0 = Input	GPIO_CS7 Signal is an Input/Output 0 = Input							
				1 = Outp	1 = Output							
	5 CS6_PRI		GPIO_CS6 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up									
			1 = Cause activity or wake up									
	4 CS6_DIR		GPIO_CS6 Signal is an Input/Output 0 = Input									
			1 = Output									
	3 CS5_PRI		GPIO_CS5 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up									
				1 = Cause activity or wake up								
	2 CS5_DIR		GPIO_CS5 Signal is an Input/Output 0 = Input									
				1 = Output								
	1	CS	64_PRI	GPIO_C Enable 0 = Not a	S4 Signal is activity or wak	a Primary Ac æ up	tivity and Wa	ake-up (Fallin	ig Edge)			
				1 = Caus	se activity or v	vake up						
	0	CS4_DIR		GPIO_CS4 Signal is an Input/Output 0 = Input								
				1 = Outp	put							

GPIO_CS Function Select Register C

	7		6	5	4	3	2	1	0		
Bit	CS11_F	PRI	CS11_DIR	CS10_PRI	CS10_DIR	CS9_PRI	CS9_DIR	CS8_PRI	CS8_DIR		
Default	0		0	0	0	0	0	0	0		
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Dit Nome		Function								
	/ CS11_PRI		GPIO_CS11 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up								
				1 = Cau	1 = Cause activity or wake up						
	6	CS	S11_DIR	GPIO_CS11 Signal is an Input/Output 0 = Input							
			1 = Output								
	5	CS10_PRI		GPIO_CS10 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up							
				1 = Cause activity or wake up							
	4	CS10_DIR		GPIO_CS10 Signal is an Input/Output 0 = Input							
				1 = Output							
	3	CS9_PRI		GPIO_CS9 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up							
			1 = Cause activity or wake up								
	2	CS9_DIR		GPIO_CS9 Signal is an Input/Output 0 = Input							
				1 = Outp	1 = Output						
	1	CS	88_PRI	GPIO_C Enable 0 = Not a	S8 Signal is activity or wak	a Primary Ac e up	tivity and Wa	ike-up (Fallin	ig Edge)		
	0 CS8_DIF			1 = Cau	se activity or v	vake up					
			S8_DIR	GPIO_CS8 Signal is an Input/Output 0 = Input							
				1 = Outp	out						

GPIO_CS Function Select Register D

	7		6	5	4	3	2	1	0		
Bit	Reserv	ed	GPIO15_DIR	CS14_PRI	CS14_DIR	CS13_PRI	CS13_DIR	CS12_PRI	CS12_DIR		
Default	х		0	0	0	0	0	0	0		
R/W			R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	BitName7Reserved6GPIO15_DIR5CS14_PRI4CS14_DIR3CS13_PRI		me	Function							
			served	Reserved During read/modify/write operations, software must preserve this bit. GPIO15 Signal is an Input/Output 0 = Input							
			PIO15_DIR								
				1 = Output							
			GPIO_CS14 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up								
			1 = Cause activity or wake up								
			GPIO_CS14 Signal is an Input/Output 0 = Input								
			1 = Output								
			GPIO_CS13 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up								
				1 = Cause activity or wake up							
	2 CS13_DIR		13_DIR	GPIO_CS13 Signal is an Input/Output 0 = Input							
			1 = Output								
	1 CS12_PRI			GPIO_CS12 Signal is a Primary Activity and Wake-up (Falling Edge) Enable 0 = Not activity or wake up							
				1 = Cause activity or wake up							
	0 CS12_DIR		12_DIR	GPIO_CS12 Signal is an Input/Output 0 = Input							
				1 = Output							

GPIO Function Select Register E

I/O Address 22h/23h Index A4h

	7	6	5	4	3	2	1	0
Bit	GPIO23_DIR	GPIO22_DIR	GPIO21_DIR	GPIO20_DIR	GPIO19_DIR	GPIO18_DIR	GPIO17_DIR	GPIO16_DIR
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	GPIO23_DIR	GPIO23 Signal is an Input/Output 0 = Input
		1 = Output
6	GPIO22_DIR	GPIO22 Signal is an Input/Output 0 = Input
		1 = Output
5	GPIO21_DIR	GPIO21 Signal is an Input/Output 0 = Input
		1 = Output
4	GPIO20_DIR	GPIO20 Signal is an Input/Output 0 = Input
		1 = Output
3	GPIO19_DIR	GPIO19 Signal is an Input/Output 0 = Input
		1 = Output
2	GPIO18_DIR	GPIO18 Signal is an Input/Output 0 = Input
		1 = Output
1	GPIO17_DIR	GPIO17 Signal is an Input/Output 0 = Input
		1 = Output
0	GPIO16_DIR	GPIO16 Signal is an Input/Output 0 = Input
		1 = Output
GPIO Function Select Register F

I/O Address 22h/23h Index A5h

	7	6	5	4	3	2	1	0
Bit	GPIO31_DIR	GPIO30_DIR	GPIO29_DIR	GPIO28_DIR	GPIO27_DIR	GPIO26_DIR	GPIO25_DIR	GPIO24_DIR
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	GPIO31_DIR	GPIO31 Signal is an Input/Output 0 = Input
		1 = Output
6	GPIO30_DIR	GPIO30 Signal is an Input/Output 0 = Input
		1 = Output
5	GPIO29_DIR	GPIO29 Signal is an Input/Output 0 = Input
		1 = Output
4	GPIO28_DIR	GPIO28 Signal is an Input/Output 0 = Input
		1 = Output
3	GPIO27_DIR	GPIO27 Signal is an Input/Output 0 = Input
		1 = Output
2	GPIO26_DIR	GPIO26 Signal is an Input/Output 0 = Input
		1 = Output
1	GPIO25_DIR	GPIO25 Signal is an Input/Output 0 = Input
		1 = Output
0	GPIO24_DIR	GPIO24 Signal is an Input/Output 0 = Input
		1 = Output

GPIO Read-Back/Write Register A

	7	6	5	4	3	2	1	0
Bit	GP7STAT_ CTL	GP6STAT_ CTL	GP5STAT_ CTL	GP4STAT_ CTL	GP3STAT_ CTL	GP2STAT_ CTL	GP1STAT_ CTL	GP0STAT_ CTL
Default	х	Х	Х	Х	Х	Х	Х	Х
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	GP7STAT_CTL	GPIO_CS7 Status and Control Read GPIO_CS7 value and write GPIO_CS7 value when pin = output
6	GP6STAT_CTL	GPIO_CS6 Status and Control Read GPIO_CS6 value and write GPIO_CS6 value when pin = output
5	GP5STAT_CTL	GPIO_CS5 Status and Control Read GPIO_CS5 value and write GPIO_CS5 value when pin = output
4	GP4STAT_CTL	GPIO_CS4 Status and Control Read GPIO_CS4 value and write GPIO_CS4 value when pin = output
3	GP3STAT_CTL	GPIO_CS3 Status and Control Read GPIO_CS3 value and write GPIO_CS3 value when pin = output
2	GP2STAT_CTL	GPIO_CS2 Status and Control Read GPIO_CS2 value and write GPIO_CS2 value when pin = output
1	GP1STAT_CTL	GPIO_CS1 Status and Control Read GPIO_CS1 value and write GPIO_CS1 value when pin = output
0	GP0STAT_CTL	GPIO_CS0 Status and Control Read GPIO_CS0 value and write GPIO_CS0 value when pin = output

Programming Notes

At power-on reset, the GPIO pins referenced by this register default to inputs, hence the values read back from this register depend on what is driving them external to the ÉlanSC400 microcontroller. The value read back can also be influenced by the use of the programmable termination. See GPIO Termination Control Register A at CSC index 3Bh for more detail. Also note that if, while its associated pin is configured as an input, any these bits is written to, the value written will be latched. If the pin is then configured as an output, the latched value will be driven to the GPIO_CS pin.

The value read back from this register may not necessarily correspond to what was last written to this register.

GPIO Read-Back/Write Register B

I/O Address 22h/23h Index A7h

	7	6	5	4	3	2	1	0
Bit	GP15STAT_ CTL	GP14STAT_ CTL	GP13STAT_ CTL	GP12STAT_ CTL	GP11STAT_ CTL	GP10STAT_ CTL	GP9STAT_ CTL	GP8STAT_ CTL
Default	Х	Х	Х	Х	Х	Х	Х	Х
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	GP15STAT_CTL	GPIO_CS15 Status and Control Read GPIO_CS15 value and write GPIO15 value when pin = output
6	GP14STAT_CTL	GPIO_CS14 Status and Control Read GPIO_CS14 value and write GPIO_CS14 value when pin = output
5	GP13STAT_CTL	GPIO_CS13 Status and Control Read GPIO_CS13 value and write GPIO_CS13 value when pin = output
4	GP12STAT_CTL	GPIO_CS12 Status and Control Read GPIO_CS12 value and write GPIO_CS12 value when pin = output
3	GP11STAT_CTL	GPIO_CS11 Status and Control Read GPIO_CS11 value and write GPIO_CS11 value when pin = output
2	GP10STAT_CTL	GPIO_CS10 Status and Control Read GPIO_CS10 value and write GPIO_CS10 value when pin = output
1	GP9STAT_CTL	GPIO_CS9 Status and Control Read GPIO_CS9 value and write GPIO_CS9 value when pin = output
0	GP8STAT_CTL	GPIO_CS8 Status and Control Read GPIO_CS8 value and write GPIO_CS8 value when pin = output

Programming Notes

At power-on reset, the GPIO pins referenced by this register default to inputs, hence the values read back from this register depend on what is driving them external to the ÉlanSC400 microcontroller. The value read back can also be influenced by the use of the programmable termination. See GPIO Termination Control Register B at CSC index 3Ch for more detail. Also note that if, while its associated pin is configured as an input, any these bits is written to, the value written will be latched. If the pin is then configured as an output, the latched value will be driven to the GPIO_CS pin.

The value read back from this register may not necessarily correspond to what was last written to this register.

GPIO Read-Back/Write Register C

	7	6	5	4	3	2	1	0
Bit	GP23STAT_ CTL	GP22STAT_ CTL	GP21STAT_ CTL	GP20STAT_ CTL	GP19STAT_ CTL	GP18STAT_ CTL	GP17STAT_ CTL	GP16STAT_ CTL
Default	х	х	х	х	х	х	х	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit Na	me	Functio	n				

7	GP23STAT_CTL	GPIO23 Status and Control Read GPIO23 value and write GPIO23 value when pin = output
6	GP22STAT_CTL	GPIO22 Status and Control Read GPIO22 value and write GPIO22 value when pin = output
5	GP21STAT_CTL	GPIO21 Status and Control Read GPIO21 value and write GPIO21 value when pin = output
4	GP20STAT_CTL	GPIO20 Status and Control Read GPIO20 value and write GPIO20 value when pin = output
3	GP19STAT_CTL	GPIO19 Status and Control Read GPIO19 value and write GPIO19 value when pin = output
2	GP18STAT_CTL	GPIO18 Status and Control Read GPIO18 value and write GPIO18 value when pin = output
1	GP17STAT_CTL	GPIO17 Status and Control Read GPIO17 value and write GPIO17 value when pin = output
0	GP16STAT_CTL	GPIO16 Status and Control Read GPIO16 value and write GPIO16 value when pin = output

Programming Notes

At power-on reset, the GPIO pins referenced by this register default to inputs, hence the values read back from this register depend on what's driving them external to the ÉlanSC400 microcontroller. The value read back can also be influenced by the use of the programmable termination. See GPIO Termination Control Register C at CSC index 3Dh for more detail. Also note that if, while its associated pin is configured as an input, any these bits is written to, the value written will be latched. If the pin is then configured as an output, the latched value will be driven to the GPIO_CS pin.

GPIO Read-Back/Write Register D

I/O Address 22h/23h Index A9h

	7	6	5	4	3	2	1	0
Bit	GP31STAT_ CTL	GP30STAT_ CTL	GP29STAT_ CTL	GP28STAT_ CTL	GP27STAT_ CTL	GP26STAT_ CTL	GP25STAT_ CTL	GP24STAT_ CTL
Default	х	х	х	х	х	х	х	х
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	GP31STAT_CTL	GPIO31 Status and Control Read GPIO31 value and write GPIO31 value when pin = output
6	GP30STAT_CTL	GPIO30 Status and Control Read GPIO30 value and write GPIO30 value when pin = output
5	GP29STAT_CTL	GPIO29 Status and Control Read GPIO29 value and write GPIO29 value when pin = output
4	GP28STAT_CTL	GPIO28 Status and Control Read GPIO28 value and write GPIO28 value when pin = output
3	GP27STAT_CTL	GPIO27 Status and Control Read GPIO27 value and write GPIO27 value when pin = output
2	GP26STAT_CTL	GPIO26 Status and Control Read GPIO26 value and write GPIO26 value when pin = output
1	GP25STAT_CTL	GPIO25 Status and Control Read GPIO25 value and write GPIO25 value when pin = output
0	GP24STAT_CTL	GPIO24 Status and Control Read GPIO24 value and write GPIO24 value when pin = output

Programming Notes

At power-on reset, the GPIO pins referenced by this register default to inputs, hence the values read back from this register depend on what's driving them external to the ÉlanSC400 microcontroller. The value read back can also be influenced by the use of the programmable termination. See GPIO Termination Control Register D at CSC index 3Eh for more detail.

Also note that if, while its associated pin is configured as an input, any these bits is written to, the value written will be latched. If the pin is then configured as an output, the latched value will be driven to the GPIO_CS pin.

GPIO_PMUA Mode Change Register

I/O Address 22h/23h Index AAh

	7	6	5	4	3	2	1	0
Bit	Res	erved	GPMUA_HY_ LEV	GPMUA_HS_ LEV	GPMUA_LS_ LEV	GPMUA_ TLS_LEV	GPMUA_SB_ LEV	GPMUA_SU_ LEV
Default	х	x	0	0	0	0	0	0
R/W			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	GPMUA_HY_LEV	Drive GPIO_PMUA Signal with Programmed Value in Hyper-Speed Mode
		0 = Drive GPIO pin associated with GPIO_PMUA Low when Hyper-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUA High when Hyper-Speed mode entered
4	GPMUA_HS_LEV	Drive GPIO_PMUA Signal with Programmed Value in High-Speed Mode
		0 = Drive GPIO pin associated with GPIO_PMUA Low when High-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUA High when High-Speed mode entered
3	GPMUA_LS_LEV	Drive GPIO_PMUA Signal with Programmed Value in Low-Speed Mode
		0 = Drive GPIO pin associated with GPIO_PMUA Low when Low-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUA High when Low-Speed mode entered
2	GPMUA_TLS_LEV	Drive GPIO_PMUA Signal with Programmed Value in Temporary Low-Speed Mode
		0 = Drive GPIO pin associated with GPIO_PMUA Low when Temporary Low-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUA High when Temporary Low-Speed mode entered
1	GPMUA SB LEV	Drive GPIO PMUA Signal with Programmed Value in Standby Mode
		0 = Drive GPIO pin associated with GPIO_PMUA Low when Standby mode entered
		1 = Drive GPIO pin associated with GPIO_PMUA High when Standby mode entered
0	GPMUA_SU_LEV	Drive GPIO_PMUA Signal with Programmed Value in Suspend or Critical Suspend Mode
		0 = Drive GPIO pin associated with GPIO_PMUA Low when Suspend or Critical Suspend mode entered
		1 = Drive GPIO pin associated with GPIO_PMUA High when Suspend or Critical Suspend mode entered

Programming Notes

Setting bit 0 of this register will cause the GPIO pin, which is selected via CSC index AEh[3–0], to go active when the PMU is either in Suspend or Critical Suspend mode. To distinguish between

Suspend and Critical Suspend modes, look at the state of the $\overline{LBL2}$ pin which, when active, indicates that the PMU is in Critical Suspend PMU mode.

See CSC index AEh[3–0] for GPIO_PMUA to GPIO_CS pin mapping.

GPIO_PMUB Mode Change Register

I/O Address 22h/23h Index ABh

	7	6	5	4	3	2	1	0
Bit	Res	erved	GPMUB_HY_ LEV	GPMUB_HS_ LEV	GPMUB_LS_ LEV	GPMUB_ TLS_LEV	GPMUB_SB_ LEV	GPMUB_SU_ LEV
Default	х	х	0	0	0	0	0	0
R/W			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	GPMUB_HY_LEV	Drive GPIO_PMUB Signal with Programmed Value in Hyper-Speed
		0 = Drive GPIO pin associated with GPIO_PMUB Low when Hyper-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUB High when Hyper-Speed mode entered
4	GPMUB_HS_LEV	Drive GPIO_PMUB Signal with Programmed Value in Hyper-Speed
		0 = Drive GPIO pin associated with GPIO_PMUB Low when High-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUB High when High-Speed mode entered
3	GPMUB_LS_LEV	Drive GPIO_PMUB Signal with Programmed Value in Low-Speed
		0 = Drive GPIO pin associated with GPIO_PMUB Low when Low-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUB High when Low-Speed mode entered
2	GPMUB_TLS_LEV	Drive GPIO_PMUB Signal with Programmed Value in Temporary
		0 = Drive GPIO pin associated with GPIO_PMUB Low when Temporary Low-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUB High when Temporary Low-Speed mode entered
1	GPMUB_SB_LEV	Drive GPIO_PMUB Signal with Programmed Value in Standby Mode 0 = Drive GPIO pin associated with GPIO_PMUB Low when Standby mode entered
		1 = Drive GPIO pin associated with GPIO_PMUB High when Standby mode entered
0	GPMUB_SU_LEV	Drive GPIO_PMUB Signal with Programmed Value in Suspend or Critical Suspend Mode
		0 = Drive GPIO pin associated with GPIO_PMUB Low when Suspend or Critical Suspend mode entered
		1 = Drive GPIO pin associated with GPIO_PMUB High when Suspend or Critical Suspend mode entered

Programming Notes

Setting bit 0 of this register will cause the GPIO pin, which is selected via CSC index AEh[7–4], to go active when the PMU is either in Suspend or Critical Suspend mode. To distinguish between

Suspend and Critical Suspend modes, look at the state of the $\overline{LBL2}$ pin which, when active, indicates that the PMU is in Critical Suspend PMU mode.

See CSC index AEh[7–4] for GPIO_PMUB to GPIO_CS pin mapping.

GPIO_PMUC Mode Change Register

I/O Address 22h/23h Index ACh

	7	6	5	4	3	2	1	0
Bit	Res	erved	GPMUC_HY_ LEV	GPMUC_HS_ LEV	GPMUC_LS_ LEV	GPMUC_ TLS_LEV	GPMUC_SB_ LEV	GPMUC_SU_ LEV
Default	х	х	0	0	0	0	0	0
R/W			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	GPMUC_HY_LEV	Drive GPIO_PMUC Signal with Programmed Value in Hyper-Speed Mode
		0 = Drive GPIO pin associated with GPIO_PMUC Low when Hyper-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUC High when Hyper-Speed mode entered
4	GPMUC_HS_LEV	Drive GPIO_PMUC Signal with Programmed Value in Hyper-Speed
		0 = Drive GPIO pin associated with GPIO_PMUC Low when High-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUC High when High-Speed mode entered
3	GPMUC_LS_LEV	Drive GPIO_PMUC Signal with Programmed Value in Low-Speed
		0 = Drive GPIO pin associated with GPIO_PMUC Low when Low-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUC High when Low-Speed mode entered
2	GPMUC_TLS_LEV	Drive GPIO_PMUC Signal with Programmed Value in Temporary
		0 = Drive GPIO pin associated with GPIO_PMUC Low when Temporary Low-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUC High when Temporary Low-Speed mode entered
1	GPMUC_SB_LEV	Drive GPIO_PMUC Signal with Programmed Value in Standby Mode 0 = Drive GPIO pin associated with GPIO_PMUC Low when Standby mode entered
		1 = Drive GPIO pin associated with GPIO_PMUC High when Standby mode entered
0	GPMUC_SU_LEV	Drive GPIO_PMUC Signal with Programmed Value in Suspend or Critical Suspend Mode
		0 = Drive GPIO pin associated with GPIO_PMUC Low when Suspend or Critical Suspend mode entered
		1 = Drive GPIO pin associated with GPIO_PMUC High when Suspend or Critical Suspend mode entered

Programming Notes

Setting bit 0 of this register will cause the GPIO pin, which is selected via CSC index AFh[3–0], to go active when the PMU is either in Suspend or Critical Suspend mode. To distinguish between

Suspend and Critical Suspend modes, look at the state of the $\overline{LBL2}$ pin which, when active, indicates that the PMU is in Critical Suspend PMU mode.

See CSC index AFh[3–0] for GPIO_PMUC to GPIO_CS pin mapping.

GPIO_PMUD Mode Change Register

I/O Address 22h/23h Index ADh

	7	6	5	4	3	2	1	0
Bit	Res	erved	GPMUD_HY_ LEV	GPMUD_HS_ LEV	GPMUD_LS_ LEV	GPMUD_ TLS_LEV	GPMUD_SB_ LEV	GPMUD_SU_ LEV
Default	х	х	0	0	0	0	0	0
R/W			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	GPMUD_HY_LEV	Drive GPIO_PMUD Signal with Programmed Value in Hyper-Speed Mode
		0 = Drive GPIO pin associated with GPIO_PMUD Low when Hyper-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUD High when Hyper-Speed mode entered
4	GPMUD_HS_LEV	Drive GPIO_PMUD Signal with Programmed Value in Hyper-Speed
		0 = Drive GPIO pin associated with GPIO_PMUD Low when High-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUD High when High-Speed mode entered
3	GPMUD_LS_LEV	Drive GPIO_PMUD Signal with Programmed Value in Low-Speed
		0 = Drive GPIO pin associated with GPIO_PMUD Low when Low-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUD High when Low-Speed mode entered
2	GPMUD_TLS_LEV	Drive GPIO_PMUD Signal with Programmed Value in Temporary
		0 = Drive GPIO pin associated with GPIO_PMUD Low when Temporary Low-Speed mode entered
		1 = Drive GPIO pin associated with GPIO_PMUD High when Temporary Low-Speed mode entered
1	GPMUD_SB_LEV	Drive GPIO_PMUD Signal with Programmed Value in Standby Mode 0 = Drive GPIO pin associated with GPIO_PMUD Low when Standby mode entered
		1 = Drive GPIO pin associated with GPIO_PMUD High when Standby mode entered
0	GPMUD_SU_LEV	Drive GPIO_PMUD Signal with Programmed Value in Suspend or Critical Suspend Mode
		0 = Drive GPIO pin associated with GPIO_PMUD Low when Suspend or Critical Suspend mode entered
		1 = Drive GPIO pin associated with GPIO_PMUD High when Suspend or Critical Suspend mode entered

Programming Notes

Setting bit 0 of this register will cause the GPIO pin, which is selected via CSC index AFh[7–4], to go active when the PMU is either in Suspend or Critical Suspend mode. To distinguish between

Suspend and Critical Suspend modes, look at the state of the $\overline{LBL2}$ pin which, when active, indicates that the PMU is in Critical Suspend PMU mode.

See CSC index AFh[7–4] for GPIO_PMUD to GPIO_CS pin mapping.

GPIO_PMU to GPIO_CS Map Register A

I/O Address 22h/23h Index AEh



1 1 1 0 = GPIO_CS14 1 1 1 1 = Disabled

Programming Notes

When mapping GPMUA/B to external GPIO_CS pins for the purpose of controlling the GPIO_CS pins based on the PMU mode, you must also configure the desired GPIO_CS pins to be outputs (see CSC indexes A0–A3h). You must also ensure that the bits in index register A6h or A7h that correspond to the GPIO_CS pins you are controlling based on PMU mode have been cleared.

GPIO_PMU to GPIO_CS Map Register B

I/O Address 22h/23h Index AFh

	7	6	5	4	3	2	1	0
Bit		GPMUD_MUX	[3–0]			GPMUC_	MUX[3–0]	
Default	1	1	1	1	1	1	1	1
R/W		R/W				R	/W	
	Bit	Name	Fund	tion				
	7–4	GPMUD_MUX[3-0]	Map The i	GPIO_PMUD number progra	to One of the	e GPIO_CS F ponds to the	Pins GPIO_CS tha	at is mapped:
			000	$0 = GPIO_CS$	S0			
			000	$1 = GPIO_CS$	S1			
			111	$0 = GPIO_CS$	S14			
			111	1 = Disabled				
	3–0	GPMUC_MUX[3-0]	Map The i	GPIO_PMUC number progra	to One of the ammed corres	e GPIO_CS F ponds to the	'ins GPIO_CS tha	at is mapped:
			000	$0 = GPIO_CS$	S0			
			000	$1 = GPIO_CS$	S1			
			111	$0 = GPIO_CS$	614			
			111	1 = Disabled				

Programming Notes

When mapping GPMUC/D to external GPIO_CS pins for the purpose of controlling the GPIO_CS pins based on the PMU mode, you must also configure the desired GPIO_CS pins to be outputs (see CSC indexes A0–A3h). You must also ensure that the bits in index register A6h or A7h that correspond to the GPIO_CS pins you are controlling based on PMU mode have been cleared.

GPIO_XMI to GPIO_CS Map Register

I/O Address 22h/23h Index B0h

	7		6	5	4	3	2	1	0				
Bit			Reserved		GPIO_XMI_SEL		GPXMI_N	/IUX[3–0]					
Default	х		Х	х	0	1	1	1	1				
R/W					R/W		R/	W					
	Bit	Na	mo	Functio	n								
	7–5	Re	served	Reserv During	ed read/modifv/wr	ite operations	. software mu	st preserve th	ese bits.				
	4	GP	IO_XMI_SEL	GPIO_ 0 = GPI	GPIO_XMI SMI/NMI Selection 0 = GPIO_XMI interrupts are SMI								
				1 = GPI	1 = GPIO_XMI interrupts are NMI								
	3–0	GP	XMI_MUX[3-	0] Map or This all SMI/NM register GPIO_0	Map one of the GPIO_CS Pins to the Internal GPIO_XMI Input Signal This allows logic external to the ÉlanSC400 microcontroller to generate an SMI/NMI by driving a falling edge onto the GPIO_CS pin selected via this register. The number programmed into this register corresponds to the GPIO_CS pin that is to be internally routed to the GPIO_XMI input:								
				0000	= GPIO_CS0								
				0001	0 0 0 1 = GPIO_CS1								
				1110	1 1 1 0 = GPIO_CS14								
				1111	1 1 1 1 = Disabled								
				To avoi support	To avoid generating unwanted XMIs when mapping GPIO_XMI to a supported GPIO_CS pin, follow these steps:								
				1. Disa 9Dh	able XMIs to th [0]. For NMIs,	e CPU core. I this is done v	For SMIs, this ia CSC index	is done via C 9Dh[2].	SC index				
				2. Sele B0h	ect whether GF [4].	PIO_XMI prod	uces an SMI o	or NMI via CS	C index				
				3. Map 0].	 Map a GPIO_CS pin to the GPIO_XMI signal using CSC index B0h[3– 0]. 								
				4. Clea	ar the GPIO_W	AS_XMI bit a	t CSC index 9	96h[5].					
				5. Ena abo	Enable XMIs to the CPU core by reversing the action from step 1 above.								
				XMIs and clear	e fully enabled aring the XMI f	l if steps 1–5 or GPIO_XMI	nave been per is performed	rformed. Read via index 96h	ling status [5].				

Standard Decode to GPIO_CS Map Register

I/O Address 22h/23h Index B1h

	7		6	5	4	3	2	1	0
Bit			GPROM_CS	2 - MUX[3–0]	GPSCP_MUX[3-0]				
Default	1		1	1	1	1	1	1	1
R/W			R/	W			R	W	
	Bit	Nam	ne		Function				
	7–4	GPR	ROM_CS2-M	IUX[3–0]	Map ROM Chi The number p mapped:	p Select 2 (R rogrammed co	OMCS2) to C prresponds to	one of the GP the GPIO_CS	IO_CS Pins S that is
					0 0 0 0 = GPIC	D_CS0			
					0 0 0 1 = GPIC	D_CS1			
					1 1 1 0 = GPIC	D_CS14			
					1 1 1 1 = Disal	bled			
	3–0	GPS	SCP_MUX[3-	-0]	Map Keyboar 64h) to One o The number p mapped:	d Controller (f the GPIO_C rogrammed co	(external SCI S Pins prresponds to	P) Chip Select the GPIO_CS	e t (60h and S that is
					0 0 0 0 = GPIC	D_CS0			
					0 0 0 1 = GPIC	D_CS1			
					1 1 1 0 = GPIC	D_CS14			
					1 1 1 1 = Disal	bled			
					If this feature i one of the GP regardless of t	s enabled (i.e O_CS pins), t he setting of (., external SC then the chip CSC index C1	P chip select select will be g h[3–2].	mapped to generated

Programming Notes

When mapping either the internal SCP address decoder or ROMCS2 signal to external GPIO_CS pins for the purpose of generating external chip selects, you must also configure the desired GPIO_CS pins to be outputs (see CSC indexes A0–A3h). In addition, you must ensure that the bits in index register A6h or A7h that correspond to the GPIO_CS pins you are using as chip selects have been cleared.

GP_CS to GPIO_CS Map Register A

I/O Address 22h/23h Index B2h

	7		6	5	4	3	2	1	0				
Bit			GPCSB_I	MUX[3–0]		GPCSA_MUX[3–0]							
Default	1		1	1	1	1	1						
R/W			R/	W			R/	W					
	Bit	Nai	me	Fund	tion								
	7–4	GP	CSB_MUX[3-	-0] Map The r	GP_CSB to C number progra	One of the GF ammed corres	PIO_CS Pins	GPIO_CS that	t is mapped:				
				000	0 0 0 0 = GPIO_CS0								
				000	$1 = GPIO_CS$	S1							
				•									
				111	$0 = GPIO_CS$	S14							
				111	1 = Disabled								
	3–0	GP	CSA_MUX[3-	–0] Map The r	GP_CSA to C number progra	One of the GF ammed corres	PIO_CS Pins ponds to the	GPIO_CS that	t is mapped:				
				000	$0 = GPIO_CS$	50							
				000	$1 = GPIO_CS$	51							
				•									
				•									
				111	$0 = GPIO_CS$	S14							
				111	1 = Disabled								

Programming Notes

When mapping GP_CSA/B to external GPIO_CS pins for the purpose of generating external chip selects, you must also configure the desired GPIO_CS pins to be outputs (see CSC indexes A0–A3h). In addition, you must ensure that the bits in index register A6h or A7h that correspond to the GPIO_CS pins you are using as chip selects have been cleared.

GP_CS to GPIO_CS Map Register B

I/O Address 22h/23h Index B3h

	7		6	5	4	3	2	1	0				
Bit			GPCSD_I	MUX[3–0]			GPCSC_	MUX[3–0]					
Default	1		1	1	1	1	1	1	1				
R/W			R/	W	R/W								
	Bit	Na	me	Function	on								
	7–4	GP	CSD_MUX[3-	-0] Map G The nu	Map GP_CSD to One of the GPIO_CS Pins The number programmed corresponds to the GPIO_CS that is mapped:								
				0000	= GPIO_CS0								
				0001	= GPIO_CS1								
				1110	= GPIO_CS1	4							
				1111	= Disabled								
	3–0	GP	CSC_MUX[3-	-0] Map G The nu	P_CSC to On mber program	e of the GPIC med correspo	D_CS Pins ands to the GF	PIO_CS that is	s mapped:				
				0000	= GPIO_CS0								
				0001	= GPIO_CS1								
				1110	= GPIO_CS1	4							

1 1 1 1 = Disabled

Programming Notes

When mapping GP_CSC/D to external GPIO_CS pins for the purpose of generating external chip selects, you must also configure the desired GPIO_CS pins to be outputs (see CSC indexes A0–A3h). You must also ensure that the bits in index register A6h or A7h that correspond to the GPIO_CS pins you are using as chip selects have been cleared.

GP_CSA I/O Address Decode Register

I/O Address 22h/23h Index B4h



GP_CSA I/O Address Decode and Mask Register

I/O Address 22h/23h Index B5h

	7	6	5	4	3	2	1	0
Bit	Reserved		CSA_SA3_ MASK	CSA_SA2_ MASK	CSA_SA1_ MASK	CSA_SA0_ MASK	CSA_AD	DR[9-8]
Default	х	x	0	0	0	0	0	0
R/W			R/W	R/W	R/W	R/W		

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits
5	CSA_SA3_MASK	Mask SA3 0 = Masked
		1 = Not masked
4	CSA_SA2_MASK	Mask SA2 0 = Masked
		1 = Not masked
3	CSA_SA1_MASK	Mask SA1 0 = Masked
		1 = Not masked
2	CSA_SA0_MASK	Mask SA0 0 = Masked
		1 = Not masked
1–0	CSA_ADDR[9-8]	Chip Select A Address Bits 9–8 SA 9–8 for I/O Chip Select A generation.

GP_CSB I/O Address Decode Register

I/O Address 22h/23h Index B6h



GP_CSB I/O Address Decode and Mask Register

I/O Address 22h/23h Index B7h

	7	6	5	4	3	2	1	0
Bit	Res	erved	CSB_SA3_ MASK	CSB_SA2_ MASK	CSB_SA1_ MASK	CSB_SA0_ MASK	CSB_SA	0_MASK
Default	х	x	0	0	0	0	0	0
R/W			R/W	R/W	R/W	R/W	R/	W

Bit	Name	Function
7–6	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
5	CSB_SA3_MASK	Mask SA3 0 = Masked
		1 = Not masked
4	CSB_SA2_MASK	Mask SA2 0 = Masked
		1 = Not masked
3	CSB_SA1_MASK	Mask SA1 0 = Masked
		1 = Not masked
2	CSB_SA0_MASK	Mask SA0 0 = Masked
		1 = Not masked
1–0	CSB_ADDR[9-8]	Chip Select B Address Bits 9–8 SA 9–8 for I/O Chip Select B generation.

GP_CSA/B I/O Command Qualification Register

I/O Address 22h/23h Index B8h

	7	6	5	4	3	2	1	0
Bit	Reserved	GP_CSB_ X8_X16	CSB_GATE	D_IOX[1-0]	Reserved	GP_CSA_ X8_X16	CSA_GATE	D_IOX[1–0]
Default	х	0	0	0	х	0	0	х
R/W		R/W	R/W			R/W	R/	W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	GP_CSB_X8_X16	GP_CSB ISA I/O Cycle Data Bus Width and Timing Selector 0 = 8-bit data bus size and timings will be used for ISA bus I/O transactions using GP_CSB
		1 = 16-bit data size and timings will be used for GP_CSB ISA bus I/O transactions
		If IOCS16 is sampled active at the proper time per the ISA bus I/O timing requirements, 16-bit data size and timings will be used.
5–4	CSB_GATED_IOX[1-0]	Qualify GP_CSB with IOR/IOW GP_CSB generation, whose address decode is specified by indexes B6h and B7h, is always qualified with AEN being deasserted. It can be additionally qualified by IOR and/or IOW as follows:
		0.0 = Not additionally qualified by IOR or by IOW
		0 1 = Additionally qualified by \overline{IOR} only
		1 0 = Additionally qualified by \overline{IOW} only
		1 1 = Additionally qualified by either IOR or IOW
		These bits qualify an I/O address range hit to help define what will constitute a I/O chip select. A chip select has two main (and not necessarily related) uses which are to drive an external chip select pin for the purpose of selecting an external device and for use as an internally routed input to the PMU for generating PMU activity. In order to generate a CSB external chip select, an external pin must be selected via CSC index B2h[7–4]. In order to generate CSB activity, this must be enabled via CSC index 60h[1].
3	Reserved	Reserved During read/modify/write operations, software must preserve this bit.

Bit	Name	Function
2	GP_CSA_X8_X16	GP_CSA ISA I/O Cycle Data Bus Width and Timing Selector 0 = 8-bit data bus size and timings will be used for ISA bus I/O transactions using GP_CSA
		1 = 16-bit data size and timings will be used for GP_CSA ISA bus I/O transactions.
		If IOCS16 is sampled active at the proper time per the ISA bus I/O timing requirements, 16-bit data size and timings will be used.
1–0	CSA_GATED_IOX[1-0]	Qualify GP_CSA with IOR/IOW GP_CSA generation whose address decode is specified by indexes B6h and B7h is always qualified with AEN being deasserted. It may be additionally qualified by IOR and/or IOW as follows:
		$0.0 = Not$ additionally qualified by \overline{IOR} or by \overline{IOW}
		0 1 = Additionally qualified by IOR only
		1 0 = Additionally qualified by \overline{IOW} only
		1 1 = Additionally qualified by either \overline{IOR} or \overline{IOW}
		These bits qualify an I/O address range hit to help define what will constitute a I/O chip select. A chip select has two main (and not necessarily related) uses: to drive an external chip select pin for the purpose of selecting an external device and for use as an internally routed input to the PMU for generating PMU activity. In order to generate a CSA external chip select, an external pin must be selected via CSC index B2h[3–0]. In order to generate CSA activity, this must be enabled via CSC index 60h[0].

GP_CSC Memory Address Decode Register

I/O Address 22h/23h Index B9h



Index BAh

I/O Address 22h/23h

GP_CSC Memory Address Decode and Mask Register

	7	6	5	4	3	2	1	0
Bit	CSC_SA17_ MASK	CSC_SA16_ MASK	CSC_SA15_ MASK	CSC_SA14_ MASK	CSC_ADDR[17-14]			
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W			

Bit	Name	Function
7	CSC_SA17_MASK	Mask SA17 0 = Masked
		1 = Not masked
6	CSC_SA16_MASK	Mask SA16 0 = Masked
		1 = Not masked
5	CSC_SA15_MASK	Mask SA15 0 = Masked
		1 = Not masked
4	CSC_SA14_MASK	Mask SA14 0 = Masked
		1 = Not masked
3–0	CSC_ADDR[17-14]	Chip Select C Address Bits 17–14 SA17–14 for Memory Chip Select C generation.

GP_CSD Memory Address Decode Register

I/O Address 22h/23h Index BBh



Index BCh

I/O Address 22h/23h

GP_CSD Memory Address Decode and Mask Register

	7	6	5	4	3	2	1	0
Bit	CSD_SA17_ MASK	CSD_SA16_ MASK	CSD_SA15_ MASK	CSD_SA14_ MASK	CSD_ADDR[17–14]			
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W			

Bit	Name	Function
7	CSD_SA17_MASK	Mask SA17 0 = Masked
		1 = Not masked
6	CSD_SA16_MASK	Mask SA16 0 = Masked
		1 = Not masked
5	CSD_SA15_MASK	Mask SA15 0 = Masked
		1 = Not masked
4	CSD_SA14_MASK	Mask SA14 0 = Masked
		1 = Not masked
3–0	CSD_ADDR[17– 14]	Chip Select D Address Bits 17–14 SA17–14 for Memory Chip Select D generation.

GP_CSC/D Memory Command Qualification Register

I/O Address 22h/23h Index BDh

	7	6	5	4	3	2	1	0
Bit	GP_CSD_ X8_X16	CSD_GATED_MEMX[2-0]			GP_CSC_ X8_X16	CSC_GATED_MEMX[2-0]		
Default	0	0	0	0	0	0	0	0
R/W	R/W		R/W			R/w		

Bit	Name	Function
7	GP_CSD_X8_X16	GP_CSD ISA Memory Cycle Data Bus Width and Timing Selector
		0 = 8-bit data bus size and timings will be used for ISA bus memory transactions using GP_CSD
		1 = 16-bit data size and timings will be used for GP_CSD ISA bus memory transactions
		If MCS16 is sampled active at the proper time per the ISA bus memory timing requirements, 16-bit data size and timings will be used.
6–4	CSD_GATED_MEMX[2-0]	Qualify GP_CSD with MEMR/MEMW or CPU Address Valid 0 0 0 = Chip select D is a function of SA25–SA14 decode only
		0 0 1 = Qualify SA25–SA14 decode with MEMR
		0 1 0 = Qualify SA25–SA14 decode with MEMW
		0 1 1 = Qualify SA25–SA14 decode with either $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$
		1 0 0 = Qualify SA25–SA14 with CPU address valid
		1 0 1 – 1 1 1 = Reserved
		These bits qualify a memory address range hit to help define what will constitute a memory chip select. A chip select has two main (and not necessarily related) uses which are to drive an external chip select pin for the purpose of selecting an external device and for use as an internally routed input to the PMU for generating PMU activity. In order to generate a CSD external chip select, an external pin must be selected via CSC index B3h[7–4]. In order to generate CSD activity, this must be enabled via CSC index 60h[3].
		Bit pattern '000b' should not be selected If GP_CSD is to be used as a PMU activity source since this setting does not qualify GP_CSD with the CPU address being valid. Use of '000b' can result in the generation of false activities.

Chip Setup and Control Indexed Registers

Bit	Name	Function
3	GP_CSC_X8_X16	 GP_CSC ISA Memory Cycle Data Bus Width and Timing Selector 0 = 8-bit data bus size and timings will be used for ISA bus memory transactions using GP_CSC
		1 = 16-bit data size and timings will be used for GP_CSC ISA bus memory transactions
		If MCS16 is sampled active at the proper time per the ISA bus memory timing requirements, 16-bit data size and timings will be used.
2–0	CSC_GATED_MEMX[2-0]	Qualify GP_CSC with MEMR/MEMW or CPU Address Valid 0 0 0 = Chip Select C is a function of SA25–SA14 decode only
		0 0 1 = Qualify SA25–SA14 decode with MEMR
		0 1 0 = Qualify SA25–SA14 decode with MEMW
		0 1 1 = Qualify SA25–SA14 decode with either $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$
		1 0 0 = Qualify SA25–SA14 with CPU address valid
		1 0 1 - 1 1 1 = Reserved
		These bits qualify a memory address range hit to help define what will constitute a memory chip select. A chip select has two main, (and not necessarily related) uses which are to drive an external chip select pin for the purpose of selecting an external device and for use as an internally routed input to the PMU for generating PMU activity. In order to generate an ElanSC400 microcontroller external chip select, an external pin must be selected via CSC index B3h[3–0]. In order to generate CSC activity, this must be enabled via CSC index 60h[2].
		Bit pattern '000b' should not be selected if GP_CSC is to be used as a PMU activity source since this setting does not qualify GP_CSC with the CPU address being valid. Use of '000b' can result in the generation of false activities.

Keyboard Configuration Register A

I/O Address 22h/23h Index C0h

	7	6	5	4	3	2	1	0
Bit	INT_ON_ RST_CMD	INT_ON_ A20_CMD	MOU_ IRQ12_EN	KEY_IRQ1_ EN	KBROW14_ CAN_XMI	RST_ SNOOP_DIS	A20G_ SNOOP_DIS	M_BUF_ FULL_SLCT
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit Na 7 IN	ame T_ON_RST_C	Fu CC Se	nction CP Reset Com Introl SMI/NMI quence ('FE')	nmand XMI E generation if is seen:	nable SCP CPU col	re reset comn	nand
			0 =	If CSC index generation for command wr cause the inp register which	91h[6] = '1b', or an input buf itten = FEh. Ir but buffer full f h can be read	clearing this b fer write via po addition, the lag to be set i back from po	bit overrides the overrides the overrides the overrides the override over the overrides the override	ne XMI the e does not d status
			1 =	The above-m special cases index 91h[6]	nentioned I/O s, and an XMI = 1.	writes to ports will be genera	64/60h are no ated in both ca	ot treated as ases if CSC
			Th	is bit has no e	ffect if CSC ir	dex 91h[6] = '	0b'.	
	6 IN	T_ON_A20_C	MD SC Co ('D	CP GateA20 C Introl SMI/NMI 1', data) is se	command XM generation if en:	I Enable SCP GateA20) command s	equence
			0 =	If CSC index generation for command wr byte written to In addition, n cause the inp Register, whi	91h[6] = '1b', or an input buf itten = D1h. T o the input bur either the por but buffer full f ich can be rea	clearing this b fer write via po he XMI is also fer providing t t 64h write nor lag to be set in d back from p	bit overrides the ort 64h when o inhibited for that it occurs of the port 60h n the Keyboar ort 64h.	ne XMI the the next via port 60h. write will rd Status
			1 =	The above-m as special ca CSC index 9	nentioned I/O ises and an X 1h[6] = 1.	writes to ports MI will be gen	64h/60h are erated in both	not treated cases if
			Th	is bit has no e	ffect if CSC ir	dex 91h[6] = '	0b'.	
	5 M	OU_IRQ12_EI	N SC 0 =	P Mouse Em ₌ IRQ12 won't	ulation IRQ1 be generated	2 Control as a result of	a write to CS	C index C4h
			1 =	= IRQ12 will be	e generated a	s a result of a	write to CSC	index C4h
			Th '10 se	is bit has no fu b'. Mouse IRC t.	Inction when t Q12 won't be	he external So generated if C	CP is enabled SC index C0ł	C1h[3–2] = n[0] is not
	4 KE	EY_IRQ1_EN	SC 0 =	P Emulation = IRQ1 will not	XT Keyboard be generated	I IRQ1 Contro by C3h write	ol s or XT keybo	oard data in
			1 =	= IRQ1 will be	generated by	subsequent C	3h writes or 2	KT data in
			Se	e the table b	elow for mo	re informatio	n.	

- Name **Function** KBROW14_CAN_XMI Keyboard Row 14 XMI Enable The SUS RES and matrix keyboard row 14 inputs share the same ElanSC400 microcontroller pin, making row 14 a special case. If CSC index 91h[4] is set, matrix scan key presses can generate an SMI/ NMI. Key presses that involve row 14 are excluded from this by default. This bit allows key presses that involve row 14 to be included in the SMI/NMI generation. Systems that use the pin as a SUS RES input only can thus be configured have matrix key presses generate an SMI/NMI without forcing this attribute on SUS_RES. Selection of SMI versus NMI is via CSC index 98[3]. 0 = SUS_RES/KBD_ROW14 pin won't generate an SMI/NMI 1 = SUS_RES/KBD_ROW14 pin will generate a keypressed SMI/NMI if so enabled for the other rows (CSC index 91h[4] = 1) RST_SNOOP_DIS SCP Reset Command Snooping Disable The ElanSC400 microcontroller has no external input pin for the Hot Reset signal that would normally be driven by a PC/AT compatible external System Control Processor (SCP). In order to maintain software compatibility, hardware is provided to watch the busses for SCP Hot Reset pin control command sequences. When this bit is cleared, these command sequences will be automatically intercepted and processed by a hardware state machine within the ElanSC400 microcontroller. When set, the ElanSC400 microcontroller will not snoop for SCP Hot Reset control commands. This bit has no effect on whether or not the SCP Hot Reset control command sequence is driven off the ElanSC400 microcontroller. If a Hot Reset command is detected, the processor SRESET signal will be pulsed. 0 = Enabled
 - 1 = Disabled

Bit

3

2

1

0

A20G_SNOOP_DIS

SCP A20 Gate Command Snooping Disable

The ÉlanSC400 microcontroller has no external input pin for the GateA20 signal that would normally be driven by a PC/AT-compatible external System Control Processor (SCP). In order to maintain software compatibility, hardware is provided to watch the buses for SCP GateA20 pin control command sequences. When this bit is cleared, these command sequences will be automatically intercepted and processed by a hardware state machine within the ElanSC400 microcontroller. When set, the ÉlanSC400 microcontroller will not snoop for SCP GateA20 control commands This bit has no effect on whether or not the SCP GateA20 control command sequence is driven off the ÉlanSC400 microcontroller.

- 0 = Enabled
- 1 = Disabled

The A20 line must propagate immediately following master reset to enable proper system operation. The state machine underlying this register bit ensures that the internal GateA20 control will force CPU A20 to propagate at this time. A20 will continue to propagate as a result of this control until software turns it off via the appropriate SCP command. When this bit is disabled, the A20Gate command snoop state machine is disabled and will no longer force CPU A20 to propagate.

M_BUF_FULL_SLCT Mouse Output Buffer Full Select

This bit selects whether bit 5 of the emulated Keyboard Status Register (direct-mapped port 64h) is the PC/AT compatible keyboard interface transmit time-out indicator, or the PS/2 compatible mouse output buffer full indicator. When used as the time-out bit, SCP emulation software must control port 64h[5] via the Keyboard Status Register Write Register (CSC index C5h). When configured to emulate the mouse output buffer full status bit, port 64h[5] is automatically set when the Mouse Output Buffer Write Register (CSC index C4h) is written to, and cleared when the Keyboard Output Buffer Write Register (CSC index C3h) is written to. No mouse IRQ12 will be generated unless this bit is set regardless of CSC index C0h[5].

- 0 = Emulated SCP port 64h[5] = PC/AT keyboard interface time-out
- 1 = Emulated SCP port 64h[5] = PS/2 mouse output buffer full bit

Programming Notes

SCP Support	XT KB Enabled	XT Intr Type	Effect of Setting Index Bit C0h[4]
External	N/A	N/A	No effect
None	No	N/A	No effect
None	Yes	XMI	No effect
None	Yes	IRQ1	Allows IRQ1 to be generated as a result of data being received from the XT keyboard interface.
Internal	No	N/A	Allows IRQ1 to be generated as a result of CSC index C3h being written to.
Internal	Yes	XMI	Allows IRQ1 to be generated as a result of CSC index C3h being written to.
Internal	Yes	IRQ1	Allows IRQ1 to be generated as a result of data being received from the XT keyboard interface OR as a result of CSC index C3h being written to. When configured like this, if either IRQ1 source is being asserted, the other source will not be able to generate an IRQ1. Care must be taken in the IRQ1 handler for this specialized case since if both sources of IRQ1 are asserted simultaneously (i.e., a write to CSC index C3h is quickly followed by arrival of data from the XT keyboard interface). The handler must not exit until one of the following has occurred:
			- Both IRQ1 sources are cleared
			- CSC index C0[4] has been toggled after one of the IRQ1 sources has been cleared to generate an edge for the remaining IRQ source.
			Failure to perform one of the above can result in the loss of further IRQ1 requests being detected by the PIC, as an edge is required for this.

This table shows the operation of CSC index C0h, bit 4 as it relates to other keyboard bit settings. SCP support is controlled by CSC index C1h[3–2], XT keyboard interface enable is controlled via CSC index C1h[4], and the XT interrupt type is controlled by CSC index C1h[5].

Keyboard Configuration Register B

I/O Address 22h/23h Index C1h

	7	6	5	4	3	2	1	0
Bit	Reserved	KEY_TIM_ STAT_CLR	XTKB_INTR_ SEL	XT_IF_ ENABLE	SCP_IF	SLCT	XTKB_ACK	XTKB_IF_EN
Default	Х	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/	W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	KEY_TIM_STAT_ CLR	Keyboard Timer SMI/NMI Status/Clear This bit is set when an SMI or NMI occurs as a result of a time-out on the keyboard-specific timer. Clearing this bit resets the SMI/NMI. Setting this bit has no effect. Keyboard timer SMIs/NMIs are enabled via CSC index 91h[5].
5	XTKB_INTR_SEL	XT Keyboard SMI/NMI, or IRQ1 Generation Select This bit has no meaning if the XT keyboard is disabled via bit 4 of this register.
		0 = A byte received from the XT keyboard interface will generate IRQ1.
		1 = A byte received from the XT keyboard interface will generate either an SMI or an NMI depending on the setting of CSC index 98h[3]. In order to generate an XT keyboard SMI/NMI, CSC index 91h[4] must also be set. SMI/NMI status for these interrupts is then read back from (and the SMI/NMI is cleared at CSC index 95h[4].
		When this bit is set, key presses from the matrix keyboard will not generate SMI/NMIs, regardless of the state of CSC index 91h[4]. C0h[4] must also be set in order to generate an IRQ1 to the PIC.
4	XT_IF_ENABLE	XT Keyboard Interface Enable When this bit is set, data that is shifted in from the XT keyboard data line will be latched into the on-chip output buffer so that it can be read by the CPU at direct-mapped port 60h.
		0 = XT keyboard interface is disabled
		1 = XT keyboard interface is enabled
		Bits 3–2 of this register must = '01b', for port 60h reads to return data shifted in from the XT keyboard interface. Besides enabling the basic XT keyboard interface, this configuration also allows SCP emulation to be performed while using a PC/XT keyboard versus a scanned matrix keyboard. If the external SCP interface is enabled bits 3–2 of this register = '10b' at the same time as the XT keyboard interface, reads from direct-mapped port 60h will be from the external SCP.

Bit	Name	Function
3–2	SCP_IF_SLCT	Enable Internal SCP Emulation Registers or External SCP Chip Select at 60h and 64h 0 0 = I/O accesses to ports 60h and 64h go neither off the ÉlanSC400 microcontroller to the ISA bus nor to the internally emulated SCP input buffer, output buffer, or status register
		0 1 = Enable Internal SCP emulation registers (Input Buffer, Output Buffer, and Status Register). I/O cycles to ports 60h and 64h will not go to the external ISA bus, but will instead access the internal emulation of the SCP input buffer, output buffer, and status register.
		1 0 = Enable external SCP support. I/O cycles to ports 60h and 64h will go to the external ISA bus
		1 1 = Same as 0 0
		Bits 3–2 of this register in no way affect the A20Gate/hot reset snooping functionality. These features are independently controlled via the Keyboard Configuration Register A at CSC index C0h[2–1]. In addition, I/O writes to the output buffer at port 60h or 64h will put data in the internal emulation of the SCP output buffer. The external SCP chip select is set up using CSC index B1h. The internal IRQ1 and IRQ12 for supporting keyboard/mouse emulation are disabled when the external SCP support is enabled.
1	XTKB_ACK	XT Keyboard Acknowledge When the XT keyboard function is enabled, writing this bit has three functions. This bit can be set by software to disable the keyboard interface by holding the data line low. In order for the XT keyboard to be able to transmit date, this bit should be cleared. In addition, for each byte that the system receives from the keyboard, this bit must be toggled–first written high and then low. This performs the other two functions: clears the XT keyboard data shift register so that false keyboard data port at I/O location 60h being cleared), and acknowledges to the keyboard that the system has read the last byte. Reading this bit returns the last value written. When the XT keyboard function is disabled, this bit has no effect on system operation. In a PC/XT Compatible system, this bit normally resides at direct-mapped port 61h[7].
0	XTKB_IF_EN	XT Keyboard Interface Enable When the XT keyboard function is enabled, set this bit to enable the keyboard interface, clear this bit to disable the XT keyboard interface (by holding the clock line low). Reading this bit returns the last value written. When the XT keyboard function is disabled, this bit has not effect on system operation. In a PC/XT Compatible system, this bit normally resides at direct-mapped port 61h[6].
Keyboard Input Buffer Read-Back Register

I/O Address 22h/23h Index C2h



Keyboard Output Buffer Write Register



Programming Notes

Bits 7–0: If the XT keyboard interface is enabled (CSC index C1h[4] = '1b'), then data shifted in from the XT keyboard data pin will be placed in the emulated keyboard output buffer. If internal SCP emulation is enabled as well, then the output buffer can contain data from either the XT keyboard data input, writes to CSC index C3h, or writes to CSC index C4h, whichever occurred last.





Programming Notes

Bits 7–0: If the XT keyboard interface is enabled, (CSC index C1h[4] = '1b') then data shifted in from the XT keyboard data pin will be placed in the emulated keyboard output buffer. If internal SCP emulation is enabled as well, then the output buffer can contain data from either the XT keyboard data input, writes to CSC index C3h, or writes to CSC index C4h, whichever occurred last.

Keyboard Status Register Write Register

I/O Address 22h/23h Index C5h



Keyboard Timer Register



Keyboard Column Register

	7		6	5	4	3	2	1	0					
Bit	MATKI COL7	B_ 7	MATKB_ COL6	MATKB_ COL5	MATKB_ COL4	MATKB_ COL3	MATKB_ COL2	MATKB_ COL1	MATKB_ COL0					
Default	1		1	1	1	1	1	1	1					
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W					
	Bit	Na	me	Functio	n									
	7	MA	ATKB_COL7	COL7 S Write = S	ignal Set Column pi	in High or Low	ı							
				Read = \$	Read = State of Column pin									
				0 = Signa	al drives Low									
				1 = I/O p CAh	in driver is thr	ee-stated with	n termination a	as selected by	CSC index					
	6	MA	TKB_COL6	COL6 S Write = S	ignal Set Column pi	in High or Low	1							
				Read = \$	State of Colur	nn pin								
				0 = Signa	al drives Low									
				1 = I/O p CAh	in driver is thr	ee-stated with	n termination a	as selected by	CSC index					
	5	MA	TKB_COL5	COL5 S Write = S	COL5 Signal Write = Set Column pin High or Low									
				Read = \$	State of Colur	nn pin								
				0 = Signa	al drives Low									
				1 = I/O p CAh	in driver is thr	ee-stated with	n termination a	as selected by	CSC index					
	4	MA	TKB_COL4	COL4 S Write = S	ignal Set Column pi	in High or Low	I							
				Read = \$	State of Colur	nn pin								
				0 = Signa	al drives Low									
				1 = I/O p CAh	in driver is thr	ee-stated with	n termination a	as selected by	CSC index					
	3	MA	TKB_COL3	COL3 S Write = S	ignal Set Column pi	in High or Low	I							
				Read = State of Column pin										
				0 = Signa	al drives Low									
	1 = I/O pin driver is three-stated with termination a CAh						as selected by	CSC index						
	2	MA	TKB_COL2	COL2 S Write = S	ignal Set Column pi	in High or Low	I							
				Read = \$	State of Colur	nn pin								
				0 = Signa	al drives Low									
				1 = I/O p CAh	in driver is thr	ee-stated with	n termination a	as selected by	CSC index					

Bit	Name	Function
1	MATKB_COL1	COL1 Signal Write = Set Column pin High or Low
		Read = State of Column pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated with termination as selected by CSC index CAh
0	MATKB_COL0	COL0 Signal Write = Set Column pin High or Low
		Read = State of Column pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated with termination as selected by CSC index CAh

Programming Notes

When the XT keyboard interface is enabled (CSC index 39h[3] = '1b'), writes to bits 1–0 of this register are undefined. Reads from these bits return the states of the respective pins.

Keyboard Row Register A

I/O Address 22h/23h Index C8h

	7	6	5	4	3	2	1	0
Bit	MATKB_ ROW7	MATKB_ ROW6	MATKB_ ROW5	MATKB_ ROW4	MATKB_ ROW3	MATKB_ ROW2	MATKB_ ROW1	MATKB_ ROW0
Default	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	MATKB_ROW7	ROW7 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
6	MATKB_ROW6	ROW6 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
5	MATKB_ROW5	ROW5 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
4	MATKB_ROW4	ROW4 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
3	MATKB_ROW3	ROW3 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
2	MATKB_ROW2	ROW2 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated

Bit	Name	Function
1	MATKB_ROW1	ROW1 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
0	MATKB_ROW0	ROW0 Signal Write = Set row pin High or Low Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated

Programming Notes

No programmable termination is provided for matrix keyboard row I/O pins. These pins are pulled up internally with the option to disable the pull-ups in Suspend mode.

Keyboard Row Register B

I/O Address 22h/23h Index C9h

	7	6	5	4	3	2	1	0
Bit	Reserved	MATKB_ SUS_RES	MATKB_ ROW13	MATKB_ ROW12	MATKB_ ROW11	MATKB_ ROW10	MATKB_ ROW9	MATKB_ ROW8
Default	х	1	1	1	1	1	1	1
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
6	MATKB_SUS_RES	Row 14/Suspend-Resume Signal Write = No effect
		Read = State of shared keyboard ROW14/SUS_RES pin
5	MATKB_ROW13	ROW13 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
4	MATKB_ROW12	ROW12 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
3	MATKB_ROW11	ROW11 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
2	MATKB_ROW10	ROW10 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
1	MATKB_ROW9	ROW9 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated
0	MATKB_ROW8	ROW8 Signal Write = Set row pin High or Low
		Read = State of row pin
		0 = Signal drives Low
		1 = I/O pin driver is three-stated

Programming Notes

No programmable termination is provided for matrix keyboard row I/O pins. These pins are pulled up internally with the option to disable the pull-ups in Suspend mode.

Keyboard Column Termination Control Register

I/O Address 22h/23h Index CAh

	7	6	5	4	3	2	1	0					
Bit	COL7PULLU	P COL6PULLUP	COL5PULLUP	COL4PULLUP	COL3PULLUP	COL2PULLUP	COL1PULLUP	COLOPULLUP					
Default	1	1	1	1	1	1	1	1					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					
	Bit M 7 (lame COL7PULLUP	Functio COL7 To Write = 5	n ermination Set column re	sistor pull-up	or pull-down							
			Read = I	Read = Last value written									
			0 = Pull-	down resistor									
			1 = Pull-	un resistor									
	6 (OL6PULLUP	COL6 T Write = S	ermination Set column re	sistor pull-up	or pull-down							
			Read = I	Read = Last value written									
			0 = Pull-	0 = Pull-down resistor									
			1 = Pull-	up resistor									
	5 (OL5PULLUP	COL5 Te Write = \$	ermination Set column re	sistor pull-up	or pull-down							
			Read = Last value written										
			0 = Pull-	down resistor									
			1 = Pull-	up resistor									
	4 (OL4PULLUP	COL4 T Write = \$	ermination Set column re	sistor pull-up	or pull-down							
			Read = I	Last value wri	tten								
			0 = Pull-	down resistor									
			1 = Pull-	up resistor									
	3 (OL3PULLUP	COL3 To Write = S	ermination Set column re	sistor pull-up	or pull-down							
			Read = I	Last value wri	tten								
			0 = Pull-	down resistor									
			1 = Pull-	up resistor									
	2 (OL2PULLUP	COL2 T Write = \$	ermination Set column re	sistor pull-up	or pull-down							
			Read =	Last value wri	tten								
			0 = Pull-	down resistor									
			1 = Pull-	up resistor									

Bit	Name	Function
1	COL1PULLUP	COL1 Termination Write = Set column resistor pull-up or pull-down
		Read = Last value written
		0 = Pull-down resistor
		1 = Pull-up resistor
0	COLOPULLUP	COL0 Termination Write = Set column resistor pull-up or pull-down
		Read = Last value written
		0 = Pull-down resistor
		1 = Pull-up resistor

Programming Notes

The termination state that is specified using bits 7–0 is not actually felt at the pins until the Pin Termination Latch Command bit at CSC index E5[0] is set.

Internal I/O Device Disable/Echo Z-Bus Configuration Register

I/O Address 22h/23h Index D0h

_	7		6		5	4	3	2	1	0			
Bit		Rese	erved	EXT_ Z	_ECHO_ BUS	IO_ECHO _ZBUS	DMA1_DIS	DMA0_DIS	PCC_ENB	RTC_DIS			
Default	х		х		0	0	0	0	0	0			
R/W				I	R/W	R/W	R/W	R/W	R/W	R/W			
	Bit	Na	me		Functio	on							
	7–6	Re	served		Reserv During	ed read/modify/\	vrite operation	s, software m	ust preserve t	nese bits.			
	5	ΕX	T_ECHO_ZB	US	Chip S 0 = CS0	etup and Co	ntrol Index Re	e gister Echo s will not be ec	choed to the IS	SA bus			
					 1 = CSC indexed register accesses will echo address 22h/23h and control signals to the ISA bus Data bus signals will exit the ÉlanSC400 microcontroller, but will not make it to the ISA bus since the DBUFOE signal is not driven off the microcontroller for echoed internal register accesses. For an I/O read from an internal register, the data read will be driven off the microcontroller for debug purposes. All echoed internal register accesses will occur at ISA speed. During ECHO_ZBUS cycles, AEN is also asserted so that ISA I/O devices will not decode the ECHO ZBUS cycles. 								
	4	4 IO_ECHO_ZBUS				Internal I/O Register Echo 0 = Internal I/O device accesses will not be echoed to the ISA bus							
					1 = Internal I/O device accesses will echo address and control signals to the ISA Bus								
					Regard and alw display same a	less of the sta ays propaga cards. Writes s port 80h.	ate of this bit, I te to the ISA bi to ports 84h,	/O writes to po us to support p 86h, 88h, 8Ch	ort 80h are a s oort 80h BIOS n, and 8Eh op	pecial case checkpoint erate the			
	3	DN	IA1_DIS		DMA 1 Slave Controller Disable This bit controls the I/O address decode for the internal slave DMA controller core.								
					0 = DMA 1(Slave) controller enabled								
					1 = DM	A 1 (Slave) c	ontroller disab	led					
When this bit is cleared, I/O accesses to the slave DMA controller I/O control and status ports go exclusively to the slave DMA controller. Accesses to direct mapped ports C0h, C2h, C4h, C6h, C8h, CAh, CCh CEh, D0h, D2h, D4h, D6h, D8h, DAh, DCh, and DEh are considered accesses to internal registers and no VL or ISA bus cycle will be generated for accesses to them.							oller I/O oller. Ah, CCh, idered pe						
	generated for accesses to them. When this bit is set, the internal I/O address decode for these ports i disabled, so these same accesses generate external bus cycles. Disa the I/O decode does not disable or reset the master/slave DMA cont core in any way. Accesses to these ports are not considered access internal registers and VL or ISA bus cycles will be generated when t								ports is s. Disabling A controller ccesses to /hen they				

Bit	Name	Function
2	DMA0_DIS	DMA 0 Slave Controller Disable This bit controls the I/O address decode for the internal master DMA controller core.
		0 = DMA 0 (master) controller enabled
		1 = DMA 0 (master) controller disabled
		When this bit is cleared, I/O accesses to the master DMA controller I/O control and status ports go exclusively to the master/slave DMA controller. Accesses to direct mapped ports 00–0Fh are considered internal registers and no VL or ISA bus cycle will be generated for accesses to them.
		When this bit is set, the internal I/O address decode for these ports is disabled, so these same accesses generate external bus cycles. Disabling the I/O decode does not disable or reset the master DMA controller core in any way. Accesses to direct mapped ports 00–0Fh are not considered internal registers and VL or ISA bus cycles will be generated when they are accessed.
1	PCC_ENB	PC Card Controller Enable This bit controls the I/O address decode for the internal PC Card controller. When cleared, all I/O accesses to ports 3E0h and 3E1h generate external bus cycles. When set, I/O writes to port 3E0h go to the internal PC Card controller and to the external buses to support an external secondary PC Card controller.
		0 = Internal PC Card controller disabled Accesses to addresses 3E0h and 3E1h go off the ÉlanSC400 microcontroller to the VL or ISA bus.
		1 = Internal PC Card controller enabled In order to support an external second PC Card controller, writes to 3E0h go to both the internal PC Card controller and to the ISA bus. I/O reads from port 3E0h come from the internal PC Card controller only. Destination selection for writes to port 3E1h are based on the last value written to port 3E0h. If the last value written to port 3E0h was less than 80h, the destination of data written to port 3E1h will be in the internal PC Card controller. If the last value written to port 3E0h was greater than 80h, the write to 3E1h will generate an external bus cycle.
		Disabling the I/O decode does not disable or reset the PC Card controller core in any way, nor does it disable redirection of ROMCSx to PC Card Socket A.
0	RTC_DIS	RTC Controller Enable This bit controls the I/O address decode for the internal RTC core. When cleared, I/O accesses to ports 70h and 71h go exclusively to the internal RTC core. When set, the internal I/O decode the 70h and 71h are disabled, so these same accesses generate external bus cycles. Disabling the I/O decode does not disable or reset the core in any way.
		0 = Internal RTC enabled
		1 = Internal RTC disabled

When this bit is cleared, accesses to direct-mapped ports 70h and 71h are considered internal registers and VL or ISA bus cycles will be generated for accesses to them.

When this bit is set, accesses to direct mapped ports 70h and 71h are not considered internal registers and VL or ISA bus cycles will be generated when they are accessed. This allows use of an ISA-based external RTC module if required by the system design. Disabling the internal RTC does not automatically disable the internal IRQ8 connection between the RTC and the PIC. If an external RTC is used, all internal RTC IRQs must be masked off at the RTC (i.e., the PIE, AIE, and UIE bits must all be cleared).

Programming Notes

To enable the set up of MMS Windows C–F, the internal PC Card controller must be enabled (D0h[1] = 1) and operating in standard mode (F1h[0] = 0). Once any of MMS Windows C–F are opened (via 3E0h/3E1h index space), disabling the internal PC Card controller does not disable the

MMS window(s), but disallows their re-configuration until the internal PC Card controller is re-enabled. When the internal PC Card controller is disabled, I/O accesses to 3E0h/3E1h go off the ÉlanSC400 microcontroller to the sub-ISA bus.

Parallel/Serial Port Configuration Register

	7	6	5	4	3	2	1	0
Bit		Rese	erved		PP_CONFIG	PP_ENB	SP_CONFIG	UART_ENB
Default	х	х	х	х	0	0	0	1
R/W					R/W	R/W	R/W	R/W

Bit	Name	Function
7–4	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
3	PP_CONFIG	Parallel Port Base Address Configuration 0 = Internal parallel port base address = 378h (LPT1)
		1 = Internal parallel port base address = 278h (LPT2)
		Parallel port IRQ levels are separately mapped via CSC index D8[4–3].
2	PP_ENB	Internal Parallel Port Enable 0 = Internal Parallel Port disabled
		1 = Internal Parallel Port enabled
		When the internal parallel port is disabled, accesses to I/O locations in the 378–37Fh and 278–27Fh ranges go off the ÉlanSC400 microcontroller to the ISA bus.
1	SP_CONFIG	Serial Port Base Address Configuration 0 = Internal serial port base address = 3F8h (COM1)
		1 = Internal serial port base address = 2F8h (COM2)
		Serial port IRQ levels are separately mapped via CSC index D8h[6-5].
0	UART_ENB	Internal UART Enable 0 = Internal UART disabled
		1 = Internal UART enabled
		When this bit is cleared, the serial port and serial infrared interfaces are powered down (Power Down Group D), and the associated pins are three-stated with internal pull-downs. When the internal UART is disabled, accesses to I/O locations in the 3F8–3FFh and 2F8–2FFh ranges go off the ElanSC400 microcontroller to the ISA bus.

Parallel Port Configuration Register

I/O Address 22h/23h Index D2h

	7		6	5	4	3	2	1	0
Bit				Reserved			PP_TO_EN	PP_MO	DE[1-0]
Default	х		х	х	х	x	0	0	0
R/W						•	R/W	R	Ŵ
	Bit	Name		Function	1				

DIL	Name	
7–3	Reserved	Reserved During read/modify/write operations, software must preserve these bits.
2	PP_TO_EN	Parallel port EPP Mode Time-Out Enable Bit This bit is undefined unless the EPP mode of operation is selected via bits 1–0 of this register.
		0 = EPP time-out is disabled
		1 = EPP time-out is enabled
1–0	PP_MODE[1-0]	Enhanced Parallel Port (EPP) Enable 0 0 = Set/reset DMA Channel 4 DMA request per the REQDMA bit
		0 1 = Set/reset DMA Channel 5 DMA request per the REQDMA bit
		1 0 = Set/reset DMA Channel 6 DMA request per the REQDMA bit
		1 1 = Set/reset DMA Channel 7 DMA request per the REQDMA bit
		If EPP mode is selected, automatic address and data strobes are generated when I/O writes are performed to the EPP address (port x7Bh) and data ports ($x7C-x7Fh$ where $x = 2$ or 3) respectively. In addition, the parallel status port meaning is changed slightly.
		If Bidirectional mode is selected, data can be transmitted over the parallel port in either direction. See direct-mapped port x7Ah ($x = 2 \text{ or } 3$), bit 5 for more detail on bidirectional operation.

UART FIFO Control Shadow Register

I/O Address 22h/23h Index D3h

	7		6	5	4	3	2 1 0						
Bit		RFRT	[1–0]	Rese	erved	Reserved	TFCLR	RFCLR	FIFOEN				
Default	0		0	х	х	х	0	0	0				
R/W					R R R R								
	Bit 7–6	Na RF	me RT[1–0]	Functio Receive When in which th available fills to th $0 \ 0 = 1 \ 1 \ 0 \ 1 = 4 \ 1 \ 1 = 14$	 Function Receiver FIFO Register Trigger Bits When in 16550-compatible mode, this bit field specifies the trigger level at which the Interrupt Identification Register will report that a received data available interrupt is pending. If received data available interrupts are enabled in the IER, the system will be interrupted when the receive FIFO fills to the trigger as follows: 0 0 = 1 byte 0 1 = 4 bytes 1 0 = 8 bytes 1 1 = 14 bytes 								
				When th will be c	e data in the r leared.	eceive FIFO fa	alls below this	trigger level, t	he interrupt				
	5–4	Re	served	Reserve These b	ed its will read ba	ack '00b'.							
	3	Re	served	Reserve This bit	Reserved This bit will read back '1b'.								
	2	TF	CLR	Transm Since th 02FAh)	Transmit FIFO Clear Since the direct-mapped version of this bit (see direct-mapped 03FAh/ 02FAh) is self-clearing, it always reads back '0b'.								
	1	RF	CLR	Receive Since th 02FAh)	e FIFO Clear e direct-mapp is self-clearing	ed version of g, it always rea	this bit (see d ads back '0b'.	irect-mapped	03FAh/				
	0	FIF	OEN	FIFOs E 0 = UAR	nabled (1655 T is in 16450	0-Compatibl compatible m	e Mode Enab ode	led)					
				1 = UAR	T is in 16550	compatible m	ode						
				This bit must be '1b' when other FIFO control register bits are written to c they will not be programmed. Any mode switch will clear both FIFOs. The FIFOs must be enabled for the IrDA interface to operate in High-Speed mode. Accesses to receive and transmit FIFOs, and to all FIFO control bi in the write-only FIFO Control Register at direct-mapped I/O address 03FAh/02FAh (except bit 0) are disabled. Accesses to receive and transm FIFOs, and to all FIFO control bits in the write-only FIFO Control Register at direct-mapped I/O address 03FAh/02FAh are enabled.									

Interrupt Configuration Register A

I/O Address 22h/23h Index D4h

	7	6	5	4	3	2	1	0		
Bit		PIRQ1	S[3–0]			PIRQ0	S[3–0]			
Default	0	0	0	0	0	0	0	0		
R/W		R/	W			R/	W			
	Bit	Name	Functio	on						
	7–4	PIRQ1S[3–0]	Progra The val (PIRQ1 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 1 1	Programmable Interrupt Request 1 Routing The value in this 4-bit field maps Programmable Interrupt Request 1 (PIRQ1) to an IRQ on the cascaded 8259. $0 \ 0 \ 0 = \text{Disables PIRQ1}$ as an input $0 \ 0 \ 1 = \text{IRQ1}$ $0 \ 0 \ 1 = \text{IRQ1}$ $0 \ 1 \ 0 = \text{Reserved}$ $0 \ 1 \ 1 = \text{IRQ3}$ $0 \ 1 \ 0 = \text{IRQ4}$ $0 \ 1 \ 1 = \text{IRQ5}$ $0 \ 1 \ 0 = \text{IRQ6}$ $0 \ 1 \ 1 = \text{IRQ7}$ $1 \ 0 \ 0 = \text{IRQ8}$ $1 \ 0 \ 1 = \text{IRQ9}$ $1 \ 0 \ 1 = \text{IRQ9}$ $1 \ 0 \ 1 = \text{IRQ10}$ $1 \ 0 \ 1 = \text{IRQ10}$ $1 \ 0 \ 1 = \text{IRQ11}$ $1 \ 1 \ 0 = \text{IRQ12}$ $1 \ 1 \ 0 = \text{IRQ13}$ $1 \ 1 \ 0 = \text{IRQ14}$ $1 \ 1 \ 1 = \text{IRQ15}$						
	30	PIRQ0S[3-0]	Progra The val (PIRQ0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	mmable Interr ue in this 4-bit) to an IRQ on = Disables PIF = IRQ1 = Reserved = IRQ3 = IRQ4 = IRQ5 = IRQ6 = IRQ7 = IRQ8 = IRQ9 = IRQ10 = IRQ12 = IRQ13 = IRQ14	rupt Reques field maps P the cascade QO as an inp	t 0 Routing rogrammable I d 8259. out	nterrupt Req	juest 0		

Interrupt Configuration Register B

I/O Address 22h/23h Index D5h

	7	6	5	4	3	2	1	0			
Bit		PIRQ3S	[3–0]			PIRQ2	2S[3–0]				
Default	0	0	0	0	0	0	0	0			
R/W		R/W	/			R	/W				
	Bit	Name	Functi	on							
	7–4	PIRQ3S[3-0]	Progra	Programmable Interrupt Request 3 Routing							
			The va (PIRQ3	The value in this 4-bit field maps Programmable Interrupt Request 3 (PIRQ3) to an IRQ on the cascaded 8259.							
			0000	= Disables PIR	Q3 as an in	iput					
			0001	= IRQ1							
			0010	= Reserved							
			0011	= IRQ3 - IRO4							
			0100	= IRQ5							
			0110	= IRQ6							
			0111	= IRQ7							
			1000	= IRQ8							
			1001	= IRQ9							
			1010	= IRQ10 - IRO11							
			1100	1 0 1 1 = IRQ11 $1 1 0 0 = IRQ12$ $1 1 0 1 = IRQ13$ $1 1 0 = IRQ14$ $1 1 1 = IRQ15$							
			1101								
			1110								
			1111								
	3–0	PIRQ2S[3-0]	Progra The va (PIRQ2	Programmable Interrupt Request 2 Routing The value in this 4-bit field maps Programmable Interrupt Request 2 (PIRQ2) to an IRQ on the cascaded 8259.							
			0000	= Disables PIR	Q2 as an in	iput					
			0001	= IRQ1							
			0010	= Reserved							
			0011	= IRQ3							
			0100	= IRQ4 - IRO5							
			0101	= IRQ5 = IRQ6							
			0110	= IRQ7							
			1000	= IRQ8							
			1001	= IRQ9							
			1010	= IRQ10							
			1011	= IRQ11							
			1100	= IKQ12 - IRO12							
			1110	= IRQ14							
			1111	= IRQ15							

Interrupt Configuration Register C

I/O Address 22h/23h Index D6h

	7	6	5	4	3	2	1	0				
Bit		PIRQ55	6[3–0]			PIRQ4	S[3–0]					
Default	0	0	0	0	0	0	0	0				
R/W		R/V	V			R/	W					
	Bit	Name	Functi	on								
	7-4	PIRQ5S[3-0]	Progra	Programmable Interrupt Request 5 Routing								
	, ,		The va (PIRQ	The value in this 4-bit field maps Programmable Interrupt Request 5 (PIRQ5) to an IRQ on the cascaded 8259.								
			0000	= Disables PIR = IRQ1	Q5 as an inp	out						
			0010	= Reserved								
			0011	= IRQ3								
			0100	= IRQ4								
			0101	= IRQ5								
			0110	= IRQ6								
			1000	= IRQ7 = IRQ8								
			1001	= IRQ9								
			1010	1 0 1 0 = IRQ10								
			1011	= IRQ11								
			1100	= IRQ12								
			1101	1 1 0 1 = IRQ13								
			1110	1110 = IRQ14 1111 = IRQ15								
	3_0		Progra	Programmable Interrupt Request 4 Routing								
	5-0	1 11(0+0[3-0]	The va (PIRQ4	The value in this 4-bit field maps Programmable Interrupt Request 4 (PIRQ4) to an IRQ on the cascaded 8259.								
			0000	= Disables PIR	Q4 as an inp	out						
			0001	= IRQ1								
			0010	= Reserved								
			0100	= IRQ3 = IRQ4								
			0101	= IRQ5								
			0110	= IRQ6								
			0111	= IRQ7								
			1000	= IRQ8								
			1001	= IRQ9								
			1010									
			1100	= IRQ12								
			1101	= IRQ13								
			1110	= IRQ14								
			1111	= IRQ15								

Interrupt Configuration Register D

I/O Address 22h/23h Index D7h

	7	6	5	4	3	2	1	0				
Bit		PIRQ7	6[3–0]			PIRQ6	S[3–0]					
Default	0	0	0	0	0	0	0	0				
R/W		R/\	N			R/	W					
	Bit	Name	Functio	Function Programmable Interrupt Request 7 Routing								
	7–4	PIRQ7S[3-0]	Progra									
			The val	ue in this 4-bit	field maps F	Programmable I	nterrupt Req	uest 7				
				(PIRQ) to an IRQ on the cascaded 8259.								
			0001	= IRQ1		put						
			0010	= Reserved								
			0011	= IRQ3								
			0100	= IRQ4								
			0101	= IRQ5								
			0110	= IRQ6								
			0111	= IRQ7 - IRO8								
			1000	= IRQ9								
			1010	= IRQ10								
			1011	1 0 1 1 = IRQ11 1 1 0 0 = IRQ12								
			1100									
			1101	= IRQ13								
			1110	= IRQ14								
			1111	= IRQ15								
	3–0	PIRQ6S[3–0]	Program The val	Programmable Interrupt Request 6 Routing The value in this 4-bit field maps Programmable Interrupt Request 6								
				(PIRQb) to an IRQ on the cascaded 8259. 0.0.0.0 = Disables PIRO6 as an input								
			0000	= IRQ1		put						
			0010	= Reserved								
			0011	= IRQ3								
			0100	= IRQ4								
			0101	= IRQ5								
			0110	= IRQ6								
			0111	= IRQ7 - IRQ8								
			1000	= IRQ8 - IRQ9								
			1010	= IRQ10								
			1011	= IRQ11								
			1100	= IRQ12								
			1101	= IRQ13								
			1110	= IRQ14								
			1111	= IRQ15								

Interrupt Configuration Register E

	7		6	5	4	3	2	1	0		
Bit	CURCO IRQ_E	N_ N	UART_IRD	A_IRQS[1–0]	PPORT_	IRQS[1-0]		Reserved			
Default	0		0	0	0	0	0	0	0		
R/W	R/W		R	/W	R	/W		R/W			
	Bit 7	Na CU	me RCON_IRQ_	EN	Function Cursor Address Register Access IRQ Enable						
					When this bit is set, writes to the 6845-compatible cursor address registers at CSC indexes 0Eh and 0Fh of 3x4/3x5h address space will generate IRQ9 to the system. This interrupt can be used to keep track of the cursor location independent of application software when the physical display screen is smaller than the frame buffer.						
					0 = IRQ9 is no high/low r	ot generated to egisters	the PIC by w	rites to cursor	address		
					1 = IRQ9 is generated to the PIC by writes to cursor address high/ low registers						
	6–5 UART_IRDA_IRQS[1–0]				UART and Ir Controls map IRQ to the pro	DA IRQ Routin ping of either t ogrammable in	ng he UART or tl terrupt contro	he IrDA core's ller.	internal		
					0 0 = Disables UART/IRDA IRQs as an input to the PIC						
					0 1 = UART/IRDA IRQ mapped to the IRQ3 input of the PIC						
					1 0 = UART/IRDA IRQ mapped to the IRQ4 input of the PIC						
					1 1 = Disables UART/IRDA IRQ as an input to the PIC						
					In regard to UART/IrDA IRQs, when CSC index EAh[0] = 0 (UART mode), only normal UART (16450/550) IRQ generation sources are available. When CSC index EAh[0] = 1, and CSC index EAh[1] = 0 (Slow-Speed IrDA mode), only normal UART (16450/550) IRQ generation sources are available. When CSC index EAh[0] = 1, and CSC index EAh[1] = 1 (High-Speed IrDA mode), only IrDA IRQ sources (see CSC index EBh[6–4]) are available.						
	4–3 PPORT_IRQS[1–0]			-0]	Parallel Port Controls map programmabl	IRQ Routing ping of the on e interrupt con	board parallel troller.	port's interna	I IRQ to the		
				0 0 = Disable	s PPORT_IRG	as an input to	o the PIC				
					0 1 = PPORT	IRQ mapped	to the IRQ5 in	put of the PIC			
					1 0 = PPORT IRQ mapped to the IRQ7 input of the PIC						
				1 1 = Disables PPORT IRQ as an input							
	2–0 Reserved				Reserved						

DMA Channel 0-3 Extended Page Register

I/O Address 22h/23h Index D9h

	7	6	5	4	3	2	1	0
Bit	DMA3[25–24]		DMA2[25–24]		DMA1[25–24]		DMA0[25-24]	
Default	0 0		0	0	0 0		0 0	
R/W	R/W		R/W		R/W		R/W	

Bit	Name	Function
7–6	DMA3[25-24]	DMA Channel 3 Page Register Extension Highest two bits of memory address [A25–A24] for Channel 3.
5–4	DMA2[25-24]	DMA Channel 2 Page Register Extension Highest two bits of memory address [A25–A24] for Channel 2.
3–2	DMA1[25-24]	DMA Channel 1 Page Register Extension Highest two bits of memory address [A25–A24] for Channel 1.
1–0	DMA0[25-24]	DMA Channel 0 Page Register Extension Highest two bits of memory address [A25–A24] for Channel 0.

DMA Channel 5-7 Extended Page Register

I/O Address 22h/23h Index DAh

	7		6	5	5 4		3 2		0	
Bit	Reserved			DMA7[25–24]		DMA6[25–24]		DMA5[25-24]		
Default	x x		х	0	0	0	0	0	0	
R/W				R/W		R/W		R/W		
	Bit 7–6	Name Reserve	d	Function Reserved During read/modify/write operations, software must preserve the						
	5–4	DMA7[28	5–24]] DMA Channel 7 Page Register Extension Highest two bits of memory address [A25–A24] for Channel 7.						
	3–2	DMA6[28	5–24]	DMA Ch Highest	two bits of me	e Register Ex emory address	jister Extension / address [A25–A24] for Channel 6.			
	1–0	DMA5[28	5–24]	DMA Channel 5 Page Register Extension Highest two bits of memory address [A25–A24] for Channel 5.						

DMA Resource Channel Map Register A

I/O Address 22h/23h Index DBh

	7	6		5	4	3	2	1	0			
Bit	IRDA	CH_SEL[1-(0]	PDMA1_CH_SEL[2-0]		PDI	MA0_CH_SEL[2	-0]				
Default	0	0)	0	0	0	0	0			
R/W		R/W			R/W			R/W				
	Bit	Name		Function								
	7–6	IRDA_CH_	SEL[1-0]	IR 0 (IRDA Controller DMA Channel Routing 0 0 = Unconnected							
				0 1	I = Channel 0	8-bit channe	l)					
				1 () = Channel 1 (8-bit channe	l)					
				1 1	I = Unconnecte	ed						
	5–3 PDMA1_CH_SEL			Pr Ma co	Programmable DMA Controller Channel 1 Routing Map PDRQ1/PDACK1 programmable DMA pins to an internal DMA controller channel:							
				0 0 0 = Unconnected								
				0 0	0 0 1 = Channel 0 (8-bit channel)							
				0 1	0 1 0 = Channel 1 (8-bit channel)							
				0 1	0 1 1 = Channel 2 (8-bit channel)							
				1 0 0 = Channel 3 (8-bit channel)								
				1 (1 0 1 = Channel 5 (16-bit channel)							
				1 1	1 1 0 = Channel 6 (16-bit channel)							
				1 1	1 1 1 = Channel 7 (16-bit channel)							
	2–0 PDMA0_CH_SI		H_SEL[2–0]	Pr Ma co	ogrammable I ap PDRQ0/PD/ ntroller channe	DMA Control ACK0 program I:	ler Channel (mmable DMA) Routing pins to an inte	rnal DMA			
				0 0	0 0 0 = Unconnected							
				0 0) 1 = Channel () (8-bit chanr	nel)					
				0 1	0 = Channel	I (8-bit chanr	nel)					
				0 1	1 1 = Channel 2	2 (8-bit chanr	nel)					
				1 (0 0 = Channel 3	3 (8-bit chanr	nel)					
				1 () 1 = Channel (5 (16-bit char	nel)					
				1 1	0 = Channel 6	6 (16-bit char	nnel)					
				1 1 1 = Channel 7 (16-bit channel)								

DMA Resource Channel Map Register B

I/O Address 22h/23h Index DCh

6	5	4	3	2	1	0
Rese	rved		PCMB_CH_SEL[1-0]		PCMA_CH_SEL[1-0]	
х	х	х	0	0	0	0
			R	/W	R	/W
Name Reserved PCMB_CH_SEL	Fun Res Duri [1-0] PC (ction erved ng read/modify Card Socket E	//write operati 5 DMA Chanı	ons, software nel Routing	must preserv	e these bits.
		= Channel 3 (8 = Channel 2 (8 = Channel 2 (1	3-bit channel) 3-bit channel) 16-bit channe	I)		
PCMA_CH_SEL	[1-0] PC (0 0 0 1 1 0 1 1	Card Socket A = Unconnecter = Channel 3 (8 = Channel 2 (8 = Channel 5 (1	DMA Chanı d 3-bit channel) 3-bit channel) 16-bit channe	nel Routing		
	6 Rese Reserved PCMB_CH_SEL	6 5 Reserved x x Name Fund Reserved Reserved PCMB_CH_SEL[1-0] PC 0 00 01 10 11 PCMA_CH_SEL[1-0] PC 0 01 10 11 10 11 10 11 10 11 10 11 10 11 10 11 10 11 10 11 10 11 10 11 10	6 5 4 Reserved x x x x x x Name Function Reserved During read/modify PCMB_CH_SEL[1-0] PC Card Socket E 0 0 = Unconnected 0 1 = Channel 3 (& 1 0 = Channel 2 (& 1 1 = Channel 5 (1 PCMA_CH_SEL[1-0] PC Card Socket A 0 0 = Unconnected 0 1 = Channel 2 (& 1 1 = Channel 3 (& 1 0 = Channel 3 (& 1 0 = Channel 3 (& 1 0 = Channel 3 (& 1 0 = Channel 3 (& 1 0 = Channel 3 (& 1 1 = Channel 3 (& 1 0 = Channel 3 (& 1 1 = Channel 3 (& 1 0 = Channel 3 (& 1 1 = Channel 3 (& 1 1 = Channel 3 (&	6 5 4 3 Reserved PCMB_CH x x x 0 x x x 0 Reserved Reserved Reserved DUring read/modify/write operation 00 = Unconnected PCMB_CH_SEL[1-0] PC Card Socket B DMA Channelly 0 0 = Unconnected 0 1 = Channel 3 (8-bit channel) 1 0 = Channel 2 (8-bit channel) 1 1 = Channel 5 (16-bit channel) PCMA_CH_SEL[1-0] PC Card Socket A DMA Channelly 0 0 = Unconnected 0 1 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 1 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 1 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 1 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 1 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 1 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel)	6 5 4 3 2 Reserved PCMB_CH_SEL[1-0] x x x 0 0 Reserved Reserved Reserved PCMB_CH_SEL[1-0] PC Card Socket B DMA Channel Routing 0 0 = Unconnected 0 1 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 2 (8-bit channel) 1 1 = Channel 5 (16-bit channel) 0 0 = Unconnected 0 1 = Channel 3 (8-bit channel) 1 1 = Channel 3 (8-bit channel) PCMA_CH_SEL[1-0] PC Card Socket A DMA Channel Routing 0 0 = Unconnected 0 1 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 0 = Channel 3 (8-bit channel) 1 1 = Channel 5 (16-bit channel) 1 1 = Channel 5 (16-bit channel)	6 5 4 3 2 1 Reserved PCMB_CH_SEL[1-0] PCMA_CH x x x 0 0 0 x x x 0 0 0 0 Reserved During read/modify/write operations, software must preserv PCMB_CH_SEL[1-0] PC Card Socket B DMA Channel Routing 0

Internal Graphics Control Register A

	7		6	5	4	3	2	1	0					
Bit	VERTDO	OUB	DOT320	DOTDOUB	DRWIDTH	DUAL_SCRN	VID_ENB	FLATENB	COMP_MOD					
Default	0		0	0	0	0	0	0	0					
R/W	R/W	/	R/W	R/W	R/W	R/W	R/W	R/W	R/W					
	Bit	Na	me	Function										
	7	VE	RTDOUB	Vertical 0 = Norn	Line Doublin nal (no doubli	n g Enable ng)								
				1 = Doul	ole each verti	cal line (e.g., c	lisplay 120 lin	es on 240 scr	een)					
	6	DC	DT320	Horizon 0 = Unco	tal Dot Doub anditionally do	ling Qualifier	ontrolled by b	oit 5						
				1 = Dout pixel	 Double horizontal dots only in CGA modes which display 320 horizontal pixels (e.g., double in 40-column mode, but not in 80-column mode) 									
				To use t	his mode, bit	0 of this regist	er must be cle	eared.						
	5	DC	DTDOUB	Horizontal Dot Doubling Enable 0 = Normal (no doubling).										
				1 = Double horizontal dots (e.g., display 320 dots on 640 screen)										
	4	DF	RWIDTH	Drive Width Select (Applies to Single Scan Panels Only) 0 = Select 4 bits per shift										
				1 = Select 8 bits per shift (requires 8-bit data interface to panel)										
	3	DL	JAL_SCRN	Panel Type Select 0 = Single scan, single drive										
				1 = Dual scan, dual drive										
	2	VI	D_ENB	Enable Graphics Controller 0 = Internal graphics disabled										
				1 = Internal graphics enabled										
		The internal graphics controller will not work when any other 3 interface is enabled such as the DRAM and ROM interfaces. In the graphics controller should not be enabled at the same time VESA bus interface (see CSC index 14h[3]) since they share p ElanSC400 microcontroller.						2-bit addition, as the ins on the						
	1	FL	ATENB	Select Linear Flat-mapped Graphics Mode 0 = CGA/MDA compatible mode										
				1 = Enable linear flat-mapped graphics										
	0	СС	MP_MOD	Compat 0 = 3D4/	ibillty Mode ⁄3D5h visible,	compatibility r	node will be (CGA						
				1 = 3B4/	3B5h visible,	compatibility r	node will be N	IDA						

Internal Graphics Control Register B

	7		6	5	4	3	2	1	0				
Bit	UNDERE	NB	REGLOCK	PIXDEF	TH[1–0]	GRAPOL	TXTPOL	BLANKDAT	NONDISP				
Default	0		0	0	0	0	0	0	0				
R/W	R/W		R/W	R/W		R/W	R/W	R/W	R/W				
	Bit	Na	me	Functio	Function								
	7 UNDEREND		0 = Disa ignoi CGA	0 = Disable underline attribute. Bit 3 of the character attribute byte will be ignored in MDA mode, but will be used in character color processing in CGA mode.									
					1 = Enable underline attribute. Bit 3 of the character attribute byte will add an underline to a character. Bit 3 will not be used in character color processing.								
	6	REGLOCK		Lockou 0 = Enat conti	t for Graphic ble graphics co coller must be	s Controller I ontroller index enabled also)	ndexed Regi ed registers a	sters at 3x4/3 at 3x4/3x5h (G	x5h raphics				
				1 = Lock	1 = Lockout graphics controller indexed registers at 3x4/3x5h								
	5–4	PIXDEPTH[1-0]		Pixel De 0 0 = 1 k	Pixel Depth for Linear Flat-mapped Modes 0 0 = 1 bit per pixel								
				0 1 = 2 k	0 1 = 2 bits per pixel								
				1 0 = 4 k	1 0 = 4 bits per pixel								
				1 1 = Re	served								
	3	GR	APOL	Graphic Modes Data Polarity 0 = Do not invert output data in Graphics modes									
				1 = Inve	1 = Invert all output data in Graphics modes								
	2	ΤX	TPOL	Text Mo 0 = Do r	Text Mode Data Polarity 0 = Do not invert output data in text modes								
				1 = Inve	1 = Invert all output data in text modes								
	1	BLANKDAT		Blanked This bit of region b between overridd Register	I Data Value controls the sl ut contains no Display End en in some m (ports 3x4h/3	hading of data memory map and Border Er odes by settin 8x5h index 43h	that is within pped pixel info nd). The shad g bit 7 of the n).	the displayed ormation (i.e., e set by this b Gray Shade M	screen pixels it can be lode				
				0 = Set I	planked data t	to 0							
				1 = Set I	planked data f	to 1							
	0 NONDISP		Non-dis This bit beyond lines reg setting.	Non-display Data Value This bit controls the shading of data which can be output on excess lines beyond the limit of the displayed area. Applicable only if the non-display lines register is programmed to a non-zero value. Bits 2–3 do not affect this setting.									
				0 = Set i	non-display da	ata to 0							
				1 = Set i	non-display da	ata to 1							

Write-protected System Memory (DRAM) Window/Overlapping ISA Window Enable Register

I/O Address 022h/023h Index E0h

	7		6	5	4	3	2	1	0			
Bit	Reserv	ed	ISAWIN_EN			WPWIN_S	FOP[25–20]					
Default	х		0	0	0	0	0	0	0			
R/W			R/W			R/	W					
	Bit	Name			Function							
	7	Re	Reserved		Reserved During read/modify/write operations, software must preserve this bit.							
	6	6 ISAWIN_EN		Enable Overlap 0 = Programmal	ping ISA Win	dow w disabled						
					1 = Programmable ISA window enabled							
					This ISA Window is defined as an address range that, when enabled, will overlap physical system memory (DRAM). When this window is enabled, CPU accesses to this address range will generate an VL or ISA bus cycle instead of a DRAM cycle. This feature allows an ISA memory hole to be created within DRAM space anywhere below 16 Mbyte.							
	5–0	WF	PWIN_STOP[2	25–20]	Stop Address I Contains bits 5– window. There a boundaries betw address space. protect window g	Bits SA25–SA 0 of the stop a are 63 valid sto veen 64 Mbyte The start addr grows downwa	20 address bits fo op addresses is and 1 Mbyte ess is always ard.	or this write-pr which reside o e of the physio 3FFFFFFh, s	otected on 1 Mbyte cal DRAM o the write			
					[3Fh] = 1 Mbyte window size (from 3FFFFFF–3F00000h)							
					[3Eh] = 2 Mbyte	window size (from 3FFFFF	F–3E00000h)				
					[01h] = 63 Mbyte	e window size	(from 3FFFFI	FF–0100000h)			
					[00h] = System DRAM write protect window is disabled							
					Note that this wirds system DRAM resources residen no effect on those	rite protect win esides from 0- e above that, th se memory-ma	dow applies of -4MB, and oth he DRAM write apped resourc	only to system her memory m e protect windo ces.	DRAM. If lapped ow will have			

Overlapping ISA Window Start Address Register

I/O Address 022h/023h Index E1h



Overlapping ISA Window Size Register

I/O Address 022h/023h Index E2h



Suspend Pin State Register A

	7		6	5		4	3	2	1	0			
Bit	NOPWF PCMB_S	₹_ ธับธ	NOPWR_ PCMA_SUS	NOPWR_ SUS	VL_	Reserved	NOPWR_ UART_SUS	NOPWR_ ISA_SUS	NOPWR_ ROM_SUS	NOPWR_ DRAM_SUS			
Default	0		0	0		0	0	0	0	0			
R/W	R/W		R/W	R/W		R/W	R/W	R/W	R/W	R/W			
	Bit	Na	me		Function								
	7	NOPWR_PCMB_SUS			PC Card Socket B Interface Powered or Not Powered in Suspend Mod IOR and IOW need special handling if the ISA interface is not powered down (Power Down Group H).								
						Powered, sig	nals stopped	inactive					
					1 =	Not powered	l, signals three	e-state with pu	ull-downs				
	6	NOPWR_PCMA_SUS			PC 101 (Pc	Card Socke R and IOW ne ower Down G	t A Interface ed special hai roup G).	Powered or N ndling if the IS	lot Powered A interface is	in Suspend Mode not powered down			
					0 =	Powered, sig	gnals stopped	inactive					
					1 = Not powered, signals three-state with pull-downs								
	5	NC	NOPWR_VL_SUS			VL Local Bus Interface Powered or Not Powered in Suspend Mode (Power Down Group F) 0 = Powered, signals stopped inactive							
					1 =	Not powered	l, signals three	e-state with pu	ull-downs				
	4	Re	served		Re	served							
	3	NC	NOPWR_UART_SUS			Serial Port and Serial Infrared Interfaces Powered or Not Powered in Suspend Mode (Power Down Group D) 0 = Powered, signals stopped inactive							
					1 = Not powered, signals three-state with pull-downs								
					lf C are mo	CSC index D1 powered dow odes, so this b	h[0] is cleared vn with pins th it has no effec	l, the serial po pree-stated ar ct.	rt and serial ind internally p	nfrared interfaces ulled down in all			
	2	NC	NOPWR_ISA_SUS			 ISA Bus Interface Powered or Not Powered in Suspend Mode The ISA signals that share pins with other functions will only be at this register if they are enabled rather than the alternate function. IOW need special handling if both PC Card interfaces are not pow down. (Power Down Group C) 							
					0 =	Powered, sig	nals stopped	inactive					
					1 =	Not powered	l, signals three	e-state with pu	ull-downs				
	1	NC	NOPWR_ROM_SUS		ROM Interface Powered or Not Powered in Suspend Mode (Power Down Group B) 0 = Powered, signals stopped inactive								
					1 = Not powered, signals three-state with pull-downs								
	0	NC	PWR_DRAM	_SUS	DRAM Interface Powered or Not Powered in Suspend Mode (Power Down Group A) 0 = Powered, signals active for DRAM refresh								
					1 =	Not powered	l, signals three	e-state with pu	ull-downs				

Suspend Pin State Register B

I/O Address 22h/23h Index E4h

	7	6	5	4	3	2	1	0			
Bit				Reserved				NOPWR_ SDBUF_SUS			
Default	х	х	х	x	х	х	х	0			
R/W								R/W			
	Bit 7–1	Name Reserved		Function Reserved During read/modify/write operations, software must preserve these bits.							
	0	NOPWR_SDBU	F_SUS	DBUFOE, R32BFOE Powered or Not Powered in Suspend Mode (Power Down Group A) 0 = Powered							
				1 = Not powered	l, signals three	e-state with p	ull-downs				
				This bit has no n the DBUFOE or enabled if the R software prograr enables R32BF programming de	neaning unles R32BFOE sig OMCS0 32-bi ns the ROMC DE). See CSC tails.	s either pin st nals (R32BF0 t interface is s S0 interface t ; index 20h[1-	raps are set u DE is automat elected via pi o be 32-bit (th -0] for ROMCS	ip to enable ically n strap), or nis also 50 width			

Suspend Mode Pin State Override Register

I/O Address 22h/23h Index E5h

	7	6	5	4	3	2	1	0
Bit	SKTB_OVRD	SKTA_OVRD	SDBUF_OVRD	Reserved	Reserved	ISA_OVRD	ROM_OVRD	TERM_LATCH
Default	0	0	0	Х	х	0	0	0
R/W	R/W	R/W	R/W			R/W	R/W	R/W

Bit	Name	Function
7	SKTB_OVRD	PC Card Socket B Termination Override When the PC Card Socket B interface remains powered in Suspend mode, setting this bit will cause the Power Down Group H output signals, which are normally driven high, to be three-stated instead. This can be used to override the suspend pin state setting that results when bit 7 of the Suspend Pin State Register $A = '0b'$.
		0 = The Power Down Group H signals are driven high if the interface is to remain powered in Suspend mode as configured via bit 7 of the Suspend Pin State Register A
		1 = The Power Down Group H signals are three-stated if the interface is to remain powered in Suspend mode
6	SKTA_OVRD	PC Card Socket A Termination Override When the PC Card Socket A interface remains powered in Suspend mode, setting this bit will cause the Power Down Group G output signals, which are normally driven high, to be three-stated instead. This can be used to override the suspend pin state setting that results when bit 6 of the Suspend Pin State Register $A = '0b'$.
		0 = The Power Down Group G signals are driven high if the interface is to remain powered in Suspend mode as configured via bit 6 of the Suspend Pin State Register A
		1 = The Power Down Group G signals are three-stated if the interface is to remain powered in Suspend mode
5	SDBUF_OVRD	Suspend Mode Termination Override When the DBUFOE, R32BFOE signals remain powered in Suspend mode, setting this bit will cause these output signals, which are normally driven high, to be three-stated instead. This can be used to override the suspend pin state setting that results when bit 0 of the Suspend Pin State Register B = '0b'.
		0 = The DBUFOE, R32BFOE signals are driven high if the interface is to remain powered in Suspend mode as configured via bit 0 of the Suspend Pin State Register B
		1 = The DBUFOE, R32BFOE signals are three-stated if the interface is to remain powered in Suspend mode
		This bit has no meaning unless either pin straps are set up to enable the DBUFOE or R32BFOE signals (R32BFOE is automatically enabled if the ROMCS0 32-bit interface is selected via pin strap), or software programs the ROMCS0 interface to be 32-bit (this also enables R32BFOE). See CSC index 20h[1–0] for ROMCS0 width programming details.
4	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
Bit	Name	Function
-----	------------	---
3	Reserved	Reserved During read/modify/write operations, software must preserve this bit.
2	ISA_OVRD	ISA Interface Termination Override When the ISA interface remains powered in Suspend mode, setting this bit will cause the Power Down Group C output signals, which are normally driven high, to be three-stated instead. This can be used to override the suspend pin state setting that results when bit 2 of the Suspend Pin State Register A = '0b'.
		0 =The Power Down Group C signals are driven high if the interface is to remain powered in Suspend mode as configured via bit 2 of the suspend Pin State Register A
		1 =The Power Down Group C signals are three-stated if the interface is to remain powered in Suspend mode
1	ROM_OVRD	ROM Interface Termination Override When the ROM interface remains powered in Suspend mode, setting this bit will cause the Power Down Group B output signals, which are normally driven high, to be three-stated instead. This can be used to override the suspend pin state setting that results when bit 1 of the Suspend Pin State Register A = '0b'.
		0 = The Power Down Group B signals are driven high if the interface is to remain powered in Suspend mode as configured via bit 1 of the Suspend Pin State Register A
		1 = The Power Down Group B signals are three-stated if the interface is to remain powered in Suspend mode
0	TERM_LATCH	Pin Termination Latch Command This bit affects CSC index registers 3B–3Eh, CAh, EA[6], and F2h, all of which control termination for certain pins on the device. Writing to these CSC index registers does not result in a change in the termination at the pins until this bit is set. While the actual pin terminations are in the process of being configured internally, this bit will read back '1b' to indicate that further pin termination changes should not be attempted by software. When this bit reads back '0b', it is safe to reconfigure terminations. Writing this bit to '0b' has no effect. For termination control bits that only affect termination during suspend, it is not necessary to set this bit for the changes to take effect since this will automatically occur when suspend is entered.

IrDA Control Register

	7		6	5	4	3	2	1	0			
Bit	EOT_SL	CT.	SIRIN_PD_DIS	RECV_ BLOCKING	IRDA_RECEIVE	IRQ_ENABLE	START_DMA	SELMODE	SELDEVICE			
Default	х		0	0	0	0	0	0	0			
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W			
	Bit	Na	me	Functio	on							
	7	EC	T_SLCT	End of	Transmissio	n Status Bit S	Select	nal count stat				
				0 = TC/ 1 = TC/	EOT status bi	it in CSC inde	x = Bh = ond c	f transmission				
				T = TC/		at CSC index I	EBb[6] for mo	n transmission ro dotail	TSIAIUS			
	6	CIE										
	0	Sir		Serial I (regard 0 = SIR	lless of PMU	mode). I pull-down re	sistor is enabl	ed	adie			
				1 = SIR	IN pin interna	l pull-down re	sistor is disab	led				
				The pul felt at th E5[0] is	The pull-down resistor state that is specified using this bit is not actually felt at the pin until the Pin Termination Latch Command bit at CSC index E5[0] is set.							
	5	RE	CV_BLOCKIN	NG Receiv 0 = Ena	Receive Blocking 0 = Enables receive blocking during transmit							
				1 = Dis	1 = Disables receive blocking during transmit							
	4	IRI	DA_RECEIVE	IrDA R This bit	IrDA Receive This bit determines the IrDA data direction.							
				0 = IrD	0 = IrDA is in Transmit mode							
				1 = IrD/	1 = IrDA is in Receive mode							
	3	IR	Q_ENABLE	High-S This bit interrup in High	High-Speed IrDA IRQ Enable This bit controls the generation of high speed mode (DMA-based) IrDA interrupt requests. This bit is only valid when the IrDA interface is operated in High-Speed (DMA) IrDA mode.							
				0 = Dis	ables the over	flow, underflo	w, and termin	al count IrDA	IRQs			
				1 = Ena generat	1 = Enables the overflow, underflow, and terminal count (TC) IRQs generated from IrDA							
	2	2 START_DMA		IrDA D 0 = No	IrDA DMA Start-Up Control 0 = No effect							
				1 = Indi mod	cates to the H de	ligh-Speed IrE	DA block to ini	tiate DRQs in	Transmit			
				The bit on a DN DMA tra	is automatica MA channel th ansmit modes	lly cleared whe at is routed to	en the TC (ter the IrDA bloc	minal count) i k during the H	s reached l igh-Speed			

Name	Function
SELMODE	IrDA Data Rate Select 0 = IrDA Slow-Speed mode (115 Kbits/second)
	1 = IrDA High-Speed mode (1.15 Mbits/second)
	High-Speed IrDA mode uses DMA only. Normal UART interrupts generated due to receive buffer full, Transmit Holding Register empty, and status changes do not apply, and will not be generated. In order to operate in High-Speed IrDA mode, the UART must be set up for 16550-compatible mode, that is, FIFOs enabled, via the FIFO Control Register at direct-mapped I/O location 03FAh/02FAh. Slow-Speed IrDA mode operation requires that the UART be set up for 8 data bits, no parity, and 1 stop bit via the UART Line Control Register at direct-mapped I/O location 03FBh/02FBh. Slow-Speed IrDA mode does not use DMA, and uses all of the traditional UART interrupts and controls for data transfer.
SELDEVICE	UART or IrDA Mode Select 0 = UART mode
	1 = IrDA mode
	When UART mode is selected, the IrDA interface and all associated control and status bits have no meaning except this bit. When IrDA mode is selected and is operated in Slow-Speed IrDA mode by clearing this bit, use all of the normal 16550 UART control and status bits to transmit and receive data over the IrDA interface.
	Name SELMODE SELDEVICE

Programming Notes

The use of either Low- or High-Speed IrDA requires that the on-board UART be enabled by setting CSC index D1h[0].

IrDA Status Register

I/O Address 22h/23h Index EBh

	7	6	5	4	3	2	1	0	
Bit	HS_IRDA_ IRQ_STATUS	TC/EOT	RECV_OVER FLOW	XMIT_ UNDERFLOW	RECV_FIFO_ FULL	RECV_FIFO_ EMPTY	XMIT_FIFO_ FULL	XMIT_FIFO_ EMPTY	
Default	0	0	0	0	0	1	0	1	
R/W	R	R/W	R/W	R/W	R	R	R	R	
	Bit N	ame	I	Function					
	7 F	S_IRDA_IRQ_	STATUS I T C L L C C	High-Speed Mode IrDA Interrupt Request Status This bit indicates the status of a High-Speed mode IrDA interrupt request. It is a logical OR of bits 4, 5, and 6 of this register, only if CSC index EAh[3] (IRQ_ENABLE) is set; otherwise, this bit reads back '0b'. This bit is cleared automatically when all of the latched IRQ status represented by bits 4, 5, and 6 of this register have been cleared.					
			() = High-Spee When slow 16550-con generate II	ed mode IRQ f v speed IrDA i npatible regist RQs, and rece	rom IrDA has s selected, the ers are used t eive status.	not occurred e normal to control the	FIFO,	
				1 = High-Spee	ed mode IRQ f	rom IrDA has	occurred		
	6 T	C/EOT	<u> </u> -	IrDA DMA Terminal Count/End of Transmission Status This bit is only valid when operating the IrDA interface in High-Speed (DMA) mode.					
			(0 = DMA TC/EOT did not generate an IrDA IRQ If CSC index EAh[7] = 0, this is the IrDA TC (Terminal Count) status and interrupt clear bit. This bit will be set, and an IRQ will be generated, if IrDA DMA mode related IRQs are enabled via CSC index EAh[3], and the DMA controller signals that it has transferred all data possible without further software intervention (the DMA transfer count has expired). Software should write a '0b' to this bit to clear the TC interrupt (a write of '1b' has no effect).					
				1 = DMA TC/E If CSC ind Transmiss and an IRC are enable transferred transfer ha condition v having rec	OT did gener ex EAh[7] = 1 ion) status an Q will be gene d via CSC inc to the transm s actually bee vill be true wh eived the inter	ate an IrDA IR , this is the IrD d interrupt cle rated, if IrDA I lex EAh[3], an hit FIFO for a g en transmitted en 8 bit-times rnal IrDA DMA	Q A EOT (End ar bit. This bit DMA mode-re d all data that given IrDA DM out the IrDA p have transpir A TC signal.	Of will be set, lated IRQs has been IA block bort. This ed after	
	5 R	ECV_OVERFL	OW I	Receive FIFO This bit is only High-Speed (I generated, if In ndex EAh[3], oyte into the ra- he DMA contra n indication to data from the receiver is fillir his bit to clean nas no effect).	Overflow Sta valid when op DMA) mode. T rDA DMA mode and the IrDA in ecceive FIFO in roller, but the o software that receive FIFO ing the receive F	atus berating the Ir his bit will be de related IRC receiver attem of preparation f receive FIFO it the DMA con to system men FIFO. Softwa IFO overflow	DA interface i set and an IR as are enabled of storage to for storage to is completely ntroller could mory as fast a are should writ interrupt (a w	n Q will be I via CSC eceived a memory by full. This is not transfer s the IrDA e a '0b' to rite of '1b'	
			(0 = Overflow o	lid not genera	te an IrDA IRO	Q		
				1 = Overflow g	generated an I	rDA IRQ			

Bit	Name	Function
4	XMIT_UNDERFLOW	Transmit FIFO Underflow Status This bit is only valid when operating the IrDA interface in High-Speed (DMA) mode. This bit will be set and an IRQ will be generated, if IrDA DMA mode related IRQs are enabled via CSC index EAh[3], and the IrDA transmitter attempts to remove a byte from the transmit buffer in preparation for transmission, but the transmit FIFO buffer is completely empty. This is an indication to software that the DMA controller could not transfer data from system memory to the transmit FIFO as fast as the IrDA transmitter is emptying the transmit FIFO. Software should write a '0b' to this bit to clear the transmit FIFO underflow interrupt (a write of '1b' has no effect).
		0 = Underflow did not generate an IrDA IRQ
		1 = Underflow generated an IrDA IRQ
3	RECV_FIFO_FULL	Receive FIFO Full Status 0 = Receive FIFO is not full
		1 = 16 byte receive FIFO is full
2	RECV_FIFO_EMPTY	Receive FIFO Empty Status 0 = Receive FIFO is not empty
		1 = 16 byte receive FIFO is empty
1	XMIT_FIFO_FULL	Transmit FIFO Full Status 0 = Transmit FIFO is not full
		1 = 16 byte transmit FIFO is full
0	XMIT_FIFO_EMPTY	Transmit FIFO Empty Status 0 = Transmit FIFO is not empty
		1 = 16 byte transmit FIFO is empty

Programming Notes

If CSC index EAh[3] is ever disabled and bit 7 = 1, bits 6–4 of this register should be cleared by software. Also note that if more than one of bits 6–4 is set and software does not clear all of the pending interrupts during the write to CSC index EBh, special hardware will automatically generate another edge to the PIC so that another IRQ will occur when the current Interrupt Handling Routine (IHR) finishes and exits. This allows the IHR to handle one event per IRQ without risk of losing an IRQ. If software clears all pending IRQ sources simultaneously, hardware will not generate this automatic edge to the PIC.

IrDA CRC Status Register

I/O Address 022h/023h Index ECh

	7	6	5	4	3	2	1	0
Bit	RECV_ABORT	FRM7_CRC_ ERR	FRM6_CRC_ ERR	FRM5_CRC_ ERR	FRM4_CRC_ ERR	FRM3_CRC_ ERR	FRM2_CRC_ ERR	FRM1_CRC_ ERR
Default	х	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Name	Function
7	RECV_ABORT	Receive Abort 0 = Receive abort has not occurred
		1 = Receive abort has occurred
6	FRM7_CRC_ERR	Frame #7 CRC Error Detect 0 = No CRC error detected in frame #7
		1 = CRC error detected in frame #7
5	FRM6_CRC_ERR	Frame #6 CRC Error Detect 0 = No CRC error detected in frame #6
		1 = CRC error detected in frame #6
4	FRM5_CRC_ERR	Frame #5 CRC Error Detect 0 = No CRC error detected in frame #5
		1 = CRC error detected in frame #5
3	FRM4_CRC_ERR	Frame #4 CRC Error Detect 0 = No CRC error detected in frame #4
		1 = CRC error detected in frame #4
2	FRM3_CRC_ERR	Frame #3 CRC Error Detect 0 = No CRC error detected in frame #3
		1 = CRC error detected in frame #3
1	FRM2_CRC_ERR	Frame #2 CRC Error Detect 0 = No CRC error detected in frame #2
		1 = CRC error detected in frame #2
0	FRM1_CRC_ERR	Frame #1 CRC Error Detect 0 = No CRC error detected in frame #1
		1 = CRC error detected in frame #1

Programming Notes

Bits 7–0: These bits are cleared by writing data of arbitrary value to this index register.

IrDA Own Address Register

I/O Address 022h/023h Index EDh



IrDA Frame Length Register A

I/O Address 022h/023h Index EEh



IrDA Frame Length Register B

I/O Address 022h/023h Index EFh



PC Card Extended Features Register

	7		6	5		4	3	2	1	0	
Bit			MEM_WIN_	SEL[3-	-0]		Reserved		FORCE_CD_B	FORCE_CD_A	
Default	0		0	0		0	х	х	0	0	
R/W			R/V	V					R/W	R/W	
	Bit 7–4	Na ME	me :M_WIN_SEL[3	3–0]	Func PC C Thes	tion ard Memory e bits have no	Window Sele effect in PC C	ct Card Enhance	d mode (i.e., v	when 10 PC	
					In Sta Wind resou be re show	memory wind andard mode, ows 0–4 from urce sharing b directed to Sc n in the table	ows are enab six total PC C Socket A, and etween the so icket B using t below.	ied). ard memory d Window 0 fi ckets, Windo [,] his bit field.T	windows are a om Socket B. ws 1–4 from S he socket map	available: To support ocket A can opings are	
	3–2	3–2 Reserved			Reserved During read/modify/write operations, software must preserve these bits.						
	1	FO	RCE_CD_B		Sock This I follow Chan	tet B Force C bit is reset to 0 ving effect on lige Register:	ard Detect Ev) when this rea the CD_CHNO	/ent gister is read. G bit in the So	Writing to this ocket B Card S	s bit has the Status	
					0 = N	o effect (i.e., o	current state is	s unaffected)			
					1 = S R R	et the FORCE egister and th egister to 1	E_CD_B bit in e CD_CHNG	the PC Card bit in the Socl	Extended Fea ket B Card Sta	itures tus Change	
					The (asynd when Chan gene	CD_CHNG bit chronously by CD_CHNG is ge Register, a rated due to th	in the Socket writing to the cleared after another card s ne fact that the	B Card Statu FORCE_CD reading the status change FORCE_CE	IS Change Re _B bit. This mo Socket B Carc interrupt will I D_B bit is still s	gister is set eans that I Status not be set.	
	0	FO	RCE_CD_A		Sock This I follow Chan	et A Force C bit is reset to (ving effect on ge Register:	ard Detect Ev) when this reg the CD_CHNO	/ent gister is read. G bit in the So	Writing to this ocket A Card S	s bit has the Status	
					0 = N	o effect (i.e., o	current state is	s unaffected)			
					1 = S R R	et the FORCE egister and th egister to 1	E_CD_A bit in e CD_CHNG	the PC Card bit in the Socl	Extended Fea ket A Card Sta	itures tus Change	
					The (asynd when Chan gene	CD_CHNG bit chronously by CD_CHNG is ge Register, a rated due to th	in the Socket writing to the s cleared after another card s he fact that the	A Card Statu FORCE_CD reading the tatus change FORCE_CE	A bit. This me A bit. This me Socket A Carc interrupt will i D_A bit is still s	gister is set eans that I Status not be set.	

Index F0h MEM_WIN_SEL	Socket A Men 1–4 Socket	nory Windows Mappings	Index F0h MEM_WIN_SEL	Socket A Memory Windows 1–4 Socket Mappings		
[3-0]	Socket A		[3=0]	Socket A	Socket B	
0000 (0h)	1,2,3,4	None	1000 (8h)	1,2,3	4	
0001 (1h)	2,3,4	1	1001 (9h)	2,3	1,4	
0010 (2h)	1,3,4	2	1010 (Ah)	1,3	2,4	

Index F0h MEM_WIN_SEL	Socket A Men 1–4 Socket	nory Windows t Mappings	Index F0h MEM_WIN_SEL	Socket A Memory Windows 1–4 Socket Mappings		
[3–0]	Socket A	Socket B	[3-0]	Socket A	Socket B	
0011 (3h)	3,4	1,2	1011 (Bh)	3	1,2,4	
0100 (4h)	1,2,4	3	1100 (Ch)	1,2	3,4	
0101 (5h)	2,4	1,3	1101 (Dh)	2	1,3,4	
0110 (6h)	1,4	2,3	1110 (Eh)	1	2,3,4	
0111 (7h)	4	1,2,3	1111 (Fh)	None	1,2,3,4	

PC Card Mode and DMA Control Register

I/O Address 22/23h Index F1h

	7	6	5	4	3	2	1	0			
Bit	DN	1A_EN_B[1–0]	DMA_E	DMA_EN_A[1-0]		Reserved		MODE			
Default	0	0	0	0	Х	Х	0	0			
R/W		R/W	R	/W			R/W	R/W			
	Bit Name 7–6 DMA_EN_B[1–0])] Fu)] So Th en Ba Co by 0 (0 - 1 (Function Socket B DMA Enable These bits enable and disable DMA mode for Socket B. When enabled, these bits also determine which pin is used at the DMA Request signal to forward to the DRQs via the PC CARD Controller Data Request Signal (Socket B). The actual DRQ that the PC CARD Controller Data Request Signal (Socket B) is mapped to is controlled by the DMA controller block. 0 0 = DMA disabled 0 1 = DMA disabled 1 0 = WP_B/IOS16_B is DMA request							
			1 '	1 1 = BVD2_B/SPKR_B is DMA request							
			Th me	e MODE bit m eaning.	lust be set (En	hanced mode	e) for bits 7–6	to have any			
	5–4	DMA_EN_A[1–(0] So Th en Re Da Co by	ocket A DMA I lesse bits enabl abled, these b equest signal to ata Request Si ontroller Data F the DMA cont	Enable e and disable its also deterr o forward to th gnal (Socket / Request Signa troller block.	DMA mode fo nine which pir ne DRQs via to A). The actual Il (Socket A) is	or Socket A. V n is used at th he PC CARD DRQ that the s mapped to is	Vhen e DMA Controller PC CARD s controlled			
			0 () = DMA Disat	bled						
			0 '	1 = DMA Disat	bled						
			1 ($O = WP_A/IOS$	16_A is DMA	Request					
			1 '	$1 = BVD2_A/S$	PKR_A is DM	A Request					
			Th me	e MODE bit m eaning.	lust be set (En	hanced mode	e) for bits 5–4	to have any			
	3–2	Reserved	Re Du bit	eserved uring read/moc s.	lify/write opera	ations, softwa	re must prese	rve these			

Bit	Name	Function
1	CLK_SEL	Clock Select Selects the clock speed at which the PC Card controller runs. See PC Card Timing Control Registers for details on the effects this bit has on PC Card cycles.
		0 = Nominal 8 MHz ISA bus clock When the CPU clock is ≥ 8 Mhz, the PC Card controller will run at 8 MHz. When the CPU clock is < 8 Mhz, the PC Card controller will run at the CPU clock rate.
		1 = Nominal 33 MHz local bus clock (can be reduced under PMU control)
0	MODE	PC Card Controller Mode Selects the PC Card controller operating mode.
		0 = Standard mode In this mode, only six of the memory windows are available for PC Cards (two are dedicated and four are floating), the CLK_SEL bit has no meaning (only nominal 8 MHz ISA bus clock is available), and all DMA features are disabled.
		1 = Enhanced mode In this mode, all ten memory windows are available for PC Cards, the CLK_SEL bit can be used to select a high speed operating mode, and the DMA features are enabled.

PC Card Socket A/B Input Pull-up Control Register

I/O Address 22h/23h Index F2h



Programming Notes

The termination state that is specified using bits 1–0 is not actually felt at the pins until the Pin Termination Latch Command bit at CSC index E5h[0] is set.

ÉlanSC400 Microcontroller Revision ID Register

I/O Address 22h/23h Index FFh



Programming Notes

The value read back depends on the current major.minor versions of a specific ÉlanSC400 microcontroller.



RTC AND CMOS RAM INDEXED REGISTERS

4.1 **OVERVIEW**

The registers described in this chapter function as the configuration, setup, and status for the Real-Time Clock (RTC), as well as user-configurable RAM locations. They are listed in hexadecimal order by function in Table 4-1.

- RTC indexed registers 00–09h contain RTC seconds, minutes, hours, day of week, day of month, months of year, and year status, as well as second, minute, and hour alarm configuration controls. Binary and BCD formats for these registers are listed in a single table on page 4-5.
- Detailed register descriptions are included for the RTC indexed registers 0A–0Dh, which are used to configure the RTC.
- All index values from 0E–7Fh can be used as read/write RAM locations.

The 114 general-purpose RAM bytes are not dedicated within the RTC. They can be used by system or application level software and are fully available during the RTC update cycle. The 114 user RAM bytes provide low-power CMOS battery-backed storage and additional RAM.

RAM locations of the RTC are accessed using a two-step process.

- Identify a RAM location to be accessed by writing the RAM index to I/O port 70h, the RTC/CMOS RAM index register. The address must be in the range of 0E–7Fh.
- After writing the RTC/CMOS RAM Address Port, read the contents of the indexed CMOS RAM location from the RTC/CMOS RAM Data Port, port 71h, or by writing the desired data byte to this port.

The RTC registers are always accessed with ISA bus timings.

Table 4-1 RTC and CMOS RAM Register Map

Register Name	I/O (Port) Address	Index	Page Number
RTC/CMOS RAM Index Register	0070h		page 4-3
RTC/CMOS RAM Data Port	0071h		page 4-4
Time, Calendar, and Alarm Group		00–09h	page 4-5
RTC Current Second Register		00h	page 4-5
RTC Alarm Second Register		01h	page 4-6
RTC Current Minute Register		02h	page 4-7
RTC Alarm Minute Register		03h	page 4-8
RTC Current Hour Register		04h	page 4-9
RTC Alarm Hour Register		05h	page 4-10

Register Name	I/O (Port) Address	Index	Page Number
RTC Current Day of Week Register		06h	page 4-10
RTC Current Day of Month Register		07h	page 4-11
RTC Current Month Register		08h	page 4-12
RTC Current Year Register		09h	page 4-13
RTC Configuration Group		0A–0Dh	
Register A		0Ah	page 4-16
Register B		0Bh	page 4-18
Register C		0Ch	page 4-19
Register D		0Dh	page 4-20
CMOS RAM		0E–7Fh	

4.2 **REGISTER DESCRIPTIONS**

Each RTC and CMOS RAM indexed register is described on the following pages. Additional information about using these registers to program the ÉlanSC400 microcontroller can be found in the *ÉlanSC400 User's Manual* (order #21030).

RTC/CMOS RAM Index Register

I/O Address 0070h



Programming Notes

Bit 7 of this register is the master NMI gate control in a typical PC/AT Compatible system. For various reason, this bit has been made to reside at CSC index 9Dh[2] on the ÉlanSC400 microcontroller. Compatibility issues are minimized since the ÉlanSC400 microcontroller does not support generation of either of the legacy NMI sources (channel check or parity error).

RTC/CMOS RAM Data Port



RTC Current Second Register

I/O Address 70h/71h Index 00h

	7	6	5	4	3	2	1	0
r i	'	0	5	-	5	L	I	0
Bit				RTC_SI	ECOND			
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit 7–0	Name RTC_SECOND	Functio RTC Cu Software register seconds	n rrent Second e may initialize in either binar component o	Initialization the seconds y or BCD (Bin f the RTC tim	and Readba value for the F ary Coded De e may be read	Ick Register RTC by writing ecimal) format d from this reg	data to this s. The jister. The

Programming Notes

RTC Alarm Second Register

	7	6	5	4	3	2	1	0
Bit				RTC_ALARI	M_SECOND			
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit M 7–0 F	lame RTC_ALARM_S	ECOND	Function RTC Alarm So Software may writing data to Decimal) form may be read fr to this register card. For exar registers to CC once per seco once per seco once per seco once not occur unle cards. The RT occurred. Valio	econd Initiali initialize the a this register in this regist makes the se nple, setting th h will cause a nd. The wild c ss the hours a C logic checks d values for th	zation and Re larm seconds n either binary seconds cor er. Writing an econds compo ne hours, min an RTC alarm and minutes a sonce per sec is register ran	eadback Reg value for the or BCD (Bina nponent of the y value from 0 onent of the ala utes, and seco event to be g ce-per-second larm settings cond to see if a ge from 0 to 55	ister RTC by ary Coded ⇒ RTC time COH to FFH arm a wild onds alarm enerated d alarm will are also wild an alarm has 9 and all wild

card values.

Programming Notes

See the SET bit (RTC index 0BH[7]), the DM bit (RTC index 0BH[2]), and the RTC alarm IRQ status and control bits in RTC index 0CH for further information that is pertinent to programming this register.

RTC Current Minute Register

I/O Address 70h/71h Index 02h

	-	2	-		•	•		•
	/	6	5	4	3	2	1	0
Bit				RTC_M	IINUTE			
ılt	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Programming Notes

RTC Alarm Minute Register

				•	5	6	7	
			M_MINUTE	RTC_ALAR				Bit
0	0	0	0	0	0	0	0	Default
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
_	0 R/W	Default R/W						

Bit	Name	Function
7–0	RTC_ALARM_MINUTE	RTC Alarm Minute Initialization and Readback Register Software may initialize the alarm minutes value for the RTC by writing data to this register in either binary or BCD (Binary Coded Decimal) formats. The alarm minutes component of the RTC time may be read from this register. Writing a value of COH-FFH to this register makes the minutes component of the alarm a wild card. For example, setting the hours and minutes alarm registers to COH will cause an RTC alarm event to be generated once per minute. The wild card based once-per-minute alarm will not occur unless the hours alarm setting is also a wild card. The RTC logic checks once per second to see if an alarm has occurred. Valid values for this register range from 0 to 59 and all wild card values.

Programming Notes

See the SET bit (RTC index 0BH[7]), the DM bit (RTC index 0BH[2]), and the RTC alarm IRQ status and control bits in RTC index 0CH for further information that is pertinent to programming this register.

RTC Current Hour Register

I/O Address 70h/71h Index 04h

	7	6	5	4	3	2	1	0
Bit				RTC_	HOUR			
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
					•	•		
		m 0	Function					

BIt	Name	Function
7–0	RTC_HOUR	RTC Current Hour Initialization and Readback Register Software may initialize the hours value for the RTC by writing data to this register in either binary or BCD (Binary Coded Decimal) formats. The hours component of the RTC time may be read from this register. The RTC logic updates this register once per second.
		If the 24/12 bit (see RTC index 0BH[1])is cleared, bit 7 of this register indicates whether the current hour is AM or PM. If the high order bit is set, the current hour is PM. If the high order bit is cleared, the current hour is AM. In 24 hour mode, valid values for this register range from 0 to 23. In 12 hour mode, valid values for this register range from 1 to 12.

Programming Notes

See the SET bit (RTC index 0BH[7]), the DM bit (RTC index 0BH[2]) and the 24/12 bit (RTC index 0BH[1]) for further information that is pertinent to programming this register.

RTC Alarm Hour Register

	7	6	5	4	3	2	1	0
Bit				RTC_ALA	RM_HOUR			
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit 7–0	Name RTC_ALARM_H	Function HOUR RTC Softw to thi The a regis comp alarm once alarm	etion Alarm Hour vare may initia s register in e alarm hours o ter. Writing a ponent of the n register to C per hour. The has occurre 24/12 bit (se	Initialization a alize the alarm omponent of t value of COH- alarm a wild ca COH will cause e RTC logic ch d.	and Readbac hour value fo BCD (Binary he RTC time i FFH to this re ard. For exam an RTC alarn hecks once pe	k Register for the RTC by Coded Decim may be read f gister makes ple setting the n event to be g resecond to se ared bit Z of the	writing data hal) formats. rom this the hours e hours generated ee if an
			indica the a AM. I and a range writte	ates whether larm hour is f ln 24 hour mo all wild card v e from 1 to 12 en with a wild	the alarm hour PM. If the high ode, valid value alues. In 12 ho and all wild c card when 12	is AM or PM. order bit is cleased of the set of this regour mode, valiand values. Note that the set of the set	If the high orc eared, the ala ister range fro d values for th ote that if this selected, the A	ler bit is set, rm hour is m 0 to 23 his register register is

Programming Notes

See the SET bit (RTC index 0BH[7]), the DM bit (RTC index 0BH[2]), the 24/12 bit (RTC index 0BH[1]), and the RTC alarm IRQ status and control bits in RTC index 0CH for further information that is pertinent to programming this register.

a don't care since an alarm will occur every hour regardless.

RTC Current Day of the Week Register

I/O Address 70h/71h Index 06h

	7		6	5	4	3	2	1	0
Bit					RTC	_DAY			
Default	0		0	0	0	0	0	0	0
R/W	R/W	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit	Nar	me	Functio	n				
	7–0	RT	C_DAY	RTC Cu Valid val	rrent Day of ues for this re	t he Week egister range i	from 1 to 7 wh	iere:	
				1 = Suno	day				
				2 = Mon	day				
				3 = Tues	sday				
				4 = Wed	nesday				
				5 = Thur	sday				
				6 = frida	у				
				7 = Satu	rday				

Programming Notes

RTC Current Day of the Month Register

I/O Address 70h/71h Index 07h

	7	6	5	4	3	2	1	0
Bit				RTC_M	MONTH			
efault	0	0	0	0	0	0	0	0
र/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/V
•					·			
	Bit	Name	Functio	'n				

Programming Notes

RTC Current Month Register

I/O Address 70h/71h Index 08h

	7		6	5	4	3	2	1	0
Bit					RTC_N	MONTH			
Default	0		0	0	0	0	0	0	0
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit	Nar	ne	Functio	n				
	7–0	RT	C_MONTH	RTC Cu Valid va	rrent Month lues for this re	egister range fr	rom 1 to 12 w	here:	
				1 = Janu	uary				
				2 = Febr	ruary				
				3 = Mare	ch				
				4 = Apri	l				
				5 = May					
				6 = June	e				
				7 = July					
				8 = Aug	ust				
				9 = Sept	tember				
				10 = Oc	tober				
				11 = No	vember				

12 = December

Programming Notes

RTC Current Year Register

	7	6	5	4	3	2	1	0
Bit				RTC_	YEAR			
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit	Name	Functio	'n				

Programming Notes

General Purpose CMOS RAM (114 bytes)

I/O Address 70h/71h Indexes 0E-7Fh

	7	6	5	4	3	2	1	0		
Bit	RTC_CMOS_REG_X									
Default	х	x	х	х	х	х	х	х		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Bit 7–0	Name RTC_CMOS_RE	EG_X Gene for U There PC/A syste store BIOS	etion eral Purpose, se by Syster e are 114 byte T-compatible m BIOS. The d in a given C o vendors or e	Battery-Back n Firmware, A es of CMOS R system many number of by: MOS RAM by ven between of S RAM location	ked (Nonvola Applications, AM available of these byte tes used, and te location ma different version	tile) Storage etc. to the system s can be used the meaning ay vary betwe ons of a single	Location . In a d by the of data en different en BIOS.		

Accesses to CMOS RAM locations can be performed without any regard for RTC operations. For example, DM bit (RTC index 0BH[2]) has no effect on CMOS RAM data. If CSC index D0H[0] (RTC_DIS) is set, the CMOS RAM will be unavailable, but not lost (unless both main and backup power to the RTC core is removed). Re-enabling the RTC IO decode via the RTC_DIS bit will allow access to the CMOS RAM with its contents intact.

Register A

I/O Address 70h/71h Index 0Ah

	7	6	5	4	3	2	1	0
Bit	UIP		DV2–DV0		RS3–RS0			
Default	0	0	0	0	0	0	0	0
R/W	R	R/W			R/W			

Bit	Name	Function
7	UIP	Update in Progress This bit is provided for use by software that needs to modify the time, calendar or alarm registers in the real time clock. When this bit reads back '1b', these internal registers are unavailable for access by software since internal RTC logic is using them. When this bit reads back '0b', software will have a guaranteed minimum window of 244 μ s in which modifications to these registers are allowed. Setting RTC index 0BH[7] inhibits RTC register update cycles and clears the UIP status bit.
		The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is 0, it is not in transition. The UIP bit is a read- only bit and is not affected by reset. Writing the Set bit in Register B to a 1 inhibits any update cycle and then clears the UIP status bit.
6–4	DV2-DV0	Internal Oscillator Control Bits 0 1 0 = Turn the oscillator on, use an internal time base of 32768 Hz, and enable the countdown chain to run at the internal time base frequency. This is the normal operational setting for DV2-DV0.
		1 1 X = This value turns the oscillator on, but holds the count down chain in reset. In this mode, the time and date update cycles do not occur. This mode is useful for precision setting of the clock. If entering this mode from the "oscillator off" mode, a 200 millisecond delay must be observed to allow for oscillator stabilization prior to attempting to set the time. Time and date update cycles begin 500 milliseconds after the count down chain reset is removed.
		All other values = Programming DV2-DV0 to any value except '010b' or '11Xb' turns the oscillator off. In this mode, time and date update cycles do not occur, but the real time clock draws slightly less power.
		Upon exiting this mode, a 200 millisecond delay should be observed before reconfiguring or using the time and date information to allow for oscillator stabilization. These three bits are not affected by a reset of the RTC subsystem.
		The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program can start the divider at the

The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program can start the divider at the precise time stored in the RAM. When the divider reset is removed, the first update cycle begins 500 ms later. These three read/write bits are not affected by RTCRST.

Bit	Name	Function				
3–0	RS3-RS0	Rate Selection On a discrete RTC implementation the square wave output and period microcontroller, the square wave of the periodic interrupt output of the available for use. RS3–RS0 contro may be driven to IRQ8 as follows:	n, these bits control the rate selection for dic interrupt features. On the ÉlanSC400 butput feature is not available. However, RTC is internally tied to IRQ8 and is of the rate at which periodic interrupts			
		0 0 0 0 = Periodic interrupt disabled 1 0 0 0 = 3.906 milliseconds				
		0 0 0 1 = 3.906 milliseconds	1 0 0 1 = 7.812 milliseconds			
		0 0 1 0 = 7.812 milliseconds	1 0 1 0 = 15.625 milliseconds			
		0 0 1 1 = 122.070 microseconds	1 0 1 1 = 31.250 milliseconds			
		0 1 0 0 = 244.141 microseconds	1 1 0 0 = 62.500 milliseconds			
		0 1 0 1 = 488.281 microseconds	1 1 0 1 = 125.000 milliseconds			
		0 1 1 0 = 976.563 microseconds	1 1 1 0 = 250.000 milliseconds			
		0 1 1 1 = 1.953 milliseconds	1 1 1 1 = 500.000 milliseconds			

Register B

I/O Address 70h/71h Index 0Bh

0

DSE

1

24/12

Bit Default R/W

7

SET

6

PIE

5

AIE

4

UIE

3

SQWE

2

DM

х			0	0	0	0	х	х	х				
R/W		R	/W	R/W	R/W	R/W	R/W	R/W	R/W				
Bit	Na	mo	Fund	tion									
7	Nai	T	Set E);(())));4									
7	SE	I	Wher occur cycle allow an up subsy 0BH[Set Bit When the SET bit is written to '0b', time and date update cycles are enabled, and will occur one-per-second. When the SET bit is written to a '1b', time and date update cycles are disabled, and any update in progress is aborted. This feature is useful for allowing time and date registers to be updated by software without being disturbed by an update cycle occurring while initializing. Neither internal functions nor RTC subsystem resets affect this bit. SET should be written to '1b' while updating index 0BH[2–0], and cleared afterward.									
6	PIE	<u>.</u>	Periodic Interrupt Enable When this bit is set, the internal RTC periodic interrupt signal will latch the IRQF to '1b' (see RTC index 0CH[7]) upon a PF status bit transition from '0b' to '1b' (see RTC index 0CH[6]). If the PF status bit = '1b' when the PIE bit is set by software, IRQF will be asserted immediately. When this bit is cleared, no RTC periodic intervent is possible. PIE is not modified by any internal RTC functions, but is reset RTC index 0CH[6] for latched status of RTC index 0CH[6] for latched status of RTC index 0CH[6].										
5	AIE		Alarr Wher '1b' (: RTC IRQF event RTC RTC interr	Alarm Interrupt Enable When this bit is set, the internal RTC alarm interrupt signal will latch the IRQF flag to '1b' (see RTC index 0CH[7]) upon an AF status bit transition from '0b' to '1b' (see RTC index 0CH[5]). If the AF status bit = '1b' when the AIE bit is set by software, IRQF will be asserted immediately. When this bit is cleared, no RTC alarm interrupt event is possible. AIE is not modified by any internal RTC functions, but is reset by a RTC subsystem reset. Use RTC indexes 01H, 03H, and 05H to configure when an RTC alarm interrupt will occur, and RTC index 0CH[5] for latched status of RTC alarm									
4	UIE	Ξ	Upda Wher flag to (see IRQF interr reset	ate-Ended Int n this bit is set o '1b' (see RT RTC index 0C will be assert upt event is po by either an F	errupt Enable , the internal F C index 0CH[H[4]). If the U ted immediate ossible. UIE is RTC subsyste	e RTC update er 7]) upon a UF F status bit = ' ly. When this not modified m reset, or by	nded interrupt status bit trai 1b' when the bit is cleared, by any intern writing the Sl	signal will late nsition from '0 UIE bit is set t no RTC upda al RTC functio ET bit to '1b'.	ch the IRQF b' to '1b' by software, ite ended bns, but is				
3	SQ	WE	Squa This I	are-Wave Ena bit has not bee	i ble en implemente	ed on the Élar	SC400 micro	controller.					
2	DM		Data The c binar this b forma after	Data Mode The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. Neither internal functions nor RTC subsystem resets affect this bit. When DM = '0', time and calendar data use BCD (binary coded Decimal) format. When DM = '1b', binary format is used. RTC indexes 0–9 must be re-initialized after changing this bit.									
1	24/	12	24 He Wher repre hour index	our Mode Sel this bit = '0b' sents PM whe format. Neithe kes 4 and 5 m	ect Bit ', hours data u en '1b', and Al er internal fund ust be re-initia	uses 12-hour f M when '0b'. V ctions nor RTC Ilized after cha	ormat, and the When this bit = C subsystem r anging this bit	e MSB of the - '1b', hours d resets affect th	hours bytes ata uses 24 his bit. RTC				
0	DS	E	Dayli Settir next additi 1:00: interr	ight Savings ng this bit enab time reading a ion, the next ti 00 AM. These nal functions n	Enable bles two speci fter 1:59:59 A me reading at special upda or RTC subsy	al time update M on the last fter 1:59:59 or tes do not occ /stem resets a	es to automation Sunday in Ap In the last Sund Cur when the I Suffect this bit.	cally occur. W ril will be 3:00 day in Octobe DSE bit = '0b'.	hen set, the 1:00 AM. In r will be Neither				

Register C

I/O Address 70h/71h Index 0Ch

	7	6	5	4	3	2	1	0				
Bit	IRQF	PF	AF	UF		Reserved						
Default	х	х	x	х	0	0	0	0				
R/W	R	R	R	R			R					
	Bit N	ame	Functio	n (D								
	7 IRQF		When th microcol will gene = '0b', th inactive. PF, AF, enable(s RTC inte was alre by an R	Interrupt Request Flag When this bit transitions from '0b' to '1b', the IRQ8 input of the ÉlanSC400 microcontroller Prioritized Interrupt Controller (PIC) is driven active which will generate a CPU interrupt if IRQ8 is unmasked at the PIC. When this bit = '0b', the IRQ8 input of the ÉlanSC400 microcontroller's PIC will be driven inactive. The IRQF bit will be latched to a '1b' when any one (or more) of PF, AF, or UF flags transition from '0b' to '1b' while its/their respective enable(s) are also asserted. The IRQF bit will also be latched to a '1b' if an RTC interrupt source enable is written to '1b' when its associated flag bit was already asserted. RTC index 0CH is read/reset, and will also be reset by an RTC subsystem reset.								
			If the Ela disabled IRQF sta intent is signal, th masked 71h I/O	If the ElanSC400 microcontroller's internal RTC I/O address decode is disabled via CSC index D0H[0], the internal signal associated with the IRQF status bit will not automatically be disconnected from the PIC. If the intent is to use an external RTC to drive IRQ8 from an external PIRQ signal, then all internal RTC interrupt sources (PIE, AIE, UIE) must be masked off at the internal RTC prior to disabling the internal RTC port 70h/ 71h I/O decode via CSC index D0H[0].								
	6 P	F	Periodic This bit i the state occur at reset, ar	Periodic Interrupt Flag This bit is set when an RTC periodic interrupt event occurs regardless of the state of its individual enable (the PIE bit). Periodic interrupt events will occur at a rate that is configured via RTC index 0AH[3:0]. This bit is read/ reset, and will also be reset by an RTC subsystem reset.								
	5 AF		Alarm Ir This bit i state of i a time re time (as (as confi wildcard COH to F subsyste	Alarm Interrupt Flag This bit is set when an RTC alarm interrupt event occurs regardless of the state of its individual enable (the AIE bit). Alarm events can only occur with a time resolution of 1 second. An alarm event will occur when the current time (as defined by RTC indexes 0, 2, and 4) is equal to the alarm setting (as configured via RTC indexes 1, 3, and 5). The alarm time can contain wildcards for hour, minute, or second settings. A wild card is any value from COH to FFH. This bit is read/reset, and will also be reset by an RTC subsystem reset.								
	4 U	F	Update- This bit i read/res	Update-Ended Interrupt Flag This bit is set upon termination of each time/date update cycle. This bit is read/reset, and will also be reset by an RTC subsystem reset.								
	3–0 R	eserved	Reserve These b	ed its are reserve	ed. Each of the	em always rea	ads back as '0	b'.				

I/O Address 70h/71h Index 0Dh



Programming Notes

The default value for this register (index 0Dh) refers to the RTC-only reset. The RTC-only reset may or may not occur when a master power-on reset occurs.

Register D
GRAPHICS CONTROLLER INDEXED REGISTERS

5.1 **OVERVIEW**

The registers described in this chapter function as configuration, setup, and status for the LCD graphics controller. They are listed in hexadecimal order by function in Table 5-2.

Graphics controller registers are indexed using I/O ports 3D4h (index) and 3D5h (data) for Color Graphics Adapter (CGA) mode and I/O ports 3B4h (index) and 3B5h (data) for Monochrome Display Adapter (MDA) mode. Different ports are used, depending on the graphics mode selected. The mode is selected using bit 0 of the Internal Graphics Control Register A (CSC index DDh).

- When MDA mode is selected, the MDA index and data registers are located at 3B4h and 3B5h, respectively, in the I/O address space.
- When CGA mode is selected, the CGA index and data registers are located at 3D4h and 3D5h, respectively, in the I/O address space.

The graphics controller indexed registers are accessed using a two-step process:

- An I/O write to the I/O address port for the chosen mode is performed. The data written is the index of the requested graphics controller register.
- This I/O write is followed by an I/O read or write to the data port for the chosen mode. This access causes the graphics controller to allow access to the addressed configuration register.

The graphics controller indexed registers are typically accessed at CPU speeds.

Table 5-2 Graphics Controller Register Map

Register Name	I/O (Port) Address	Index	Page Number
CGA/MDA Index	03x4h		page 5-4
CGA/MDA Data	03x5h		page 5-5
CGA/MDA Mode	03x8h		
Palette	03D9h		
Status	03xAh		
Clear LPS	03DBh		
Set LPS	03DCh		
HGA Configuration	03BFh		
Legacy CGA/MDA Group		0A–11h	
Cursor Start Register		0Ah	page 5-6
Cursor Stop Register		0Bh	page 5-7
Start Address High Register		0Ch	page 5-8

Register Name	I/O (Port) Address	Index	Page Number
Start Address Low Register		0Dh	page 5-9
Cursor Address High Register		0Eh	page 5-10
Cursor Address Low Register		0Fh	page 5-11
Light Pen High Register		10h	page 5-12
Light Pen Low Register		11h	page 5-13
Extended Group		30–52h	
Horizontal Total Register		30h	page 5-14
Horizontal Display End Register		31h	page 5-15
Horizontal Line Pulse Start Register		32h	page 5-16
Horizontal Border End Register		33h	page 5-17
Non-Display Lines Register		34h	page 5-18
Vertical Adjust Register		35h	page 5-19
Overflow Register		36h	page 5-20
Vertical Display End Register		37h	page 5-21
Vertical Border End Register		38h	page 5-22
Frame Sync Delay Register		39h	page 5-23
Reserved		3Ah	
Dual Scan Row Adjust Register		3Bh	page 5-24
Dual Scan Offset Address High Register		3Ch	page 5-25
Dual Scan Offset Address Low Register		3Dh	page 5-26
Offset Register		3Eh	page 5-27
Underline Location Register		3Fh	page 5-28
Maximum Scan Line Register		40h	page 5-29
LCD Panel AC Modulation Clock Control Register		41h	page 5-30
Font Table Register		42h	page 5-31
Grayscale Mode Register		43h	page 5-32
Grayscale Remap Register 1		44h	page 5-34
Grayscale Remap Register 2		45h	page 5-34
Grayscale Remap Register 3		46h	page 5-34
Grayscale Remap Register 4		47h	page 5-34
Grayscale Remap Register 5		48h	page 5-34
Grayscale Remap Register 6		49h	page 5-34
Grayscale Remap Register 7		4Ah	page 5-34
Grayscale Remap Register 8		4Bh	page 5-34
Pixel Clock Control Register		4Ch	page 5-36
Frame Buffer Base Address High Byte		4Dh	page 5-37

Register Name	I/O (Port) Address	Index	Page Number
Font Buffer Base Address High Byte		4Eh	page 5-38
Frame/Font Buffer Base Address Low		4Fh	page 5-39
PMU Control Register 1		50h	page 5-40
PMU Control Register 2		51h	page 5-41
Extended Feature Control Register		52h	page 5-42

5.2 **REGISTER DESCRIPTIONS**

Each graphics controller index register is described on the following pages. Additional information about using these registers to program the ÉlanSC400 microcontroller can be found in the *ÉlanSC400 User's Manual* (order #21030).

CGA/MDA Index Register

I/O Address 03x4h



CGA/MDA Data Port

I/O Address 03x5h



Programming Notes

Graphics Controller Indexed Registers

Cursor Start Register

I/O Address 3x4h/3x5h Index 0Ah

	7		6	5	4	3	2	1	0			
Bit	Reserv	ved CUR_CON[1		ON[1–0]		0]						
Default	х		х	х	х	х	х	х	х			
R/W			R/	W	R/W							
	Bit	Nar	ne	Functio	n							
	/	Res	served	Reserve	Reserved							
	6–5	CUI	R_CON[1–0]	Cursor Controls	Cursor Control Register Controls the alphanumeric cursor according to the following table:							
				Bits	6–5 C	ursor Displa	y Mode					
				0	0 N	lormal blinkin	g cursor					
				0	1 N	lo cursor disp	lay					
				1	0 N	lo blinking, ha	alf intensity cu	rsor				
				1	1 N	lo blinking, fu	Il intensity cur	sor				
	4–0	CUI	R_START[4-	0] Cursor Start Register Defines the starting line of the alphanumeric cursor for bits 4–0. Compat with the 6845 definition.								

Cursor End Register

I/O Address 3x4h/3x5h Index 0Bh

	7	6	5	4	3	2	1	0
Bit		CUR_END[4-0]				Reserved		
Default	x	x	х	х	х	х	х	х
R/W						R/W		
	Bit 7–5 4–0	Name Reserved CUR_END[4–0]	Function Reserve Cursor I Defines definition	n ed End Register the last line o h	• Bits 4–0 f the alphanur	meric cursor. C	Compatible wi	th the 6845

Start Addre	ess Hi	gh Register				I/O Ad	ldress 3x Ir	x4h/3x5h 1dex 0Ch
	7	6	5	4	3	2	1	0
Bit				STRTAD	DR[15-8]			
Default	0	0	0	0	0	0	0	0
R/W				R	/W			
	Bit 7–0	Name STRTADDR[15–8	Functio Data St High-ord displaye with the 1bpp mo most sig is exten	on art Address F der bits of the ed at the top of 6845 definitio ode, the regist gnificant bit. In ded by two bit	Register Bits starting addre f the screen. In n (most signif ter is extender Linear Packe s, so that bit 7	15–8 ess that detern n CGA mode, icant bit is bit d by one bit, s d-Pixel 4 and 7 becomes the	mines the first this register is 5). In Linear P to that bit 6 be 2bpp modes, most signific	a data to be s compatible Packed-Pixel ecomes the the register cant bit.

I/O Address 3x4h/3x5h **Start Address Low Register** Index 0Dh 5 4 3 2 0 7 6 1 Bit STRTADDR[7-0] Default 0 0 0 0 0 0 0 0 R/W R/W Function Bit Name 7–0 STRTADDR[7-0] Data Start Address Register Bits 7-0 Low-order bits of the starting address that determines the first data to be displayed at the top of the screen. Compatible with the 6845 definition.

Cursor Address High Register

I/O Address 3x4h/3x5h Index 0Eh

	7		6	5	4	3	2	1	0
Bit		Reserv	red			CUR_AD	DR[13–8]		
Default	x		х	х	х	х	х	х	х
R/W						R/	W		
	Bit	Nam	e	Function					
	Bit 7–6	Nam Rese	e erved	Function Reserved	l				

I/O Address 3x4h/3x5h **Cursor Address Low Register** Index OFh 7 6 5 4 3 2 0 1 Bit CUR_ADDR[7-0] Default х х х х х х х х R/W R/W Function Bit Name 7–0 CUR_ADDR[7-0] Cursor Address Location Bits 7–0 Low-order bits of the address that determines the location of the alphanumeric cursor. Compatible with the 6845 definition.

Light Pen H	ligh R	I/O Ad	ldress 3 II	x4h/3x5h ndex 10h						
	7	6	5	4	3	2	1	0		
Bit		Reserved			LIGHTP	EN[13–8]	[13–8]			
Default	х	x	x	х	x	x	x	x		
R/W				R						
	Bit	Name	Functio	on						
	7–6	Reserved	Reserv	ed						
	5–0	LIGHTPEN[13-8]	Light P This rea address	en Location E ad-only registe s high register a	Bits 13–8 r reads back and is provide	as a mirror of ed for CGA so	the value in t	he Cursor atibility.		



Horizontal	Total	Register				I/O Ac	ldress 3 I	x4h/3x5h ndex 30h		
	7	6	5	4	3	2	1	0		
Bit	Reserv	ved			HTOTAL[6–0]					
Default	х	x	x	x	х	x	x	х		
R/W					R/W					
	Bit	Name	Functio	on						
	7	Reserved	Reserved Software should write this bit to 0.							
	6–0	HTOTAL[6–0]	 Horizontal Total Bits 6–0 The horizontal total minus 2. The horizontal total is the total number of character counts in a horizontal line, where a character is 8–16 pixels w Programming this register to a larger value than the Horizontal Display register allows the frame rate to be slowed. 							

Horizontal Display End Register

I/O Address 3x4h/3x5h Index 31h



Horizontal Line Pulse Start Register

I/O Address 3x4h/3x5h Index 32h



Horizontal Border End Register

I/O Address 3x4h/3x5h Index 33h



Non-display	y Line	es Register				I/O Ad	dress 3) Ir	x4h/3x5h 1dex 34h
	7	6	5	4	3	2	1	0
Bit			Rese	erved			NDIS	PADJ
Default	x	X	x	Х	x	x	X	x
	Bit 7–2 1–0	Name Reserved NDISPADJ	Function Reserve Software Non-dis These bi	n ed e should write play Adjust its allow 2 or if the vertical	this bit to 0. Bits 1–0 4 additional no	on-display line	es to be added	d to the
			displaye B (ÉlanS	d during these SC400 microc	e lines comes ontroller confi	from Internal (guration index	Graphics Con ced register D	trol Register Eh), bit 0.
			NDISPA NDISPA	.DJ1- N .DJ0: d	lumber of no lisplay lines a	n- added:		
			0	0	0			
			0	1	2			
			1	0	4			
			1	1	1			

Vertical Adjust Register



Overflow Register

	7		6	5	4	3	2	1	0	
Bit			Reserved		FLMMODE	Reserved	VBRDEND	VDEND	Reserved	
Default	х	x		х	x	х	х	х	х	
R/W					R/W		R/W	R/W		
	Bit	Nam	ie	Functio	n					
	7–5	Rese	erved	Reserve Software	ed e should write	this bit to 0.				
	4	FLM	MODE	FLM (Ve 0 = FLM 1 = FLM	ertical Sync) I will be assert will be assert	Mode ed at the end ed before the	of the first sca start of the fir	an line st scan line		
	3	Rese	erved	Reserve Softwar	ed re should wri	te this bit to	0.			
	2	VBR	DEND[8]	Vertical Border End Bit 8 This is the eighth bit of the Vertical Border End Register. See graphics index 38h for more detail.						
	1	VDE	ND[8]	Vertical Display Enable End Bit 8 This is the eighth bit of the Vertical Display Enable End Register. See graphics index 37h for more detail.						
	0	Rese	erved	Reserve Software	ed e should write	this bit to 0.				



Vertical Border End Register I/O Address 3x4h/3x5h Index 38h 7 5 4 3 2 0 6 1 Bit VBRDEND[7-0] Default х х х х х х х х R/W R/W Bit Function Name Vertical Border End Bits 7-0 7–0 VBRDEND[7-0] Determines the last character line to be output to the panel at the bottom of the display. Value = (number of horizontal displayed character lines) -1. If the Vertical Display End register is programmed to a lower value than this register, the scan lines numbered between Vertical Display End and this register will be sent to the panel with the programmed overscan values. VBRDEND8 is in the Overflow Register at graphics index 36h. Useful when the display mode selected does not use the entire screen area.

Frame Sync Delay Register I/O Address 3x4h/3x5h Index 39h 5 3 0 7 6 4 2 1 Bit Reserved FRMDLY[1-0] Default х х х х х х х х R/W R/W Bit Name Function 7–2 Reserved Reserved Software should write this bit to 0. **Frame Sync Delay Register Bits 1–0** Number of character clocks to delay Frame sync from beginning of horizontal line pulse. Delay = (value programmed * 4) + 1. FRMDLY[1-0] 1–0

Dual Scan Row Adjust Register

	7	6	5	4	3	2	1	0			
Bit		Reserved		DSUPRWAJ[5–0]							
Default	х	x	х	х	х	х	x	x			
R/W					R	/W					
	Bit	Name	Functio	n							
	7–6	Reserved	Reserve Software	ed e should write	this bit to 0.						
	5–0	DSUPRWAJ[5–	0] Dual-So When a display, the porti number scan line single-s	Dual-Scan Row Adjust Register Bits 5–0 When a character row overlaps the upper and lower screens in a dual-scan display, this register must be programmed with the number of scan lines in the portion of the character row which is within the lower screen. If the number of scan lines in a half-screen is an integer multiple of the number of scan lines in a character row, program this register to 0. Has no effect in single-scan mode.							

Dual Scan Offset Address High Register

I/O Address 3x4h/3x5h Index 3Ch



Dual Scan Offset Address Low Register

I/O Address 3x4h/3x5h Index 3Dh



Offset Register

I/O Address 3x4h/3x5h Index 3Eh



Underline Location Register

	7	6		5	4	3	2	1	
Bit		Reser	rved				ULINE[4-0]		
efault	x	x		х	х	х	x	х	
R/W							R/W		
	Bit 7–5	Name Reserved		Function Reserve	n				

Maximum Scan Line Register

I/O Address 3x4h/3x5h Index 40h

	7	6	5	4	3	2	1	(
Bit		Reserved				MAXSCAN[4–0]	
Default	x	x	x	х	х	x	х	
R/W						R/W		
	Bit 7–5	Name Reserved	Function	ı d				

LCD Panel AC Modulation Clock

I/O Address 3x4h/3x5h Index 41h



Font Table Register

I/O Address 3x4h/3x5h Index 42h

	7	6	5	4	3	2	1	0
Bit	FONTWRP	CHARV	/ID[1–0]	FONTOFF[4–0]				
Default	0	0	0	0	0	0	0	0
R/W	R/W	R	W	R/W				

Bit	Name	Function
7	FONTWRP	Font Table Write-protect 0 = Do not write-protect font table
		1 = Write-protect font table
6–5	CHARWID[1–0]	Character Width Select Character width in pixels is as follows: 0 0 = 8 pixel width 0 1 = 10 pixel width 1 0 = 16 pixel width
4–0	FONTOFF[4-0]	Font Plane Offset Bits 4–0 Sets the offset into the font table during display. Useful in displaying alternate font sets.

Graphics Controller Grayscale Mode Register

I/O Address 3x4h/3x5h Index 43h

	7		6	5	4	3	2	1	0				
Bit	BORDE	ĒR	COLORSTN	GRAYMAP MODE	GRAYCONT	SHAD4S	SEL[1-0]	GRAYMOD	GRYREMAP				
Default	0		0	0	0	0	0	0	0				
R/W	R/W		R/W	R/W	R/W	R/	W	R/W	R/W				
	Bit 7	Bit Name 7 BORDER		Functio Enable 0 = Bit 1 the b	Function Enable Color Border 0 = Bit 1 of Internal Graphics Control Register B (CSC index DEh) controls the border color in all modes.								
	6	00		1 = Bits and t Mode grap	3–0 of 3D9 wi flat-mapped p e Register 2 a hics modes.).	II be used to s acked-pixel m Iways controls	et the border nodes (bit 1 of s the border s	color in CGA Graphics Col hade in MDA	text modes ntroller and CGA				
	6		JLORSTN	0 = Mon 1 = Colo	ochrome pane or STN panel r	el mode node (must be	e single-scan	panel)					
	5	GRAYMAPMODE		E Graysca Should b 0 = Colo	Grayscale Mapping Mode Should be set only when bit 1 = 0. See also bit 4 of this register. 0 = Color mapping mode								
	4	GF	RAYCONT	Graysca	Grayscale Contrast Enhance								
				Used wh 0 = Norn In co selec non- chara	 0 = Normal contrast In color mapping mode (normal contrast), the R and G bits are used to select the output gray shade. In monochrome mapping mode, non-intensified characters are mapped to shades 0 and 3, intensified characters are mapped to shades 1 and 2. 								
					1 = Enhanced contrast In color mapping mode (enhanced contrast), enables 16x2 gray shade palette (bit 0 must also be set). The least significant two bits of each of the gray shades remapping registers can be used to map any of the four gray shades to each of the 16 possible IRGB values (see the table below). In monochrome mapping mode, intensified characters are mapped to shades 0 and 3, non-intensified characters are mapped to shades 0 and 2. This bit is ignored when bit 1 = 1.								
	3–2	2 SHAD4SEL[1–0]		Option Selects the Gray selected	Option 1 Shade Mode Select Bits 1–0 Selects between one of four 4-color shading modes used in option 1. See the Gray Shading section for a description. Ignored when option 2 is selected.								
	1	GF	RAYMOD	Graysca 0 = Optio 1 = Optio	Grayscale Mode 0 = Option 1 (4 shades) 1 = Option 2 (16 shades)								
	0 GRYREMAP		Graysca 0 = Disa 1 = Enal	Grayscale Remapping Enable 0 = Disable mapping registers 1 = Enable mapping registers									

Relationship of Horizontal/Vertical display and border signals to display output data								
Horizontal Display Enable	Horizontal Border	Vertical Display Enable	Vertical Border	Output Data				
1	0	1	0	Normal display data				
0	0	1	0	Overscan				
x	0	0	0	Overscan				
x	0	0	1	Non-display (Internal Graphics Control Register B, bit 0)				
0	1	х	х	No data output				

Graphics Controller Grayscale Remapping Register

I/O Address 3x4h/3x5h Index 44-4Bh



Programming Notes

The graphics controller supports 16 or four gray levels of CGA text mode shades. To allow contrast adjustment between various panels, a Color Mapping function is provided to allow software adjustment of the mapping of color to the gray level displayed by the LCD controller. This color mapping is controlled by the Color Mapping Register(s). This function is enabled by graphics index 43h[0]. There are eight color mapping registers, located at graphics indexes 44–4Bh. Each register contains two 4-bit nibbles, for a total of 16 nibbles. Each nibble controls the mapping of one of the 16 or four CGA gray levels; each gray level is defined by the 4-bit quantity: R, G, B, I. The mapping is shown in the chart below:

R	G	в	I	Register Index	Bit Field (16 Gray Shades)	Bit Field (4 Gray Shades)
0	0	0	0	44h	3–0	1–0
0	0	0	1	44h	7–4	5–4
0	0	1	0	45h	3–0	1–0
0	0	1	1	45h	7–4	5–4
0	1	0	0	46h	3–0	1–0
0	1	0	1	46h	7–4	5–4
0	1	1	0	47h	3–0	1–0
0	1	1	1	47h	7–4	5–4
1	0	0	0	48h	3–0	1–0
1	0	0	1	48h	7–4	5–4
1	0	1	0	49h	3–0	1–0
1	0	1	1	49h	7–4	5–4
1	1	0	0	4Ah	3–0	1–0
1	1	0	1	4Ah	7–4	5–4
1	1	1	0	4Bh	3–0	1–0
1	1	1	1	4Bh	7–4	5–4

CGA Example (16 gray-shades mode):

Write to Index Register 3D4:44h

Write to Data Register 3D5:EFh

CGA gray level RGBI (0000) will be displayed as gray level (1111)

CGA gray level RGBI (0001) will be displayed as gray level (1110)

CGA Example (4 gray-shades mode):

Write to Index Register 3D4:44h

Write to Data Register 3D5:23h

CGA gray level RGBI (0000) will be displayed as gray level (11)

CGA gray level RGBI (0001) will be displayed as gray level (10)

Pixel Clock Control Register

I/O Address 3x4h/3x5h Index 4Ch

	7		6	5	4	3	2	1	0
Bit		Reserved			CLOCKI	DIV[1–0]	PLLRATIO[2-0]		
Default	х		х	х	0	0	0	0	0
R/W					R/	W		R/W	
	Bit 7–5	Na i Re:	me served	Functio Reserve	n ed				
	4–3	CL	OCKDIV[1–0]	Dot Clo Divides generate in the tal	ck Divide Sel the base dot c the dot clock ble below.	ect lock (as contr rate that is us	olled by bits 2 sed by the gra	e-0 above) by phics controlle	1, 2, or 4 to er as shown
	2–0	2–0 PLLRATIO[2–0]		$\begin{array}{c} \textbf{Dot Clo}\\ 0 \ 0 \ 0 \ 0 \ 2 \\ 0 \ 0 \ 1 \ 2 \\ 0 \ 1 \ 0 \ 2 \\ 0 \ 1 \ 0 \ 2 \\ 1 \ 0 \ 1 \ 2 \\ 1 \ 0 \ 0 \ 2 \\ 1 \ 0 \ 1 \ 2 \\ 1 \ 0 \ 1 \ 2 \\ 1 \ 0 \ 1 \ 2 \\ 1 \ 0 \ 1 \ 2 \\ 1 \ 1 \ 0 \ 2 \\ 1 \ 1 \ 1 \ 2 \ 1 \ 1 \ 1 \ 2 \\ 1 \ 1 \ 1 \ 1 \ 2 \ 1 \ 1 \ 1 \ 1 \ 1 \$	Ck Base Freq 20.736 MHz 23.040 MHz 25.344 MHz 27.648 MHz 29.952 MHz 32.256 MHz 34.560 MHz 36.864 MHz its are used in pown as the pix	conjunction vel clock) rate	t vith bits 4–3 t as shown in t	o determine th he table belov	ie dot clock v.

	Dot Clock Frequency (MHz) Bits 4–3							
Bits 2–0	0 0:Divide by 4	0 1:Divide by 2	1 0:Divide by 1					
000	5.19	10.38	20.76					
0 0 1	5.77	11.53	23.06					
010	6.34	12.68	25.36					
011	6.92	13.84	27.68					
100	7.50	14.99	29.98					
101	8.07	16.14	32.28					
110	8.65	17.30	34.60					
111	9.23	18.45	36.90					
Frame Buffer Base Address I/O Address 3x4h/3x5h **Index 4Dh** 5 4 3 7 6 2 1 0 Bit FRMBUFWIN[23-16] 0 0 Default 0 0 0 0 0 0 R/W R/W Bit Name Function 7–0 FRMBUFWIN[23-16] Frame Buffer Window Base Address Bits 23–16 Sets the base address at which the frame buffer is visible within a 16 Mbytes shared memory address space (high order bits, see also graphics index 4Fh[1–0]).

Font Buffer Base Address High Byte

I/O Address 3x4h/3x5h Index 4Eh



Frame/Font Buffer Base Address Register Low

I/O Address 3x4h/3x5h Index 4Fh

	7		6	5	4	3	2	1	0	
Bit	VID_DR	AM	LCD_FRM_ BUF_WIN_ ENA	PAGES	SEL[1-0]	FONTWI	N[15–14]	FRMBUFV	VIN[15–14]	
Default	0		0	0	0	0	0	0	0	
R/W	R/W R/W		R	/W	R	/W	R/	W		
	Ri+	Na	mo	Funz	stion					
	7			l'und						
	1	VIL		0 = D	RAM is not al	located to the	graphics con	troller		
				1 = E m	nable address nemory size as	s spaces spec s DRAM alloc	cified by FRME ated to the gra	BUFWIN, FON aphics control	ITWIN, and ler	
	6	LC WI	D_FRM_BUF N_ENA	_ LCD 0 = G	Frame Buffe	r Window oller MMS wir	ndow is disable	ed		
			1 = Enable the 16 Kbytes graphics frame buffer MM fixed in system address space from 0B8000–0B						r MMS window which is 0–0BBFFFh	
				This confi conti block addru visibl	MMS window gured for text guous 16 Kby of system DF ess which is p le through the	not available mode. This w tes windows o RAM accessib rogrammed v window is sel	when the grap indow provide of system DRA le via this win ia index 4Dh[7 lected using b	bhics controlle s access to of AM only. The 6 dow starts at t 7–0]. The winc its 5–4 below.	er is ne of four 64 Kbytes the base low (C–F)	
	5–4	PA	GESEL[1-0]	Page Selec visibl	e Select Bits f ct one of four (le at address (1–0 contiguous 16)B8000–0BBF	Kbytes MMS FFFh. See bit	windows to b 6 of this regist	ecome ter.	
	3–2	FO	NTWIN[15–14	4] Font Sets Mbyt	Font Buffer Window Base Address Bits 15–14 Sets the base address at which the font buffer is visible within a 16 Mbytes shared memory address space (low order bits).					
	1–0	-0 FRMBUFWIN[15–14]		i–14] Fran Sets Mbyt regis is lar confi writte	the Buffer Win the base addr es shared me ter is set, thes ger than 16 Kl gured for a lin en to '0b'.	dow Base Ad ress at which mory address the two bits mu bytes (such as ear packed pi	ddress Bits 1 the frame buff space (low o st be written to s when the gra xel mode), bit	5–14 er is visible w rder bits). If bi o '00b'. If the f aphics controll 0 of this regis	ithin a 16 t 6 of this rame buffer ler is tter must be	

PMU Control Register 1

I/O Address 3x4h/3x5h Index 50h

	7		6	5	4	3	2	1	0		
Bit	LCDPWF	REN	PMUMODE	P\	WRUPDLY2[2-	0]	PWRUPDLY1[2-0]				
Default	0		0	0	0	0	0	0	0		
R/W	R/W R/W			R/W			R/W				
	Bit	Bit Name		Functio	n						
	7 LCDPWREN		LCD Sot 0 = Disal 5–0)	itware Power ole LCD powe	-up and Dow r and signals	/n (sequencing	time controlle	d by bits			
				1 = Enab	le LCD powe	and signals	(sequencing t	ime controlled	l by bits 5–0)		
				This bit, (see enab	This bit, when set, will be overridden by a PMU initiated disable of the LCD (see bit 6 of this register). This bit, when cleared, will override LCD enable control by the PMU (see bit 6 of this register).						
	6	ΡM	IUMODE	Externa l 0 = Do n	External PMU Control Enable 0 = Do not allow PMU to disable power to LCD (bit 7 can still be used)						
				1 = Allow by bi	 1 = Allow PMU to disable/enable power to LCD (sequencing time controlled by bits 5–0, except during emergency power-down) 						
					If the internal graphics controller is enabled (CSC index register DDh[2]='1b'), and the PMU is enabled to shut down the LCD in standby mode (CSC index register 40h[5]='1b'), this bit (graphics index 50h[6]) must also be set.						
	5–3	ΡW	/RUPDLY2[2-	0] Power-u Program control s delay tim into bits	Power-up Power Sequencing Delay 2 Programs the delay time between the sequential events of LCD panel control signal activation and VEE activation during power-up. The actudelay time value equals (N + 1)*7.81 ms, where N is the value program into bits 5–3.						
	2–0 PWRUPDLY1[2–0]			0] Power-L Program and LCD delay tim into bits	Power-up Power Sequencing Delay 1 Programs the delay time between the sequential events of VDD activation and LCD panel data/control signal activation during power-up. The actual delay time value equals $(N + 1)$ *7.81 ms, where N is the value programmed into bits 2–0.						

PMU Control Register 2

I/O Address 3x4h/3x5h Index 51h

	7	6	5	4	3	2	1	0	
Bit		Reserved		PWRDWNDLY2[2–0]	PV	VRDWNDLY1[2	-0]	
Default	х	x	0	0	0	0	0	0	
R/W				R/W			R/W		
	Bit 7–6 5–3	Name Reserved PWRDWNDLY2	Fi R [2–0] Pi da po po	unction eserved ower-down Pov rograms the dela ata/control signa ower-down. The	ver Sequenci ay time betwee deactivation actual delay ti	ng Delay 2 en the sequent and VDD dead me value equa	tial events of L ctivation during als (N + 1)*62.	-CD panel g normal 5ms, where	
	2–0 PWRDWNDLY1[2		(2–0) Po Pi de na m	N is the value programmed into bits 5–3. Power-down Power Sequencing Delay 1 Programs the delay time between the sequential events of VEE deactivation and LCD panel data/control signal deactivation during normal power-down. The actual delay time value equals (N + 1)*62.5 ms, where N is the value programmed into bits 2–0.					

Extended Feature Control Register

I/O Address 3x4h/3x5h Index 52h

	7		6	5	4	3	2	1	0			
Bit	HIDDEN FLUSH	l_ 	PGM1_E_RB	HGAGR_E_RB	HGA_EN	FCURSOR	FRAME_ DLY_DIS	LEG_TRAP_ EN	RGBEN			
Default	0		0	0	0	0	0	0	0			
R/W	R/W		R	R	R/W	R/W	R/W	R/W	R/W			
	Bit	Na	me	Function	Function							
	7	HIDDEN_FLUSH		H Graphic 0 = Grap scan	Graphics Controller FIFO Hidden Flush Enable 0 = Graphics controller will perform FIFO flush/reload at the end of the last scan line, whether it is displayed or not							
				1 = Grap the la	hics controlle ast non-displa	r will perform yed scan line	FIFO flush/rel	oad at the beg	ginning of			
				When se also be s and Hori program (graphic When th end of a	When setting this bit, bit 2 of the Extended Feature Control Register must also be set. In this case, the Horizontal Total Register (graphics index 30h) and Horizontal Border End Register (graphics index 33h) can be programmed to the same value. In addition, the Non-Display Lines Register (graphics index 34h) must be programmed to a non-zero value (1, 2 or 3). When this option is used, there is no need for any additional delay at the end of a horizontal scan line for FIFO flush/reloads.							
	6	PG	GM1_E_RB	Page Me This bit i in the HC bit is vali Register	Page Memory Enable Readback This bit is the readback for the write-only PG_MEM1_EN bit that is located in the HGA Configuration Register at direct mapped register 03BFh[1]. This bit is valid only when the Comp_Mod bit in the Internal Graphics Control Register A (CSC index register DDh[0]) is set.							
	5	ΗG	GAGR_E_RB	HGA Re This bit is the HGA bit is vali Register	HGA Readback This bit is the readback for the write-only HGA_GR_EN bit that is lo the HGA Configuration Register at direct mapped register 03BFh[0 bit is valid only when the Comp_Mod bit in the Internal Graphics C Register A (CSC index register DDh[0]) is set.				s located in ⁻ h[0]. This s Control			
	4	HG	GA_EN	Enable I This bit I Control I 0 = Disa 1 = Enab	Enable HGA Register Extensions in MDA Mode This bit has effect only when the Comp_Mod bit in the Internal Gra Control Register A (CSC index register DDh[0]) is set. 0 = Disable HGA register extensions in MDA mode 1 = Enable HGA register extension in MDS mode				Graphics			
	3	FCURSOR		Normal 0 = 1 Hz 1 = 2 Hz	Normal Cursor Blink Rate Control 0 = 1 Hz 1 = 2 Hz							
	2 FRAME_DLY_DIS		IS Inter-Fra 0 =The horiz data contr	 Inter-Frame FIFO Flush/refill Delay Disable 0 = The graphics controller inserts a delay between the last LCD panel horizontal line pulse signal at the end of a frame, and before shifting data out for the first line of the next frame to allow for a graphics controller FIFO flush/refill 								

1 =Automatic FIFO flush/refill delay disabled

Bit	Name	Function
1	LEG_TRAP_EN	CGA Legacy I/O Trap SMI/NMI Generation Enable 0 = Disables I/O Trap SMI/NMI generation for accesses to the CGA/MDA legacy registers [Cursor Start (index 0Ah), Cursor End (index 0Bh), Start Address High (index 0Ch), Start Address Low (index 0Dh), Cursor Address High (index 0Eh), Cursor Address Low (index 0Fh), Light Pen High (index 10h), and Light Pen Low (index 11h)] when the internal graphics I/O Trap SMI/NMI generation feature is enabled via setting bit 3 of the graphics controller index register at index location 99h
		1 = Enables I/O Trap SMI/NMI generation for accesses to the CGA/ MDA legacy registers [Cursor Start (index 0Ah), Cursor End (index 0Bh), Start Address High (index 0Ch), Start Address Low (index 0Dh), Cursor Address High (index 0Eh), Cursor Address Low (index 0Fh), Light Pen High (index 10h), and Light Pen Low (index 11h) when the internal graphics I/O Trap SMI/NMI generation feature is enabled via setting bit 3 of the graphics controller index register at index location 99h
0	RGBEN	Switch to RGBI Output 0 = Normal operation
		1 = Low order grayscale bits switched to RGBI, data shift clock becomes pixel clock, M becomes display enable

Programming Notes

Bit 2: When graphics index $4Ch[2-0] \leftarrow 011b'$, the delay = $202^*(1/dot clock base frequency)$. When 4Ch[2-0] > 011b', the delay = $256^*(1/dot clock base frequency)$. The delay range is $6.93-9.73 \ \mu$ s.

The "character time" depends upon the dot clock frequency as programmed via graphics index 4Ch, the character width as programmed via graphics index 42h, the horizontal dot doubling enable as programmed via the Internal Graphics Control register A (CSC index DDh[5]), and whether or not a dual scan panel is used as configured via CSC index DDh[3]. If this bit is set, and hidden flush is not enabled via bit 7 of this register, the time defined by the Horizontal Total register setting, the Horizontal Border End register setting must be made long enough to allow the FIFO flush/refill to complete (happens once per frame).

```
Character clock period (character time) = (dot clock period) * (character width) * (horizontal doubling) * (dual scan)
```

where:

dot clock period = 1/dot clock frequency, character width = 8, 10, or 16, horizontal doubling = 2 if doubling enabled, 1 otherwise, and dual scan = 2 if dual scan panel, 1 otherwise.

The time required for this depends on the mode and panel type as shown below:

Mode	Panel	Flush Delay (Minimum)
Graphics	Single-scan	2.7 µs
Text	Single-scan	3.9 µs
Graphics	Dual-scan	3.9 µs
Text	Dual-scan	5.8 µs





PC CARD CONTROLLER INDEXED REGISTERS

6.1 **OVERVIEW**

The registers described in this chapter function as configuration, control, and status for the PC Card controller. They are listed in hexadecimal order by function in Table 6-1.

PC Card controller registers are indexed using I/O ports 3E0h (address) and 3E1h (data).

The PC Card controller indexed registers are accessed using a two-step process:

- An I/O write to I/O address 3E0h is first performed. The data written is the actual index address of the PC Card controller index register.
- This I/O write is followed by an I/O read or write to address 3E1h. This access causes the PC Card controller to allow access to the addressed configuration register. For example:

```
mov DX, 3E0h
mov al, index
out DX, al
inc DX
mov al, new data
out DX, al
```

The PC Card controller registers are typically accessed at CPU speeds.

I/O (Port) Page **Register Name** Index Address Number PC Card Index Register 03E0h page 6-5 PC Card Data Port 03E1h page 6-6 **General Control Group (Socket A)** 00-05h Identification and Revision Register 00h page 6-7 Interface Status Register 01h page 6-8 Power and RESETDRV Control Register 02h page 6-9 Interrupt and General Control Register 03h page 6-11 Card Status Change Register 04h page 6-12 Card Status Change Interrupt Configuration 05h page 6-13 Register Address Window Enable Register 06h page 6-15 I/O Window Mapping Group (Socket A) 07-0Fh I/O Window Control Register 07h page 6-16 I/O Window 0 Start Address Low Register 08h page 6-17

Table 6-1 PC Card Controller Register Map

Register Name	I/O (Port) Address	Index	Page Number
I/O Window 0 Start Address High Register		09h	page 6-18
I/O Window 0 Stop Address Low Register		0Ah	page 6-19
I/O Window 0 Stop Address High Register		0Bh	page 6-20
I/O Window 1 Start Address Low Register		0Ch	page 6-21
I/O Window 1 Start Address High Register		0Dh	page 6-22
I/O Window 1 Stop Address Low Register		0Eh	page 6-23
I/O Window 1 Stop Address High Register		0Fh	page 6-24
Memory Window Mapping Group (Socket A)		10–35h	
Memory Window 0 Start Address Low Register		10h	page 6-25
Memory Window 0 Start Address High Register		11h	page 6-26
Memory Window 0 Stop Address Low Register		12h	page 6-27
Memory Window 0 Stop Address High Register		13h	page 6-28
Memory Window 0 Address Offset Low Register		14h	page 6-29
Memory Window 0 Address Offset High Register		15h	page 6-32
Memory Window 1 Start Address Low Register		18h	page 6-31
Memory Window 1 Start Address High Register		19h	page 6-32
Memory Window 1 Stop Address Low Register		1Ah	page 6-33
Memory Window 1 Stop Address High Register		1Bh	page 6-34
Memory Window 1 Address Offset Low Register		1Ch	page 6-35
Memory Window 1 Address Offset High Register		1Dh	page 6-36
Memory Window 2 Start Address Low Register		20h	page 6-37
Memory Window 2 Start Address High Register		21h	page 6-38
Memory Window 2 Stop Address Low Register		22h	page 6-39
Memory Window 2 Stop Address High Register		23h	page 6-40
Memory Window 2 Address Offset Low Register		24h	page 6-41
Memory Window 2 Address Offset High Register		25h	page 6-42
Memory Window 3 Start Address Low Register		28h	page 6-43
Memory Window 3 Start Address High Register		29h	page 6-44
Memory Window 3 Stop Address Low Register		2Ah	page 6-45
Memory Window 3 Stop Address High Register		2Bh	page 6-46
Memory Window 3 Address Offset Low Register		2Ch	page 6-47
Memory Window 3 Address Offset High Register		2Dh	page 6-54
Memory Window 4 Start Address Low Register		30h	page 6-49
Memory Window 4 Start Address High Register		31h	page 6-50
Memory Window 4 Stop Address Low Register		32h	page 6-51

Register Name	I/O (Port) Address	Index	Page Number
Memory Window 4 Stop Address High Register		33h	page 6-52
Memory Window 4 Address Offset Low Register		34h	page 6-53
Memory Window 4 Address Offset High Register		35h	page 6-54
Timing Control Group		3A–3Fh	
Setup Timing 0 Register		3AH	page 6-55
Command Timing 0 Register		3Bh	page 6-56
Recovery Timing 0 Register		3Ch	page 6-57
Setup Timing 1 Register		3DH	page 6-58
Command Timing 1 Register		3Eh	page 6-59
Recovery Timing 1 Register		3Fh	page 6-60
General Control Group (Socket B)		40–05h	
Identification and Revision Register		40h	page 6-7
Interface Status Register		41h	page 6-8
Power and RESETDRV Control Register		42h	page 6-9
Interrupt and General Control Register		43h	page 6-11
Card Status Change Register		44h	page 6-12
Card Status Change Interrupt Configuration Register		45h	page 6-13
Address Window Enable Register		46h	page 6-15
I/O Window Mapping Group (Socket B)		47–4Fh	
I/O Window Control Register		47h	page 6-16
I/O Window 0 Start Address Low Register		48h	page 6-17
I/O Window 0 Start Address High Register		49h	page 6-18
I/O Window 0 Stop Address Low Register		4Ah	page 6-19
I/O Window 0 Stop Address High Register		4Bh	page 6-20
I/O Window 1 Start Address Low Register		4Ch	page 6-21
I/O Window 1 Start Address High Register		4Dh	page 6-22
I/O Window 1 Stop Address Low Register		4Eh	page 6-23
I/O Window 1 Stop Address High Register		4Fh	page 6-24
Memory Window Mapping Group (Socket B)		50–75h	
Memory Window 0 Start Address Low Register		50h	page 6-25
Memory Window 0 Start Address High Register		51h	page 6-26
Memory Window 0 Stop Address Low Register		52h	page 6-27
Memory Window 0 Stop Address High Register		53h	page 6-28
Memory Window 0 Address Offset Low Register		54h	page 6-29

Register Name	I/O (Port) Address	Index	Page Number
Memory Window 0 Address Offset High Register		55h	page 6-32
Memory Window 1 Start Address Low Register		58h	page 6-31
Memory Window 1 Start Address High Register		59h	page 6-32
Memory Window 1 Stop Address Low Register		5Ah	page 6-33
Memory Window 1 Stop Address High Register		5Bh	page 6-34
Memory Window 1 Address Offset Low Register		5Ch	page 6-35
Memory Window 1 Address Offset High Register		5Dh	page 6-36
Memory Window 2 Start Address Low Register		60h	page 6-37
Memory Window 2 Start Address High Register		61h	page 6-38
Memory Window 2 Stop Address Low Register		62h	page 6-39
Memory Window 2 Stop Address High Register		63h	page 6-40
Memory Window 2 Address Offset Low Register		64h	page 6-41
Memory Window 2 Address Offset High Register		65h	page 6-42
Memory Window 3 Start Address Low Register		68h	page 6-43
Memory Window 3 Start Address High Register		69h	page 6-44
Memory Window 3 Stop Address Low Register		6Ah	page 6-45
Memory Window 3 Stop Address High Register		6Bh	page 6-46
Memory Window 3 Address Offset Low Register		6Ch	page 6-47
Memory Window 3 Address Offset High Register		6Dh	page 6-54
Memory Window 4 Start Address Low Register		70h	page 6-49
Memory Window 4 Start Address High Register		71h	page 6-50
Memory Window 4 Stop Address Low Register		72h	page 6-51
Memory Window 4 Stop Address High Register		73h	page 6-52
Memory Window 4 Address Offset Low Register		74h	page 6-53
Memory Window 4 Address Offset High Register		75h	page 6-54
Timing Control Group		7A–7Fh	
Setup Timing 2 Register		7Ah	page 6-55
Command Timing 2 Register		7Bh	page 6-56
Recovery Timing 2 Register		7Ch	page 6-57
Setup Timing 3 Register		7Dh	page 6-58
Command Timing 3 Register		7Eh	page 6-59
Recovery Timing 3 Register		7Fh	page 6-60

6.2 **REGISTER DESCRIPTIONS**

Each PC Card controller index register is described on the following pages. Additional information about using these registers to program the ÉlanSC400 microcontroller can be found in the *ÉlanSC400 User's Manual* (order #21030).

Primary 82365-Compatible PC Card Controller Index Register

I/O Address 03E0h



Primary 82365-Compatible PC Card Controller Data Port

I/O Address 03E1h



Identification and Revision Register

I/O Address 3E0h/3E1h (Socket A) Index 00h (Socket B) Index 40h

	7	6	5	4	3	2	1	0
Bit	11	INFC_ID[1-0]		Reserved		REVISION[3-0]		
Bit				PCC_REV[7-0]				
Default	1 0		0	0	0	0	1	0
R/W		R		R			R	
R/W				F	२			
	Bit 7–6 5–4 3–0	Name INFC_ID[1-0] RESERVED REVISION[3-0]	Function Interface These b controlle Reserve These b Revision The se b	Function Interface ID These bits identify PC Card interface types supported by the P controller. They read back 10b. Reserved These bits read back 0. Revision Level The initial revision of the PC Card controller will be 0010.				
7–0 PCC_REV[7–0] PC Card Controller Revision This is a remapping of the REVISIC this device-specific revision level. T immediately after a write to this regi any other read or write precedes a REVISION and INFC_ID bits will be				DN and INFC_ These bits will jister (the data read of this re e read back as	ID bits for ider read back F1h written is not gister, the nor s 82h.	ntification of n only relevant.) If mal		

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

Interface Status Register

I/O Address 3E0h/3E1h (Socket A) Index 01h (Socket B) Index 41h

	7	6	5	4	3	2	1	0
Bit	Scratch Bit	PWR_ACT	RDY_BUSY	WR_PROT	CARD_DET2	CARD_DET1	BVD2-	-BVD1
Default	0	0	х	Х	х	х	Х	Х
R/W	R/W	R	R	R	R	R	F	२

Bit	Name	Function
7	Scratch Bit	Scratch Bit In the original 82365SL design, this bit was the GPI status. This bit was used to sample the opposite state of the GPI input pin. The intention was to use this input to indicate valid VPP level or other miscellaneous function. In this implementation the I/O pin is not present and therefore this bit is a general read/write bit with no specific hardware status functionality.
6	PWR_ACT	Slot Power Status This bit indicates the power status of the socket. If 0, power to the socket is disabled. If this bit is set, power to the socket is enabled. See the table below to see the interaction this bit has with relation to the power control functions of index register 01h and 42h.
5	RDY_BUSY	Ready/Busy Signal Status This bit reflects the state of the RDY_x pin of the PC Card.
4	WR_PROT	Memory Write Protect Signal Status This bit reflects the state of the WP_x pin of the PC Card.
3	CARD_DET2	Card Detect 2 Signal Status This bit will always read back the same value as bit 2.
2	CARD_DET1	Card Detect 1 Signal Status This bit at index 01h reflects the inverted state of the $\overline{\text{CD}_x}$ of the PC Card for Socket A. This bit at index 41h reflects the inverted state of the $\overline{\text{CD}_x}$ pin of the PC Card for Socket B when Socket B is enabled. If the Socket A interface is configured to support both CD inputs (i.e., $\overline{\text{CD}_A}$ and $\overline{\text{CD}_A2}$) via the pin configuration option, this bit will reflect the logical anding of these inputs. In this configuration, a value of one indicates that both inputs are asserted. A value of zero indicates that these inputs are not
1–0	BVD2–BVD1	both asserted. Battery Voltage Detect 2 and 1 (Respectively) Signal Status When the socket is configured for the memory-only interface, this bit is used to detect the state of the BVD2_x and BVD1_x pins. These bits are used to determine the state of the card battery. When the socket is configured for the I/O and memory interface these bits are used to detect the state of the BVD2_x and BVD1_x pins, which function as the card's SPKR and STSCHG/RI pins. 0 0 = Battery Dead 0 1 = Battery Dead 1 0 = Warning 1 1 = Battery Good

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

Power and RESETDRV Control Register

I/O Address 3E0h/3E1h (Socket A) Index 02h (Socket B) Index 42h

	7	6	5	4	3	2	1	0
Bit	Unused Bit	Unused Bit	AUTO_PWR_ ENX	VCC_ENX	Unused Bit	Unused Bit	VPP1X_CNT_1	VPP1X_CNT_0
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	Unused Bit	Unused Bit In the original 82365SL implementation, this bit is output enable. This bit was used, in conjunction with the Card Detect inputs, to three-state or enable the socket interface signals and to activate the enable signal for the external buffers (address and data). This implementation does not support an 82365SL compatible enable signal for socket address and data buffers, and this bit is therefore not supported. A buffered PC Card solution can be implemented using one of the GPIO pins as an output to enable or disable the buffers that could be used to isolate a PC Card from the system address and data bus.
6	Unused Bit	Unused Bit In the original 82365SL implementation, this bit is Disable RESETDRV. This bit was used to disable the reset of some of the controller's internal configuration registers when an ISA bus RESETDRV pulse was generated due to a RESUME operation. This feature was required when working with particular system chip sets. It is not required for this implementation and will be fully read/writable while not affecting any other hardware. This implementation is compatible with the CL-PD6720.
5	AUTO_PWR_ENX	Auto Power Enable This bit in conjunction with bits 0, 1, and 4 are used to control the PCMx_VCC signal if this pin functionality is selected. This output is used to control the socket VCC supply. This bit is used to allow the card detect inputs to automatically cause power to be applied to the socket interface. "VCC Control Signal Definition" on page 6-10.
4	VCC_ENX	Socket VCC Enable This bit in conjunction with bits 0, 1, and 5 are used to control the PCMx_VCC signal if this pin functionality is selected. This output is used to control the socket VCC supply. See the following table.
3	Unused Bit	Unused Bit In the original 82365SL implementation, this bit is Vpp2 control Bit 1. In this implementation, this bit is fully read writable but does not have any other hardware function. In the original 82365SL controller, an independent control for the two VPP signals of a single PC Card socket existed. Since most designs physically tie together the two VPP pins at the socket interface, this mechanism has been deleted from the controller. This VPP control implementation is consistent with the CL-PD6720.
2	Unused Bit	Unused Bit In the original 82365SL implementation, this bit is Vpp2 control Bit 0. In this implementation, this bit is fully read writable but does not have any other hardware function. In the original 82365SL controller, an independent control for the two VPP signals of a single PC Card socket existed. Since most designs physically tie together the two VPP pins at the socket interface, this mechanism has been deleted from the controller. This VPP control implementation is consistent with the CL-PD6720.

Bit	Name	Function
1	VPP1X_CNT_1	VPP1 Control This bit, in conjunction with bits 0 and 4 of this register controlled the PCMx_VPP1 and PCMx_VPP2 output signals if this pin functionality is selected. These signals are used to switch the socket Vpp supply between 0, 5, and 12 Volts. See "VPP Control Signal Definition" on page 6-10.
0	VPP1X_CNT_0	VPP1 Control This bit, in conjunction with bits 1 and 4 of this register control the PCMx_VPP1 and PCMx_VPP2 output signals if this pin functionality is selected. These signals are used to switch the socket Vpp supply between 0, 5, and 12 Volts. See "VCC Control Signal Definition" on page 6-10.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

Bit 4 V _{cc} Power	Bit 1 V _{pp} Control Bit 1	Bit 2 V _{pp} Control Bit 0	PCMX_VPP2	PCMX_VPP1	PCMX_VCC	Comments
1	0	0	0	0	0	V _{pp} is N/C V _{CC} enabled
1	0	1	0	1	0	V _{pp} = VCC V _{CC} enabled
1	1	0	1	0	0	V _{pp} = +12 V V _{CC} enabled
1	1	1	0	0	0	V _{pp} is N/C V _{CC} enabled
0	Х	Х	0	0	1	V _{pp} is N/C V _{CC} disabled

VPP Control Signal Definition

VCC Control Signal Definition

Socket CD_X Low	Bit 5 Auto Power Control	Bit 4 Vcc Power	PCMX_VCC	PC Card Power Active (Bit 6 of Interface Status Register)	Comments
Х	Х	0	1	0	Socket forced off
Х	0	1	0	1	Socket forced on
No	1	1	1	0	Auto power enabled and no card inserted
Yes	1	1	0	1	Auto power enabled and card inserted/powered

Interrupt and General Control Register

I/O Address 3E0h/3E1h (Socket A) Index 03h (Socket B) Index 43h

	7	6	5	4	3	2	1	0		
Bit	RI_EN	I CARD_RST	CARD_IS_IO	CSC_INT_ DEST		IRQ	[3–0]			
Default	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W		R	/W			
	Bit	Name	Functio	n						
	7	RI_EN	Ring Inc This bit I General When th RI_EN h 0 = The 1 = The is rou	dicate Enable has no functio Control Regis le CARD_IS_I has the followin BVD1_X (STS BVD1_X (STS uted to the PC	n when the C. ter is configu O bit is config ng meaning: CHG_x) sign CHG_x) sign CHG_x) sign	ARD_IS_IO b red for the me jured for the l, al is used as al is used as a idicate PMU in	it in the Interr emory-only in /O and memo a status chan a ring indicatio nput signal	rupt and terface. ry interface, ge indication on signal and		
	6		This disables use of BVD1_X (STSCHG_X) as a status change indic (see the BATT_DEAD bit in the Card Status Change Register).							
	$0 = RST_X$ is active $1 = RST_X$ is inactive									
	5	CARD_IS_IO	PC Card 0 = Sock	 is inderive d Is I/O <et configured<="" td=""><td>for the memo</td><td>orv-only interf</td><td>ace</td><td></td></et>	for the memo	orv-only interf	ace			
			1 = Sock	ket configured	for I/O and m	emory interfa	ice			
	4	CSC_INT_DES	T Card Sta Controls the PML PC Card in the Pf	atus Change the destination J's PC Card S I Status Chang MU block.	Interrupt Dest on that the car tatus Change ge interrupt ing	stination d status chan interrupt inpu put for NMI/SI	ige is routed t it. The use of VI generation	o: an IRQ or the PMU's is controlled		
			0 = The CSC Conf to dis	card status ch _IRQ3–CSC_ iguration Reg sable generati	ange interrup IRQ0 in the C ster (CSC_IR on of a card s	t signal is rou Card Status Cl Q3–CSC_IR Status change	ted to the IRC hange Interru Q0 can also b interrupt on a	Q encoded in pt pe encoded any IRQ)		
			1 = The Char	1 = The card status change interrupt is routed to the PMU's PC Card Status Change interrupt input						
	3–0	IRQ[3–0]	PC Card Routes t	IRQ Routing the PC Card I) RQ to the app	ropriate PIC I	RQ input as f	ollows:		
			0 0 0 0 = 0 0 0 1 = 0 0 1 0 = 0 0 1 1 = 0 1 0 0 = 0 1 0 1 =	$0\ 0\ 0 = Disabled$ $0\ 0\ 1 = Reserved$ $0\ 0\ 1\ 0 = Reserved$ $0\ 1\ 1 = IRQ3$ enabled $0\ 1\ 0 = IRQ4$ enabled $0\ 1\ 0\ 1 = IRQ5$ enabled						
0 1 1 0 = IRQ6 enabled										
			0 1 1 0 = 0 1 1 1 = 1 0 0 0 = 1 0 1 = 1 0 1 0 = 1 0 1 1 = 1 1 0 0 = 1 1 0 1 = 1 1 0 1 = 1 1 1 1 =	= IRQ6 enable = IRQ7 enable = Reserved = IRQ9 enable = IRQ10 enable = IRQ11 enable = IRQ12 enable = Reserved = IRQ14 enable = IRQ15 enable	d d ed ed ed ed ed					

Card Status Change Register

I/O Address 3E0h/3E1h (Socket A) Index 04h (Socket B) Index 44h

	7	6	5	4	3	2	1	0
Bit		Rese	erved		CD_CHNG	RDY_CHNG	BATT_WARN	BATT_DEAD
Default	0	0	0	0	0	0	0	0
R/W		F	र		R	R	R	R

Bit	Name	Function
7–4	RESERVED	Reserved Always reads back 0.
3	CD_CHNG	Card Detect Change Detected This bit is reset to 0 when this register is read.
		0 = A transition (low to high or high to low) has not occurred on the $\overline{CD_X}$ pin since the last time this register was read
		1 = A transition (low to high or high to low) has occurred
2	RDY_CHNG	Ready Change Detected This bit is reset to 0 when this register is read. This bit has meaning only when the socket is configured for the memory-only interface. In the I/O and memory interface it reads back a 0.
		0 = A transition (low to high or high to low) has not occurred on the RDY_X (IREQ_X) pin since the last time this register was read
		1 = A transition (low to high or high to low) has occurred
1	BATT_WARN	Battery Warning Detected This bit is reset to 0 when this register is read. This bit has meaning only when the socket is configured for the memory-only interface. In the I/O and memory interface it reads back a 0.
		0 = A transition (high to low) has not occurred on the BVD2_X pin since the last time this register was read
		1 = A transition (high to low) has occurred
0	BATT_DEAD	Battery Dead Change or Status Change Detected This bit is reset to 0 when this register is read.
		0 = A transition (high to low) has not occurred on the BVD1_X (STSCHG_X) pin since the last time this register was read
		1 = A transition (high to low) has occurred
		When the socket is configured for the memory-only interface, this bit indicates a Battery Dead condition has been asserted on the BVD1_X signal if this bit is set.
		When the socket is configured for the I/O and memory interface, the state of this bit is determined by the state of the RI_EN bit in the Interrupt and General Control Register and the state of the BVD1_X/STSCHG_X pin. If the RI_EN bit is 0, then the BATT_DEAD bit is set to 1 when the STSCHG_X pin is asserted. If the RI_EN bit is set to 1, then the BATT_DEAD bit will always reads back 0.

Card Status Change Interrupt Configuration Register I/O Address 3E0h/3E1h (Socket A) Index 05h (Socket B) Index 45h

	7	6	5	4	3	2	1	0
Bit		CSC_IF	RQ[3–0]		CD_EN	RDY_EN	BATT_ WARN_EN	BATT_ DEAD_EN
Default	0	0	0	0	0	0	0	0
R/W		R/W				R/W	R/W	R/W

Bit	Name	Function
7–4	CSC_IRQ[3–0]	Card Status Change IRQ Routing Enables and selects the IRQ line to issue the PC Card status change interrupt on. The state of the CSC_INT_DEST bit in Interrupt and General Control Register determines how CSC_IRQ3–CSC_IRQ0 is interpreted. If CSC_INT_DEST is set, no IRQ line is used; if it is cleared, the IRQ line is selected according to the following CSC_IRQ3–CSC_IRQ0 table:
		0 0 0 0 = Disabled
		0 0 0 1 = Reserved
		0 0 1 0 = Reserved
		0 0 1 1 = IRQ3 enabled
		0 1 0 0 = IRQ4 enabled
		0 1 0 1 = IRQ5 enabled
		0 1 1 0 = Reserved
		0 1 1 1 = IRQ7 enabled
		1 0 0 0 = Reserved
		$1 \ 0 \ 0 \ 1 = IRQ9$ enabled
		1 0 1 0 = IRQ10 enabled
		1 0 1 1 = IRQ11 enabled
		1 1 0 0 = IRQ12 enabled
		1 1 0 1 = Reserved
		1 1 1 0 = IRQ14 enabled
		1 1 1 1 = IRQ15 enabled
3	CD_EN	Card Detect IRQ Enable Enables CD_CHNG (bit 3) of the Card Status Change Register (PC Card index 04/44h) to generate a card status change interrupt.
		0 = CD_CHNG bit of the Card Status Change Register does not generate a card status change interrupt
		1 = CD_CHNG bit of the Card Status Change Register does generate a card status change interrupt
2	RDY_EN	Ready IRQ Enable Enables RDY_CHNG (bit 2) of the Card Status Change Register (index 04h/44h) to generate a card status change interrupt. This bit is ignored when the socket is configured for I/O interface.
		0 = RDY_CHNG bit of the Card Status Change Register does not generate a card status change interrupt
		1 =RDY_CHNG bit of the Card Status Change Register does generate a card status change interrupt

Bit	Name	Function
1	BATT_WARN_EN	 Battery Warning IRQ Enable Enables BATT_WARN (bit 1) of the Card Status Change Register (PC Card index 04h/44h) to generate a card status change interrupt. This bit is ignored when the socket is configured for I/O interface. 0 = BATT_WARN bit of the Card Status Change Register does not generate a card status change interrupt
		1 =BATT_WARN bit of the Card Status Change Register does generate a card status change interrupt
0	BATT_DEAD_EN	Battery Dead or Status Change IRQ Enable Enables BATT_DEAD (bit 0) of the Card Status Change Register (PC Card index 04h/44h) to generate a card status change interrupt when BATT_DEAD is 1.
		0 = BATT_DEAD bit of the Card Status Change Register does not generate a card status change interrupt
		1 =BATT_DEAD bit of the Card Status Change Register does generate a card status change interrupt

Address Window Enable Register

I/O Address 3E0h/3E1h (Socket A) Index 06h (Socket B) Index 46h

	7	6	5	4	3	2	1	0
Bit	IO_WIN_ EN[1]	IO_WIN_ EN[0]	Scratch Bit	MEM_WIN_ EN[4]	MEM_WIN_ EN[3]	MEM_WIN_ EN[2]	MEM_WIN_ EN[1]	MEM_WIN _EN[0]
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	IO_WIN_EN[1]	I/O Window 1 Enable
6	IO_WIN_EN[0]	I/O Window 0 Enable
5	Scratch Bit	This is the 'MEMCS16 Decode A23–A12' bit in the 82365SL (Rev. B).
4	MEM_WIN_EN[4]	Memory Window 4 Enable
3	MEM_WIN_EN[3]	Memory Window 3 Enable
2	MEM_WIN_EN[2]	Memory Window 2 Enable
1	MEM_WIN_EN[1]	Memory Window 1 Enable
0	MEM_WIN_EN[0]	Memory Window 0 Enable

Programming Notes

Bits 4–1: This device has two PC Card modes of operation referred to as Standard mode and Enhanced mode. Standard mode is the default mode of operation. Enhanced mode can be enabled via bit 0 of the Chip Setup and Control (CSC) register F1h. In the Standard PC Card mode of operation, a total of six PC Card memory windows are available. These PC Card windows are enabled via memory window C–F enable bits of the Address Window Enable Register for Socket A and the Memory Window C Enable bit of the Address Window Enable Register for Socket B. The memory window C–F enable bits for Socket B are used to enable/disable the MMS Windows C–F in Standard PC Card mode. This is due to the fact that in Standard PC Card mode, the memory window resources that are typically Socket B memory window control are used for Memory Management System (MMS) Windows C–F control. See the table below for the PC Card Socket B resources used for MMS Windows C–F when in Standard PC Card mode.

The MMS windows are disabled when the Enhanced PC Card mode is selected. In the Enhanced PC Card mode the Address Window 1–4 enable bits for Socket B are used to enable or disable the PC Card memory windows for Socket B normally.

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

PC Card Socket B Memory Window Resources Used for MMS

PC Card Socket B Memory Window Control	MMS Window	PC Card Controller Index Registers Used (Index address and data port = 3E0h/3E1h)		
Window 0	None	None		
Window 1	MMS 0	46h (bit 1), 58–5Dh		
Window 2	MMS 1	46h[2], 60–65h		
Window 3	MMS 2	46h[3], 68–6Dh		
Window 4	MMS 3	46h[4], 70–75h		

I/O Window Control Register

I/O Address 3E0h/3E1h (Socket A) Index 07h (Socket B) Index 47h

	7	6	5	4	3	2	1	0
Bit	TIM_SEL_1	Scratch Bit	IO_WIN_AUTO_ SIZE_1	IO_WIN_ SIZE_1	TIM_SEL_0	Scratch Bit	IO_WIN_AUTO_ SIZE_0	IO_WIN_ SIZE_0
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7	TIM_SEL_1	 I/O Window 1 Timing Set Select This bit selects one of two timing sets to use for PC Card cycles generated on hits to I/O window 1. 0 = Timing set 0 is used for I/O cycle timings 1 = Timing set 1 is used for I/O cycle timings This is the I/O window 1 Wait State bit in the 82365SL (Rev. B). It selected the number of ISA bus wait states to use during PC Card I/ O cycles. Since this design implements cycle timing differently, this bit has a different meaning.
6	Scratch Bit	Scratch Bit This is the 'I/O Window 1 Zero Wait State' bit in the 82365SL (Rev. B). In this implementation, this bit does not control any specific hardware.
5	IO_WIN_AUTO_SIZE_1	<pre>I/O Window 1 Auto-Size 0 = IO_WIN_SIZE_1 bit determines I/O window 1 size 1 = WP_X (IOIS16_x) signal determines I/O window 1 size</pre>
4	IO_WIN_SIZE_1	I/O Window 1 Size 0 = I/O window 1 is 8 bits wide 1 = I/O window 1 is 16 bits wide
3	TIM_SEL_0	 I/O Window 0 Timing Set Select This bit selects one of two timing sets to use for PC Card cycles generated on hits to I/O window 0. 0 = Timing set 0 is used for I/O cycle timings 1 = Timing set 1 is used for I/O cycle timings This is the I/O window 0 Wait State bit in the 82365SL (Rev. B). It selected the number of ISA bus wait states to use during PC Card I/O cycles. Since this design implements cycle timing differently, this bit has a different meaning.
2	Scratch Bit	Scratch Bit This is the 'I/O Window 0 Zero Wait State' bit in the 82365SL (Rev. B). In this implementation, this bit does not control any specific hardware.
1	IO_WIN_AUTO_SIZE_0	<pre>I/O Window 0 Auto-Size 0 = IO_WIN_SIZE_0 bit determines I/O window 0 size 1 = WP_X (IOIS16_x) signal determines I/O window 0 size</pre>
0	IO_WIN_SIZE_0	I/O Window 0 Size 0 = I/O window 0 is 8 bits wide 1 = I/O window 0 is 16 bits wide

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

I/O Window 0 Start Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 08h (Socket B) Index 48h



I/O Window 0 Start Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 09h (Socket B) Index 49h



I/O Window 0 Stop Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 0Ah (Socket B) Index 4Ah



I/O Window 0 Stop Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 0Bh (Socket B) Index 4Bh



I/O Window 1 Start Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 0Ch (Socket B) Index 4Ch



I/O Window 1 Start Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 0Dh (Socket B) Index 4Dh



I/O Window 1 Stop Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 0Eh (Socket B) Index 4Eh



I/O Window 1 Stop Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 0Fh (Socket B) Index 4Fh



Memory Window 0 Start Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 10h (Socket B) Index 50h



Memory Window 0 Start Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 11h (Socket B) Index 51h

	7		6	5	4	3	2	1	0	
Bit	DATA_SIZE Scratch Bit		Scratch Bit	MEM_WIN0_START[25-24]		MEM_WIN0_START[23-20]				
Default	0		0	0	0	0	0	0	0	
R/W	R/W	,	R/W	R/W			R/	W		
	Bit 7	Sit Name 7 DATA_SIZE			Function Window Data Size 0 = Enables an 8-bit data path					
	6 Scratch Bit		1							
			Sc Th	This is the Zero Wait State bit in the 82365SL (Rev. B).						
5–4 MEM_WIN0_ START[25–24] Memory Window 0 Start Address Bi Contains bits 25–24 of the system add into the PC Card memory address spa These bits are reserved in the 82365S			Iress Bits 26- tem address a ress space. 82365SL (Re	s 26–24 ess at which to start mapping æ. _ (Rev. B).						
	3–0	ME ST	M_WIN0_ ART[23-20]	Me Co inte	mory Window ntains bits 23- the PC Card	w 0 Start Add -20 of the sys memory add	Iress Bits 23- tem address a ress space.	-20 at which to sta	irt mapping	

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

Memory Window 0 Stop Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 12h (Socket B) Index 52h



Memory Window 0 Stop Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 13h (Socket B) Index 53h

	7	6	5	4	3	2	1	0
Bit	TIMER_	SEL[1-0]	MEM_WIN0_	STOP[25-24]		MEM_WIN0_	STOP[23-20]	
Default	0	0	0	0	0	0	0	0
R/W	R	Ŵ	R/W		R/W			

Bit	Name	Function
7–6	TIMER_SEL[1-0]	Memory Window Timer Set Select For this window, selects which of the four timer sets to use for PC Card (non-DMA) memory cycles.
5–4	MEM_WIN0_ STOP[25-24]	Memory Window 0 Stop Address Bits 25–24 Contains bits 25–24 of the system address at which to stop mapping into the PC Card address space. These bits are reserved in the 82365SL (Rev. B).
3–0	MEM_WIN0_ STOP[23-20]	Memory Window 0 Stop Address 23–20 Contains bits 23–20 of the system address at which to stop mapping into the PC Card address space.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.
Memory Window 0 Address Offset Low Register

I/O Address 3E0h/3E1h (Socket A) Index 14h (Socket B) Index 54h



Memory Window 0 Address Offset High Register

I/O Address 3E0h/3E1h (Socket A) Index 15h (Socket B) Index 55h

	7		6	5	4	3	2	1	0
Bit	WR_PR	от	REG_ACT	MEM_WI OFS	N0_CARD_ [25-24]	MEM_WIN0_CARD_OFS[23-20])]
Default	0		0	0	0	0	0	0	0
R/W	R/W		R/W	F	z/W		R/	/W	
	Bit 7 6	Na WF RE	me R_PROT G_ACT	Fun 0 = 1 1 = 1 REC Sele 0 = 1 1 = 1	ction dow Write Pro Permits writes Prevents writes Active cts the state o Window is map Window is map	otect to go through s from going th f the REG_X p oped to PC Ca oped to PC Ca	to the PC Car prough to the pin for access and common m and attribute m	rd PC Card es to this wind nemory iemory	low.
	5–4	5-4 MEM_WIN0_CARD_OFS[25-24] 3-0 MEM_WIN0_CARD_OFS[23-20]		RD_ Men Con addr Thes	nory Window tains bits 25–2 ress bits SA25 se bits are rese	0 PC Card Of 4 of the offset -SA24 before erved in the 82	fset Address which is to be mapping into 2365SL (Rev.	Bits 25–24 e added to sys PC Card men B).	tem hory space.
	3–0			RD_ Men Con addr	tory Window tains bits 23–2 ess bits SA23	0 PC Card Of 0 of the offset -SA20 before	fset Address which is to be mapping into	Bits 23–20 e added to sys PC Card men	tem hory space.

Programming Notes

Memory Window 1 Start Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 18h (Socket B) Index 58h



Memory WIndow 1 Start Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 19h (Socket B) Index 59h

	7	6	5	4	3	2	1	0		
Bit	DATA_S	IZE Scratch Bit	MEM_WIN START	11_CARD_ [25–24]	ME	EM_WIN1_CAR	D_START[23-2	20]		
Default	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R	/W		R/	W			
	Bit	Name	Func	tion						
	7	DATA_SIZE	Winc 0 = E 1 = E	Window Data Size 0 = Enables an 8-bit data path 1 = Enables a 16-bit data path						
	6	Scratch Bit	Scra This	tch Bit is the Zero Wa	ait State bit in	the 82365SL	(Rev. B).			
	5–4	MEM_WIN1_CA START[25–24]	RD_ Mem Cont into t Thes	Memory Window 1 PC Card Start Address Bits 25–24 Contains bits 25–24 of the system address at which to start mapp into the PC Card memory address space. These bits are reserved in the 82365SL (Rev. B).						
	3–0	MEM_WIN1_CA START[23–20]	RD_ Mem Cont into t	Memory Window 1 PC Card Start Address Bits 23–20 Contains bits 23–20 of the system address at which to start mapping into the PC Card memory address space.						

Programming Notes

Memory Window 1 Stop Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 1Ah (Socket B) Index 5Ah



Memory Window 1 Stop Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 1Bh (Socket B) Index 5Bh

	7		6	5	4	3	2	1	0
Bit	TIN	IER_	SEL[1-0]	MEM_WIN STOP	N1_CARD_ [25–24]	N	IEM_WIN1_CAF	RD_STOP[23-2	:0]
Default	0		0	0	0	0	0	0	0
R/W	R/W	1	R/W	R	/W		R/	Ŵ	
	Bit	Na	me	Fund	ction				
	7–6	7–6 TIMER_SEL[1–0])] Mem For t PC C	Memory Window Timer Set Select For this window, these bits select which of the four timer se PC Card (non-DMA) memory cycles.				s to use for
	5–4	ME ST	:M_WIN1_CA OP[25–24]	RD_ Mem Cont into t	ory Window ains bits 25–24 he PC Card ad	1 PC Card Solution 4 of the system 4 dress space	t op Address I em address at	Bits 25–24 which to stop	mapping

Programming Notes

MEM_WIN1_CARD_ STOP[23-20]

3–0

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

into the PC Card address space.

These bits are reserved in the 82365SL (Rev. B).

Memory Window 1 PC Card Stop Address Bits 23–20 Contains bits 23–20 of the system address at which to stop mapping

Memory Window 1 Address Offset Low Register

I/O Address 3E0h/3E1h (Socket A) Index 1Ch (Socket B) Index 5Ch



Memory Window 1 Address Offset High Register

I/O Address 3E0h/3E1h (Socket A) Index 1Dh (Socket B) Index 5Dh

	7		6	5	4	3	2	1	0
Bit	WR_PR	от	REG_ACT	MEM_WII OFS[N1_CARD_ 25–24]	MEM_WIN1_CARD_OFS[23-20]			0]
Default	0		0	0	0	0	0	0	0
R/W	R/W		R/W	R	/W		R/	Ŵ	
	Bit 7 6	Na WF RE	me R_PROT G_ACT	Fund 0 = F 1 = F REG Sele 0 = V 1 = V	ction dow Write Pro Permits writes Prevents writes Active cts the state o Vindow is map Vindow is map	otect to go through from going th f the REG_X p pped to PC Ca oped to PC Ca	to the PC Car prough to the pin for access and common m and attribute m	rd PC Card es to this wind nemory emory	dow.
	5–4	5–4 MEM_WIN1_CAF OFS[25–24]		RD_ Mem Cont addr Thes	ory Window ains bits 25–2 ess bits SA25 e bits are rese	1 PC Card Of 4 of the offset -SA24 before erved in the 82	fset Bits 25– which is to be mapping into 2365SL (Rev.	24 e added to sys PC Card mer B).	stem nory space.
	3–0	ME OF	M_WIN1_CA S[23–20]	RD_ Mem Cont addr	ory Window ains bits 23–2 ess bits SA23	1 PC Card Of 0 of the offset -SA20 before	fset Bits 23– which is to be mapping into	20 e added to sys PC Card mer	stem nory space.

Programming Notes

Memory Window 2 Start Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 20h (Socket B) Index 60h



Memory Window 2 Start Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 21h (Socket B) Index 61h

	7	6	5	4	3	2	1	0		
Bit	DATA_S	ZE Scratch Bit	MEM_WIN2_S	START[25–24]	MEM_WIN2_START[23-20]					
Default	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/	W		R/	W			
	Bit 7	Name DATA_SIZE	Function Window 0 = Enab	n 7 Data Size bles an 8-bit d	ata path					
			1 = Enat	1 = Enables a 16-bit data path						
	6	Scratch Bit	Scratch This is th	Scratch Bit This is the Zero Wait State bit in the 82365SL (Rev. B).						
	5–4	5–4 MEM_WIN2_ START[25–24]		Window 2 Sease bits 25–24 of Card memory a	t art Address the system a address spac	Bits 26–24 address at whi e.	ch to start ma	pping into		
	3–0	MEM_WIN2_ START[23-20]	Memory Contains the PC C	Memory Window 2 Start Address Bits 23–20 Contains bits 23–20 of the system address at which to start mapping into the PC Card memory address space.						

Programming Notes

Bits 5–4: These bits are reserved in the 82365SL (Rev. B).

Memory Window 2 Stop Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 22h (Socket B) Index 62h



Memory Window 2 Stop Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 23h (Socket B) Index 63h

	7	6	5	4	3	2	1	0
Bit	TIMER_S	SEL[1-0]	MEM_WIN2_	STOP[25-24]		MEM_WIN2_	STOP[23-20]	
Default	0	0	0	0	0	0	0	0
R/W	R/W		R/W			R	W/W	

Bit	Name	Function
7–6	TIMER_SEL[1-0]	Memory Window Timer Set Select For this window, these bits select which of the four timer sets to use for PC Card (non-DMA) memory cycles.
5–4	MEM_WIN2_ STOP[25-24]	Memory Window 2 Stop Address Bits 25–24 Contains bits 25–24 of the system address at which to stop mapping into the PC Card address space. These bits are reserved in the 82365SL (Rev. B).
3–0	MEM_WIN2_ STOP[23-20]	Memory Window 2 Stop Address Bits 23–20 This field contains bits 23–20 of the system address at which to stop mapping into the PC Card address space.

Programming Notes



I/O Address 3E0h/3E1h (Socket A) Index 24h (Socket B) Index 64h



Memory Window 2 Address Offset High Register

I/O Address 3E0h/3E1h (Socket A) Index 25h (Socket B) Index 65h

	7	6	5	4	3	2	1	0				
Bit	WR_PR	OT REG_ACT	MEM_WIN OFS[2	12_CARD_ 25–24]	MEM_WIN2_CARD_OFS[23-20]							
Default	0	0	0	0	0	0	0	0				
R/W	R/W	R/W	R	/W		R/	W					
	Bit	Bit Name 7 WR PROT		tion	staat							
	7	WR_PROT		0 = Permits writes to go through to the PC Card 1 = Prevents writes from going through to the PC Card								
	6	REG_ACT	REG Select 0 = \ 1 = \	REG Active Selects the state of the REG_X pin for accesses to this window. 0 = Window is mapped to PC Card common memory 1 = Window is mapped to PC Card attribute memory								
	5–4	MEM_WIN2_CA OFS[25-24]	RD_ Mem This syste space Thes	ory Window field contains em address bit e. e bits are rese	2 PC Card Of bits 25–24 of s SA25–SA24 erved in the 82	fset Address the offset whic before mapp 2365SL (Rev.	Bits 25–24 ch is to be add ing into PC Ca B).	ded to ard memory				
	3–0	MEM_WIN2_CA OFS[23-20]	RD_ Mem This syste space	ory Window field contains m address bit e.	2 PC Card Of bits 23–20 of s SA23–SA20	fset Address the offset whit before mapp	Bits 23–20 ch is to be add ing into PC Ca	ded to ard memory				

Programming Notes

Memory Window 3 Start Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 28h (Socket B) Index 68h



Memory Window 3 Start Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 29h (Socket B) Index 69h

	7		6	5	4	3	2	1	0		
Bit	DATA_S	DATA_SIZE Sc		MEM_WIN3_	START[25–24]	MEM_WIN3_START[23-20]					
Default	0		0	0	0	0	0	0	0		
R/W	R/W	/	R/W	R	R/W R/W						
	Bit 7	Bit Name 7 DATA_SIZE			Function Window Data Size 0 = Enables an 8-bit data path 1 = Enables a 16-bit data path						
	0	Sch	alch bil	This is the	This is the Zero Wait State bit in the 82365SL (Rev. B).						
	5–4	5–4 MEM_WIN3_ START[25–24]		Memory This field mapping These b	Memory Window 3 Start Address Bits 26–24 This field contains bits 25–24 of the system address at which to start mapping into the PC Card memory address space. These bits are reserved in the 82365SL (Rev. B).						
	3–0	ME STA	M_WIN3_ Art[23-20]	Memory This field mapping	Window 3 S d contains bits g into the PC C	a rt Address 23–20 of the ard memory	Bits 23–20 system addre address spac	ess at which to e.	start		

Programming Notes

Memory Window 3 Stop Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 2Ah (Socket B) Index 6Ah



Memory Window 3 Stop Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 2Bh (Socket B) Index 6Bh

	7	6	5	4	3	2	1	0
Bit	TIMER_	SEL[1-0]	MEM_WIN3_	STOP[25-24]		MEM_WIN3_	STOP[23-20]	
Default	0	0	0	0	0	0	0	0
R/W	R/	W	R/	Ŵ		R	/W	

Bit	Name	Function
7–6	TIMER_SEL[1-0]	Memory Window Timer Set Select For this window, this field selects which of the four timer sets to use for PC Card (non-DMA) memory cycles.
5–4	MEM_WIN3_ STOP][25-24]	Memory Window 3 Stop Address Bits 25–24 This field contains bits 25–24 of the system address at which to stop mapping into the PC Card address space. These bits are reserved in the 82365SL (Rev. B).
3–0	MEM_WIN3_ STOP][23-20]	Memory Window 3 Stop Address Bits 23–20 This field contains bits 23–20 of the system address at which to stop mapping into the PC Card address space.

Programming Notes

Memory Window 3 Address Offset Low Register

I/O Address 3E0h/3E1h (Socket A) Index 2Ch (Socket B) Index 6Ch



Memory Window 3 Address Offset High Register

I/O Address 3E0h/3E1h (Socket A) Index 2Dh (Socket B) Index 6Dh

	7	6	5	4	3	2	1	0				
Bit	WR_PR	OT REG_ACT	MEM_WIN OFS[2	N3_CARD_ 25–24]	MEM_WIN3_CARD_OFS[23-20]							
Default	0	0	0	0	0	0	0	0				
R/W	R/W	R/W	R	R/W R/W								
	Bit	Name	Func	ction								
	7	WR_PROT	Winc 0 = F 1 = F	Window Write Protect 0 = Permits writes to go through to the PC Card 1 = Prevents writes from going through to the PC Card								
	6	REG_ACT	REG This 0 = V 1 = V	REG Active This bit selects the state of the REG_X pin for accesses to this window. 0 = Window is mapped to PC Card common memory 1 = Window is mapped to PC Card attribute memory								
	5–4	MEM_WIN3_C OFS[25-24]	ARD_ Mem This syste spac Thes	Memory Window 3 PC Card Offset Address Bits 25–24 This field contains bits 25–24 of the offset which is to be added to system address bits SA25–SA24 before mapping into PC Card memory space.								
	3–0	MEM_WIN3_C OFS[23-20]	ARD_ Mem This syste space	field contains am address bit e.	3 PC Card Of bits 23–20 of s SA23–SA20	fset Address the offset whic before mappi	Bits 23–20 th is to be add ng into PC Ca	led to ard memory				

Programming Notes

Memory Window 4 Start Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 30h (Socket B) Index 70h



Memory Window 4 Start Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 31h (Socket B) Index 71h

	7		6	5	4	3	2	1	0	
Bit	DATA_SIZE Scratch Bit ME		MEM_WIN4_S	EM_WIN4_START[25–24]		MEM_WIN4_START[23-20]				
Default	0		0	0	0	0	0	0	0	
R/W	R/W	'	R/W	R/	W		R/	W		
	Bit 7	Na DA	me TA_SIZE	Function Window Data Size 0 = Enables an 8-bit data path 1 = Enables a 16-bit data path						
	6	Scratch Bit		Scratch This is th	Scratch Bit This is the Zero Wait State bit in the 82365SL (Rev. B).					
	5–4	MEM_WIN4_ START[25–24] Memory Window 4 this field contains bits mapping into the PC These bits are reserv		Window 4 S contains bits into the PC C its are reserve	Start Address Bits 26–24 s 25–24 of the system address at which to start Card memory address space. red in the 82365SL (Rev. B).					
	3–0	ME ST	:M_WIN4_ ART[23-20]	Memory This field mapping	Window 4 S contains bits into the PC C	tart Address 23–20 of the Card memory	Bits 23–20 system addre address space	ess at which to e.) start	

Programming Notes

Memory Window 4 Stop Address Low Register

I/O Address 3E0h/3E1h (Socket A) Index 32h (Socket B) Index 72hl



Memory Window 4 Stop Address High Register

I/O Address 3E0h/3E1h (Socket A) Index 33h (Socket B) Index 73h

	7	6	5	4	3	2	1	0
Bit	TIMER_	SEL[1-0]	MEM_WIN4_	STOP[25-24]		MEM_WIN4_	STOP[23-20]	
Default	0	0	0	0	0	0	0	0
R/W	R/W		R/W		R/W			

Bit	Name	Function
7–6	TIMER_SEL[1-0]	Memory Window Timer Set Select For this window, this field selects which of the four timer sets to use for PC Card (non-DMA) memory cycles.
5–4	MEM_WIN4_ STOP[25-24]	Memory Window 4 Stop Address Bits 25–24 This field contains bits 25–24 of the system address at which to stop mapping into the PC Card address space. These bits are reserved in the 82365SL (Rev. B).
3–0	MEM_WIN4_ STOP[23-20]	Memory Window 4 Stop Address Bits 23–20 This field contains bits 23–20 of the system address at which to stop mapping into the PC Card address space.

Programming Notes

Memory Window 4 Address Offset Low Register

I/O Address 3E0h/3E1h (Socket A) Index 34h (Socket B) Index 74h



Memory Window 4 Address Offset High Register

I/O Address 3E0h/3E1h (Socket A) Index 35h (Socket B) Index 75h

	7	6	5	4	3	2	1	0	
Bit	WR_PR	OT REG_ACT	MEM_WIN OFS[2	14_CARD_ 25–24]	MEM_WIN4_CARD_OFS[23-20]				
Default	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R	/W		R/	W		
	Bit		Fund	tion	staat				
	7	WR_PROT	0 = P 1 = P	Permits writes Prevents writes	to go through s from going th	to the PC Car prough to the	[.] d PC Card		
	6	REG_ACT	REG Selec 0 = V 1 = V	REG Active Selects the state of the REG_X pin for accesses to this window. 0 = Window is mapped to PC Card common memory 1 = Window is mapped to PC Card attribute memory					
	5–4	MEM_WIN4_CA OFS[25-24]	NRD_ Mem This syste space Thes	Memory Window 4 PC Card Offset Address Bits 25–24 This field contains bits 25–24 of the offset which is to be added to system address bits SA25–SA24 before mapping into PC Card memory space. These bits are reserved in the 82365SL (Rev. B).					
	3–0	MEM_WIN4_CA OFS[23-20]	ARD_ Mem This syste space	ory Window field contains em address bit e.	4 PC Card Of bits 23–20 of s SA23–SA20	fset Address the offset whic before mapp	Bits 23–20 ch is to be add ing into PC Ca	ded to ard memory	

Programming Notes

Setup Timing 0 Register

5–0

	7	6	5	Λ	2	n	1	0
	/	0	5	4	3	2	I	0
Bit	SETU	JP_PRESC[1-0]			SETUP_N	1ULT[5–0]		
Default	0	0	0	0	0	0	0	0
R/W		R/W			R/	W		
	Bit	Name	Fund	tion				

Programming Notes

SETUP_MULT[5-0]

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (Setup, Command active, or Recovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

section for a description of the formula.

section for a description of the formula.

For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with N_{pres} to select the number of clocks of setup time from valid address before the PC Card command goes active. See the top of this

Setup Timing Multiplier Value

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

	7	6	5	4	3	2	1	0
Bit	CME	D_PRESC[1-0]			CMD_M	ULT[5–0]		
Default	0	0	0	0	1	1	1	1
R/W		R/W			R/	/W		
	Bit	Name	Functio	n				
	7–6	CMD_PRESC[1-	0] Comma For this prescale the top of	nd Timing Pre timing set, this N _{val} to select of this section	escaler Select s field selects t the number of for a descripti	t N _{pres} from on of clocks of co on of the form	e of four value mmand active nula.	es to time. See
	5–0	CMD_MULT[5-0]	Comma For this t to select section f	nd Timing Mu timing set, this the number of or a description	Iltiplier Value field selects N clocks of com n of the formula	_{val} from 0 to 63 Imand active ti a.	to be multiplie me. See the to	d with N _{pres} p of this

Command Timing 0 Register

I/O Address 3E0h/3E1h Index 3Bh

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

Recovery Timing 0 Register

	7	6	5	4	3	2	1	0
Bit	REC_PR	ESC[1-0]			REC_MU	JLT[5-0]		
Default	0	0	0	0	0	0	0	0
R/W	R/W		R/W					

Bit	Name	Function
7–6	REC_PRESC[1-0]	Recovery Timing Prescaler Select For this timing set, this field selects N_{pres} from one of four values to prescale N_{val} to select the number of clocks of recovery time (address hold time after the PC Card command goes inactive until the address changes state.) See the top of this section for a description of the formula.
5–0	REC_MULT[5-0]	Recovery Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with N_{pres} to select the number of clocks of recovery time (address hold time after the PC Card command goes inactive until the address changes state.) See the top of this section for a description of the formula.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

7 6 5 4 3 2 1 0 Bit SETUP_PRESC[1-0] SETUP_MULT[5-0] 0 Default 0 0 0 0 0 0 0 R/W R/W R/W Bit Name Function 7-6 SETUP_PRESC[1-0] Setup Timing Prescaler Select For this timing set, this field selects N_{pres} from one of four values to prescale N_{val} to select the number of clocks of setup time from valid address before the PC Card command goes active. See the top of this section for a description of the formula. 5–0 SETUP_MULT[5-0] Setup Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with Npres to select the number of clocks of setup time from valid address before the PC Card command goes active. See the top of this section for a description of the formula.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

Setup Timing 1 Register

Command Timing 1 Register

	7	6	5	4	3	2	1	0
Bit	CMI	D_PRESC[1-0]			CMD_MU	JLT[5–0]		
Default	0	0	0	0	2	2	2	2
R/W		R/W			R/	W		
	Bit	Name	Func	tion				
7–6 CMD_PRESC[1–0] Comm For this			mand Timing his timing set,	Prescaler Se this field select	elect cts N _{pres} from	n one of four va	alues to	

		prescale N _{val} to select the number of clocks of command active time. See the top of this section for a description of the formula.
5–0	CMD_MULT[5-0]	Command Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with N_{pres} to select the number of clocks of command active time. See the top of this section for a description of the formula.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

-							In	dex 3F
	7	6	5	4	3	2	1	0
Bit	RE	C_PRESC[1-0]			REC_M	JLT[5–0]		
Default	0	0	0	0	0	0	0	0
R/W		R/W			R	Ŵ		
	Bit	Name	Fund	ction				
	7–6	REC_PRESC[1-	-0] Reco For t prese hold chan	overy Timing his timing set, cale N _{val} to se time after the ges state.) Se	Prescaler Se this field sele lect the numb PC Card com se the top of th	lect cts N _{pres} from er of clocks of mand goes in nis section for	one of four va f recovery time active until the a description	alues to e (address e address of the
	5–0	REC_MULT[5-0)] Reco For t with	ula. overy Timing his timing set, N _{ares} to select	Multiplier Va this field sele	lue cts N _{val} from (of clocks of red	0 to 63 to be n coverv time (ad	nultiplied ddress hold

I/O Address 3E0h/3E1h

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

time after the PC Card command goes inactive until the address changes state.) See the top of this section for a description of the formula.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

AMDZ

Recovery Timing 1 Register

Setup Timing 2 Register

5–0

	7	6	5	4	3	2	1	0
Bit	SETI	JP_PRESC[1-0]			SETUP_	MULT[5–0]		
Default	0	0	0	0	0	0	0	0
R/W		R/W		•	R	/W		•
	Bit	Name	Func	tion				
	7–6	SETUP_PRESC	C[1-0] Setu For the present	p Timing Pres his timing set, cale N _{vol} to sel	scaler Selec this field sele lect the numb	t ects N _{pres} from per of clocks of	one of four v setup time fr	alues to om valid

SETUP_MULT[5–0] Setup Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with N_{pres} to select the number of clocks of setup time from valid address before the PC Card command goes active. See the top of this section for a description of the formula.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

Command Timing 2 Register 7 6 5 4 3 2 Bit CMD_PRESC[1-0] CMD_MULT[5-0] 3 Default 0 0 0 0 3

Bit	Name	Function
7–6	CMD_PRESC[1-0]	Command Timing Prescaler Select For this timing set, this field selects N_{pres} from one of four values to prescale N_{val} to select the number of clocks of command active time. See the top of this section for a description of the formula.
5–0	CMD_MULT[5-0]	Command Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with N_{pres} to select the number of clocks of command active time. See the top of this section for a description of the formula.

R/W

Programming Notes

R/W

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

R/W

I/O Address 3E0h/3E1h 3Index 7Bh

1

3

0

3

Recovery Timing 2 Register

Index 7Ch

	7	6	5	4	3	2	1	0
Bit	REC_PR	ESC[1-0]	REC_MULT[5-0]					
Default	0	0	0	0	0	0	0	0
R/W	R	/W			R/	W		

Bit	Name	Function
7–6	REC_PRESC[1-0]	Recovery Timing Prescaler Select For this timing set, this field selects N_{pres} from one of four values to prescale N_{val} to select the number of clocks of recovery time (address hold time after the PC Card command goes inactive until the address changes state.) See the top of this section for a description of the formula.
5–0	REC_MULT[5-0]	Recovery Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with N_{pres} to select the number of clocks of recovery time (address hold time after the PC Card command goes inactive until the address changes state.) See the top of this section for a description of the formula.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

7 6 5 4 3 2 1 0 Bit SETUP_PRESC[1-0] SETUP_MULT[5-0] 0 Default 0 0 0 0 0 0 0 R/W R/W R/W Bit Name Function 7-6 SETUP_PRESC[1-0] Setup Timing Prescaler Select For this timing set, this field selects N_{pres} from one of four values to prescale N_{val} to select the number of clocks of setup time from valid address before the PC Card command goes active. See the top of this section for a description of the formula. 5–0 SETUP_MULT[5-0] Setup Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with Npres to select the number of clocks of setup time from valid address before the PC Card command goes active. See the top of this section for a description of the formula.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val}, is combined with the Prescaler Weighting, N_{pres}, to determine the number of clocks to count for the current state (Setup, Command active, or Recovery). The Current State $(S,C, or R) = (N_{pres} \times N_{val}) + 1.$

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

Setup Timing 3 Register

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096
Command Timing 3 Register

	7	6	5	4	3	2	1	0
Bit	СМ	D_PRESC[1-0]			CMD_M	ULT[5–0]		
Default	0	0	0	0	0	1	0	0
R/W		R/W			R	/W		
	Bit	Name	Fund	tion				
	Dit	Name	i unc					
	7–6	CMD_PRESC[1–0] Com	mand Timing	Prescaler S	elect		

7-0		For this timing set, this field selects N_{pres} from one of four values to prescale N_{val} to select the number of clocks of command active time. See the top of this section for a description of the formula.
5–0	CMD_MULT[5-0]	Command Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with N_{pres} to select the number of clocks of command active time. See the top of this section for a description of the formula.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

Recovery Timing 3 Register

	7	6	5	4	3	2	1	0
Bit	REC_PR	ESC[1-0]			REC_MU	JLT[5-0]		
Default	0	0	0	0	0	0	0	0
R/W	R/	W	R/W					

Bit	Name	Function
7–6	REC_PRESC[1-0]	Recovery Timing Prescaler Select For this timing set, this field selects N_{pres} from one of four values to prescale N_{val} to select the number of clocks of recovery time (address hold time after the PC Card command goes inactive until the address changes state.) See the top of this section for a description of the formula.
5–0	REC_MULT[5-0]	Recovery Timing Multiplier Value For this timing set, this field selects N_{val} from 0 to 63 to be multiplied with N_{pres} to select the number of clocks of recovery time (address hold time after the PC Card command goes inactive until the address changes state.) See the top of this section for a description of the formula.

Programming Notes

All register bit descriptions that are shaded deviate from strict 83865SL implementation.

The Multiplier Value, N_{val} , is combined with the Prescaler Weighting, N_{pres} , to determine the number of clocks to count for the current state (**S**etup, **C**ommand active, or **R**ecovery). The Current State (S,C, or R) = ($N_{pres} \times N_{val}$) + 1.

Field Value	Prescaler Weighting
00	N _{pres} =1
01	N _{pres} =16
10	N _{pres} =256
11	N _{pres} =4096

INDEX

Α

Activity Classification Register A (CSC Index 6Ah), 3-79 Activity Classification Register B (CSC Index 6Bh), 3-80 Activity Classification Register C (CSC Index 6Ch), 3-81

Activity Classification Register D (CSC Index 6Dh), 3-82

- Activity Source Enable Register A (CSC Index 62h), 3-71
- Activity Source Enable Register B (CSC Index 63h), 3-72
- Activity Source Enable Register C (CSC Index 64h), 3-73
- Activity Source Enable Register D (CSC Index 65h), 3-74
- Activity Source Status Register A (CSC Index 66h), 3-75
- Activity Source Status Register B (CSC Index 67h), 3-76
- Activity Source Status Register C (CSC Index 68h), 3-77
- Activity Source Status Register D (CSC Index 69h), 3-78
- Address Window Enable Register (PC Card Index 06h/ 46h), 6-15
- Alternate CPU Reset Control Port (Port 00EFh), 2-101
- Alternate Gate A20 Control Port (Port 00EEh), 2-100

В

Battery Low and ACIN SMI/NMI Enable Register (CSC Index 93h), 3-97

Battery Low and ACIN SMI/NMI Status Register (CSC Index 97h), 3-102

- Battery/AC Pin Configuration Register A (CSC Index 70h), 3-83
- Battery/AC Pin Configuration Register B (CSC Index 71h), 3-85
- Battery/AC Pin State Register (CSC Index 72h), 3-86

С

Cache and VL Miscellaneous Register (CSC Index 14h), 3-23

- Card Status Change Interrupt Configuration Register (PC Card Index 05h/45h), 6-13
- Card Status Change Register (PC Card Index 04h/44h), 6-12
- CGA Color Select Register (Port 03D9h), 2-138
- CGA Index Address Register (Port 03D4h), 2-135
- CGA Index Data Port (Port 03D5h), 2-136
- CGA Mode Control Register (Port 03D8h), 2-137
- CGA Status Register (Port 03DAh), 2-139
- CGA/MDA Data Port (Graphics Index 03x5h), 5-5
- CGA/MDA Index Register (Graphics Index 03x4h), 5-4
- Chip Setup and Control (CSC) Index Registers, 3-1
 - Activity Classification Register A (CSC Index 6Ah), 3-79
 - Activity Classification Register B (CSC Index 6Bh), 3-80
 - Activity Classification Register C (CSC Index 6Ch), 3-81
 - Activity Classification Register D (CSC Index 6Dh), 3-82
 - Activity Source Enable Register A (CSC Index 62h), 3-71
 - Activity Source Enable Register B (CSC Index 63h), 3-72
 - Activity Source Enable Register C (CSC Index 64h), 3-73
 - Activity Source Enable Register D (CSC Index 65h), 3-74
 - Activity Source Status Register A (CSC Index 66h), 3-75
 - Activity Source Status Register B (CSC Index 67h), 3-76
 - Activity Source Status Register C (CSC Index 68h), 3-77
 - Activity Source Status Register D (CSC Index 69h), 3-78
 - Battery Low and ACIN SMI/NMI Enable Register (CSC Index 93h), 3-97
 - Battery Low and ACIN SMI/NMI Status Register (CSC Index 97h), 3-102
 - Battery/AC Pin Configuration Register B (CSC Index 71h), 3-85
 - Battery/AC Pin State Register (CSC Index 72h), 3-86
 - Cache and VL Miscellaneous Register (CSC Index 14h), 3-23

CLK IO Pin Output Clock Select Register (CSC Index 83h), 3-91 Clock Control Register (CSC Index 82h), 3-90 CPU Clock Auto Slowdown Register (CSC Index 81h), 3-88 CPU Clock Speed Register (CSC Index 80h), 3-87 DMA Channel 0–3 Extended Page Register (CSC Index D9h), 3-175 DMA Channel 5-7 Extended Page Register (CSC Index DAh), 3-176 DMA Resource Channel Map Register A (CSC Index DBh), 3-177 DMA Resource Channel Map Register B (CSC Index DCh), 3-178 DRAM Bank 0 Configuration (CSC Index 00h), 3-10 DRAM Bank 1 Configuration (CSC Index 01h), 3-11 DRAM Bank 2 Configuration (CSC Index 02h), 3-12 DRAM Bank 3 Configuration (CSC Index 03h), 3-13 DRAM Control Register (CSC Index 04h), 3-14 DRAM Refresh Control Register (CSC Index 05h), 3-16 Drive Strength Control Register A (CSC Index 06h), 3-17 Drive Strength Control Register B (CSC Index 07h), 3-18 ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Data Port (Port 0023h), 2-35, 3-9 ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Index Register (Port 0022h), 2-34, 3-8 Factory Debug Register A (CSC Index 88h), 3-92,, 3-93 GP CS Activity Enable Register (CSC Index 60h), 3-69 GP_CS Activity Status Register (CSC Index 61h), 3-70 GP_CS to GPIO_CS Map Register A (CSC Index B2h), 3-132 GP CS to GPIO CS Map Register B (CSC Index B3h), 3-133 GP_CSA I/O Address Decode and Mask Register (CSC Index B5h), 3-135 GP_CSA I/O Address Decode Register (CSC Index B4h), 3-134 GP CSA/B I/O Command Qualification Register (CSC Index B8h), 3-138 GP CSB I/O Address Decode and Mask Register (CSC Index B7h), 3-137 GP CSB I/O Address Decode Register (CSC Index B6h), 3-136 GP_CSC Memory Address Decode and Mask Register (CSC Index BAh), 3-141 GP_CSC Memory Address Decode Register (CSC Index B9h), 3-140 GP_CSC/D Memory Command Qualification Register (CSC Index BDh), 3-144 GP_CSD Memory Address Decode and Mask

GP_CSD Memory Address Decode Register (CSC Index BBh), 3-142

- GPIO as a Wake-Up or Activity Source Status Register A (CSC Index 5Ah), 3-67
- GPIO as a Wake-Up or Activity Source Status Register B (CSC Index 5Bh), 3-68
- GPIO Function Select Register E (CSC Index A4h), 3-114
- GPIO Function Select Register F (CSC Index A5h), 3-115
- GPIO Read-Back/Write Register A (CSC Index A6h), 3-116
- GPIO Read-Back/Write Register B (CSC Index A7h), 3-117
- GPIO Read-Back/Write Register C (CSC Index A8h), 3-118
- GPIO Read-Back/Write Register D (CSC Index A9h), 3-119
- GPIO Termination Control Register A (CSC Index 3Bh), 3-47
- GPIO Termination Control Register B (CSC Index 3Ch), 3-48
- GPIO Termination Control Register C (CSC Index 3Dh), 3-49
- GPIO Termination Control Register D (CSC Index 3Eh), 3-50
- GPIO_CS Function Select Register A (CSC Index A0h), 3-110
- GPIO_CS Function Select Register B (CSC Index A1h), 3-111
- GPIO_CS Function Select Register C (CSC Index A2h), 3-112
- GPIO_CS Function Select Register D (CSC Index A3h), 3-113
- GPIO_PMU to GPIO_CS Map Register A (CSC Index AEh), 3-128
- GPIO_PMU to GPIO_CS Map Register B (CSC Index AFh), 3-129
- GPIO_PMUA Mode Change Register (CSC Index AAh), 3-120
- GPIO_PMUB Mode Change Register (CSC Index ABh), 3-122
- GPIO_PMUC Mode Change Register (CSC Index ACh), 3-124
- GPIO_XMI to GPIO_CS Map Register (CSC Index B0h), 3-130
- Hyper/High-Speed Mode Timers (CSC Index 42h), 3-54
- I/O Access SMI Status Register A (CSC Index 9Bh), 3-107
- I/O Access SMI Status Register B (CSC Index 9Ch), 3-108
- Internal Graphics Control Register A (CSC Index DDh), 3-179
- Internal Graphics Control Register B (CSC Index DEh), 3-180

Index

Register (CSC Index BCh), 3-143

- Internal I/O Device Disable/Echo Z-Bus Configuration Register (CSC Index D0h), 3-164
- Interrupt Configuration Register A (CSC Index D4h), 3-170
- Interrupt Configuration Register C (CSC Index D6h), 3-172
- Interrupt Configuration Register D (CSC Index D7h), 3-173
- Interrupt Configuration Register E (CSC Index D8h), 3-174
- IrDA Control Register (CSC Index EAh), 3-188
- IrDA CRC Status Register (CSC Index ECh), 3-192
- IrDA Frame Length Register A (CSC Index EEh), 3-194
- IrDA Frame Length Register B (CSC Index EFh), 3-195
- IrDA Own Address Register (CSC Index EDh), 3-193
- IrDA Status Register (CSC Index EBh), 3-190
- Keyboard Column Register (CSC Index C7h), 3-156
- Keyboard Column Termination Control Register (CSC Index CAh), 3-162
- Keyboard Configuration Register A (CSC Index C0h), 3-146
- Keyboard Configuration Register B (Index C1h), 3-149
- Keyboard Input Buffer Read-Back Register (CSC Index C2h), 3-151
- Keyboard Output Buffer Write Register (CSC Index C3h), 3-152
- Keyboard Row Register A (CSC Index C8h), 3-158
- Keyboard Row Register B (CSC Index C9h), 3-160
- Keyboard Status Register Write Register (CSC Index C5h), 3-154
- Keyboard Timer Register (CSC Index C6h), 3-155
- Linear ROMCS0 Attributes Register (CSC Index 22h), 3-28
- Linear ROMCS0/Shadow Register (CSC Index 21h), 3-26
- Low-Speed/Standby Mode Timers Register (CSC Index 43h), 3-55
- Miscellaneous SMI/NMI Enable Register (CSC Index 90h), 3-94
- Miscellaneous SMI/NMI Status Register A (CSC Index 94h), 3-99
- MMS Window A Destination Register (CSC Index 32h), 3-40
- MMS Window A Destination/Attributes Register (CSC Index 33h), 3-41
- MMS Window B Destination Register (CSC Index 34h), 3-42
- MMS Window B Destination/Attributes Register (CSC Index 35h), 3-43
- MMS Window C–F Attributes Register (CSC Index 30h), 3-38

- MMS Window C–F Device Select Register (CSC Index 31h), 3-39
- Mode Timer SMI/NMI Enable Register (CSC Index 92h), 3-96
- Mode Timer SMI/NMI Status Register (CSC Index 96h), 3-101
- Mouse Output Buffer Write Register (CSC Index C3h), 3-153
- Non-Cacheable Window 0 Address Register (CSC Index 10h), 3-19
- Non-Cacheable Window 0 Address/Attributes/SMM Register (CSC Index 11h), 3-20
- Non-Cacheable Window 1 Address Register (CSC Index 12h), 3-21
- Non-Cacheable Window 1 Address/Attributes Register (CSC Index 13h), 3-22
- Overlapping ISA Window Enable Register (CSC Index E0h), 3-181
- Overlapping ISA Window Size Register (CSC Index E2h), 3-183
- Overlapping ISA Window Start Address Register (CSC Index E1h), 3-182
- Parallel Port Configuration Register (CSC Index D2h), 3-168
- Parallel/Serial Port Configuration Register (CSC Index D1h), 3-167
- PC Card and Keyboard SMI/NMI Enable Register (CSC Index 91h), 3-95
- PC Card and Keyboard SMI/NMI Status Register (CSC Index 95h), 3-100
- PC Card Extended Features Register (CSC Index F0h), 3-196
- PC Card Mode and DMA Control Register (CSC Index F1h), 3-198
- PC Card Socket A/B Input Pull-up Control Register (CSC Index F2h), 3-200
- Pin Mux Register A (CSC Index 38h), 3-44
- Pin Mux Register B (CSC Index 39h), 3-45
- Pin Mux Register C (CSC Index 3Ah), 3-46
- Pin Strap Status Register (CSC Index 20h), 3-25
- PMU Force Mode Register (CSC Index 40h), 3-51
- PMU Present and Last Mode Register (CSC Index 41h), 3-53
- ROMCS0 Configuration Register A (CSC Index 23h), 3-29
- ROMCS0 Configuration Register B (CSC Index 24h), 3-31
- ROMCS1 Configuration Register A (CSC Index 25h), 3-32
- ROMCS1 Configuration Register B (CSC Index 26h), 3-34
- ROMCS2 Configuration Register A (CSC Index 27h), 3-35
- ROMCS2 Configuration Register B (CSC Index 28h), 3-37
- SMI/NMI Generation and Status, 3-94

Standard Decode to GPIO_CS Map Register (CSC Index B1h), 3-131

SUS RES Pin Configuration Register (CSC Index 50h), 3-58 Suspend Mode Pin State Override Register (CSC Index E5h), 3-186 Suspend Pin State Register A (CSC Index E3h), 3-184 Suspend Pin State Register B (CSC Index E4h), 3-185 Suspend/Temporary Low-Speed Mode Timers Register (CSC Index 44h), 3-56 UART FIFO Control Shadow Register (CSC Index D3h), 3-169 Wake-Up Pause/High-speed Clock Timers Register (CSC Index 45h), 3-57 Wake-Up Source Enable Register A (CSC Index 52h), 3-59 Wake-Up Source Enable Register B (CSC Index 53h), 3-60 Wake-Up Source Enable Register D (CSC Index 55h), 3-62 Wake-Up Source Status Register A (CSC Index 56h), 3-63 Wake-Up Source Status Register B (CSC Index 57h), 3-64 Wake-Up Source Status Register C (CSC Index 58h), 3-65 Wake-Up Source Status Register D (CSC Index 59h), 3-66 Write-Protected System Memory (DRAM) Window (CSC Index E0h), 3-181 XMI Control Register (CSC Index 9Dh), 3-109 CLK IO Pin Output Clock Select Register (CSC Index 83h), 3-91 Clock Control Register (CSC Index 82h), 3-90 COM1 Baud Clock Divisor Latch Least Significant Bit (Port 03F8h), 2-144 COM1 Baud Clock Divisor Latch Most Significant Bit (Port 03F9h), 2-145 COM1 FIFO Control Register (Port 03FAh), 2-148 COM1 Interrupt Enable Register (Port 03F9h), 2-146 COM1 Interrupt ID Register (Port 03FAh), 2-147 COM1 Line Control Register (Port 03FBh), 2-149 COM1 Line Status Register (Port 03FDh), 2-151 COM1 Modem Control Register (Port 03FCh), 2-150 COM1 Modem Status Register (Port 03FEh), 2-153 COM1 Receive Buffer Register (Port 03F8h), 2-143 COM1 Scratch Pad Register (Port 03FFh), 2-154 COM1 Transmit Holding Register (Port 03F8h), 2-142 COM2 Baud Clock Divisor Latch LSB (Port 02F8h), 2-111 COM2 Baud Clock Divisor Latch MSB (Port 02F9h), 2-112

COM2 FIFO Control Register (Port 02FAh), 2-116

COM2 Interrupt Enable Register (Port 02F9h), 2-113 COM2 Interrupt ID Register (Port 2FAh), 2-114 COM2 Line Control Register (Port 02FBh), 2-117 COM2 Line Status Register (Port 02FDh), 2-119 COM2 Modem Control Register (Port 02FCh), 2-118 COM2 Modem Status Register (Port 02FEh), 2-121 COM2 Receive Buffer Register (Port 02F8h), 2-110 COM2 Scratch Pad Register (Port 02FFh), 2-122 COM2 Transmit Holding Register (Port 02F8h), 2-109 Command Timing 0 Register (PC Card Index 3Bh), 6-56 Command Timing 1 Register (PC Card Index 3Eh), 6-59 Command Timing 2 Register (PC Card Index 7Bh), 6-62 Command Timing 3 Register (PC Card Index 7Eh), 6-65 CPU Clock Auto Slowdown Register (CSC Index 81h), 3-88 CPU Clock Speed Register (CSC Index 80h), 3-87 Cursor Address High Register (Graphics Index 0Eh),

5-10 Cursor Address Low Register (Graphics Index 0Fh),

5-11 Cursor End Register (Graphics Index 0Bh), 5-7

Cursor Start Register (Graphics Index 0Ah), 5-6

D

DMA Channel 0 Page Register (Port 0087h), 2-61

- DMA Channel 0–3 Extended Page Register (CSC Index D9h), 3-175
- DMA Channel 1 Page Register (Port 0083h), 2-57
- DMA Channel 2 Page Register (Port 0081h), 2-55
- DMA Channel 3 Page Register (Port 0082h), 2-56
- DMA Channel 5 Page Register (Port 008Bh), 2-65

DMA Channel 5–7 Extended Page Register (CSC Index DAh), 3-176

DMA Channel 6 Page Register (Port 0089h), 2-63

DMA Channel 7 Page Register (Port 008Ah), 2-64

DMA Resource Channel Map Register A (CSC Index DBh), 3-177

DMA Resource Channel Map Register B (CSC Index DCh), 3-178

- DRAM Bank 0 Configuration (CSC Index 00h), 3-10
- DRAM Bank 1 Configuration (CSC Index 01h), 3-11
- DRAM Bank 2 Configuration (CSC Index 02h), 3-12

DRAM Bank 3 Configuration (CSC Index 03h), 3-13

DRAM Control Register (CSC Index 04h), 3-14

DRAM Refresh Control Register (CSC Index 05h), 3-16 Drive Strength Control Register A (CSC Index 06h),

3-17

- Drive Strength Control Register B (CSC Index 07h), 3-18
- Dual Scan Offset Address High Register (Graphics Index 3Ch), 5-25
- Dual Scan Offset Address Low Register (Graphics Index 3Dh), 5-26
- Dual Scan Row Adjust Register (Graphics Index 3Bh), 5-24

Ε

- ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Data Port (Port 0023h), 2-35, 3-9
- ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Index Register (Port 0022h), 2-34, 3-8
- Extended Feature Control Register (Graphics Index 52h), 5-42

F

- Factory Debug Register A (CSC Index 88h), 3-92,, 3-93 Font Buffer Base Address High Byte (Graphics Index 4Eh), 5-38
- Font Table Register (Graphics Index 42h), 5-31
- Frame Buffer Base Address (Graphics Index 4Dh), 5-37
- Frame Sync Delay Register (Graphics Index 39h), 5-23
- Frame/Font Buffer Base Address Register Low (Graphics Index 4Fh), 5-39

G

- General Purpose CMOS RAM (114 bytes)
 - (Indexes 0Eh-7Fh), 4-15
- General Register (Port 0080h), 2-54
- General Register (Port 0084h), 2-58
- General Register (Port 0085h), 2-59
- General Register (Port 0086h), 2-60
- General Register (Port 0088h), 2-62
- General Register (Port 008Ch), 2-66
- General Register (Port 008Dh), 2-67
- General Register (Port 008Eh), 2-68
- General Register (Port 008Fh), 2-69
- GP_CS Activity Enable Register (CSC Index 60h), 3-69
- GP_CS Activity Status Register (CSC Index 61h), 3-70
- GP_CS to GPIO_CS Map Register A (CSC Index B2h), 3-132
- GP_CS to GPIO_CS Map Register B (CSC Index B3h), 3-133
- GP_CSA I/O Address Decode and Mask Register (CSC Index B5h), 3-135

- GP_CSA I/O Address Decode Register (CSC Index B4h), 3-134
- GP_CSA/B I/O Command Qualification Register (CSC Index B8h), 3-138
- GP_CSB I/O Address Decode and Mask Register (CSC Index B7h), 3-137
- GP_CSB I/O Address Decode Register (CSC Index B6h), 3-136
- GP_CSC Memory Address Decode and Mask Register (CSC Index BAh), 3-141
- GP_CSC Memory Address Decode Register (CSC Index B9h), 3-140
- GP_CSC/D Memory Command Qualification Register (CSC Index BDh), 3-144
- GP_CSD Memory Address Decode and Mask Register (CSC Index BCh), 3-143
- GP_CSD Memory Address Decode Register (CSC Index BBh), 3-142
- GPIO as a Wake-Up or Activity Source Status Register A (CSC Index 5Ah), 3-67
- GPIO Function Select Register E (CSC Index A4h), 3-114
- GPIO Function Select Register F (CSC Index A5h), 3-115
- GPIO Read-Back/Write Register A (CSC Index A6h), 3-116
- GPIO Read-Back/Write Register C (CSC Index A8h), 3-118
- GPIO Termination Control Register A (CSC Index 3Bh), 3-47
- GPIO Termination Control Register B (CSC Index 3Ch), 3-48
- GPIO Termination Control Register C (CSC Index 3Dh), 3-49
- GPIO Termination Control Register D (CSC Index 3Eh), 3-50
- GPIO_CS Function Select Register A (CSC Index A0h), 3-110
- GPIO_CS Function Select Register B (CSC Index A1h), 3-111
- GPIO_CS Function Select Register C (CSC Index A2h), 3-112
- GPIO_CS Function Select Register D (CSC Index A3h), 3-113
- GPIO_PMU to GPIO_CS Map Register A (CSC Index AEh), 3-128
- GPIO_PMU to GPIO_CS Map Register B (CSC Index AFh), 3-129
- GPIO_PMUA Mode Change Register (CSC Index AAh), 3-120

MDZ

GPIO_PMUB Mode Change Register (CSC Index ABh), 3-122
GPIO_PMUC Mode Change Register (CSC Index ACh), 3-124
GPIO_XMI to GPIO_CS Map Register (CSC Index B0h), 3-130
Graphics Controller Grayscale Mode Register (Graphics Index 43h), 5-32
Graphics Controller Grayscale Remapping Register (Graphics Index 44–4Bh), 5-34
Graphics Controller Index Registers
CGA/MDA Data Port (Graphics Index 03x5h), 5-5
CGA/MDA Index Register (Graphics Index 03x4h), 5-4
Cursor Address High Register (Graphics Index 0Eh), 5-10
Cursor Address Low Register (Graphics Index 0Fh), 5-11
Cursor End Register (Graphics Index 0Bh), 5-7
Cursor Start Register (Graphics Index UAn), 5-6
Index 3Ch) 5-25
Dual Scan Offset Address Low Register (Graphics Index 3Dh), 5-26
Dual Scan Row Adjust Register (Graphics Index 3Bh), 5-24
Extended Feature Control Register (Graphics Index 52h), 5-42
Font Buffer Base Address High Byte (Graphics Index 4Eh), 5-38
Font Table Register (Graphics Index 42h), 5-31 Frame Buffer Base Address (Graphics Index 4Dh), 5-37
Frame Sync Delay Register (Graphics Index 39h), 5-23
Frame/Font Buffer Base Address Register Low (Graphics Index 4Fh), 5-39
Graphics Controller Grayscale Mode Register (Graphics Index 43h), 5-32
Graphics Controller Grayscale Remapping Register (Graphics Index 44–4Bh), 5-34
Horizontal Border End Register (Graphics Index 33h), 5-17
Horizontal Display End Register (Graphics Index 31h), 5-15
Horizontal Line Pulse Start Register (Graphics Index 32h), 5-16
Horizontal Lotal Register (Graphics Index 30h), 5-14
41h), 5-30
Light Pen Fligh Register (Read Only) (Graphics Index 10h), 5-12
Index 11h), 5-13

Maximum Scan Line Register (Graphics Index 40h), 5-29

- Non-Display Lines Register (Graphics Index 34h), 5-18
- Offset Register (Graphics Index 3Eh), 5-27
- Overflow Register (Graphics Index 36h), 5-20
- Pixel Clock Control Register (Graphics Index 4Ch), 5-36
- PMU Control Register 1 (Graphics Index 50h), 5-40
- PMU Control Register 2 (Graphics Index 51h), 5-41 Start Address High Register (Graphics Index 0Ch),
- 5-8 Start Address Low Register (Graphics Index 0Dh),
- 5-9
- Underline Location Register (Graphics Index 3Fh), 5-28

Vertical Adjust Register (Graphics Index 35h), 5-19 Vertical Border End Register (Graphics Index 38h), 5-22

Vertical Display End Register (Graphics Index 37h), 5-21

Graphics Controller Register Map, 5-1

н

- HGA Configuration Register (Port 03BFh), 2-134
- Horizontal Border End Register (Graphics Index 33h), 5-17
- Horizontal Display End Register (Graphics Index 31h), 5-15
- Horizontal Line Pulse Start Register (Graphics Index 32h), 5-16
- Hyper/High-Speed Mode Timers (CSC Index 42h), 3-54

- I/O Access SMI Status Register A (CSC Index 9Bh), 3-107
- I/O Access SMI Status Register B (CSC Index 9Ch), 3-108
- I/O Window 0 Start Address High Register (PC Card Index 09h/49h), 6-18
- I/O Window 0 Start Address Low Register (PC Card Index 08h/48h), 6-17
- I/O Window 0 Stop Address High Register (PC Card Index 0Bh/4Bh), 6-20
- I/O Window 0 Stop Address Low Register (PC Card Index 0Ah/4Ah), 6-19
- I/O Window 1 Start Address High Register (PC Card Index 0Dh/4Dh), 6-22
- I/O Window 1 Start Address Low Register (PC Card Index 0Ch/4Ch), 6-21

- I/O Window 1 Stop Address High Register (PC Card Index 0Fh/4Fh), 6-24
- I/O Window 1 Stop Address Low Register (PC Card Index 0Eh/4Eh), 6-23
- I/O Window Control Register (PC Card Index 07h/47h), 6-16
- Identification and Revision Register (PC Card Index 00h/40h), 6-7
- Internal Graphics Control Register A (CSC Index DDh), 3-179
- Internal Graphics Control Register B (CSC Index DEh), 3-180
- Internal I/O Device Disable/Echo Z-Bus Configuration Register (CSC Index D0h), 3-164
- Interrupt and General Control Registers (PC Card Index 03h/43h), 6-11
- Interrupt Configuration Register A (CSC Index D4h), 3-170
- Interrupt Configuration Register C (CSC Index D6h), 3-172
- Interrupt Configuration Register D (CSC Index D7h), 3-173
- Interrupt Configuration Register E (CSC Index D8h), 3-174
- IrDA Control Register (CSC Index EAh), 3-188
- IrDA CRC Status Register (CSC Index ECh), 3-192
- IrDA Frame Length Register A (CSC Index EEh), 3-194
- IrDA Frame Length Register B (CSC Index EFh), 3-195
- IrDA Own Address Register (CSC Index EDh), 3-193
- IrDA Status Register (CSC Index EBh), 3-190

K

- Keyboard Column Register (CSC Index C7h), 3-156 Keyboard Column Termination Control Register
 - (CSC Index CAh), 3-162
- Keyboard Configuration Register A (CSC Index C0h), 3-146
- Keyboard Configuration Register B (CSC Index C1h), 3-149
- Keyboard Input Buffer Read-Back Register (CSC Index C2h), 3-151
- Keyboard Output Buffer Write Register (CSC Index C3h), 3-152
- Keyboard Row Register A (CSC Index C8h), 3-158
- Keyboard Row Register B (CSC Index C9h), 3-160
- Keyboard Status Register Write Register (CSC Index C5h), 3-154
- Keyboard Timer Register (CSC Index C6h), 3-155

- Keyboard/Mouse Interface Command Register (Port 0064h), 2-51
- Keyboard/Mouse Interface Output Buffer (Port 0060h), 2-45

_

- LCD Panel AC Modulation Clock (Graphics Index 41h), 5-30
- Light Pen High Register (Read Only) (Graphics Index 10h), 5-12
- Light Pen Low Register (Read Only) (Graphics Index 11h), 5-13
- Linear ROMCS0 Attributes Register (CSC Index 22h), 3-28
- Linear ROMCS0/Shadow Register (CSC Index 21h), 3-26
- Low-Speed/Standby Mode Timers Register (CSC Index 43h), 3-55

Μ

- Master 8259 Initialization Control Word 1 Register (Port 0020h), 2-27
- Master 8259 Initialization Control Word 2 Register (Port 0021h), 2-30
- Master 8259 Initialization Control Word 3 Register (Port 0021h), 2-31
- Master 8259 Initialization Control Word 4 Register (Port 0021h), 2-32
- Master 8259 In-Service Register (Port 0020h), 2-26
- Master 8259 Interrupt Mask Register (Port 0021h), 2-33
- Master 8259 Interrupt Request Register (Port 0020h), 2-25
- Master 8259 Operation Control Word 2 Register (Port 0020h), 2-28
- Master 8259 Operation Control Word 3 Register (Port 0020h), 2-29
- Master DMA Channel 4 Memory Address Register (Port 00C0h), 2-81
- Master DMA Channel 4 Transfer Count Register (Port 000C2h), 2-82
- Master DMA Channel 5 Memory Address Register (Port 00C4h), 2-83
- Master DMA Channel 5 Transfer Count Register (Port 00C6h), 2-84
- Master DMA Channel 6 Memory Address Register (Port 00C8), 2-85

- Master DMA Channel 6 Transfer Count Register (Port 000CAh), 2-86 Master DMA Channel 7 Memory Address Register (Port 00CCh), 2-87 Master DMA Channel 7 Transfer Count Register (Port 00CEh), 2-88 Master DMA Clear Byte Pointer Register (Port 00D8h), 2-95 Master DMA Control Register for Channels 4-7 (Port 00D0h), 2-90 Master DMA Controller Reset Register (Port 00DAh), 2-96 Master DMA Controller Temporary Register (Port 00DAh), 2-97 Master DMA General Mask Register (Port 00DEh), 2-99 Master DMA Mask Register Channels 4–7 (Port 00D4h), 2-93 Master DMA Mode Register Channels 4–7 (Port 00D6h), 2-94 Master DMA Reset Mask Register (Port 00DCh), 2-98 Master DMA Status Register for Channels 4-7 (Port 00D0h), 2-89 Master Software DRQ(n) Request Register (Port 00D2h), 2-92 Maximum Scan Line Register (Graphics Index 40h), 5-29 MDA/HGA Data Port (Port 03B5h), 2-131 MDA/HGA Index Address Register (Port 03B4h), 2-130 MDA/HGA Mode Control Register (Port 03B8h), 2-132 MDA/HGA Status Register (Port 03BAh), 2-133 Memory Window 0 Address Offset High Register (PC Card Index 15h/55h), 6-30 Memory Window 0 Address Offset Low Register (PC Card Index 14h/54h), 6-29 Memory Window 0 Start Address High Register (PC Card Index 11h/51h), 6-26 Memory Window 0 Start Address Low Register (PC Card Index 10h/50h), 6-25 Memory Window 0 Stop Address High Register (PC Card Index 13h/53h), 6-28 Memory Window 0 Stop Address Low Register (PC Card Index 12h/52h), 6-27 Memory Window 1 Address Offset High Register (PC Card Index 1Dh/5Dh), 6-36 Memory Window 1 Address Offset Low Register (PC Card Index 1Ch/5Ch), 6-35 Memory WIndow 1 Start Address High Register (PC Card Index 19h/59h), 6-32 Memory Window 1 Start Address Low Register (PC Card Index 18h/58h), 6-31
- Memory Window 1 Stop Address High Register (PC Card Index 1Bh/5Bh), 6-34
- Memory Window 1 Stop Address Low Register (PC Card Index 1Ah/5Ah), 6-33
- Memory Window 2 Address Offset High Register (PC Card Index 25h/65h), 6-42
- Memory Window 2 Address Offset Low Register (PC Card Index 24h/64h), 6-41
- Memory Window 2 Start Address High Register (PC Card Index 21h/61h/), 6-38
- Memory Window 2 Start Address Low Register (PC Card Index 20h/60h), 6-37
- Memory Window 2 Stop Address High Register (PC Card Index 23h/63h), 6-40
- Memory Window 2 Stop Address Low Register (PC Card Index 22h/62h), 6-39
- Memory Window 3 Address Offset High Register (PC Card Index 2Dh/6Dh), 6-48
- Memory Window 3 Address Offset Low Register (PC Card Index 2Ch/6Ch), 6-47
- Memory Window 3 Start Address High Register (PC Card Index 29h/69h), 6-44
- Memory Window 3 Start Address Low Register (PC Card Index 28h/68h), 6-43
- Memory Window 3 Stop Address High Register (PC Card Index 2Bh/6Bh), 6-46
- Memory Window 3 Stop Address Low Register (PC Card Index 2Ah/6Ah), 6-45
- Memory Window 4 Address Offset High Register (PC Card Index 35h/75h), 6-54
- Memory Window 4 Address Offset Low Register (PC Card Index 34h/74h), 6-53
- Memory Window 4 Start Address High Register (PC Card Index 31h/71h), 6-50
- Memory Window 4 Start Address Low Register (PC Card Index 30h/70h), 6-49
- Memory Window 4 Stop Address High Register (PC Card Index 33h/73h), 6-52
- Memory Window 4 Stop Address Low Register (PC Card Index 32h/72h), 6-51
- Miscellaneous SMI/NMI Enable Register (CSC Index 90h), 3-94
- Miscellaneous SMI/NMI Status Register A (CSC Index 94h), 3-99
- MMS Window A Destination Register (CSC Index 32h), 3-40
- MMS Window A Destination/Attributes Register (CSC Index 33h), 3-41
- MMS Window B Destination Register (CSC Index 34h), 3-42

- MMS Window B Destination/Attributes Register (CSC Index 35h), 3-43
- MMS Window C-F Attributes Register (CSC Index 30h), 3-38
- MMS Window C–F Device Select Register (CSC Index 31h), 3-39
- Mode Timer SMI/NMI Enable Register (CSC Index 92h), 3-96
- Mode Timer SMI/NMI Status Register (CSC Index 96h), 3-101
- Mouse Output Buffer Write Register (CSC Index C3h), 3-153

Ν

- Non-Cacheable Window 0 Address Register (CSC Index 10h), 3-19
- Non-Cacheable Window 0 Address/Attributes/SMM Register (CSC Index 11h), 3-20
- Non-Cacheable Window 1 Address Register (CSC Index 12h), 3-21
- Non-Display Lines Register (Graphics Index 34h), 5-18

0

- Offset Register (Graphics Index 3Eh), 5-27
- Horizontal Total Register (Graphics Index 30h), 5-14
- Overflow Register (Graphics Index 36h), 5-20
- Overlapping ISA Window Enable Register (CSC Index E0h), 3-181
- Overlapping ISA Window Size Register (CSC Index E2h), 3-183
- Overlapping ISA Window Start Address Register (CSC Index E1h), 3-182

Ρ

- Parallel Port 1 Control Register (Port 037Ah), 2-127
- Parallel Port 1 Data Register (Port 0378h), 2-123
- Parallel Port 1 EPP 32-bit Data Register (Ports 037C–037Fh), 2-129
- Parallel Port 1 EPP Address Register (Port 037Bh), 2-128
- Parallel Port 1 Status Register (Bidirectional Mode) (Port 0379h), 2-125
- Parallel Port 1 Status Register (EPP Mode) (Port 0379h), 2-126
- Parallel Port 1 Status Register (Port 0379h), 2-124
- Parallel Port 2 Control Register (Port 027A), 2-106
- Parallel Port 2 Data Register (Port 0278h), 2-102

- Parallel Port 2 EPP 32-bit Data Register (Ports 027C–027Fh), 2-108
- Parallel Port 2 EPP Address Register (Port 027B), 2-107
- Parallel Port 2 Status Register (Bidirectional Mode) (Port 0279h), 2-104
- Parallel Port 2 Status Register (EPP Mode) (Port 0279h), 2-105
- Parallel Port 2 Status Register (Port 0279h), 2-103
- Parallel Port Configuration Register (CSC Index D2h), 3-168
- Parallel/Serial Port Configuration Register (CSC Index D1h), 3-167
- PC Card and Keyboard SMI/NMI Enable Register (CSC Index 91h), 3-95
- PC Card and Keyboard SMI/NMI Status Register (CSC Index 95h), 3-100
- PC Card Controller Index Registers
 - Address Window Enable Register (PC Card Index 06h/46h), 6-15
 - Card Status Change Interrupt Configuration Register (PC Card Index 05h/45h), 6-13
 - Card Status Change Register (PC Card Index 04h/ 44h), 6-12
 - Command Timing 0 Register (PC Card Index 3Bh), 6-56
 - Command Timing 1 Register (PC Card Index 3Eh), 6-59
 - Command Timing 2 Register (PC Card Index 7Bh), 6-62
 - Command Timing 3 Register (PC Card Index 7Eh), 6-65
 - I/O Window 0 Start Address High Register (PC Card Index 09h/49h), 6-18
 - I/O Window 0 Start Address Low Register (PC Card Index 08h/48h), 6-17
 - I/O Window 0 Stop Address High Register (PC Card Index 0Bh/4Bh), 6-20
 - I/O Window 0 Stop Address Low Register (PC Card Index 0Ah/4Ah), 6-19
 - I/O Window 1 Start Address High Register (PC Card Index 0Dh/4Dh), 6-22
 - I/O Window 1 Start Address Low Register (PC Card Index 0Ch/4Ch), 6-21
 - I/O Window 1 Stop Address High Register (PC Card Index 0Fh/4Fh), 6-24
 - I/O Window 1 Stop Address Low Register (PC Card Index 0Eh/4Eh), 6-23
 - I/O Window Control Register (PC Card Index 07h/ 47h), 6-16
 - Identification and Revision Register (PC Card Index 00h/40h), 6-7
 - Interface Status Register (PC Card Index 01h/41h), 6-8

Interrupt and General Control Registers (PC Card Index 03h/43h), 6-11

Memory Window 0 Address Offset High Register (PC Card Index 15h/55h), 6-30

Memory Window 0 Address Offset Low Register (PC Card Index 14h/54h), 6-29

Memory Window 0 Start Address High Register (PC Card Index 11h/51h), 6-26

Memory Window 0 Start Address Low Register (PC Card Index 10h/50h), 6-25

Memory Window 0 Stop Address High Register (PC Card Index 13h/53h), 6-28

Memory Window 0 Stop Address Low Register (PC Card Index 12h/52h), 6-27

Memory Window 1 Address Offset High Register (PC Card Index 1Dh/5Dh), 6-36

Memory Window 1 Address Offset Low Register (PC Card Index 1Ch/5Ch), 6-35

Memory WIndow 1 Start Address High Register (PC Card Index 19h/59h), 6-32

Memory Window 1 Start Address Low Register (PC Card Index 18h/58h), 6-31

Memory Window 1 Stop Address High Register (PC Card Index 1Bh/5Bh), 6-34

Memory Window 1 Stop Address Low Register (PC Card Index 1Ah/5Ah), 6-33

Memory Window 2 Address Offset High Register (PC Card Index 25h/65h), 6-42

Memory Window 2 Address Offset Low Register (PC Card Index 24h/64h), 6-41

Memory Window 2 Start Address High Register (PC Card Index 21h/61h/), 6-38

Memory Window 2 Start Address Low Register (PC Card Index 20h/60h), 6-37

Memory Window 2 Stop Address High Register (PC Card Index 23h/63h), 6-40

Memory Window 2 Stop Address Low Register (PC Card Index 22h/62h), 6-39

Memory Window 3 Address Offset High Register (PC Card Index 2Dh/6Dh), 6-48

Memory Window 3 Address Offset Low Register (PC Card Index 2Ch/6Ch), 6-47

Memory Window 3 Start Address High Register (PC Card Index 29h/69h), 6-44

Memory Window 3 Start Address Low Register (PC Card Index 28h/68h), 6-43

Memory Window 3 Stop Address High Register (PC Card Index 2Bh/6Bh), 6-46

Memory Window 3 Stop Address Low Register (PC Card Index 2Ah/6Ah), 6-45

Memory Window 4 Address Offset High Register (PC Card Index 35h/75h), 6-54

Memory Window 4 Address Offset Low Register (PC Card Index 34h/74h), 6-53

Memory Window 4 Start Address High Register (PC Card Index 31h/71h), 6-50

Memory Window 4 Start Address Low Register (PC Card Index 30h/70h), 6-49 Memory Window 4 Stop Address High Register (PC Card Index 33h/73h), 6-52

Memory Window 4 Stop Address Low Register (PC Card Index 32h/72h), 6-51

Power and RESETDRV Control Register (PC Card Index 02h/42h), 6-9

Primary 82365-Compatible PC Card Controller Data Port (Port 03E1h), 6-6

Primary 82365-Compatible PC Card Controller Index Register (Port 03E0h), 6-5

Recovery Timing 0 Register (PC Card Index 3Ch), 6-57

Recovery Timing 1 Register (PC Card Index 3Fh), 6-60

Recovery Timing 2 Register (PC Card Index 7Ch), 6-63

Recovery Timing 3 Register (PC Card Index 7Fh), 6-66

Setup Timing 0 Register (PC Card Index 3Ah), 6-55 Setup Timing 1 Register (PC Card Index 3Dh), 6-58 Setup Timing 2 Register (PC Card Index 7Ah), 6-61 Setup Timing 3 Register (PC Card Index 7Dh), 6-64

PC Card Controller Register Map, 6-1

PC Card Extended Features Register (CSC Index F0h), 3-196

PC Card Mode and DMA Control Register (CSC Index F1h), 3-198

PC Card Socket A/B Input Pull-Up Control Register (CSC Index F2h), 3-200

PC/AT Keyboard Interface Data Register (Port 0060h), 2-46

PC/AT Keyboard/Mouse Interface Status Register (Port 0064h), 2-49

PC/AT-Compatible Direct-Mapped Register Map, 2-1

PC/AT-Compatible Direct-Mapped Registers, 2-1

Alternate CPU Reset Control Port (Port 00EFh), 2-101

Alternate Gate A20 Control Port (Port 00EEh), 2-100

CGA Color Select Register (Port 03D9h), 2-138

CGA Index Address Register (Port 03D4h), 2-135

CGA Index Data Port (Port 03D5h), 2-136

CGA Mode Control Register (Port 03D8h), 2-137

CGA Status Register (Port 03DAh), 2-139

COM1 Baud Clock Divisor Latch Least Significant Bit (Port 03F8h), 2-144

COM1 Baud Clock Divisor Latch Most Significant Bit (Port 03F9h), 2-145

COM1 FIFO Control Register (Port 03FAh), 2-148

COM1 Interrupt Enable Register (Port 03F9h), 2-146

COM1 Interrupt ID Register (Port 03FAh), 2-147

COM1 Line Control Register (Port 03FBh), 2-149

COM1 Line Status Register (Port 03FDh), 2-151

COM1 Modem Control Register (Port 03FCh), 2-150

COM1 Modem Status Register (Port 03FEh), 2-153 COM1 Receive Buffer Register (Port 03F8h), 2-143 COM1 Scratch Pad Register (Port 03FFh), 2-154 COM1 Transmit Holding Register (Port 03F8h), 2-142 COM2 Baud Clock Divisor Latch LSB (Port 02F8h), 2-111 COM2 Baud Clock Divisor Latch MSB (Port 02F9h), 2-112 COM2 FIFO Control Register (Port 02FAh), 2-116 COM2 Interrupt Enable Register (Port 02F9h), 2-113 COM2 Interrupt ID Register (Port 2FAh), 2-114 COM2 Line Control Register (Port 02FBh), 2-117 COM2 Line Status Register (Port 02FDh), 2-119 COM2 Modem Control Register (Port 02FCh), 2-118 COM2 Modem Status Register (Port 02FEh), 2-121 COM2 Receive Buffer Register (Port 02F8h), 2-110 COM2 Scratch Pad Register (Port 02FFh), 2-122 COM2 Transmit Holding Register (Port 02F8h), 2-109 DMA Channel 0 Page Register (Port 0087h), 2-61 DMA Channel 1 Page Register (Port 0083h), 2-57 DMA Channel 2 Page Register (Port 0081h), 2-55 DMA Channel 3 Page Register (Port 0082h), 2-56 DMA Channel 5 Page Register (Port 008Bh), 2-65 DMA Channel 6 Page Register (Port 0089h), 2-63 DMA Channel 7 Page Register (Port 008Ah), 2-64 ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Data Port (Port 0023h), 2-35 ÉlanSC400 Microcontroller Chip Setup and Control (CSC) Index Register (Port 0022h), 2-34 General Register (Port 0080h), 2-54 General Register (Port 0084h), 2-58 General Register (Port 0085h), 2-59 General Register (Port 0086h), 2-60 General Register (Port 0088h), 2-62 General Register (Port 008Ch), 2-66 General Register (Port 008Dh), 2-67 General Register (Port 008Eh), 2-68 General Register (Port 008Fh), 2-69 HGA Configuration Register (Port 03BFh), 2-134 Keyboard/Mouse Interface Command Register (Port 0064h), 2-51 Keyboard/Mouse Interface Output Buffer (Port 0060h), 2-45 Master 8259 Initialization Control Word 1 Register (Port 0020h), 2-27 Master 8259 Initialization Control Word 2 Register (Port 0021h), 2-30 Master 8259 Initialization Control Word 3 Register (Port 0021h), 2-31 Master 8259 Initialization Control Word 4 Register (Port 0021h), 2-32 Master 8259 In-Service Register (Port 0020h), 2-26 Master 8259 Interrupt Mask Register (Port 0021h), 2-33

Master 8259 Interrupt Request Register (Port 0020h), 2-25

- Master 8259 Operation Control Word 2 Register (Port 0020h), 2-28
- Master 8259 Operation Control Word 3 Register (Port 0020h), 2-29
- Master DMA Channel 4 Memory Address Register (Port 00C0h), 2-81
- Master DMA Channel 4 Transfer Count Register (Port 000C2h), 2-82
- Master DMA Channel 5 Memory Address Register (Port 00C4h), 2-83
- Master DMA Channel 5 Transfer Count Register (Port 00C6h), 2-84
- Master DMA Channel 6 Memory Address Register (Port 00C8), 2-85
- Master DMA Channel 6 Transfer Count Register (Port 000CAh), 2-86
- Master DMA Channel 7 Memory Address Register (Port 00CCh), 2-87
- Master DMA Channel 7 Transfer Count Register (Port 00CEh), 2-88
- Master DMA Clear Byte Pointer Register (Port 00D8h), 2-95
- Master DMA Control Register for Channels 4–7 (Port 00D0h), 2-90
- Master DMA Controller Reset Register (Port 00DAh), 2-96
- Master DMA Controller Temporary Register (Port 00DAh), 2-97
- Master DMA General Mask Register (Port 00DEh), 2-99
- Master DMA Mask Register Channels 4–7 (Port 00D4h), 2-93
- Master DMA Mode Register Channels 4–7 (Port 00D6h), 2-94
- Master DMA Reset Mask Register (Port 00DCh), 2-98
- Master DMA Status Register for Channels 4–7 (Port 00D0h), 2-89
- Master Software DRQ(n) Request Register (Port 00D2h), 2-92
- MDA/HGA Data Port (Port 03B5h), 2-131
- MDA/HGA Index Address Register (Port 03B4h), 2-130
- MDA/HGA Mode Control Register (Port 03B8h), 2-132
- MDA/HGA Status Register (Port 03BAh), 2-133
- Parallel Port 1 Control Register (Port 037Ah), 2-127
- Parallel Port 1 Data Register (Port 0378h), 2-123 Parallel Port 1 EPP 32-bit Data Register

(Ports 037C-037Fh), 2-129

- Parallel Port 1 EPP Address Register (Port 037Bh), 2-128
- Parallel Port 1 Status Register (Bidirectional Mode) (Port 0379h), 2-125
- Parallel Port 1 Status Register (EPP Mode) (Port 0379h), 2-126

Parallel Port 1 Status Register (Port 0379h), 2-124 Parallel Port 2 Control Register (Port 027A), 2-106 Parallel Port 2 Data Register (Port 0278h), 2-102 Parallel Port 2 EPP 32-bit Data Register (Ports 027C-027Fh), 2-108 Parallel Port 2 EPP Address Register (Port 027B), 2-107 Parallel Port 2 Status Register (Bidirectional Mode) (Port 0279h), 2-104 Parallel Port 2 Status Register (EPP Mode) (Port 0279h), 2-105 Parallel Port 2 Status Register (Port 0279h), 2-103 PC/AT Keyboard Interface Data Register (Port 0060h), 2-46 PC/AT Keyboard/Mouse Interface Status Register (Port 0064h), 2-49 PC/XT Keyboard Data Register (Port 0060h), 2-47 Primary 82365-Compatible PC Card Controller Data Port (Port 03E1h), 2-141 Primary 82365-Compatible PC Card Controller Index Register (Port 03E0h), 2-140 Programmable Interval Timer #1 Channel 0 Count Register (Port 0040h), 2-36 Programmable Interval Timer #1 Channel 1 Count Register (Refresh Timer) (Port 0041h), 2-37 Programmable Interval Timer #1 Channel 2 Count Register (Speaker Timer) (Port 0042h), 2-38 Programmable Interval Timer #1 Counter Latch Command Register (Port 0043h), 2-43 Programmable Interval Timer #1 Mode Control Register (Port 0043h), 2-41 Programmable Interval Timer #1 Read-Back Command Register (Port 0043h), 2-44 Programmable Interval Timer #1 Status Register (Ports 0040-0042h), 2-39 RTC/CMOS RAM Data Port (Port 0071h), 2-53 RTC/CMOS RAM Index Register (Port 0070h), 2-52 Slave 8259 Initialization Control Word 1 Register (Port 00A0h), 2-73 Slave 8259 Initialization Control Word 2 Register (Port 00A1h), 2-77 Slave 8259 Initialization Control Word 3 Register (Port 00A1h), 2-78 Slave 8259 Initialization Control Word 4 Register (Port 00A1h), 2-79 Slave 8259 In-Service Register (Port 00A0h), 2-72 Slave 8259 Interrupt Mask Register (Port 00A1h), 2 - 80Slave 8259 Interrupt Request Register (Port 00A0h), 2-71 Slave 8259 Operation Control Word 2 Register (Port 00A0h), 2-75 Slave 8259 Operation Control Word 3 Register (Port 00A0h), 2-76

- Slave DMA Channel 0 Memory Address Register (Port 0000h), 2-6
- Slave DMA Channel 0 Transfer Count Register (Port 0001h), 2-7
- Slave DMA Channel 1 Memory Address Register (Port 0002h), 2-8
- Slave DMA Channel 1 Transfer Count Register (Port 0003h), 2-9
- Slave DMA Channel 2 Memory Address Register (Port 0004h), 2-10
- Slave DMA Channel 2 Transfer Count Register (Port 0005h), 2-11
- Slave DMA Channel 3 Memory Address Register (Port 0006h), 2-12
- Slave DMA Channel 3 Transfer Count Register (Port 0007h), 2-13
- Slave DMA Clear Byte Pointer Register (Port 000Ch), 2-20
- Slave DMA Control Register for Channels 0–3 (Port 0008h), 2-15
- Slave DMA Controller Reset Register (Port 000Dh), 2-21
- Slave DMA Controller Temporary Register (Port 000Dh), 2-22
- Slave DMA General Mask Register (Port 000Fh), 2-24
- Slave DMA Mask Register Channels 0–3 (Port 000Ah), 2-18
- Slave DMA Mode Register Channels 0–3 (Port 000Bh), 2-19
- Slave DMA Reset Mask Register (Port 000Eh), 2-23
- Slave DMA Status Register for Channels 0–3 (Port 0008h), 2-14
- Slave Software DRQ(n) Request Register (Port 0009h), 2-17
- System Control Port A Register (Port 0092h), 2-70
- System Control Port A Register (PS/2 Compatibility Port) (Port 0092h), 2-70
- System Control Port B/NMI Status Register (Port 0061h), 2-48
- PC/XT Keyboard Data Register (Port 0060h), 2-47
- Pin Mux Register A (CSC Index 38h), 3-44
- Pin Mux Register B (CSC Index 39h), 3-45
- Pin Mux Register C (CSC Index 3Ah), 3-46
- Pin Strap Status Register (CSC Index 20h), 3-25
- PIO as a Wake-Up or Activity Source Status Register B (CSC Index 5Bh), 3-68
- PIO Read-Back/Write Register B (CSC Index A7h), 3-117
- PIO Read-Back/Write Register D (CSC Index A9h), 3-119

Pixel Clock Control Register (Graphics Index 4Ch), 5-36

PMU Control Register 1 (Graphics Index 50h), 5-40

PMU Control Register 2 (Graphics Index 51h), 5-41

- PMU Force Mode Register (CSC Index 40h), 3-51
- PMU Present and Last Mode Register (CSC Index 41h), 3-53
- Power and RESETDRV Control Register (PC Card Index 02h/42h), 6-9
- Primary 82365-Compatible PC Card Controller Data Port (Port 03E1h), 2-141,, 6-6
- Primary 82365-Compatible PC Card Controller Index Register (Port 03E0h), 2-140,, 6-5
- Programmable Interval Timer #1 Channel 0 Count Register (Port 0040h), 2-36
- Programmable Interval Timer #1 Channel 1 Count Register (Refresh Timer) (Port 0041h), 2-37
- Programmable Interval Timer #1 Channel 2 Count Register (Speaker Timer) (Port 0042h), 2-38
- Programmable Interval Timer #1 Counter Latch Command Register (Port 0043h), 2-43
- Programmable Interval Timer #1 Mode Control Register (Port 0043h), 2-41
- Programmable Interval Timer #1 Read-Back Command Register (Port 0043h), 2-44
- Programmable Interval Timer #1 Status Register (Ports 0040–0042h), 2-39

R

- Recovery Timing 0 Register (PC Card Index 3Ch), 6-57
- Recovery Timing 1 Register (PC Card Index 3Fh), 6-60
- Recovery Timing 2 Register (PC Card Index 7Ch), 6-63
- Recovery Timing 3 Register (PC Card Index 7Fh), 6-66
- Register A (RTC Index 0Ah), 4-16
- Register B (RTC Index 0Bh), 4-18
- Register C (RTC Index 0Ch), 4-19
- Register D (RTC Index 0Dh), 4-20

Registers

- Interface Status Register (PC Card Index 01h/41h), 6-8
- ROMCS0 Configuration Register A (CSC Index 23h), 3-29
- ROMCS0 Configuration Register B (CSC Index 24h), 3-31
- ROMCS1 Configuration Register A (CSC Index 25h), 3-32
- ROMCS1 Configuration Register B (CSC Index 26h), 3-34
- ROMCS2 Configuration Register A (CSC Index 27h), 3-35
- ROMCS2 Configuration Register B (CSC Index 28h), 3-37
- RTC Alarm Hour Register (RTC Index 05h), 4-10

- RTC Alarm Minute Register (Index 03h), 4-8
- RTC Alarm Second Register (RTC Index 01h), 4-6
- RTC and CMOS RAM Index Registers
 - General Purpose CMOS RAM (114 bytes) (RTC Indexes 0Eh-7Fh), 4-15
 - Register A (RTC Index 0Ah), 4-16
 - Register B (RTC Index 0Bh), 4-18
 - Register C (RTC Index 0Ch), 4-19
 - Register D (RTC Index 0Dh), 4-20
 - RTC Alarm Hour Register (RTC Index 05h), 4-10
 - RTC Alarm Minute Register (Index 03h), 4-8
 - RTC Alarm Second Register (RTC Index 01h), 4-6
 - RTC Current Date of the Month Register (RTC Index 07h), 4-11
 - RTC Current Day of the Week Register (RTC Index 06h), 4-10
 - RTC Current Hour Register (RTC Index 04h), 4-9
 - RTC Current Minute Register (RTC Index 02h), 4-7
 - RTC Current Month Register (RTC Index 08h), 4-12
 - RTC Current Second Register (RTC Index 00h), 4-5

RTC Current Year Register (RTC Index 09h), 4-13 RTC/CMOS RAM Data Port (Port 0071h), 4-4

RTC/CMOS RAM Index Register Port 0070h), 4-3

- RTC and Configuration RAM Register Map, 4-1
- RTC Current Date of the Month Register (RTC Index 07h), 4-11
- RTC Current Day of the Week Register (RTC Index 06h), 4-10
- RTC Current Hour Register (RTC Index 04h), 4-9
- RTC Current Minute Register (RTC Index 02h), 4-7
- RTC Current Month Register (RTC Index 08h), 4-12
- RTC Current Second Register (RTC Index 00h), 4-5
- RTC Current Year Register (RTC Index 09h), 4-13
- RTC/CMOS RAM Data Port (Port 0071h), 2-53, 4-4
- RTC/CMOS RAM Index Register (Port 0070h), 2-52, 4-3

S

Setup Timing 0 Register (PC Card Index 3Ah), 6-55

Setup Timing 1 Register (PC Card Index 3Dh), 6-58

Setup Timing 2 Register (PC Card Index 7Ah), 6-61

Setup Timing 3 Register (PC Card Index 7Dh), 6-64

- Slave 8259 Initialization Control Word 1 Register (Port 00A0h), 2-73
- Slave 8259 Initialization Control Word 2 Register (Port 00A1h), 2-77

Slave 8259 Initialization Control Word 3 Register (Port 00A1h), 2-78

Slave 8259 Initialization Control Word 4 Register (Port 00A1h), 2-79

Slave 8259 In-Service Register (Port 00A0h), 2-72 Slave 8259 Interrupt Mask Register (Port 00A1h), 2-80 Slave 8259 Interrupt Request Register (Port 00A0h), 2-71 Slave 8259 Operation Control Word 2 Register (Port 00A0h), 2-75 Slave 8259 Operation Control Word 3 Register (Port 00A0h), 2-76 Slave DMA Channel 0 Memory Address Register (Port 0000h), 2-6 Slave DMA Channel 0 Transfer Count Register (Port 0001h), 2-7 Slave DMA Channel 1 Memory Address Register (Port 0002h), 2-8 Slave DMA Channel 1 Transfer Count Register (Port 0003h), 2-9 Slave DMA Channel 2 Memory Address Register (Port 0004h), 2-10 Slave DMA Channel 2 Transfer Count Register (Port 0005h), 2-11 Slave DMA Channel 3 Memory Address Register (Port 0006h), 2-12 Slave DMA Channel 3 Transfer Count Register (Port 0007h), 2-13 Slave DMA Clear Byte Pointer Register (Port 000Ch), 2-20 Slave DMA Control Register for Channels 0-3 (Port 0008h), 2-15 Slave DMA Controller Reset Register (Port 000Dh), 2-21 Slave DMA Controller Temporary Register (Port 000Dh), 2-22 Slave DMA General Mask Register (Port 000Fh), 2-24 Slave DMA Mask Register Channels 0-3 (Port 000Ah), 2-18 Slave DMA Mode Register Channels 0-3 (Port 000Bh), 2-19 Slave DMA Reset Mask Register (Port 000Eh), 2-23 Slave DMA Status Register for Channels 0-3 (Port 0008h), 2-14 Slave Software DRQ(n) Request Register (Port 0009h), 2-17 Standard Decode to GPIO CS Map Register (CSC Index B1h), 3-131 Start Address High Register (Graphics Index 0Ch), 5-8 Start Address Low Register (Graphics Index 0Dh), 5-9 SUS_RES Pin Configuration Register (CSC Index 50h), 3-58 Suspend Mode Pin State Override Register (CSC Index E5h), 3-186 Suspend Pin State Register A (CSC Index E3h), 3-184

Suspend Pin State Register B (CSC Index E4h), 3-185 Suspend/Temporary Low-Speed Mode Timers Register (CSC Index 44h), 3-56

System Control Port A Register (Port 0092h), 2-70

System Control Port A Register (PS/2 Compatibility Port) (Port 0092h), 2-70

U

- UART FIFO Control Shadow Register (CSC Index D3h), 3-169
- Underline Location Register (Graphics Index 3Fh), 5-28

V

Vertical Adjust Register (Graphics Index 35h), 5-19

- Vertical Border End Register (Graphics Index 38h), 5-22
- Vertical Display End Register (Graphics Index 37h), 5-21

W

- Wake-Up Pause/High-Speed Clock Timers Register (CSC Index 45h), 3-57
- Wake-Up Source Enable Register A (CSC Index 52h), 3-59
- Wake-Up Source Enable Register B (CSC Index 53h), 3-60
- Wake-Up Source Enable Register D (CSC Index 55h), 3-62
- Wake-Up Source Status Register A (CSC Index 56h), 3-63
- Wake-Up Source Status Register B (CSC Index 57h), 3-64
- Wake-Up Source Status Register C (CSC Index 58h), 3-65
- Wake-Up Source Status Register D (CSC Index 59h), 3-66
- Write-Protected System Memory (DRAM) Window (CSC Index E0h), 3-181

X

XMI Control Register (CSC Index 9Dh), 3-109

System Control Port B/NMI Status Register (Port 0061h), 2-48