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uforCE

Elan SC400 - Windows CE Demonstration Board Schematic


Rev 1.0: Original design

- Rev 1.1:**
- Sh. 3 Removed "no populate" designator from JP1.
 - Sh. 4 Added TP to ROMCS0#.
 - Sh. 5 Removed "no populate" designator from U6
 - Sh. 5 Added RSTA A2 errata work-around.
 - Sh. 7 Swapped nets TABXNEG & TABYPOS at J1.
 - Swapped nets LCDD0-LCDD3 at J2.
 - Changed P/N for J1 & J2.
 - Changed value of R43 (DISP_ON) & connected to LVEE
 - Sh. 10 Added 2M resistor from U21 pin 19 to VSOURCE.
 - Sh. 11 Added 2M resistor from U23 pin 19 to VSOURCE.
 - Sh. 14 Corrected BATTEMP circuit.
 - Changed values of R118-R120 for FSTCHRG#.
 - Sh. 15 Changed comparator bias voltage for VCC switch to Vbias

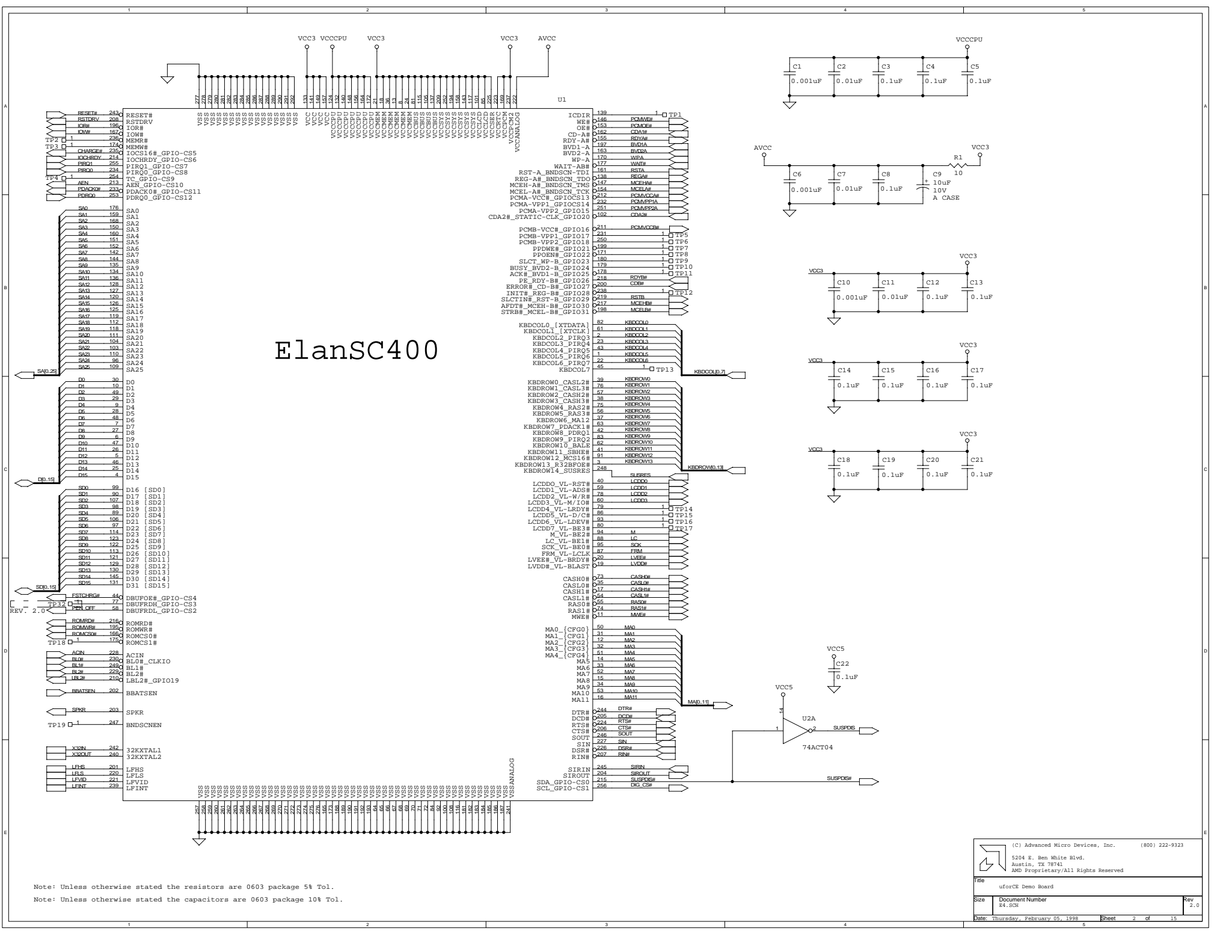
- Rev 2.0:**
- Sh. 2 Removed BATTEMP signal from GPIO-CS3 pin
 - Sh. 3 JP1 changed to 2mm spacing
 - Sh. 5 JP2 added for PCMCIA booting
 - Sh. 6 TC7SH32FU added to level shift SIRIN signal
 - U38D added to unused gates
 - Added GND to U14-9 and U14-10
 - Sh. 7 Added circuit to slow turn-on of LCD
 - TC7SH32FU added to level shift PEN_OFF signal
 - Sh. 8 R56 changed to 3.3K pull-up
 - R144 added to pull-up IOCHRDY signal
 - Filter circuit added to SPKR signal for noise suppression
 - Sh. 10 LDO regulator circuit changed to 2.85V nominal
 - Changed control of U21 PWM* mode
 - U21-9 connected to Vsourc
 - U21 output capacitor increased; added bypass capacitor
 - Sh. 11 Changed control of U23 PWM* mode
 - U23-9 connected to Vsourc
 - Added bypass capacitor to U23
 - Changed D5 to no-populate
 - Sh. 12 Changed enable for U24 to PCMVPP2A signal
 - Changed U24-8 to no-connect to cut output current
 - Slow-start circuit added to slow ramp-up of P12VOLT
 - Sh. 13 Increased L8; decreased C146 on U25 output
 - Slow-start circuit added to slow ramp-up of LCDVEE
 - Changed U25-8 to no-connect to cut output current
 - Sh. 14 U27 changed to MIC4576 for increased output current
 - Charger circuit changed to use MC33340 controller chip
 - for Fast/Trickle charge control and battery overtemperature shutoff
 - Added LED to indicate charge mode
 - Charge currents changed to 1.25A/25mA nominal
 - Changed software controls for charger circuitry to FASTCHG# and CHARGE# signals
 - Sh. 15 Changed Vbatt/12VDC switch circuit to use SI4435DY
 - and power U37 from Vsourc
 - Added current limit circuit to 12VDC
 - Modified Vbatt/12VDC switch circuit to work with MC33340
 - Adjusted BLx# sensors for 4.6V, 4.8V, 5.0V nominal
 - Removed BATTEMP circuit
 - R124 reduced to 1M for increased hysteresis
 - R128, R129, R137 increased to 5.1M for reduced hysteresis

LPD - Logic Products Division

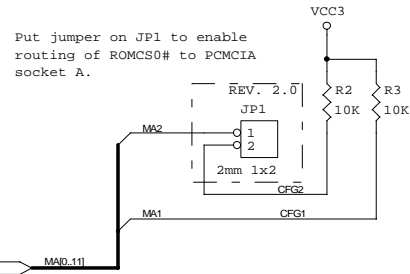
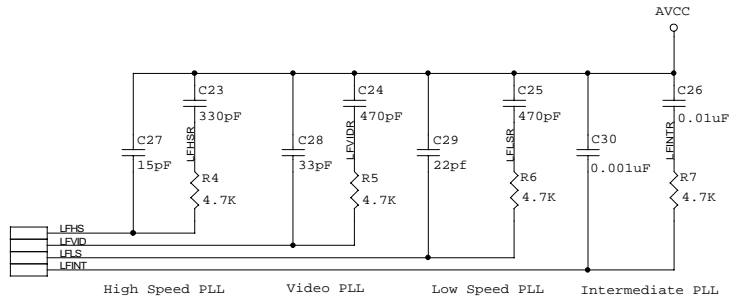
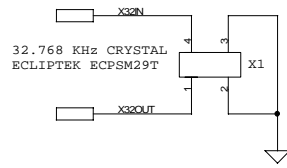
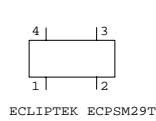


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| Title | | uforCE Demo Board |
| Size | Document Number | Rev |
| | uforCE.SCH | 2.0 |
| Date: Tuesday, October 14, 1997 | | Sheet 1 of 15 |

ElanSC400



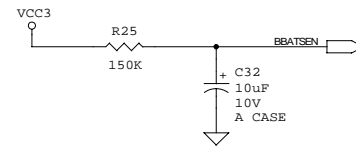
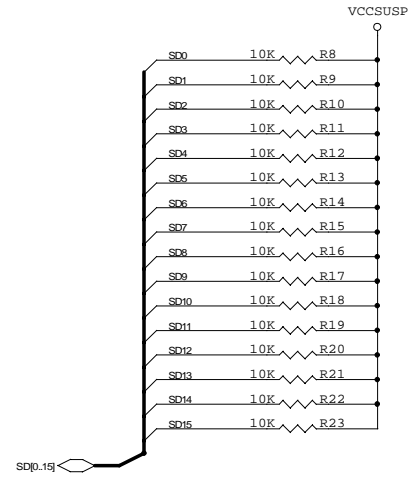
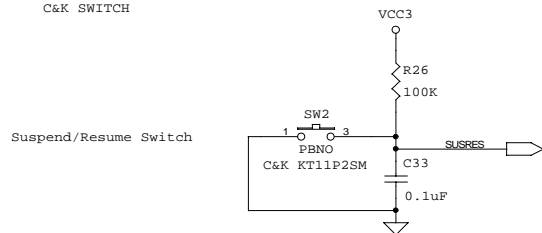
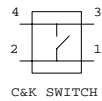
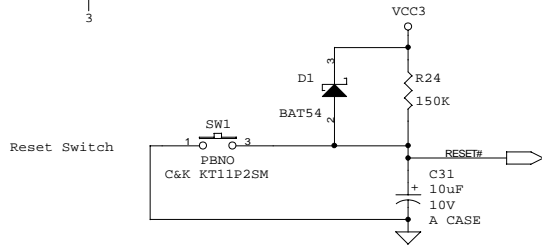
Note: Unless otherwise stated the resistors are 0603 package 5% Tol.
 Note: Unless otherwise stated the capacitors are 0603 package 10% Tol.



H2 PIN STRAP OPTIONS

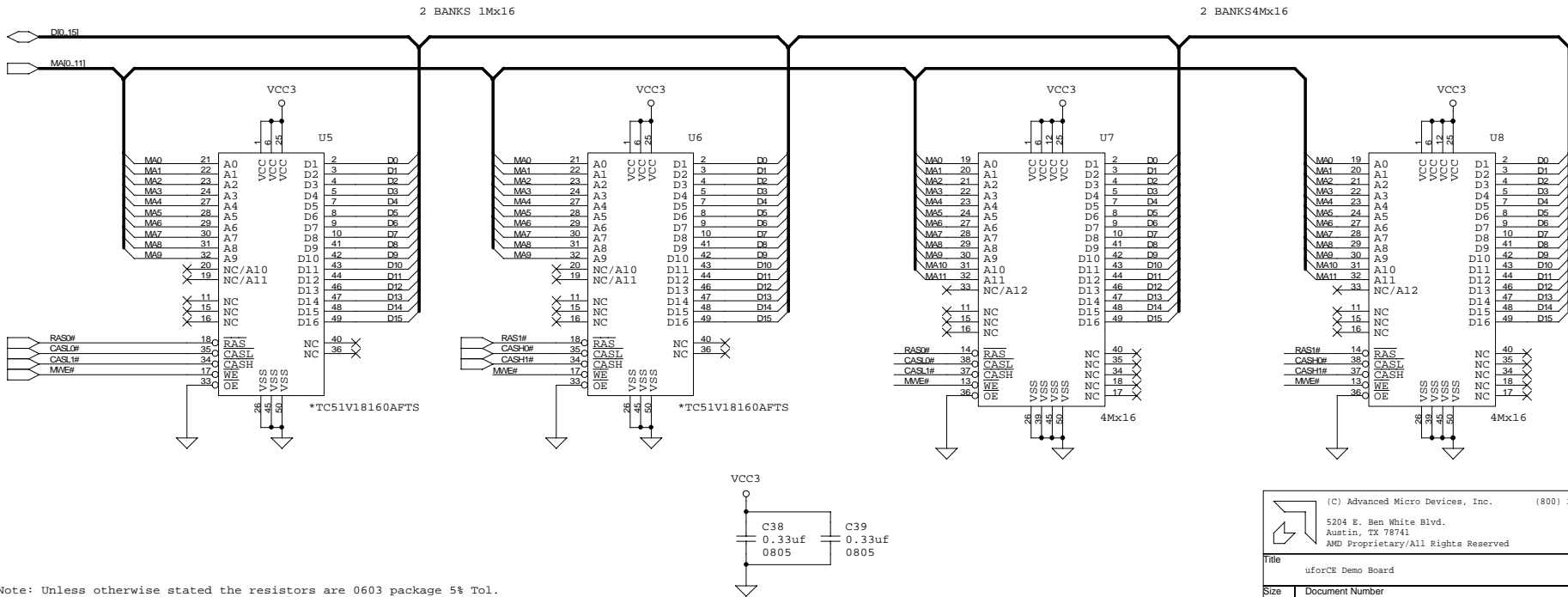
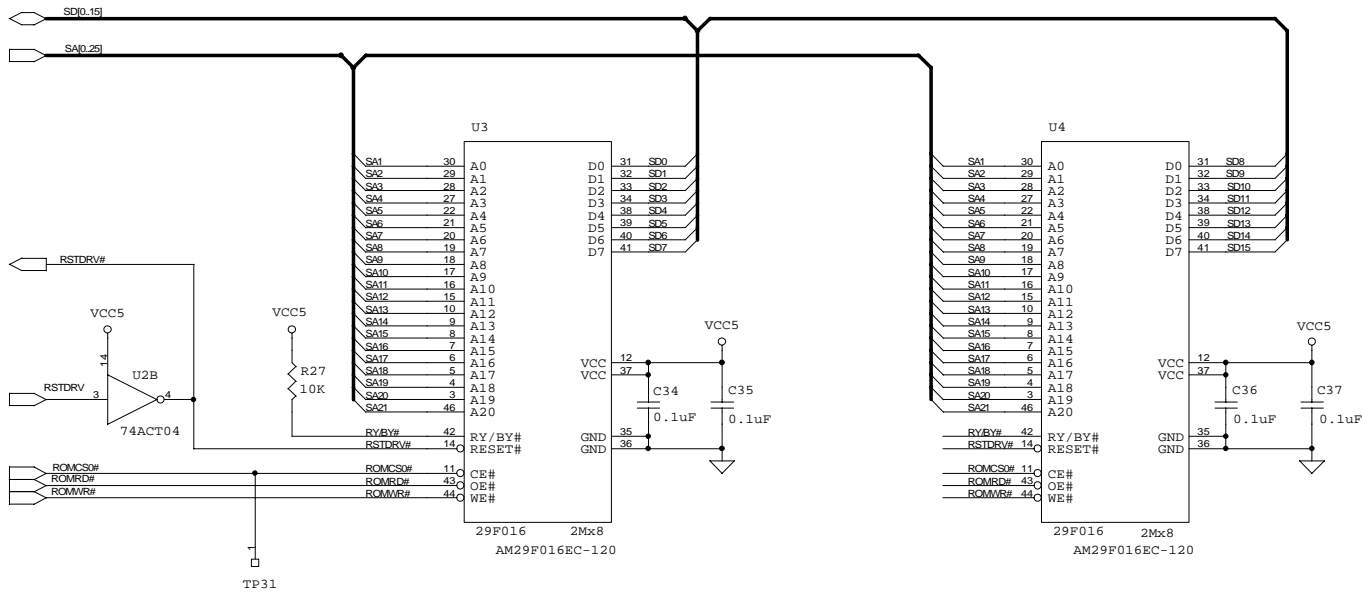
CFG1 CFG0 Configuration
 0 0 x8 ROMCS0# ROM Interface
 1 0 x16 ROMCS0# ROM Interface
 1 1 x32 ROMCS0# ROM Interface

CFG2 Configuration
 0 Enable ROMCS0# decode on the ROMCS0# pin.
 1 Enable ROMCS0# decode to access PCMCIA socket A.



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 Note: Unless otherwise stated the capacitors are 0603 package 10% Tol.

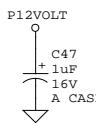
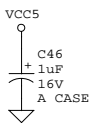
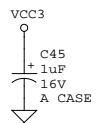
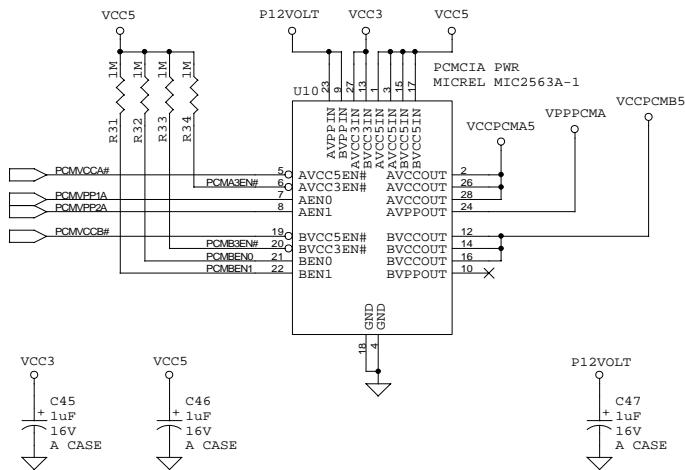
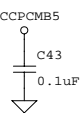
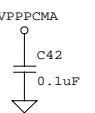
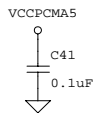
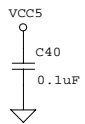
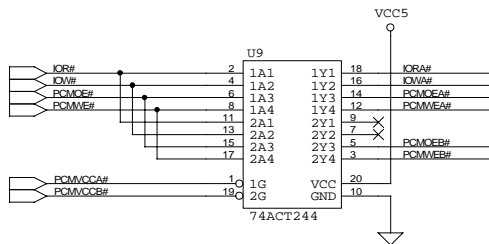
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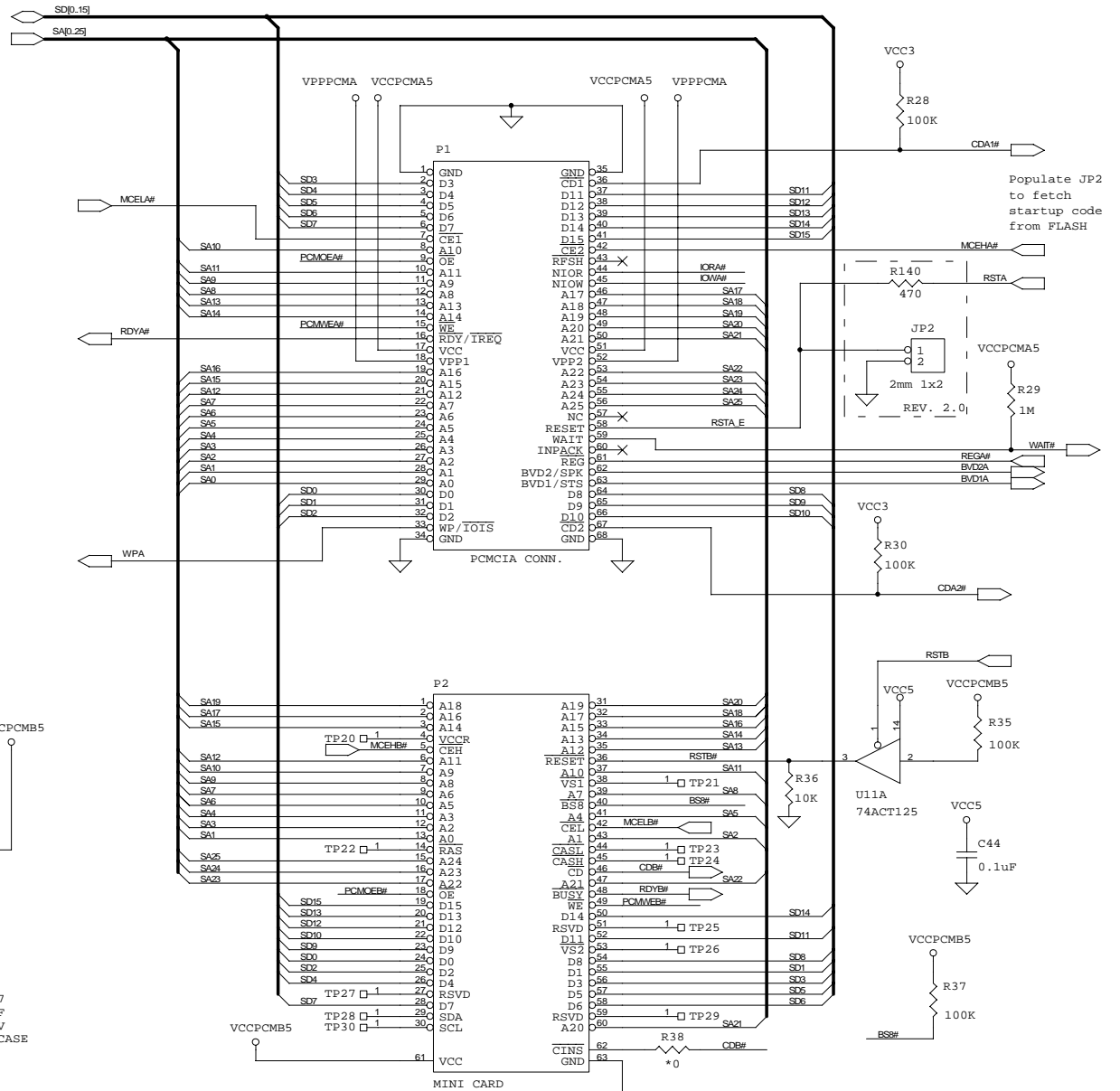
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| Size | Document Number | Rev |
| | MEMORY_SCH | 2.0 |
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Note: Unless otherwise stated the resistors are 0603 package 5% Tol.
 Note: Unless otherwise stated the capacitors are 0603 package 10% Tol.



| XVCC5EN# | XVCC3EN# | XEN1 | XEN0 | XVCCOUT | XVPPOUT |
|----------|----------|------|------|---------|---------|
| 0 | 1 | 0 | 0 | 5V | 0V |
| 0 | 1 | 0 | 1 | 5V | 5V |
| 0 | 1 | 1 | 0 | 5V | 12V |
| 0 | 1 | 1 | 1 | 5V | OFF |



Populate JP2 to fetch startup code from FLASH

The mini-card requires an active low reset which, if using just an inverted state of RSTB, the mini-card would be left in an active state during suspend since RSTB is low during this time.

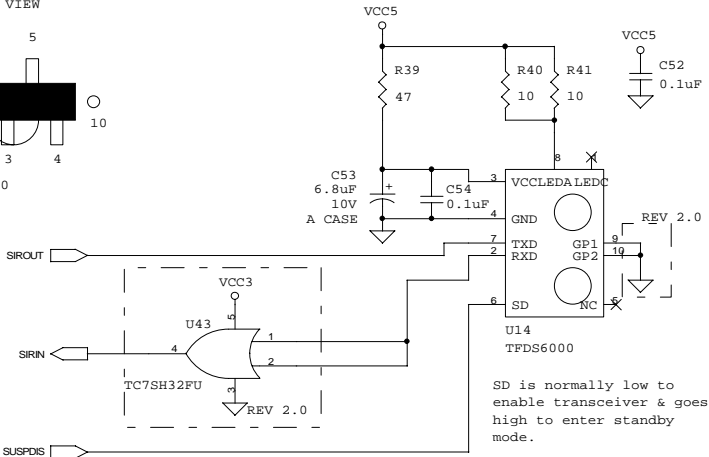
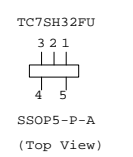
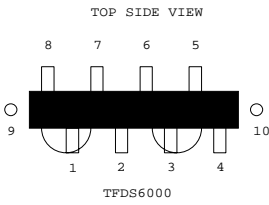
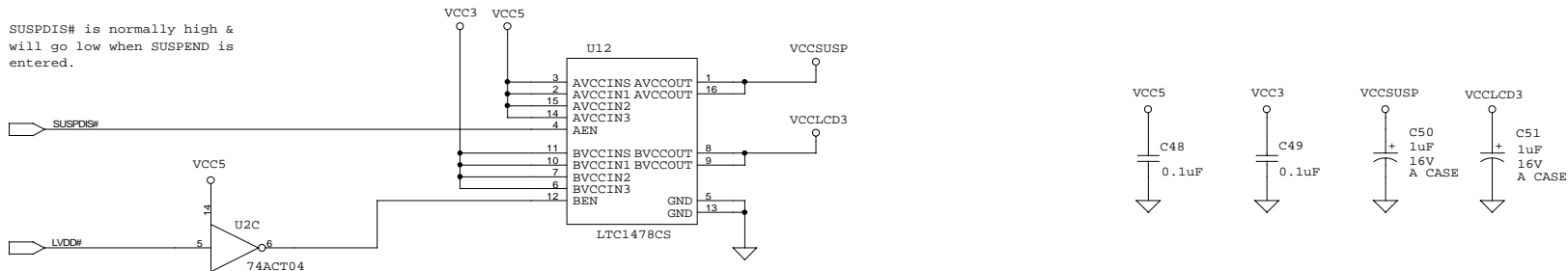
During normal power on, this implementation will cause RSTB# to be low until RSTB goes inactive, then RSTB# will follow the state of VCCPCMB5. When entering suspend, RSTB will be inactive, still allowing RSTB# to follow the state of VCCPCMB5.

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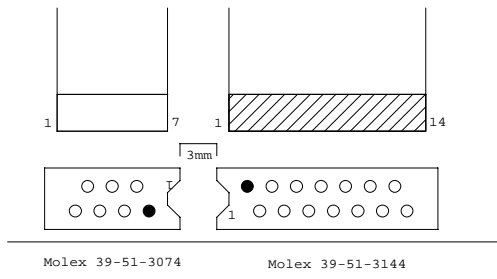
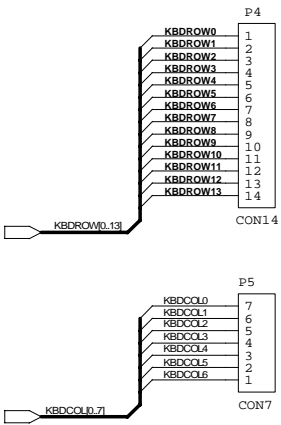
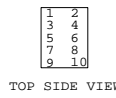
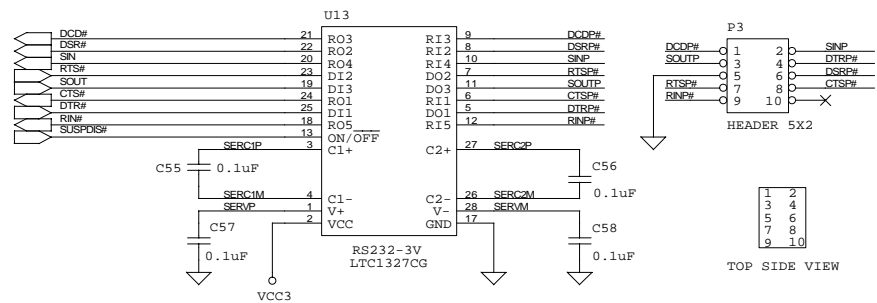
Title: uforCE Demo Board
 Size: Document Number PCMCIA.SCH Rev: 2.0
 Date: Thursday, February 05, 1998 Sheet: 5 of 15

Note: Unless otherwise stated the resistors are a 0603 package and 5% Tol.
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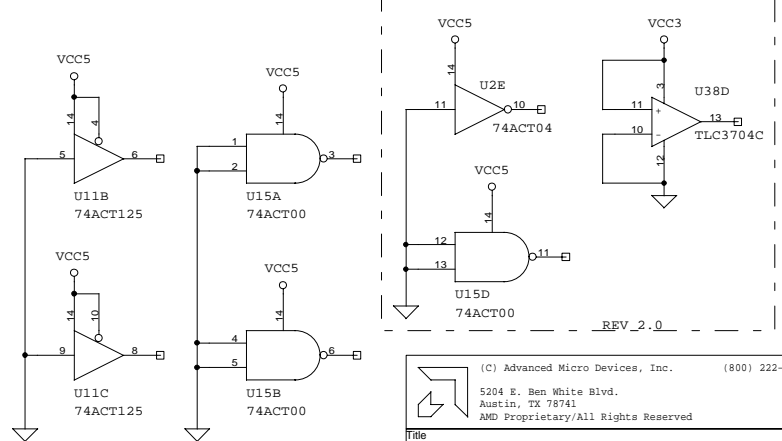
SUSPDIS# is normally high & will go low when SUSPEND is entered.



SD is normally low to enable transceiver & goes high to enter standby mode.



Edge of Board

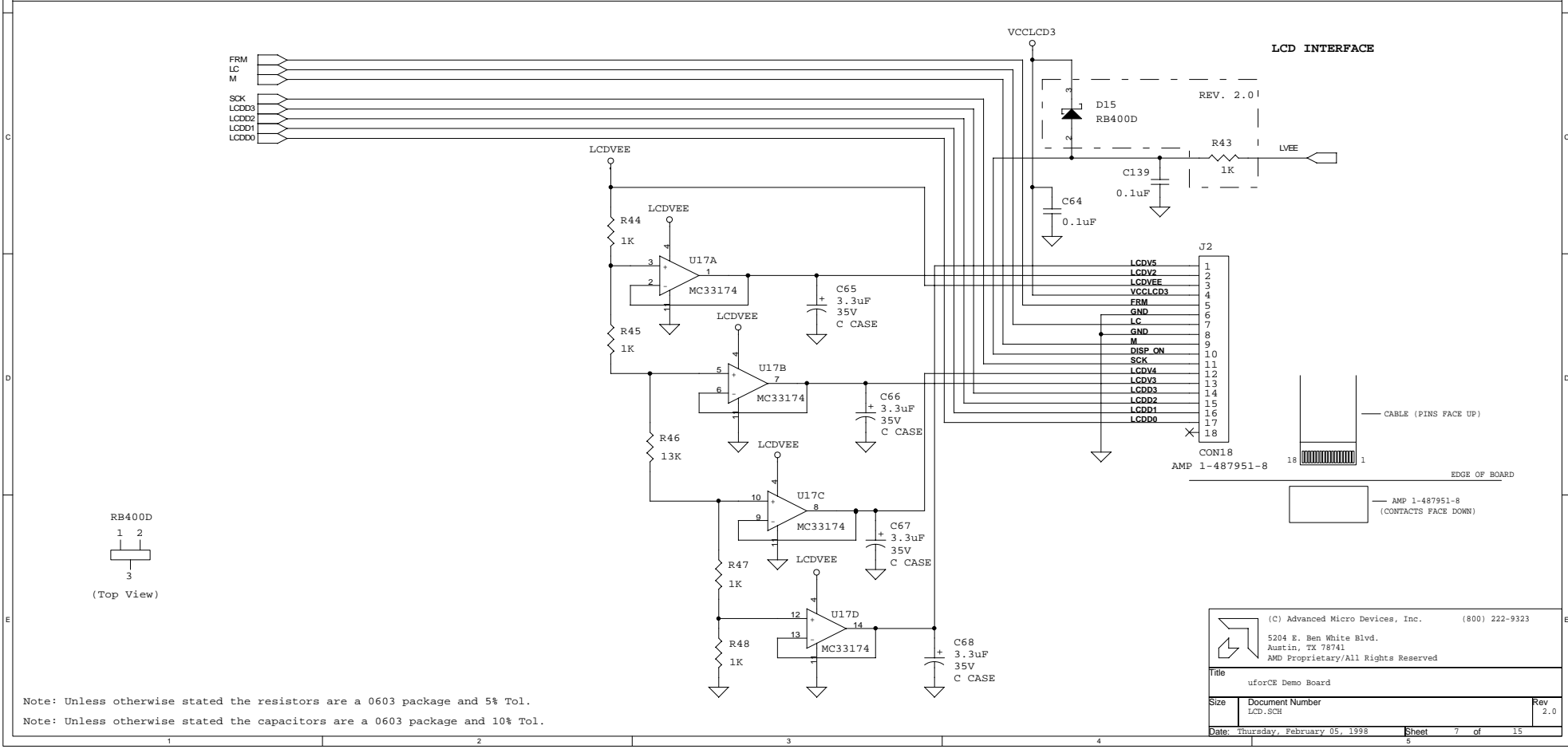
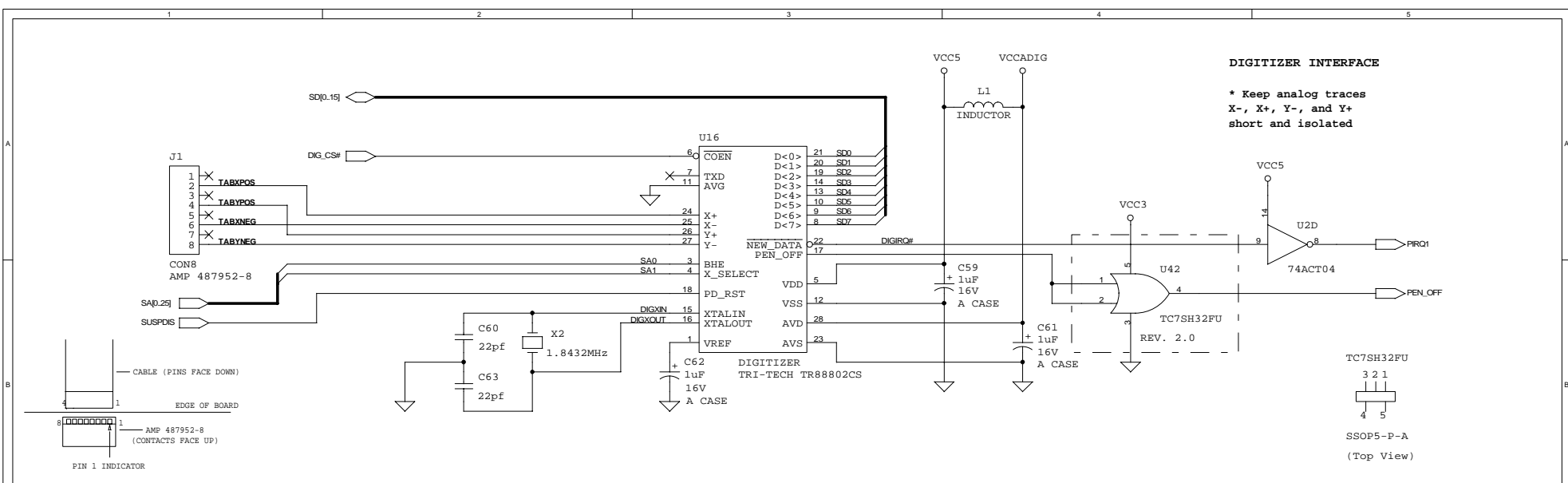


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| | MISC.SCH | 2.0 |
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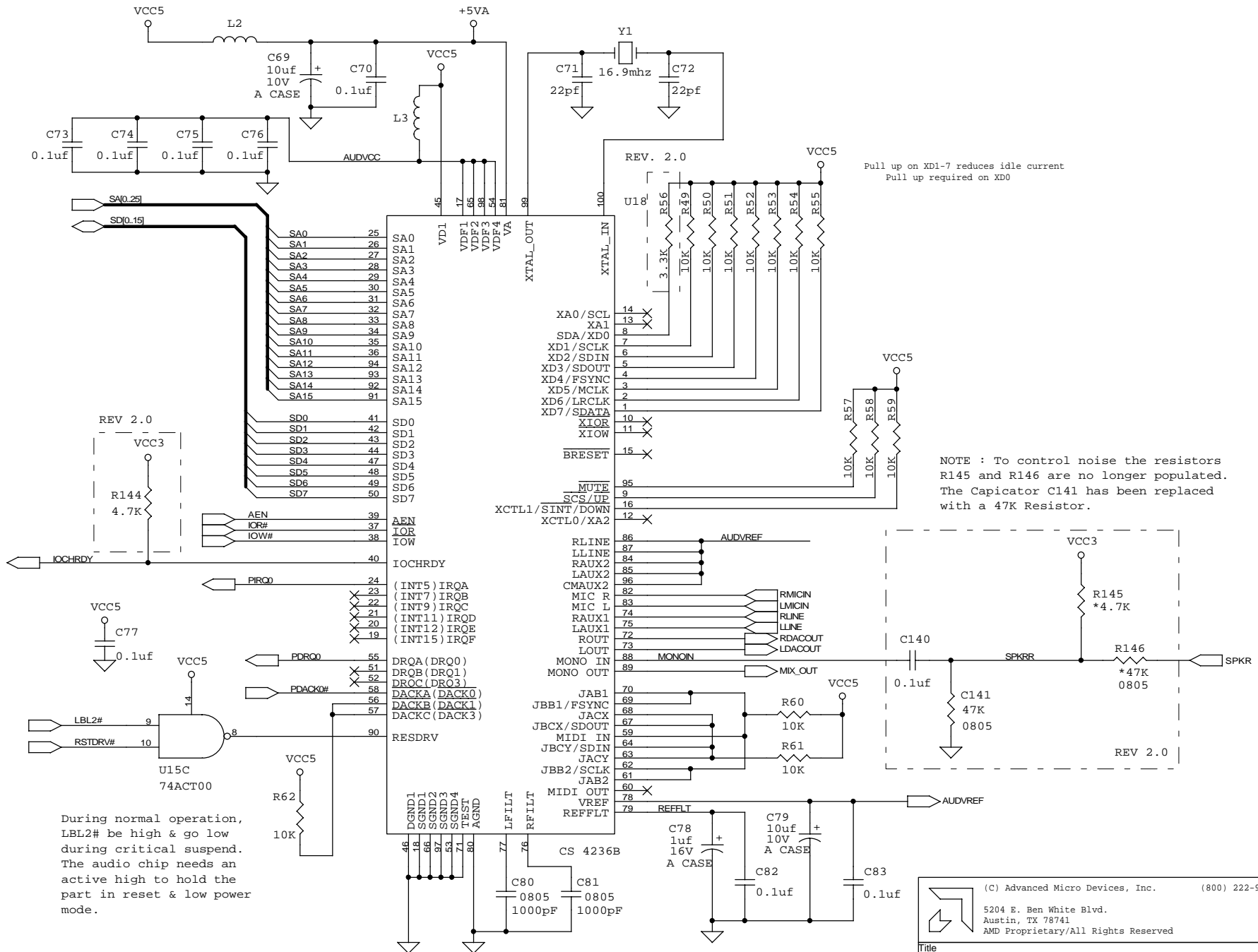
Note: Unless otherwise stated the resistors are a 0603 package and 5% Tol.
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Pull up on XD1-7 reduces idle current
Pull up required on XD0

NOTE : To control noise the resistors R145 and R146 are no longer populated. The Capacitor C141 has been replaced with a 47K Resistor.

During normal operation, LBL2# be high & go low during critical suspend. The audio chip needs an active high to hold the part in reset & low power mode.

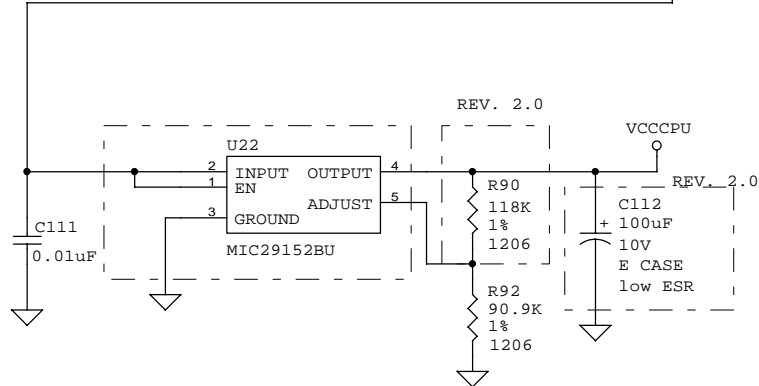
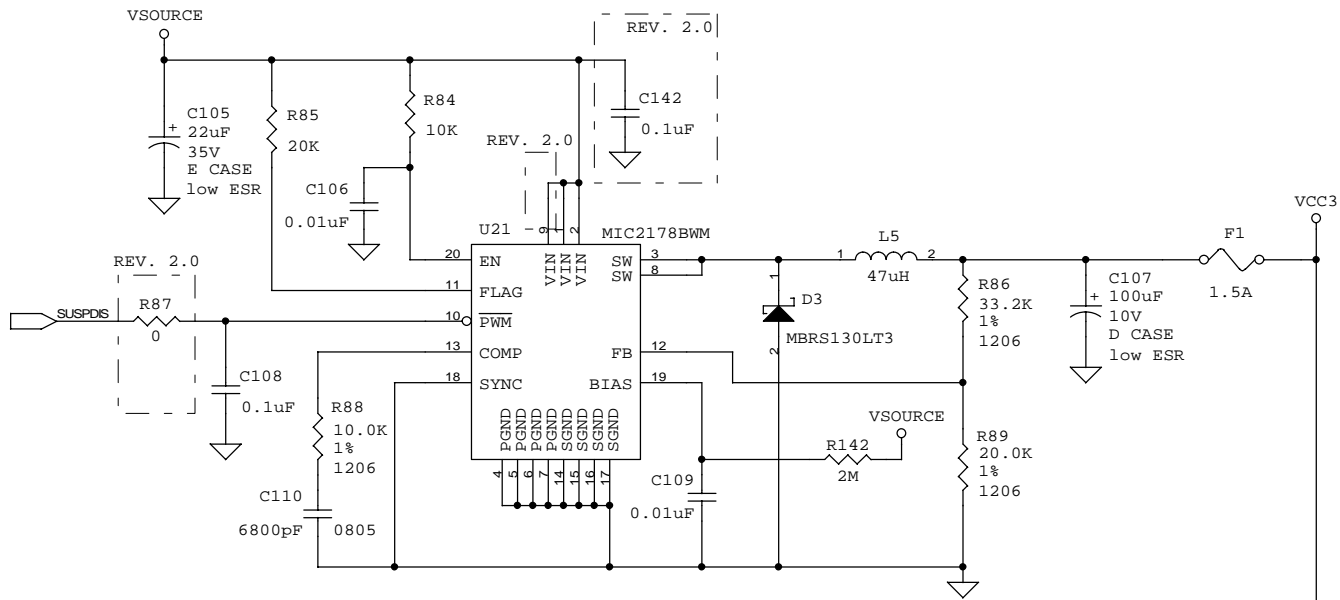
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
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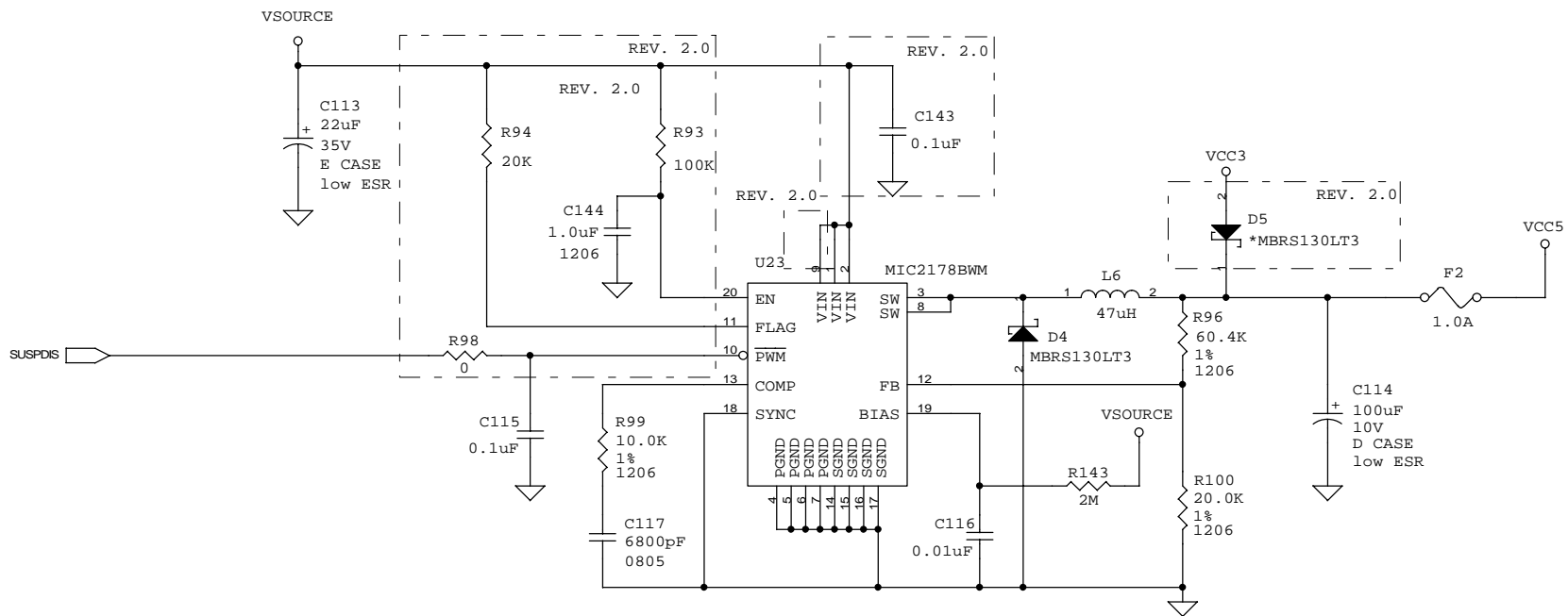
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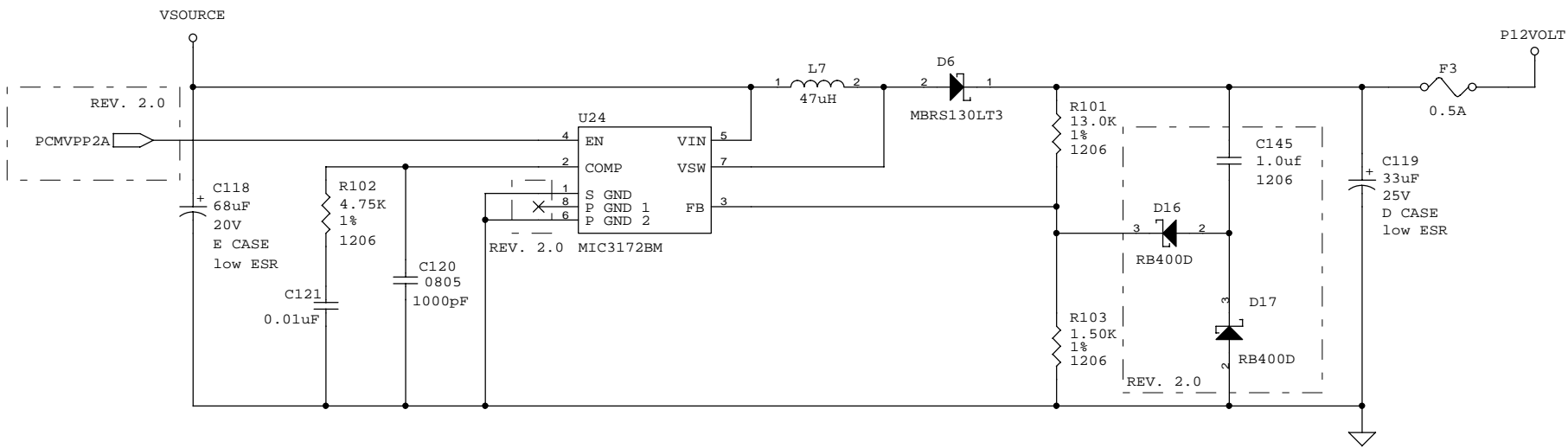
Note: Unless otherwise stated the resistors are a 0603 package and 5% Tol.
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Note: Unless otherwise stated the resistors are a 0603 package and 5% Tol.
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| | VCC5.SCH | 2.0 |
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| | 5 | |




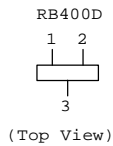
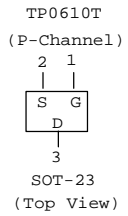
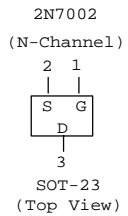
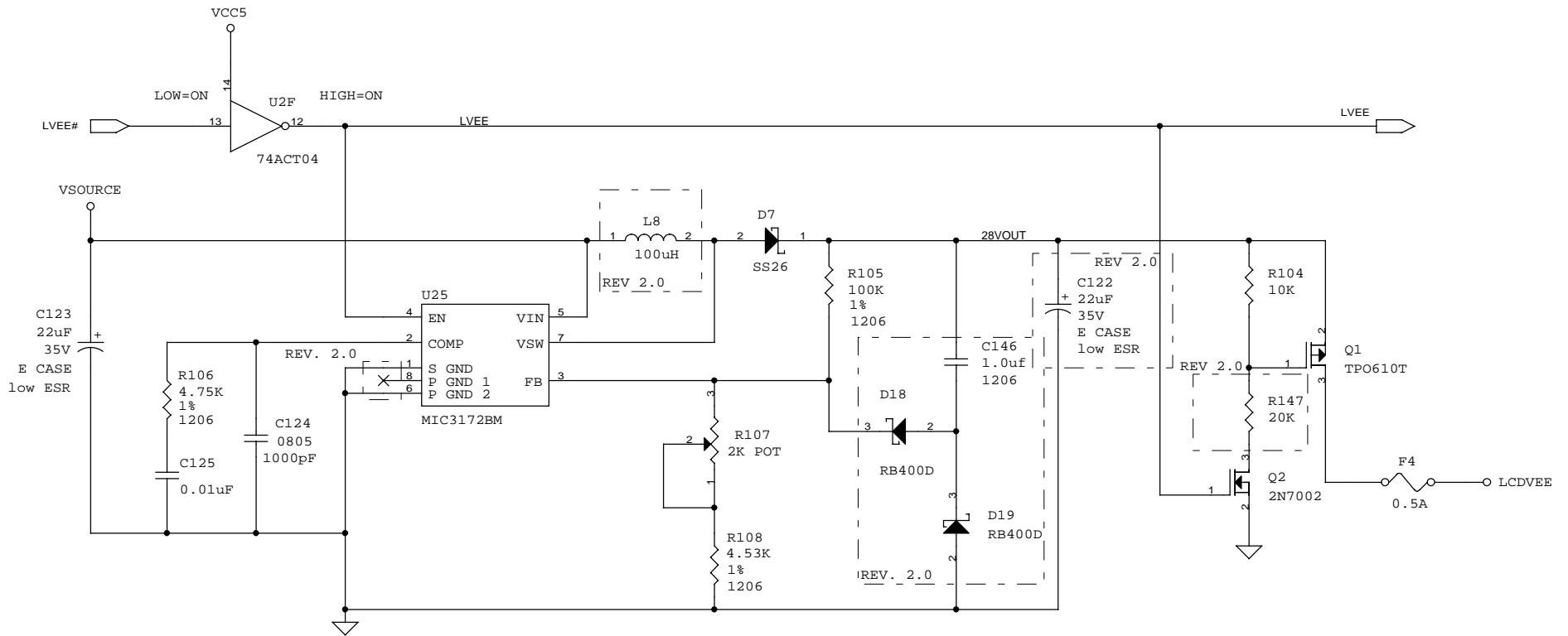
RB400D




(Top View)

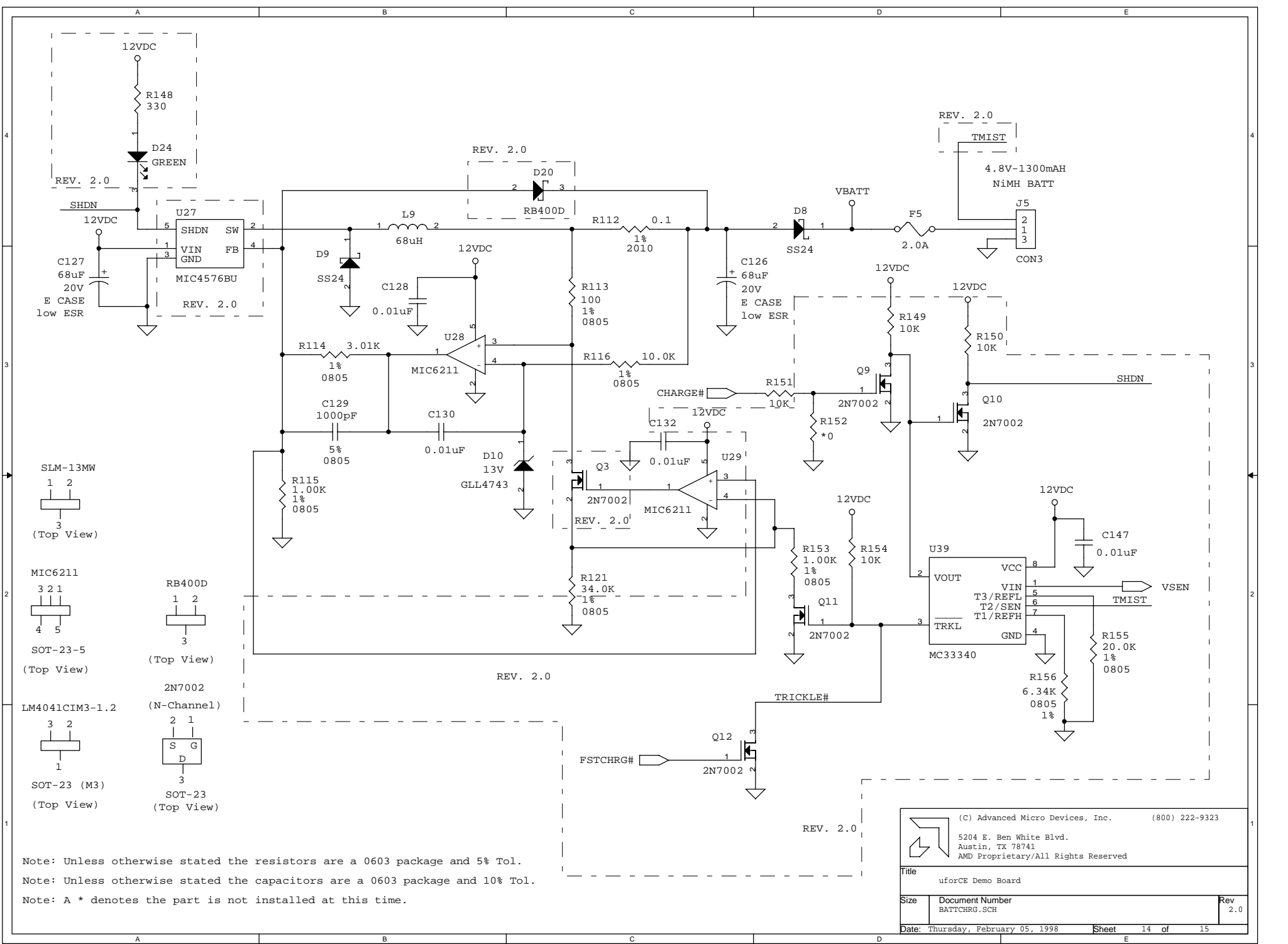
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| Size | Document Number LCDVBE.SCH | Rev |
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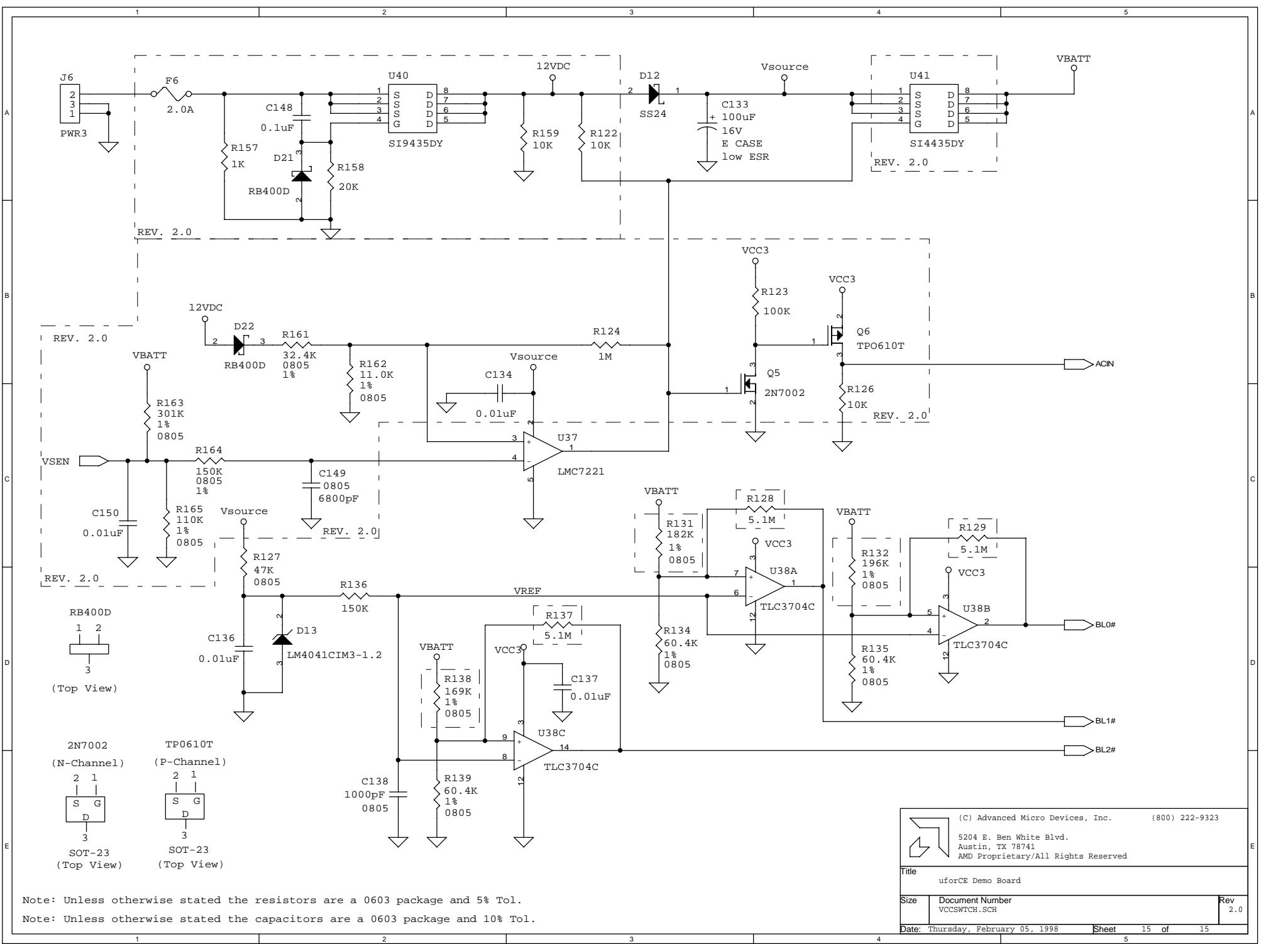


- SLM-13MW
1 2
3
(Top View)
- MIC6211
3 2 1
4 5
(Top View)
- RB400D
1 2
3
(Top View)
- 2N7002
(N-Channel)
- LM4041CIM3-1.2
3 2
1
(Top View)
- SOT-23 (M3)
1
(Top View)
- SOT-23
2 1
S G
D 3
(Top View)

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 Note: Unless otherwise stated the capacitors are a 0603 package and 10% Tol.
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REV. 2.0

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REV. 2.0

REV. 2.0

REV. 2.0

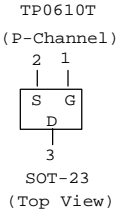
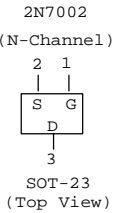
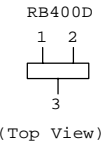
REV. 2.0

REV. 2.0

REV. 2.0

REV. 2.0

REV. 2.0



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