C80187

Math Coprocessor Core

The C80187 core implements a math coprocessor that can serve as a replacement for the Intel™ 80C187. It can interface directly with the CAST C80186tx microprocessor core, or with the original Intel 80C186 CPU.

The core extends the architecture of the Intel 80C186 processor with floating-point, extended integer, and BCD data types. A computing system that includes the C80187 fully conforms to the IEEE Floating-Point Standard.

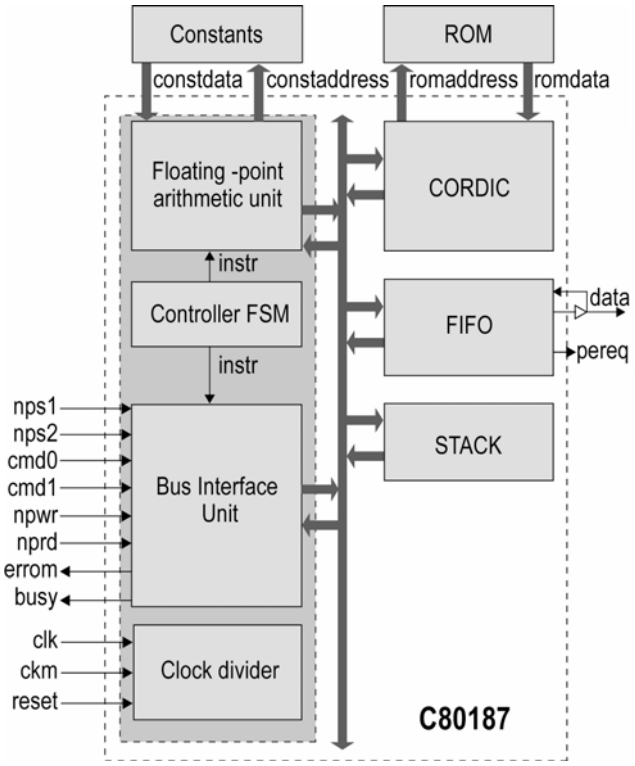
The C80187 adds over seventy mnemonics to the instruction set of the Intel 80C186, including support for arithmetic, logarithmic, exponential, and trigonometric mathematical operations. It is upward object-code compatible with the 8087-math coprocessor and will execute code written for the 80387DX and 80387SX math coprocessors.

The C80187 is a testable, microcode-free design developed for reuse in ASICs and FPGAs. It is fully synchronous and has no internal three-state buses. Extensive verification of the core has included comparison against an original 80C187 part in a hardware modeling environment.

Applications

The 80C187 is designed to be an economical replacement solution for systems using unavailable 80C187 chips. Designers might, for example, use the soft core version to consolidate a system with 80C187 functionality in a new ASIC, or use an FPGA firm core to produce a new chip to plug into a board.

Block Diagram



Features

- Implements ANSI/IEEE Standard 754-1985 for binary floating point arithmetic
- High-performance, 80-bit internal architecture provides faster processing
- Fully compatible with instruction set of 80387DX and 80387SX math coprocessors
- Implements all 80387 architectural enhancements over the 8087
- Performs a full range of transcendental operations: SINE, COSINE, TANGENT, ARCTANGENT and LOGARITHM
- Directly extends 80C186's instruction set to trigonometric, logarithmic, exponential, and arithmetic instructions for all data types
- Built-in exception handling
- Eight 80-bit numeric register
- Expands the 80C186's data types to include:
  - 32-, 64-, and 80-bit floating point numbers;
  - 32- and 64-bit integers; and
  - 18-digit BCD operands
- Interfaces directly with the CAST C80186tx core, or with the original Intel® 80C186 CPU

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Functional Description

The C80187 core is divided into several blocks as shown on the diagram above.

Controller FSM

The main control state machine, it manages all the execution units and contains the instruction decoder. All the core's built-in algorithms are coded in this unit.

Floating-point arithmetic Unit

Calculates all non transcendental arithmetic operations (addition, subtraction, multiplication, division and square root). Internally divided into exponent arithmetic and mantissa arithmetic units, and an additional align sub-block handles operand format conversions.

CORDIC

Uses CORDIC algorithms to calculate transcendental operations: sinus, cosines, tangent, exponentiation etc. It works on Double Extended, Temporary Real format data, and includes three adders for mantissa and exponent manipulation plus two shift registers for mantissa and controller. It also uses constant data stored in the ROM block.

Bus Interface Unit (BIU)

Communication unit between the C80187 and 80C186, it controls and generates all interface signals from/for the 80C186.

Clock divider

Clock control unit. When CKM is strapped high, the clock signal is derived directly from clock input. When CKM is strapped low, the clock input signal is divided by two and then used by the core.

FIFO

Used for clock domain separation, it loads and stores data from/to the 80C186. The FIFO size is fixed at 32x35 bits.

ROM

Set of constants required by the CORDIC unit for transcendental operations. Sized at 64 addresses by 70 bits. Storing these constants in a separate block allows efficient synthesis optimization and enables the use of technology-dependent dedicated ROM blocks.

Constants

Set of constants used in non-transcendental operations provided by the floating-point arithmetic unit. Sized at 64 addresses by 68 bits for mantissa and 16 bits for exponent. Storing these constants in a separate block allows efficient synthesis optimization and enables the use of technology-dependent dedicated ROM blocks.

STACK

Eight 80-bit registers joined into the stack structure, used as a place to store all sources and results. Every operation takes one source operand from the top of the stack and a second from another stack location. Each 80-bit line in the stack includes 64 bits for mantissa, 15 bits for exponent and 1 bit for sign.

Implementation Results

C80187 reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results.

FPGA Device	Area	Speed
Virtex xcv1000e-8	12,286 SLICEs	15.222 MHz
Spartan3 xc3s1500-4	10,346 SLICEs	31.118 MHz
Virtex2 xc2v3000-6	10,525 SLICEs	51.036 MHz

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements, and against the calculation results of an original 80C187 in a testbench. It has also been verified through comparison with an 80C187 part in a hardware modeling environment.

Deliverables

The core includes everything required for successful implementation:

- Post-synthesis EDIF netlist (RTL source code also available)
- An example design that shows how to build and connect memories (ROM, Constants) and the three-state buffer
- Sophisticated self-checking HDL Testbench including everything needed to test the core
- Simulation scripts, vectors, and expected results
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

CAST
info@cast-inc.com
www.cast-inc.com

CAST, Inc. 11 Stonewall Court
Woodcliff Lake, NJ 076747 USA
tel 201-391-8300 fax 201-391-8694

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we turn engineering into art
This core developed by the processor experts at Evatronix SA.