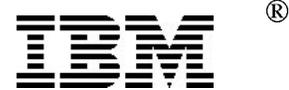


# IBM 486 DX4 CPUs

*486 DX4 Style CPUs with 8K WriteBack Cache,  
On-Chip FPU, Advanced Power Management,  
and 3 Volt Technology*



---

## *Application Note*

### **Product Overview**

The IBM Microelectronics 486 DX4 microprocessors are advanced 486 DX4 microprocessors. The 486 DX4 CPU operates at triple the external bus speed. The "486DX4" designation in the part number designations below refers to the IBM 486 DX4 microprocessor; the "-V" suffix indicates the CPU operates on a power supply lower than 5 volts.

The CPUs in the 486 DX4-V family are high speed CPUs attaining clock-tripled core speeds of up to 100 MHz. Use of the lower voltage CPUs reduces power consumption by more than half compared to using the standard 5 volt CPUs. Designed into the lower voltage family is the ability for the data, address and control pins to interface to either 3-volt or 5-volt logic.

The 486 DX4 8K Byte cache can be configured to run in traditional write-through mode or in the higher performance write-back mode. Write-back mode eliminates unnecessary external memory write cycles offering up to 15% higher overall performance (100 MHz, CPUMark16) than write-through mode.

The 486 DX4 supports 8, 16 and 32-bit data types and operates in real, virtual 8086 and protected modes. The CPU can access up to 4 GBytes of physical memory using a 32-bit burst mode bus. Floating point instructions are parallel processed using an on-chip math coprocessor.

The 486 DX4 CPUs are an ideal design solution for low-powered "Green PC" desktops as well as portable computers. These microprocessors typically draw only 2 mA, while the input clock is stopped in suspend mode, due to their static design. System Management Mode (SMM) allows the implementation of transparent system power management or the software emulation of I/O peripheral devices.

The family of 486 DX4 parts, including their operating frequency, voltage and package types is listed in the table on the following page.

- **HIGH SPEED 3.45 VOLT VERSION**

- Clock tripled core speeds up to 100 MHz
- Advanced 3.45 volt CMOS Process technology
- I/O buffers interface to either 3.3 or 5 volt logic

- **IMPROVED 486 DX4 PERFORMANCE**

- Integrated FPU 10% faster than 80486DX (Power Meter Whetstone)

- **INDUSTRY STANDARD 486 COMPATIBILITY**

- 486 DX socket and instruction set compatible
- Runs DOS, Windows, OS/2, UNIX
- Standard 168-pin PGA or 208-pin QFP package

- **ON-CHIP 8K-BYTE WRITE-BACK CACHE**

- Up to 15% higher performance than write-through (CPUMark16, 100 MHz)
- Industry wide write-back chipset support
- Burst mode write capability
- Configurable as write-back or write-through

- **ADVANCED POWER MANAGEMENT**

- Fast SMI interrupt with separate memory space
- Fully static design permits dynamic clock control
- Software or hardware initiated low-power suspend mode
- Automatic FPU power down mode

The IBM 486 DX4 3 volt CPU are advanced, 486 DX4 compatible processors. These CPUs incorporate an on-chip 8K-Byte write-back cache and an integrated math co-processor.

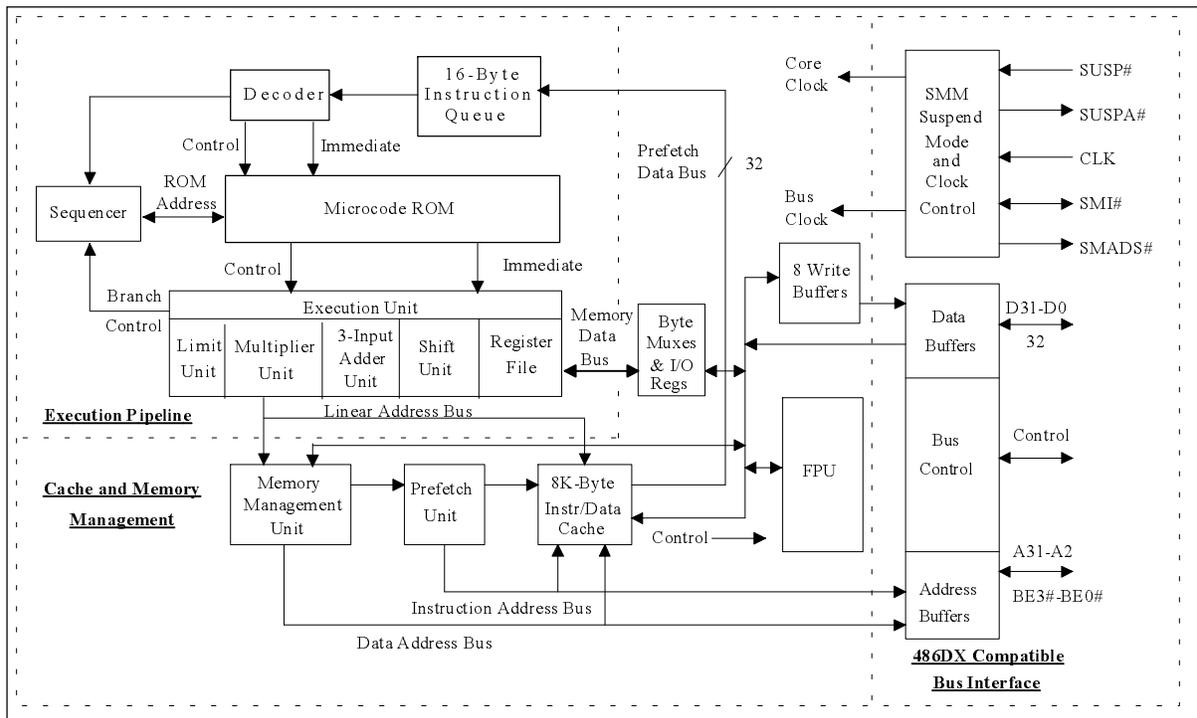
The high speed 3.45 volt 486 DX4-V family enables clock speeds up to 100 MHz. The advanced low voltage process technology power consumption is less than half the power consumption of standard 5 volt CPUs. Data, address and control pins are designed for either 3.3 or 5 volt operation.

The on-chip write-back cache allows up to 15% higher performance by eliminating unnecessary external write cycles. On traditional write-through CPUs these external write cycles can create bus bottlenecks affecting system-wide performance.

The integrated floating point unit based on Cyrix's® FasMath™ architecture improves performance up to 10% over the 80486 DXs measured using Power Meter Whetstone test.

These processors are designed to meet the power management requirements in the newest generation of low-powered desktops and notebooks. Power is saved not only by using low voltage power but by taking advantage of advanced power management features such as static circuitry, SMM and automatic FPU power-down. Fast entry and exit of SMM allows frequent use of the SMM feature without noticeable performance degradation.

This CPU family maintains compatibility with the installed base of x86 software and provides essential socket compatibility with the 486 DX4.



## 486 DX4 Part Numbers

### Rev. 4.6

Part Number	Vcc (V)	Frequency(MHz)		Package		AC Specification
		Bus	Internal	QFP	PGA	
IBM26486DX-4V3100GC (IBM DX2 Pinout)	3.45	33	100		x	Table 3-6 (Addendum)
IBM26486DX-4V375GC (IBM DX2 Pinout)	3.45	25	75		x	Table 3-5 (Addendum)
IBM26486DX-4V3100GIC (INTEL® DX2 Pinout + WB cache pins)	3.45	33	100		x	Table 3-6 (Addendum)
IBM26486DX-4V375GIC (INTEL DX2 Pinout + WB cache pins)	3.45	25	75		x	Table 3-5 (Addendum)
IBM26486DX-4V3100QIC (INTEL DX2 Pinout + WB cache pins)	3.45	33	100	x		Table 3-6 (Addendum)
IBM26486DX-4V375QIC (INTEL DX2 Pinout + WB cache pins)	3.45	25	75	x		Table 3-5 (Addendum)

---

IBM Corporation 1995. All rights reserved.

IBM and the IBM logo are registered trademarks of International Business Machines Corporation. IBM Microelectronics is a trademark of the IBM Corp.

All other product and company names are trademarks/registered trademarks of their respective holders. 1995 IBM Corp.

This document may contain preliminary information and is subject to change by IBM without notice. IBM makes no representations or warranties that the use of the information or applications herein shall be free of third party intellectual property claims and assumes no responsibility or liability from any use of the information contained herein. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties.

The products described in this document are not intended for use in implantation or other direct life support applications where malfunction may result in physical harm or injury to persons.

NO WARRANTIES OF ANY KIND, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE ARE OFFERED IN THIS DOCUMENT.

All performance data contained in this publication was obtained in a specific environment, and is presented as an illustration. The results obtained in other operating environments may vary.