The INTEL Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

The INTEL 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

- Maintenance of the microprogram address register.
- Selection of the next microinstruction based on the contents of the microprogram address register.
- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.
- Saving and testing of carry output data from the central processor (CP) array.
- Control of carry/shift input data to the CP array.
- Control of microprogram interrupts.

High Performance – 85 ns Cycle Time
TTL and DTL Compatible
Fully Buffered Three-State and Open Collector Outputs
Direct Addressing of Standard Bipolar PROM or ROM
512 Microinstruction Addressability
Advanced Organization
9-Bit Microprogram Address Register and Bus
4-Bit Program Latch
Two Flag Registers
Eleven Address Control Functions
Three Jump and Test Latch Functions
16-way Jump and Test Instruction Bus Function
Eight Flag Control Functions
Four Flag Input Functions
Four Flag Output Functions
40 Pin DIP

Figure 1. Block Diagram of a Typical System

Other members of the INTEL Bipolar Microcomputer Set:
3002 Central Processing Element 3214 Priority Interrupt Control Unit 3304A Schottky Bipolar ROM (512 x 8)
3003 Look-Ahead Carry Generator 3226 Inverting Bi-Directional Bus Driver 3601 Schottky Bipolar PROM (256 x 4)
3212 Multi-Mode Latch Buffer 3301 Schottky Bipolar ROM (256 x 4) 3604 Schottky Bipolar PROM (512 x 8)
### PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>NAME AND FUNCTION</th>
<th>TYPE(1)</th>
</tr>
</thead>
</table>
| 1-4 | PX4-PX7 | Primary Instruction Bus Inputs  
Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address. | active LOW |
| 5, 6, 8, 10 | SX0-SX3 | Secondary Instruction Bus Inputs  
Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address. | active LOW |
| 7, 9, 11 | PR0-PR2 | PR-Latch Outputs  
The PR-latch outputs are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines. | open collector |
| 12, 13, 15, 16 | FC0-FC3 | Flag Logic Control Inputs  
The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO). | active LOW |
| 14 | FO | Flag Logic Output  
The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1. | three-state |
| 17 | FI | Flag Logic Input  
The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: the flag input data is saved in the F-latch when the clock input (CLK) is low. | active LOW |
| 18 | ISE | Interrupt Strobe Enable Output  
The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description, page 6). It can be used to provide the strobe signal required by the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits. | |
| 19 | CLK | Clock Input | |
| 20 | GND | Ground | |
| 21-24 | AC0-AC6 | Next Address Control Function Inputs  
All jump functions are selected by these control lines. | |
| 37-39 | | | |
| 25 | EN | Enable Input  
When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs. | |
| 26-29 | MA0-MA3 | Microprogram Column Address Outputs | three-state |
| 30-34 | MA4-MA8 | Microprogram Row Address Outputs | three-state |
| 35 | ERA | Enable Row Address Input  
When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used with the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits to facilitate the implementation of priority interrupt systems. | |
| 36 | LD | Microprogram Address Load Input  
When in the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable. | |
| 40 | VCC | +5 Volt Supply | |

**NOTE:**  
(1) Active HIGH unless otherwise specified.
The MCU performs two major control functions. First, it controls the sequence in which microinstructions are fetched from the microprogram memory. For this purpose, the MCU contains a microprogram address register and the associated logic for selecting the next microinstruction address. The second function of the MCU is the control of the two flag flip-flops that are included for interaction with the carry input and carry output logic of the CP array. The logical organization of the MCU is shown in Figure 2.

NEXT ADDRESS LOGIC

The next address logic of the MCU provides a set of conditional and unconditional address control functions. These address control functions are used to implement a jump or jump/test operation as part of every microinstruction. That is to say, each microinstruction typically contains a jump operation field that specifies the address control function, and hence, the next microprogram address.

In order to minimize the pin count of the MCU, and reduce the complexity of the next address logic, the microprogram address space is organized as a two-dimensional array or matrix. Each microprogram address corresponds to a unit of the matrix at a particular row and column location. Thus, the 9-bit microprogram address is treated as specifying not one, but two addresses - the row address in the upper five bits and the column address in the lower four bits. The address matrix can therefore contain, at most, 32 row addresses and 16 column addresses for a total of 512 microinstructions.

The next address logic of the MCU makes extensive use of this two component addressing scheme. For example, from a particular row or column address, it is possible to jump unconditionally in one operation anywhere in that row or column. It is not possible, however, to jump anywhere in the address matrix. In fact, for a given location in the matrix, there is a fixed subset of microprogram addresses that may be selected as the next address. These possible jump target addresses are referred to as a jump set. Each type of MCU address control (jump) function has a jump set associated with it. Appendix C illustrates the jump set for each function.

FLAG LOGIC

The flag logic of the MCU provides a set of functions for saving the current value of the carry output of the CP array and for controlling the value of the carry input to the CP array. These two distinct flag control functions are called flag input functions and flag output functions.

The flag logic is comprised of two flip-flops, designated the C-flag and the Z-flag, along with a simple latch, called the F-latch, that indicates the current state of the carry output line of the CP array. The flag logic is used in conjunction with the carry and shift logic of the CP array to implement a variety of shift/rotate and arithmetic functions.

Figure 2. 3001 Block Diagram
ADDRESS CONTROL FUNCTIONS

The address control functions of the MCU are selected by the seven input lines designated AC0–AC6. On the rising edge of the clock, the 9-bit microprogram address generated by the next address logic is loaded into the microprogram address register. The next microprogram address is delivered to the microprogram memory via the nine output lines designated MA0–MA9. The microprogram address outputs are organized into row and column addresses as:

\[
\begin{align*}
MA_6 & \quad MA_2 & \quad MA_6 & \quad MA_5 & \quad MA_4 \\
row & & & & \\
MA_5 & \quad MA_2 & \quad MA_1 & \quad MA_0 \\
column & & & & \\
\end{align*}
\]

Each address control function is specified by a unique encoding of the data on the function input lines. From three to five bits of the data specify the particular function while the remaining bits are used to select part of either the row or column address desired. Function code formats are given in Appendix A, "Address Control Function Summary."

The following is a detailed description of each of the eleven address control functions. The symbols shown below are used throughout the description to specify row and column addresses.

Symbol | Meaning
--- | ---
row\(n\) | 5-bit next row address where \(n\) is the decimal row address.
col\(n\) | 4-bit next column address where \(n\) is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs to generate the next microprogram address.

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Function Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JCC</td>
<td>Jump in current column. AC0–AC4 are used to select 1 of 32 row addresses in the current column, specified by MA0–MA3, as the next address</td>
</tr>
<tr>
<td>JCF</td>
<td>Jump in current row. AC0–AC3 are used to select 1 of 16 addresses in the current row, specified by MA4–MA8, as the next address</td>
</tr>
<tr>
<td>JZR</td>
<td>Jump to zero row. AC0–AC3 are used to select 1 of 16 column addresses in row0, as the next address</td>
</tr>
<tr>
<td>JCR</td>
<td>Jump in current row. AC0–AC3 are used to select 1 of 16 addresses in the current row, specified by MA4–MA8, as the next address</td>
</tr>
<tr>
<td>JCE</td>
<td>Jump in current column/row group and enable PR-latch outputs. AC0–AC2 are used to select 1 of 8 row addresses in the current row group, specified by MA7–MA8, as the next row address. The current column is specified by MA0–MA3. The PR-latch outputs are asynchronously enabled</td>
</tr>
<tr>
<td>JZF</td>
<td>Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address</td>
</tr>
</tbody>
</table>

PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX \(x\), the current microprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Function Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFL</td>
<td>Jump/test F-Latch. AC0–AC3 are used to select 1 of 16 row addresses in the current row group, specified by MA7 and MA8, as the next row address. If the current column group, specified by MA3, is col6–col7, the F-latch is used to select col2 or col3 as the next column address. If MA3 specifies column group col8–col15, the F-latch is used to select col10 or col11 as the next column address</td>
</tr>
<tr>
<td>JPR</td>
<td>Jump/test PR-latch. AC0–AC2 are used to select 1 of 8 row addresses in the current row group, specified by MA7 and MA8, as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address</td>
</tr>
</tbody>
</table>
| JLL | Jump/test leftmost PR-latch bits. AC0–AC2 are used to select 1 of 8 row addresses in the current row group, specified by MA7 and MA8, as the next row address. PR2 and PR3 are used to
select 1 of 4 possible column addresses in col4 through col7 as the next column address.

JRL

Jump/test rightmost PR-latch bits. AC0 and AC1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA7 and MA6, as the next row address. PR0 and PR1 are used to select 1 of 4 possible column addresses in col12 through col15 as the next column address.

JPX

Jump/test PX-bus and load PR-latch. AC0 and AC1 are used to select 1 of 4 row addresses in the current row group, specified by MA5-MA8, as the next row address. PX4-PX7 are used to select 1 of 16 possible column addresses as the next column address. SX0-SX3 data is locked in the PR-latch at the rising edge of the clock.

FLAG CONTROL FUNCTIONS

The flag control functions of the MCU are selected by the four input lines designated FC0-FC3. Function code formats are given in Appendix B, "Flag Control Function Summary."

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line. Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Mnemonic Function Description
SCZ Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC Set C-flag to FI. The C-flag is set to the value of FI. The Z flag is unaffected.
HCZ Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

Mnemonic Function Description
FF0 Force FO to 0. FO is forced to the value of logical 0.
FFC Force FO to C. FO is forced to the value of the C-flag.
FFZ Force FO to Z. FO is forced to the value of the Z-flag.
FF1 Force FO to 1. FO is forced to the value of logical 1.

LOAD AND INTERRUPT STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the data on the primary and secondary instruction busses, PX4-PX7 and SX0-SX3, is loaded into the microprogram address register. PX4-PX7 are loaded into MA0-MA3 and SX0-SX3 are loaded into MA4-MA7. The high-order bit of the microprogram address register MA8 is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The interrupt strobe enable of the MCU is available on the output line designated ISE. The line is placed in the active high state whenever a JZR to col15 is selected as the address control function. Customarily, the start of a macroinstruction fetch sequence is situated at row0 and col15 so that the INTEL 3214 Priority Interrupt Control Unit may be enabled at the beginning of the fetch/execute cycle. The priority interrupt control unit may respond to the interrupt by pulling the enable row address (ERA) input line down to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC0-AC6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.
### D.C. AND OPERATING CHARACTERISTICS

**ABSOLUTE MAXIMUM RATINGS**

- Temperature Under Bias: $0^\circ$C to $70^\circ$C
- Storage Temperature: $-65^\circ$C to $+160^\circ$C
- All Output and Supply Voltages: $-0.5$V to $+7$V
- All Input Voltages: $-1.0$V to $+5.5$V
- Output Currents: $100$ mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

$T_A = 0^\circ$C to $70^\circ$C

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP$^{[1]}$</th>
<th>MAX</th>
<th>UNIT</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_C$</td>
<td>Input Clamp Voltage (All Input Pins)</td>
<td>$-0.8$</td>
<td>$-1.0$</td>
<td>V</td>
<td>$V_{CC} = 4.75$V, $I_C = -5$ mA</td>
<td></td>
</tr>
<tr>
<td>$I_F$</td>
<td>Input Load Current:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK Input</td>
<td>$-0.075$</td>
<td>$-0.75$</td>
<td>mA</td>
<td>$V_{CC} = 5.25$V, $I_F = 0.45$ mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN Input</td>
<td>$-0.05$</td>
<td>$-0.50$</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>All Other Inputs</td>
<td>$-0.025$</td>
<td>$-0.25$</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_R$</td>
<td>Input Leakage Current:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK</td>
<td>120</td>
<td>$\mu$A</td>
<td>$V_{CC} = 5.25$V, $I_R = 5.25$ V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN Input</td>
<td>80</td>
<td>$\mu$A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>All Other Inputs</td>
<td>40</td>
<td>$\mu$A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>0.8</td>
<td>V</td>
<td>$V_{CC} = 5.0$V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Power Supply Current</td>
<td>170</td>
<td>240</td>
<td>mA</td>
<td>$V_{CC} = 5.25$V$^{(2)}$</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage (All Output Pins)</td>
<td>0.35</td>
<td>0.45</td>
<td>V</td>
<td>$V_{CC} = 4.75$V, $I_{OL} = 10$ mA</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage (MA0-MA8, ISE, FO)</td>
<td>2.4</td>
<td>3.0</td>
<td>V</td>
<td>$V_{CC} = 4.75$V, $I_{OH} = -1$ mA</td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short Circuit Current (MA0-MA8, ISE, FO)</td>
<td>$-15$</td>
<td>$-28$</td>
<td>$-60$</td>
<td>$\mu$A</td>
<td>$V_{CC} = 5.0$V</td>
</tr>
<tr>
<td>$I_{O(H)}$</td>
<td>Off-State Output Current:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PR0-PR2, MA0-MA2, FO</td>
<td>$-100$</td>
<td>$\mu$A</td>
<td>$V_{CC} = 5.25$V, $V_O = 0.45$V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MA0-MA8, FO</td>
<td>100</td>
<td>$\mu$A</td>
<td>$V_{CC} = 5.25$V, $V_O = 5.25$V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. Typical values are for $T_A = 25^\circ$C and nominal supply voltage.
2. EN input grounded, all other inputs and outputs open.
A.C. CHARACTERISTICS AND WAVEFORMS  \( T_A = 0^\circ C \) to \( 70^\circ C \), \( V_{CC} = 5.0V \pm 5\%

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP(^{(1)})</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{CY} )</td>
<td>Cycle Time</td>
<td>85</td>
<td>60</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{WP} )</td>
<td>Clock Pulse Width</td>
<td>30</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Control and Data Input Set-Up Times:
- \( t_{SF} \) LD, AC\(_0\)-AC\(_6\)
- \( t_{SK} \) FC\(_0\), FC\(_1\)
- \( t_{SX} \) SX\(_0\)-SX\(_3\), PX\(_4\)-PX\(_7\)
- \( t_{SI} \) FI

Control and Data Input Hold Times:
- \( t_{HF} \) LD, AC\(_0\)-AC\(_6\)
- \( t_{HK} \) FC\(_0\), FC\(_1\)
- \( t_{HX} \) SX\(_0\)-SX\(_3\), PX\(_4\)-PX\(_7\)
- \( t_{HI} \) FI

| \( t_{CO} \) | Propagation Delay from Clock Input (CLK) to Outputs \( (MA_0-MA_8, FO) \) | 30  | 45         |     | ns   |
| \( t_{KO} \) | Propagation Delay from Control Inputs FC\(_2\) and FC\(_3\) to Flag Out (FO) | 16  | 30         |     | ns   |
| \( t_{FO} \) | Propagation Delay from Control Inputs AC\(_0\)-AC\(_6\) to Latch Outputs \( (PR_0-PR_2) \) | 26  | 40         |     | ns   |
| \( t_{EO} \) | Propagation Delay from Enable Inputs EN and ERA to Outputs \( (MA_0-MA_8, FO, PR_0-PR_2) \) | 21  | 32         |     | ns   |
| \( t_{FI} \) | Propagation Delay from Control Inputs AC\(_0\)-AC\(_6\) to Interrupt Strobe Enable Output (ISE) | 24  | 40         |     | ns   |

NOTE:
(1) Typical values are for \( T_A = 25^\circ C \) and nominal supply voltage.

TEST CONDITIONS:
Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 10 mA and 50 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:

![Test Load Circuit Diagram]

CAPACITANCE\(^{(2)}\)  \( T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
</table>
| \( C_{IN} \) | Input Capacitance:
  - CLK, EN
  - All Other Inputs | 11  | 16  |     | pF   |
| \( C_{OUT} \) | Output Capacitance | 6   | 12  |     | pF   |

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is \( f = 1 \) MHz, \( V_{BIAS} = 2.5V \), \( V_{CC} = 5V \) and \( T_A = 25^\circ C \).
TYPICAL AC AND DC CHARACTERISTICS

Clock Pulse Width vs $V_{CC}$ and Temperature

$I_{CC}$ vs Temperature

$V_{CC} = 5.0V$

Clock to MA Outputs vs $V_{CC}$ and Temperature

Output Current vs Output Low Voltage

$V_{CC} = 5.0V$

Clock to MA Outputs vs Load Capacitance

Output Current vs Output High Voltage

$V_{CC} = 5.0V$

$V_{CC} = 5.0V$

$V_{CC} = 5.0V$

$V_{CC} = 5.0V$

$V_{CC} = 5.0V$

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$V_{CC} = 5.0V$

$V_{CC} = 5.0V$

$V_{CC} = 5.0V$
### APPENDIX A  ADDRESS CONTROL FUNCTION SUMMARY

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>AC₈</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>MA₈</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>MA₃</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>JCC</td>
<td>Jump in current column</td>
<td>0</td>
<td>0</td>
<td>d₄</td>
<td>d₃</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>d₄</td>
<td>d₃</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>m₃</td>
<td>m₂</td>
<td>m₁</td>
<td>m₀</td>
</tr>
<tr>
<td>JZR</td>
<td>Jump to zero row</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>d₃</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>d₃</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
</tr>
<tr>
<td>JCR</td>
<td>Jump in current row</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>d₃</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>m₆</td>
<td>m₅</td>
<td>m₄</td>
<td>d₃</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
</tr>
<tr>
<td>JCE</td>
<td>Jump in column/enable</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>m₆</td>
<td>m₅</td>
<td>m₄</td>
<td>m₃</td>
<td>m₂</td>
<td>m₁</td>
<td>m₀</td>
</tr>
<tr>
<td>JFL</td>
<td>Jump/test F-latch</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>d₃</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>m₆</td>
<td>m₅</td>
<td>m₄</td>
<td>d₃</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
</tr>
<tr>
<td>JCF</td>
<td>Jump/test C-flag</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>m₆</td>
<td>m₅</td>
<td>m₄</td>
<td>m₃</td>
<td>0</td>
<td>1</td>
<td>f</td>
</tr>
<tr>
<td>JZF</td>
<td>Jump/test Z-flag</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>m₆</td>
<td>m₅</td>
<td>m₄</td>
<td>m₃</td>
<td>0</td>
<td>1</td>
<td>z</td>
</tr>
<tr>
<td>JPR</td>
<td>Jump/test PR-latches</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>m₆</td>
<td>m₅</td>
<td>m₄</td>
<td>1</td>
<td>p₃</td>
<td>p₂</td>
<td>p₁</td>
</tr>
<tr>
<td>JLL</td>
<td>Jump/test left PR bits</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>d₂</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>m₆</td>
<td>m₅</td>
<td>m₄</td>
<td>0</td>
<td>1</td>
<td>p₃</td>
<td>p₂</td>
</tr>
<tr>
<td>JRL</td>
<td>Jump/test right PR bits</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>1</td>
<td>d₁</td>
<td>d₀</td>
<td>1</td>
<td>1</td>
<td>p₁</td>
<td>P₀</td>
</tr>
<tr>
<td>JPX</td>
<td>Jump/test PX-bus</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>d₁</td>
<td>d₀</td>
<td>m₈</td>
<td>m₇</td>
<td>m₆</td>
<td>d₁</td>
<td>d₀</td>
<td>x₇</td>
<td>x₆</td>
<td>x₅</td>
<td>x₄</td>
</tr>
</tbody>
</table>

#### SYMBOL MEANING

- \( d_n \): Data on address control line \( n \)
- \( m_n \): Data in microprogram address register bit \( n \)
- \( p_n \): Data in PR-latch bit \( n \)
- \( x_n \): Data on PX-bus line \( n \) (active LOW)
- \( f, c, z \): Contents of F-latch, C-flag, or Z-flag, respectively

### APPENDIX B  FLAG CONTROL FUNCTION SUMMARY

#### Type: Flag Input

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>FC₁</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCZ</td>
<td>Set C-flag and Z-flag to ( f )</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>STZ</td>
<td>Set Z-flag to ( f )</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>STC</td>
<td>Set C-flag to ( f )</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>HCZ</td>
<td>Hold C-flag and Z-flag</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

#### Type: Flag Output

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>FC₃</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF0</td>
<td>Force FO to 0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>FFC</td>
<td>Force FO to C-flag</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>FFZ</td>
<td>Force FO to Z-flag</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>FF1</td>
<td>Force FO to 1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

### LOAD FUNCTION

<table>
<thead>
<tr>
<th>LOAD FUNCTION</th>
<th>NEXT ROW</th>
<th>NEXT COL</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD</td>
<td>MA₈</td>
<td>7</td>
</tr>
<tr>
<td>0</td>
<td>x₃</td>
<td>x₂</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>x₃</td>
</tr>
</tbody>
</table>

#### SYMBOL MEANING

- \( f \): Contents of the F-latch
- \( x_n \): Data on PX- or SX-bus line \( n \) (active LOW)

11
The following ten diagrams illustrate the jump set for each of the eleven
jump and jump/test functions of the
MCU. Location 341, indicated by the
black square, represents one current
row (row31) and current column (col15)
address. The blue boxes indicate the
microprogram locations that may be
selected by the particular function as
the next address.
APPENDIX D TYPICAL CONFIGURATIONS

Non-Pipelined Configuration with
512 Microinstruction Addressability

Pipelined Configuration with
2048 Microinstruction Addressability