i960® CA/i960 CF 32-Bit Superscalar Embedded Microprocessor

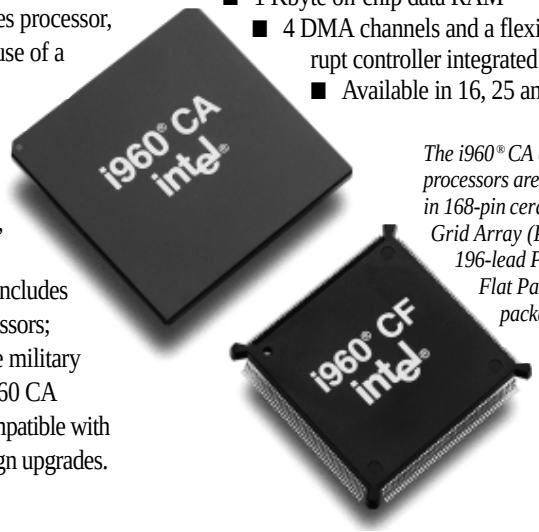
Product Overview

The i960® CA embedded RISC processor was introduced in September, 1989 as the world's first superscalar 32-bit processor developed for embedded applications. It delivers multiple instructions per clock cycle for throughput of 66 native MIPS (Millions of Instructions Per Second), doubling the performance goal of RISC (Reduced Instruction Set Computing) techniques.

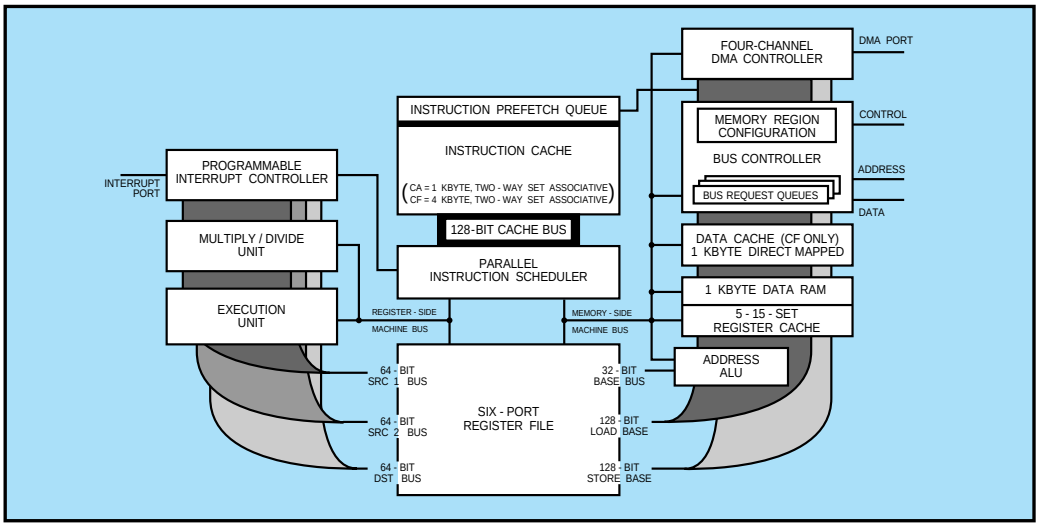
Intel also offers the second i960 C-series processor, the i960 CF microprocessor. Through the use of a superscalar CPU core and advanced cache memory design, the i960 CF processor is capable of double the performance of the i960 CA processor in many applications. The ninth member of the i960 architecture, the i960 CF processor is object code-compatible with all family members. This includes the entry-level, low-cost i960 SA/SB processors; the mid-range i960 KA/KB processors; the military i960 MC processor; and the superscalar i960 CA processor. The i960 CF device is socket-compatible with the i960 CA processor, allowing quick design upgrades.

Product Highlights

- Superscalar RISC core
- 1 Kbyte two-way set associative instruction cache (i960 CA processor only)
- 4 Kbyte two-way set associative instruction cache (i960 CF processor only)
- 1 Kbyte direct mapped data cache (i960 CF processor only)
- 1 Kbyte on-chip data RAM
- 4 DMA channels and a flexible interrupt controller integrated on-chip
- Available in 16, 25 and 33 MHz



The i960® CA and i960 CF processors are available in 168-pin ceramic Pin Grid Array (PGA) and 196-lead Plastic Quad Flat Pack (PQFP) packages.



i960® CA/i960 CF Microprocessor Block Diagram

i960® CA/i960 CF Microprocessor Produc

The integration of key performance system functions in the i960® CA and CF superscalar microprocessors brings parallel computing performance to cost- and space-sensitive applications. With nearly twice the performance of the i960 CA CPU, the i960 CF CPU brings a new level of performance to embedded RISC computing.

Features	Benefits
■ i960 CA and i960 CF processors socket and object code-compatible	■ Quick, easy design upgrades.
■ Two instructions per clock sustained execution	■ Superscalar performance doubles performance goals of RISC techniques.
■ Demultiplexed 32-bit burst bus with pipelining	
■ 32-bit parallel architecture Two instructions/clock execution Load/store architecture Sixteen, 32-bit global registers Sixteen, 32-bit local registers Manipulate 64-bit bit fields 11 addressing modes Full parallel fault model Supervisor protection model	■ Enables sustained execution of multiple instructions per clock from a sequential instruction stream.
■ Fast processor call/return model Full procedure call in four clocks RISC call in two clocks (BAL)	■ High-performance and reduced code size maintain assembly-level compatibility.
■ On-chip register cache Caches the registers on call/return Minimum of six frames provided Up to 15 frames programmable	■ Greatly reduces the external bus traffic associated with procedure context saving and restoring.
■ On-chip instruction cache 1 Kbyte two-way set associative (CA only) 4 Kbyte two-way set associative (CF only) 128-bit path to instruction sequencer Cache-lock, cache-off mode	■ Accelerates execution of standard software and time-critical interrupt routines.
■ On-chip data cache (CF only) 1 Kbyte direct-mapped, write through 128 bits per clock access on cache hit	■ Enhances performance.
■ 1 Kbyte high bandwidth on-chip data RAM	■ Eliminates bottlenecks; data is available when it is needed.
■ Four on-chip DMA channels 59 Mbytes/sec fly-by transfers 32 Mbytes/sec two-cycle transfers Data chaining, packing/unpacking Programmable priority method	■ High-speed DMA data transfers to/from internal or external locations.
■ High-speed interrupt controller Up to 248 external interrupts 32 fully programmable priorities Multi-mode 8-bit interrupt port Four internal DMA interrupts Separate, non-maskable interrupt pin Context switch in 759 ns typical	■ Eases control. Prioritization of software interrupts, hardware interrupts and the process priority.

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Features and Benefits

INTERNETWORKING

Features

- Superscalar architecture with instruction set that supports data agility
- Integrated DMA, caches, interrupt controller
- Integrated SRAM and hardware multiply
- Broad and mature tool support including optimizing compiler
- Pipelined burst-bus
- 32-level priority-based interrupt structure

Benefits

- Maximum amount of processing per packet without clogging data flow (i.e., forwarding decisions, encapsulating, translating, routing).
- Maximizes performance of critical routines with cleaner programming and quick interrupt response.
- Quicker address table access for swift forwarding/ routing decisions.
- Ease of re-use for larger programs (i.e., network management, statistics) with easy optimization of critical path.
- Provides maximum memory bandwidth.
- Provides hardware support for interrupt management.

IMAGING

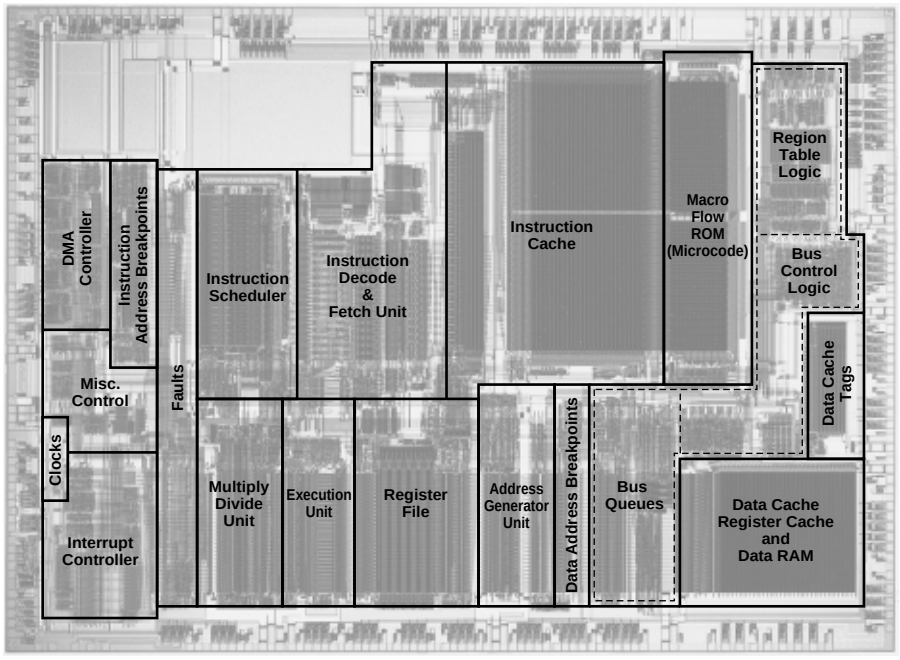
Features

- Software-configurable bus controller compensates for external memory subsystems that contain a combination of bus widths (8-, 16- or 32-bit), access times, burst-mode capabilities and data-ordering conventions
- Integrated DMA

Benefits

- Easy to configure, lower cost memory subsystems for 32-bit performance levels. Easy to deal with varying I/O (8-, 16- or 32-bit).
- Provides high-speed DMA data transfers for character input and video output.

The i960® CA and i960 CF microprocessors incorporate the right mix of peripheral integration: a 4-channel DMA controller and an 8-channel interrupt control unit. Pictured is the i960 CF superscalar microprocessor.



BUS CONTROLLER

i960® CA/i960 CF MICROPROCESSOR APPLICATION AREAS

Office Automation

Image scanners, page-printer controllers
X terminal applications
Document teleprocessing
Local-area network (LAN) controllers and communications bridges (FDDI, TI)
Database engines, department filing systems, process servers
Telecommunications and data communications equipment
I/O processing for graphics workstations

Industrial Robotics

Automated vision systems
Robotics
Image recognition
Production line coordination, communications
Factory process control, monitoring instruments
Transport system control

Medical Instrumentation

Real-time data collection and analysis instruments
Monitoring systems
Ultrasound imaging displays

Avionics and Aerospace

Flight-control equipment
Ground-to-air communications systems
Satellite navigation computers
Celestial telescope systems

i960® CA/i960 CF Microprocessor Development Support

To help minimize development costs, Intel has developed the Solutions960™ program. Currently, we have assembled over 200 tools from more than 70 companies. Included in the program are the following:

- Optimized support components
- Full suite of software development tools, including optimizing C compiler
- Operating systems
- Debug tools – in-circuit emulators, debugger/ simulators, logic analyzers
- Evaluation boards
- Specific support products for networking and laser printer application support

Support Information

Product and Sales Information	Intel product information, sales office and distributor phone numbers.	**800-628-8686**
Literature Department	To order Intel product literature.	**800-548-4725**
Development Tools Hotline	Technical applications support for Intel development tools.	**800-843-4481**
FaxBack Service	Automated response system that faxes Intel documents to your fax machine at no cost. For a listing of all i960 microprocessor documents, order FaxBack service document #2068.	**800-628-2283**
Applications Bulletin Board Service	24-hour access via modem to publicly available technical information. For a complete listing of all files available on BBS, call the FaxBack service and request catalog #6 (BBS Master File Listing).	**916-356-3600**

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