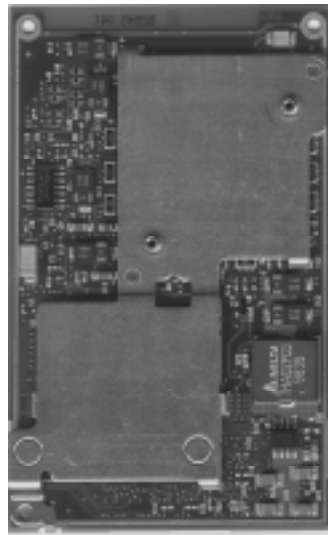




INTEL® CELERON™ PROCESSOR MOBILE MODULE: MOBILE MODULE CONNECTOR 1 (MMC-1)

- Intel® Mobile Celeron™ Processor with core frequency running at 300 MHz and 266 MHz
- On-die 2nd level cache (128K)
- Processor core voltage regulation supports input voltages from 5V to 21V
 - Above 80 percent peak efficiency
- Integrated Active Thermal Feedback (ATF) system
 - ACPI Rev. 1.0 compliant
 - Internal A/D – digital signaling (SMBus) across the module interface
 - Programmable trip point interrupt or poll mode for temperature reading
- Thermal transfer plate for heat dissipation
- Intel® 443BX Host Bridge system controller
 - DRAM controller supports EDO and SDRAM at 3.3V
 - Supports PCI CLKRUN# protocol
 - SDRAM clock enable support and self refresh of EDO or SDRAM during Suspend mode
 - Only 3.3V PCI bus control, Rev 2.1 compliant

The Intel® Celeron™ processor mobile module connector 1 (MMC-1) is a highly integrated assembly containing an Intel Celeron mobile processor and its immediate system-level support.



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CONTENTS

1.0	INTRODUCTION	5
2.0.	ARCHITECTURE OVERVIEW	5
3.0	MODULE CONNECTOR INTERFACE.....	7
3.1	Signal Definition.....	7
3.1.1.	Signal List.....	8
3.1.2.	Memory (108 Signals)	9
3.1.3.	PCI (56 Signals).....	10
3.1.4	Processor and PIIX4E/M Sideband (9 Signals).11	
3.1.5	Power Management (8 Signals).....	12
3.1.6	Clock (8 Signals).....	13
3.1.7	Voltages (39 Signals)	14
3.1.8	JTAG (7 Signals)	14
3.1.9	Miscellaneous (45 Signals)	15
3.2.	Connector Pin Assignments	16
3.3	Pin and Pad Assignments	18
4.0.	FUNCTIONAL DESCRIPTION	19
4.1.	Celeron™ processor mobile module	19
4.2.	L2 Cache.....	19
4.3.	The 443BX Host Bridge System Controller	19
4.3.1.	Memory Organization	19
4.3.2.	Reset Strap Options	20
4.3.3.	PCI Interface	20
4.3.4	AGP Feature Set	20
4.4.	Power Management.....	20
4.4.1	Clock Control Architecture.....	20
4.4.2.	Normal State	23
4.4.3.	Auto Halt State.....	23
4.4.4.	Stop Grant State	23
4.4.5.	Quick Start State.....	23
4.4.6.	HALT/Grant Snoop State	23
4.4.7.	Sleep State.....	23
4.4.8.	Deep Sleep State.....	24
4.5.	Typical POS/STR Power	24
4.6.	Electrical Requirement	25
4.6.1.	DC Requirements	25
4.6.2	AC Requirements.....	26
4.6.2.1.	System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines.....	27
4.7.	The Voltage Regulator	27
4.7.1.	Voltage Regulator Efficiency	27
4.7.2.	Control of the Voltage Regulator	28
4.7.2.1.	Voltage Signal Definition and Sequencing.....	29
4.7.3.	Power Planes: Bulk Capacitance Requirements	30
4.7.4.	Surge Current Guidelines	31
4.7.4.1.	Slew-Rate Control: Circuit Description.....	33
4.7.4.2.	Under-Voltage Lockout: Circuit Description (V_uv_lockout).....	34
4.7.4.3.	Over-Voltage Lockout: Circuit Description (V_ov_lockout).....	35
4.7.4.4.	Over-Current Protection: Circuit Description.....	35
4.8.	Active Thermal Feedback.....	35
4.9	Thermal Sensor Configuration Register.....	36
5.0.	MECHANICAL SPECIFICATION	36
5.1.	Module Dimensions	36
5.1.1.	Board Area	36
5.1.2.	MMC-1 Pin 1 Location	38
5.1.3.	Printed Circuit Board Thickness	38
5.1.4.	Height Restrictions	39
5.2.	Thermal Transfer Plate	39
5.3.	Module Physical Support.....	41
5.3.1	Module Mounting Requirements	41
5.3.2.	Module Weight	41
6.0.	THERMAL SPECIFICATION	42
6.1.	Thermal Design Power	42
6.2	Thermal Sensor Setpoint.....	42
7.0.	LABELING INFORMATION	43
8.0.	ENVIRONMENTAL STANDARDS	44

FIGURES

Figure 1. Block Diagram of the Celeron™ Processor Mobile Module 6

Figure 2. 280-Pin Connector Footprint Pad Numbers, Module Secondary Side..... 18

Figure 3. Celeron™ Processor Mobile Module Clock Control States 22

Figure 4. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pin 27

Figure 5. Power-On Sequence Timing 30

Figure 6. Instantaneous In-Rush Current Model 31

Figure 7. Instantaneous In-Rush Current 32

Figure 8. Over-Current Protection Circuit..... 33

Figure 9. Spice Simulation Using In-Rush Protection (Example Only) 34

Figure 10. Celeron™ Processor MMC-1 Board Dimensions with 280-Pin Connector Orientation 37

Figure 11. Celeron™ 280-Pin Connector - Pin 1 Orientation..... 38

Figure 12. Printed Circuit Board Thickness..... 38

Figure 13. Celeron™ Processor Mobile Module 3-D Keep-out Zone 39

Figure 14. Celeron™ Processor Mobile Module Thermal Transfer Plate 40

Figure 15. Celeron™ Processor Mobile Module Thermal Transfer Plate 41

Figure 16. Standoff Holes, Board Edge Clearance, and EMI Containment Ring 42

Figure 17. Celeron™ Processor Mobile Module Product Tracking Code 44

TABLES

Table 1. Module Connector Signal Summary 7

Table 2. Memory Signal Descriptions 9

Table 3. PCI Signal Descriptions 10

Table 4. Processor/PIIX4E/M Sideband Signal Descriptions 11

Table 5. Power Management Signal Descriptions 12

Table 6. Clock Signal Descriptions 13

Table 7. Voltage Descriptions 14

Table 8. JTAG Pins..... 14

Table 9. Miscellaneous Pins..... 15

Table 10. Connector Pin Assignments 16

Table 11. Connector Specifications 19

Table 12. Configuration Straps for the 443BX Host Bridge System Controller..... 20

Table 13. Mobile Celeron™ Processor Clock State Characteristics..... 24

Table 14. Mobile Celeron™ Processor POS/STR Power 24

Table 15. Celeron™ Processor Mobile Module Power Specifications 1 25

Table 16. Celeron™ Processor Mobile Module AC Specifications (BCLK) 26

Table 17. BCLK Signal Quality Specifications at the Processor Core 27

Table 18. Typical Voltage Regulator Efficiency 27

Table 19. Voltage Signal Definitions and Sequences 29

Table 20. Capacitance Requirements per Power Plane 30

Table 21. Thermal Sensor SMBus Address Table 35

Table 22. Thermal Sensor Configuration Register 36

Table 23. Celeron™ Processor Mobile Module (MMC-1) Maximum Power Specifications..... 43

Table 24. Environmental Standards..... 44



1.0 INTRODUCTION

This document provides the technical information for integrating the Celeron™ Processor Mobile Module Connector 1 (MMC-1) into the latest notebook systems for today's notebook market.

Building around this modular design gives the system manufacturer these advantages:

- Avoids complexities associated with designing high-speed processor core logic boards.
- Provides an upgrade path from previous Intel mobile modules using a standard interface.

2.0 ARCHITECTURE OVERVIEW

The Celeron™ processor mobile module is a highly integrated assembly containing the mobile Celeron processor core with an on-die L2 cache, the Intel 443BX Host Bridge system controller, and system level support. The Celeron processor mobile module has a 66-MHz system bus speed and runs at speeds of 300 MHz and 266 MHz.

The PIIX4E/M PCI/ISA Bridge is one of two large-scale integrated devices of the Intel® 440BX PCIsset. A notebook's system electronics must include a PIIX4E/M device to connect to the Celeron processor mobile module. The PIIX4E/M provides extensive power management capabilities and supports the second integrated device, the 443BX Host Bridge. Key features of the Intel 443BX Host Bridge system controller include the DRAM controller, which supports EDO at 3.3V with a burst read at 7-2-2-2 (60 ns) or SDRAM at 3.3V with a burst read at 8-1-1-1 (66 MHz, CL=2). The 443BX Host Bridge also provides a PCI CLKRUN# signal to request PIIX4E/M to regulate the PCI clock on the PCI bus. The 82443Bx clock

enables Self Refresh mode of EDO or SDRAM during Suspend mode, and is compatible with SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM) modes of power management. E_SMRAM mode supports write-back cacheable SMRAM up to 1 MB.

A thermal transfer plate (TTP) on the 443BX Host Bridge and the mobile Celeron™ processor provides heat dissipation and a standard thermal attach point for the notebook manufacturer's thermal solution.

An on-board voltage regulator converts the system DC voltage to the processor's core and I/O voltage. Isolating the processor voltage requirements allows the system manufacturer to incorporate different processor variants into a single notebook system.

Supporting input voltages from 5V to 21V, the processor core voltage regulator enables an above 80 percent peak efficiency and decouples processor voltage requirements from the system.

The Celeron processor mobile module also incorporates Active Thermal Feedback (ATF) sensing, compliant to the ACPI Rev 1.0 specification. A system management bus (SMBus), which is thermal sensor compliant, supports the internal and external temperature sensing with programmable trip points.

Figure 1 illustrates the block diagram of the Celeron™ processor mobile module.

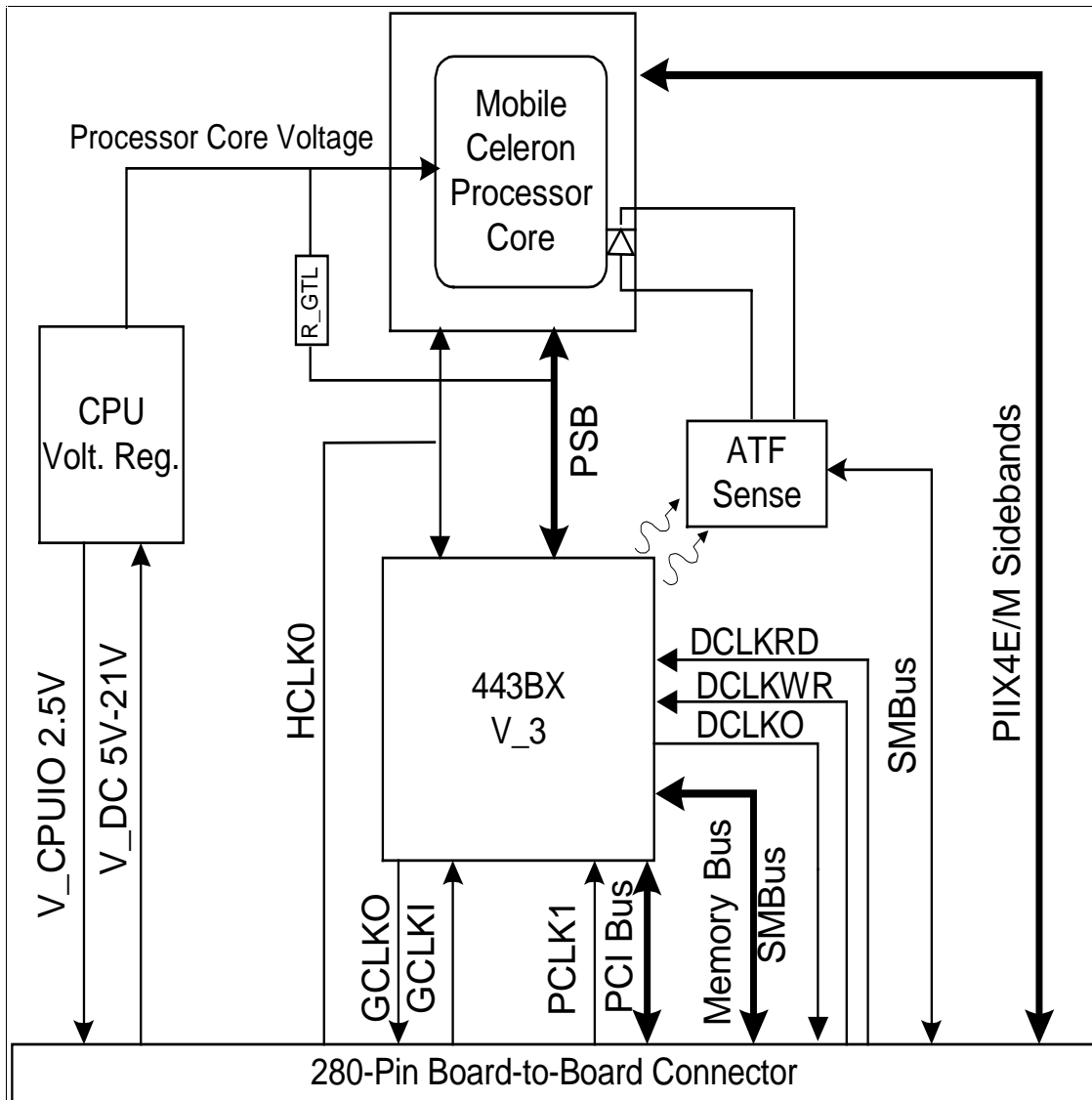


Figure 1. Block Diagram of the Celeron™ Processor Mobile Module

3.0 MODULE CONNECTOR INTERFACE

3.1 Signal Definition

This section provides information on signal groups for the Celeron™ processor MMC-1. The signals are variably defined for compatibility with future Intel mobile modules.

Table 1 provides a list of signals by category and the corresponding number of signals in each category. For proper signal termination, please contact your Intel sales representative for further information.

Table 1. Module Connector Signal Summary

Signal Group	Number
Memory	108
PCI	56
Processor/PIIX4E/M Sideband	9
Power Management	8
Clocks	8
Voltage: V_DC	10
Voltage: V_3S	20
Voltage: V_5	1
Voltage: V_3	5
Voltage: V_CPUIO	3
JTAG	7
Miscellaneous & Module ID	5
Ground	32
Reserved	8
Total	280

3.1.1. Signal List

The following notations are used to denote the signal type:

- I Input pin
- O Output pin
- O D Open Drain Output pin. This pin requires a pull up resistor.
- I D Open Drain Input pin. This pin requires a pull up resistor.
- I/O D Input / Open Drain Output pin. This pin requires a pull up resistor.
- I/O Bi-directional Input / Output pin

The signal description also includes the type of buffer used for a particular signal:

- GTL+ Open Drain GTL+ interface signal.
- PCI PCI bus interface signals.
- CMOS The CMOS buffers are Low Voltage TTL compatible signals. They are also 3.3V outputs with 5.0V tolerant inputs.

3.1.2. Memory (108 Signals)

Table 2 lists the memory interface signals.

Table 2. Memory Signal Descriptions

Name	Type	Voltage	Description
MECC[7:0]	I/O CMOS	V ₃	Memory ECC Data: These signals carry Memory ECC data during access to DRAM. These pins are not implemented on the MMC-1 and are reserved for future use.
RASA[5:0]# or CSA[5:0]#	O CMOS	V ₃	Row Address Strobe (EDO): These pins select the DRAM row. Chip Select (SDRAM): These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low.
CASA[7:0]# or DQMA[7:0]	O CMOS	V ₃	Column Address Strobe (EDO): These pins select the DRAM column. Input/Output Data Mask (SDRAM): These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.
MAB[9:0]# MAB[10] MAB[12:11]# MAB[13]	O CMOS	V ₃	Memory Address (EDO/SDRAM): This is the row and column address for DRAM. The 443BX Host Bridge system controller has two identical sets of address lines (MAA and MAB#). The Celeron™ processor mobile module supports only the MAB set of address lines. For additional addressing features, please refer to the <i>Intel® 440BX PCIsset Datasheet</i> .
MWE[A, B]#	O CMOS	V ₃	Memory Write Enable (EDO/SDRAM): MWEA# should be used as the write enable for the memory data bus.
SRAS[A, B]#	O CMOS	V ₃	SDRAM Row Address Strobe (SDRAM): When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge.
SCAS[A, B]#	O CMOS	V ₃	SDRAM Column Address Strobe (SDRAM): When active low, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access.
CKE[A, B]	O CMOS	V ₃	SDRAM Clock Enable (SDRAM): When these signals are deasserted, SDRAM enters power-down mode. CKEB is NC and not used by the system electronics.
MD[63:0]	I/O CMOS	V ₃	Memory Data: These signals are connected to the DRAM data bus. They are not terminated on the Celeron™ processor mobile module.

3.1.3. PCI (56 Signals)

Table 3 lists the PCI interface signals.

Table 3. PCI Signal Description

Name	Type	Voltage	Description
AD[31:0]	I/O PCI	V ₃	Address/Data: The standard PCI address and data lines. The address is driven with FRAME# assertion, and data is driven or received in following clocks.
C/BE[3:0]#	I/O PCI	V ₃	Command/Byte Enable: The command is driven with FRAME# assertion and byte enables corresponding to supplied or requested data are driven on the following clocks.
FRAME#	I/O PCI	V ₃	Frame: Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfers are desired by the cycle initiator.
DEVSEL#	I/O PCI	V ₃	Device Select: The 443BX Host Bridge drives this signal when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O PCI	V ₃	Initiator Ready: Asserted when the initiator is ready for data transfer.
TRDY#	I/O PCI	V ₃	Target Ready: Asserted when the target is ready for a data transfer.
STOP#	I/O PCI	V ₃	Stop: Asserted by the target to request the master to stop the current transaction.
PLOCK#	I/O PCI	V ₃	Lock: Indicates an exclusive bus operation and may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed. The 443BX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
REQ[4:0]#	I PCI	V ₃	PCI Request: PCI master requests for PCI.
GNT[4:0]#	O PCI	V ₃	PCI Grant: Permission is given to the master to use PCI.
PHOLD#	I PCI	V ₃	PCI Hold: This signal comes from the expansion bridge; it is the bridge request for PCI. The 443BX Host Bridge will drain the DRAM write buffers, drain the processor-to-PCI posting buffers, and acquire the host bus before granting the request via PHLDA#. This ensures that GAT timing is met for ISA masters. The PHOLD# protocol has been modified to include support for passive release.
PHLDA#	O PCI	V ₃	PCI Hold Acknowledge: The 443BX Host Bridge drives this signal to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release.
PAR	I/O PCI	V ₃	Parity: A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	I/O PCI	V ₃	System Error: The 443BX asserts this signal to indicate an error condition. Please refer to the <i>Intel® 440BX PCIset Datasheet</i> (Order Number 290633-001) for further information.

CLKRUN#	I/O D PCI	V_3	Clock Run: An open-drain output and input. The 443BX Host Bridge requests the central resource (PIIX4E/M) to start or maintain the PCI clock by asserting CLKRUN#. The 443BX Host Bridge tri-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset).
PCI_RST#	I CMOS	V_3	Reset: When asserted, this signal asynchronously resets the 443BX Host Bridge. The PCI signals also tri-state, compliant with PCI Rev 2.1 specifications.

3.1.4 Processor and PIIX4E/M Sideband (9 Signals)

V_CPUIO, which is supplied in the Celeron™ processor mobile module.

Table 4 lists the processor and PIIX4E/M sideband interface signals. The voltage level for these signals is determined by

Table 4. Processor/PIIX4E/M Sideband Signal Descriptions

Name	Type	Voltage	Description
FERR#	O CMOS	V_CPUIO	Numeric Coprocessor Error: This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the processor and is driven by the processor to the PIIX4E/M.
CPURST	N/C CMOS	V_CPUIO	Processor Reset: The signal is not used in the Celeron™ Processor MMC-1.
IGNNE#	ID CMOS	V_CPUIO	Ignore Error: This open drain signal is connected to the ignore error pin on the processor and is driven by the PIIX4E/M.
INIT#	ID CMOS	V_CPUIO	Initialization: INIT# is asserted by the PIIX4E/M to the processor for system initialization. This signal is an open drain.
INTR	ID CMOS	V_CPUIO	Processor Interrupt: INTR is driven by the PIIX4E/M to signal the processor that an interrupt request is pending and needs to be serviced. This signal is an open drain.
NMI	ID CMOS	V_CPUIO	Non-Maskable Interrupt: NMI is used to force a non-maskable interrupt to the processor. The PIIX4E/M ISA bridge generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. This signal is an open drain.
A20M#	ID CMOS	V_CPUIO	Address Bit 20 Mask: When enabled, this open drain signal causes the processor to emulate the address wraparound at one MB which occurs on the Intel 8086 processor.
SMI#	ID CMOS	V_CPUIO	System Management Interrupt: SMI# is an active low synchronous output from the PIIX4E/M that is asserted in response to one of many enabled hardware or software events. The SMI# open drain signal can be an asynchronous input to the processor. However, in this chip set SMI# is synchronous to PCLK.
STPCLK#	ID CMOS	V_CPUIO	Stop Clock: STPCLK# is an active low synchronous open drain output from the PIIX4E/M that is asserted in response to one of many hardware or software events. STPCLK# connects directly to the processor and is synchronous to PCICLK. When the processor samples STPCLK# asserted it responds by entering a low power state (Quick Start). The processor will only exit this mode when this signal is deasserted.

3.1.5 Power Management (8 Signals)

Table 5 lists the power management interface signals. The SM_CLK and SM_DATA signals refer to the two-wire serial SMBus interface. Although this interface is currently used

solely for the digital thermal sensor, the SMBus contains reserved serial addresses for future use. See section 4.9 for more details.

Table 5. Power Management Signal Descriptions

Name	Type	Voltage	Description
OEM_PU	I CMOS	V_3	OEM Pullup: This pullup resistor is not required on the Intel® Celeron™ processor mobile module. This signal is used by previous Intel mobile module generations.
L2_ZZ	N/C CMOS	V_CPUIO	Low-Power Mode For Cache SRAM: This signal is not used on the Intel® Celeron™ processor mobile module. It is a signal used by previous Intel mobile module generations.
SUS_STAT#	I CMOS	V_3ALWAYS ¹	Suspend Status: This signal connects to the SUS_STAT1# output of PIIX4E/M. It provides information on host clock status and is asserted during all suspend states.
VR_ON	I	V_3S	VR_ON: Voltage regulator ON. This 3.3V (5V tolerant) signal controls the operation of the voltage regulator. VR_ON should be generated as a function of the PIIX4E/M SUSB# signal which is used for controlling the "Suspend State B" voltage planes. This signal should be driven by a digital signal with a rise/fall time of less than or equal to 1 us. (VIL(max)=0.4V, VIH(min)=3.0V). See Figure 5 of this document for proper sequencing of VR_ON.
VR_PWRGD	O	V_3S	VR_PWRGD: This signal is driven high to indicate that the voltage regulator is stable and is pulled low using a 100K resistor when inactive. It can be used in some combination to generate the system PWRGOOD signal.
SM_CLK	I/O D CMOS	V_3	Serial Clock: This clock signal is used on the SMBus interface to the digital thermal sensor. Ensure proper termination based upon the <i>System Management Bus Specification, Revision 1.0</i> .
SM_DATA	I/O D CMOS	V_3	Serial Data: Open-drain data signal on the SMBus interface to the digital thermal sensor. Ensure proper termination based upon the <i>System Management Bus Specification, Revision 1.0</i> .
ATF_INT#	O D CMOS	V_3	ATF Interrupt: This signal is an open-drain output signal of the digital thermal sensor.

NOTE:

V_3ALWAYS: 3.3V supply. It is generated whenever V_DC is available and supplied to PIIX4E/M resume well.

3.1.6 Clock (8 Signals)

Table 6 lists the clock interface signals.

Table 6. Clock Signal Descriptions

Name	Type	Voltage	Description															
OEM_PD	I CMOS	V_3	OEM Pulldown: It is renamed from PCI_REF and this pulldown resistor is not required on the Intel® Celeron™ processor mobile module. It is a signal used by previous Intel mobile module generations.															
PCLK	I PCI	V_3S	PCI Clock In: PCLK is an input to the module from the CKDM66-M clock source and is one of the system's PCI clocks. This clock is used by all of the 443BX Host Bridge logic in the PCI clock domain. This clock is stopped when the PIIX4E/M PCI_STP# signal is asserted and/or during all suspend states.															
HCLK[1:0]	I CMOS	V_CPUIO	Host Clock In: These clocks are inputs to the module from the CKDM66-M clock source and are used by the processor and the 443BX Host Bridge system controller. This clock is stopped when the PIIX4 CPU_STP# signal is asserted and/or during all suspend states.															
SUSCLK	N/C CMOS	V_3	Suspend Clock: This signal is not used on the Intel® Pentium® processor mobile module.															
FQS[1:0]	O CMOS	V_3S	<p>Frequency Status: This signal provides status of the host clock frequency to the system electronics. These signals are static and are pulled either low or high to the V_3S voltage.</p> <table border="1"> <thead> <tr> <th>FQS1</th> <th>FQS0</th> <th>Frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>60 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>66 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table>	FQS1	FQS0	Frequency	0	0	60 MHz	0	1	66 MHz	1	0	Reserved	1	1	Reserved
FQS1	FQS0	Frequency																
0	0	60 MHz																
0	1	66 MHz																
1	0	Reserved																
1	1	Reserved																
CPU3.3_2.5#	O CMOS	V_CPUIO	Clock Voltage Select: Provides status to the system electronics about the voltage level at which the CKDM66-M clock generator should be operating. This signal is pulled low by the Intel® Celeron™ processor mobile module.															

3.1.7 Voltages (39 Signals)

Table 7 lists the voltage signal definitions.

Table 7. Voltage Descriptions

Name	Type	Number	Description
V_DC	I	10	DC Input: 5V - 21V
V_3S	I	20	SUSB# controlled 3.3V: Power-managed 3.3V supply. An output of the voltage regulator on the system electronics. This rail is off during STR, STD, and Soff.
V_5	I	1	SUSC# controlled 5V: Power-managed 5V supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.
V_3	I	5	SUSC# controlled 3.3V: Power-managed 3.3V supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.
V_CPUIO	O	3	Processor I/O Ring: Powers processor interface signals such as the PIIX4E/M open-drain pullups for the processor/PIIX4E/M sideband signals and the CKDM66-M clock source.

3.1.8 JTAG (7 Signals)

Table 8 lists the JTAG signals, which the system electronics can use to implement a JTAG chain and ITP port, if desired. The JTAG signals provided can not be used as an ITP port, since the definition of the ITP interface has changed

between the Pentium® processor and mobile Celeron™ processor generations.

Table 8. JTAG Pins

Name	Type	Voltage	Description
TDO	O	V_CPUIO	JTAG Test Data Out: Serial output port. TAP instructions and data are shifted out of the processor from this port.
TDI	I	V_CPUIO	JTAG Test Data In: Serial input port. TAP instructions and data are shifted into the processor from this port.
TMS	I	V_CPUIO	JTAG Test Mode Select: Controls the TAP controller change sequence.
TCLK	I	V_CPUIO	JTAG Test Clock: Testability clock for clocking the JTAG boundary scan sequence.
TRST#	I	V_CPUIO	JTAG Test Reset: Asynchronously resets the TAP controller in the processor.
ITP(1:0) ITP1 ITP0	O I	V_CPUIO	Debug Port Signals: Currently defined for the generation of Pentium processors. These signals are not used in the Celeron processor mobile module, and should not be connected.

NOTE:

DBREST# (reset target system) on the ITP debug port can be "logically ANDed" with VR_PWRGD TO PIIX4E/M's PWROK.

3.1.9 Miscellaneous (45 Signals)

Table 9 lists the miscellaneous signals.

Table 9. Miscellaneous Pins

Name	Type	Number	Description
Module ID[3:0]	O CMOS	4	Module Revision ID: These pins track the revision level of the Intel® Celeron™ processor module. A 100K pull up resistor to V_3S is required on these signals and to be placed on the system electronics for these signals.
PPP_PP#	O CMOS	1	Celeron™ processor or Pentium processor present: A high on this signal indicates to the PIIx4E/M ISA bridge CONFIG1 pin that the processor module used is based on the Pentium Pro architecture; a low indicates that it is of the Pentium processor family. This signal is allowed to float on Celeron processor mobile modules and requires a 100K pull up resistor to V_3S on the system electronics. This signal is grounded.
Ground	I	32	Ground.
Reserved	RSVD	8	Unallocated Reserved pins and should not be connected.

3.2. Connector Pin Assignments

Table 10 lists the signals for each pin of the MMC-1 to the notebook manufacturer's system electronics. Refer to

Section 3.3 for the pin assignments of the pads on the connector.

Table 10. Connector Pin Assignments

Pin#	Row	Row	Row	Row
	AA	AB	BA	BB
1	Gnd	Gnd	Gnd	Gnd
2	MD31	MD63	MID0	MID1
3	MD30	MD61	Reserved	Reserved
4	MD29	MD62	V DC	V DC
5	MD27	MD58	V DC	V DC
6	V 3S	V 3S	V DC	V DC
7	MD28	MD60	V DC	V DC
8	MD26	MD56	V DC	V DC
9	MD25	MD57	Reserved	Reserved
10	MD24	MD59	MID2	MID3
11	Gnd	Gnd	Gnd	Gnd
12	CAS3#/DQM3	CAS7#/DQM7	AD00	FRAME#
13	CAS6#/DQM6	CAS2#/DQM2	AD01	LOCK#
14	MA00	MA01	AD02	DEVSEL#
15	CKEA	CKEB	AD03	IRDY#
16	V 3S	V 3S	V 3S	V 3S
17	MA02	MA04	AD04	TRDY#
18	MA03	MA05	AD05	STOP#
19	MD55	MD22	AD06	PHOLD#
20	MD54	MD23	AD07	PHLDA#
21	Gnd	Gnd	Gnd	Gnd
22	MD51	MD20	AD08	PCI_RST#
23	MD52	MD21	AD09	PAR
24	MD53	MD19	AD10	SERR#
25	MD49	MD17	AD11	REQ0#
26	V 3S	V 3S	V 3S	REQ1#
27	MD48	MD18	AD12	REQ2#
28	MD50	MD16	AD13	REQ3#
29	SRASA#	SCASA#	AD14	GNT0#
30	SRASB#	SCASB#	AD15	GNT1#
31	Gnd	Gnd	Gnd	Gnd
32	MWEA#	MECC3	AD16	GNT2#
33	MWEB#	MECC7	AD17	GNT3#
34	RAS0#/CS0#	MECC6	AD18	L2_ZZ
35	RAS1#/CS1#	MECC2	AD19	Reserved
36	V 3S	V 3S	V 3S	V 3S
37	MD14	MECC1	AD20	Reserved
38	MD11	MECC5	AD21	PPP_PP#
39	MD15	MECC4	AD22	CLKRUN#
40	Gnd	Gnd	Gnd	Gnd
41	MD10	MECC0	RAS2#/CS2#	SM_CLK
42	MD13	MD43	RAS3#/CS3#	SM_DATA
43	MD09	MD41	RAS4#/CS4#	ATF_INT#
44	MD08	MD45	RAS5#/CS5#	SUSCLK
45	V 3S	V 3S	V 3	V 3

46	MD12	MD42	AD23	SUS_STAT#
47	MA06	MD40	AD24	V_3
48	MA07	MD44	AD25	OEM_PU
49	MA08	MD46	AD26	VR_ON
50	Gnd	Gnd	Gnd	Gnd
51	MA09	MD47	AD27	VR_PWRGD
52	CAS1#/DQM1	CAS5#/DQM5	AD28	V_3
53	CAS4#/DQM4	CAS0#/DQM0	AD29	V_3
54	MA10	MA12	AD30	Reserved
55	V_3S	V_3S	V_3S	Reserved
56	MA11	MA13	AD31	INIT#
57	MD39	MD07	C/BE0#	V_CPUIO
58	MD37	MD02	C/BE1#	INTR
59	MD38	MD00	C/BE2#	CPURST
60	Gnd	Gnd	Gnd	Gnd
61	MD36	MD04	C/BE3#	STPCLK#
62	MD33	MD01	IGNNE#	SMI#
63	MD35	MD03	FERR#	NMI
64	MD32	MD06	A20M#	V_5
65	MD34	MD05	V_CPUIO	V_CPUIO
66	V_3S	V_3S	TDO	TRST#
67	OEM_PD	PCLK	ITP0	TDI
68	FQS0	FQS1	ITP1	TMS
69	HCLK1	HCLK0	CPU3.3_2.5#	TCLK
70	Gnd	Gnd	Gnd	Gnd

3.3 Pin and Pad Assignments

The Celeron™ processor MMC-1 is a surface mount, 0.6-mm pitch, and 280-pin connector. There are currently three different sized mating connector receptacles offered for the Celeron processor mobile module. See section 5.1.4. *Height Restrictions* or contact your local Intel sales representative for more information.

Figure 2 shows the connector pad assignments for the manufacturer's system electronics. This footprint is viewed from the secondary side of the Celeron processor module (the side of the printed circuit board on which the 280-pin connector is soldered).

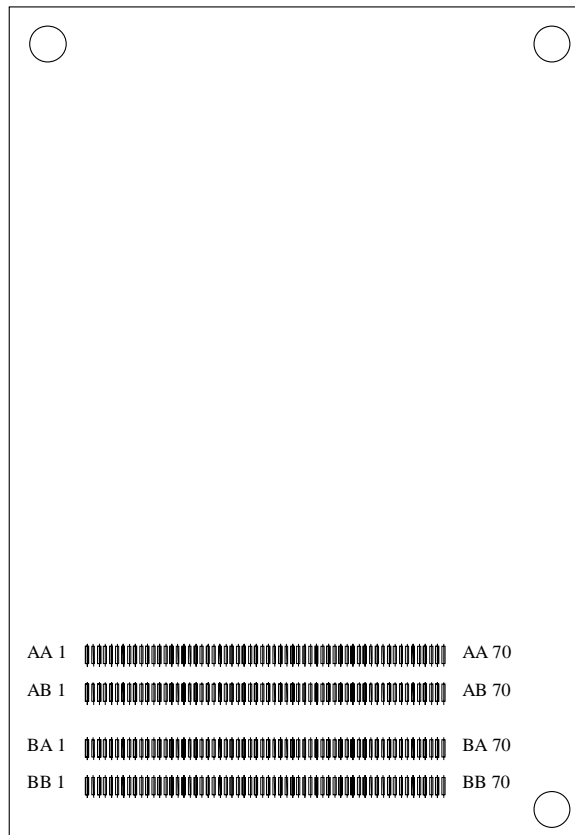


Figure 2. 280-Pin Connector Footprint Pad Numbers, Module Secondary Side



Table 11 summarizes the key specifications for the MMC-1.

Table 11. Connector Specifications

Parameter	Condition	Specification
Material	Contact	Copper Alloy
	Housing	Thermo Plastic Molded Compound: LCP
Electrical	Current	0.5 A
	Voltage	50 VAC
	Insulation Resistance	100 MΩ min. at 500 VDC
	Termination Resistance	20 mΩ max. at 20 mV open circuit with 10 mA
	Capacitance	5 pF max. per contact
Mechanical	Mating Cycles	50 cycles
	Connector Mating Force	0.9N (90 gf) max. per contact
	Contact Un-mating Force	0.1N (10 gf) min. per contact

4.0. FUNCTIONAL DESCRIPTION

4.1. Celeron processor mobile module

The Celeron™ processor mobile module supports the Mobile Celeron processor core with on-die L2 cache, the 443BX Host Bridge System Controller and system level support. The mobile Celeron processor runs at 300 MHz and 266 MHz, with a 66-MHz system bus speed.

power consumption while the system is idle, the internal 443BX Host Bridge clock is turned off (gated off) when there is no processor and PCI activity. This is accomplished by setting the G_CLK enable bit in the power management register in the 443BX through the system BIOS.

Celeron™ processor mobile modules support only the 443BX Host Bridge features in mobile compatible mode. Refer to Intel's latest revision of the 443BX Host Bridge specification for complete details.

4.2. L2 Cache

The Mobile Celeron™ processor has 128K of on-die L2 cache that is 4-way set associative and runs at the speed of the processor core.

4.3.1. Memory Organization

The memory interface of the 443BX Host Bridge is available at the MMC-1. The 443BX Host Bridge standard mode, memory configurations, and modes of operation are supported on the MMC-1 signaling interface. This allows the memory interface to support the following:

4.3. The 443BX Host Bridge System Controller

Intel's® 443BX Host Bridge system controller combines the mobile Celeron™ processor bus controller, the DRAM controller, and the PCI bus controller into one component. The 443BX Host Bridge has multiple power management features designed specifically for notebook systems such as:

- CLKRUN#, a feature that enables controlling of the PCI clock on or off.
- The 443BX Host Bridge suspend modes, which include Suspend-to-RAM (STR), Suspend-to-Disk (STD), and Powered-On-Suspend (POS).
- System Management RAM (SMRAM) power management modes, which include Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). C_SMRAM is the traditional SMRAM feature implemented in all Intel PCI chipsets. E_SMRAM is a new feature that supports write-back cacheable SMRAM space up to 1 MB. To minimize

- One set of memory control signals, sufficient to support up to three SO_DIMM sockets and six banks of SDRAM at 66 MHz.
- One CKE signal for each bank.

Memory features not supported by the 443BX Host Bridge system controller standard MMC-1 mode are:

- Support for eight banks of memory.
- Second set of memory address lines (MAA[13:0]).
- 100 MHz SDRAM (and PSB).
- Accelerated Graphics Port (AGP).

DRAM technologies supported by the 443BX Host Bridge system controller include EDO and SDRAM. These memory types should not be mixed in the system, so that all DRAM in

all rows (RAS[5:0]#) must be of the same technology. The 443BX Host Bridge system controller targets 60-ns EDO DRAMs, and 66-MHz SDRAMs.

The Celeron™ processor mobile module's clocking architecture supports the use of SDRAM. Due to the tight timing requirements of 66-MHz SDRAM clocks, the clocking mode for SDRAM or the system manufacturer custom memory configurations allows all host and SDRAM clocks to be generated from the same clocking architecture on the OEM's system electronics. For complete details about using SDRAM memory, and for trace length guidelines, refer to the *Mobile Pentium® II processor / 82443BX PCIsset Advanced Platform Recommended Design and Debug Practices*. For

details on memory device support, organization, size, and addressing refer to the *Intel® 440BX PCIsset Datasheet*.

4.3.2. Reset Strap Options

Several strap options on the memory address bus define the behavior of the Celeron™ processor mobile module after reset. Other straps are allowed to override the default settings. Table 14 shows the various straps and their implementation.

Other straps are allowed to override the default settings. Table 14 shows the various straps and their implementation on the Celeron processor mobile module.

Table 12. Configuration Straps for the 443BX Host Bridge System Controller

Signal	Function	Module Default Setting
MAB[12]#	Host Frequency Select	No strap. (66 MHz default).
MAB[11]#	In order queue depth	No strap. (Maximum Queue Depth is set (i.e. 8).
MAB[10]	Quick Start Select	Strapped high on the module for Quick Start mode.
MAB[9]#	AGP disable	Strapped to disable AGP.
MAB[7]#	MM Config	Strapped for MMC-1 compatible mode.
MAB[6]#	Host Bus Buffer Mode Select	Strapped high on the module for mobile FSB buffers.

4.3.3. PCI Interface

The PCI interface of the 443BX Host Bridge is available at the MMC-1. The 443BX Host Bridge supports the PCI Clockrun protocol for PCI bus power management. In this protocol, PCI devices assert the CLKRUN# open-drain signal when they require the use of the PCI interface. Refer to the *PCI Mobile Design Guide* for complete details on the PCI Clockrun protocol.

The 443BX Host Bridge is responsible for arbitrating the PCI bus. In MMC-1 mode, the 443BX Host Bridge can only support up to five PCI bus masters. There are five PCI Request/Grant pairs, REQ[4:0]# and GNT[4:0]#, available on the MMC-1 to the manufacturer's system electronics.

The PCI interface on MMC1 is 3.3V only. All devices that drive outputs to a 5V nominal Voh level are not supported.

The 443BX Host Bridge system controller is compliant with the PCI 2.1 specification, which improves the worst case PCI bus access latency from earlier PCI specifications. As detailed in the PCI specification, the 443BX Host Bridge supports only Mechanism #1 for accessing PCI configuration space. This implies that signals AD[31:11] are available for PCI IDSEL signals. However, since the 443BX Host Bridge is always device #0, AD11 will never be asserted during PCI configuration cycles as an IDSEL. The 443BX reserves AD12 for the AGPbus, which is not supported by MMC-1.

Thus, AD13 is the first available address line usable as an IDSEL. AD18 should be used by the PIIX4E/M.

4.3.4. AGP Feature Set

The Intel® Celeron™ MMC-1 family does not support the AGP graphics port interface. However, the MMC-2 supports the AGP interface. Refer to the *Celeron Processor Mobile Module: Mobile Module Connector 2 (MMC-2) Datasheet*.

4.4. Power Management

4.4.1. Clock Control Architecture

The Celeron™ processor mobile module's clock control architecture (Figure 3) is optimal for notebook designs. The Auto Halt state provides a low power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low power, low exit latency clock state that can be used for hardware controlled "idle" computer states. The Deep Sleep State

provides an extremely low power state that can be used for "Power-on Suspend" computer states, which is an alternative to shutting off the processor's power.

Compared to the Pentium® processor mobile module exit latency of 1 msec, the exit latency of the Deep Sleep state has been reduced to 30 µsec in the Celeron™ processor mobile module. The Stop Grant states and Sleep states shown in Figure 3 are intended for use in "Deep Green" desktop and server systems – not in mobile systems. Performing state transitions not shown in Figure 3 is neither recommended nor supported.

The clock control architecture consists of seven different clock states: Normal, Stop Grant, Auto Halt, Quick Start, HALT/Grant Snoop, Sleep, and Deep Sleep states. The Stop Grant and Quick Start clock states are mutually exclusive, for example a strapping option on signal A15# chooses which state is entered when the STPCLK# signal is asserted. Strapping the A15# signal to ground at Reset enables the Quick Start state. Otherwise, asserting the STPCLK# signal puts the Celeron processor into the Stop Grant state. The Stop Grant state has a higher power level than the Quick Start state and is designed for SMP platforms. The Quick Start state has a much lower power level, but it can only be used in uniprocessor (UP) platforms.

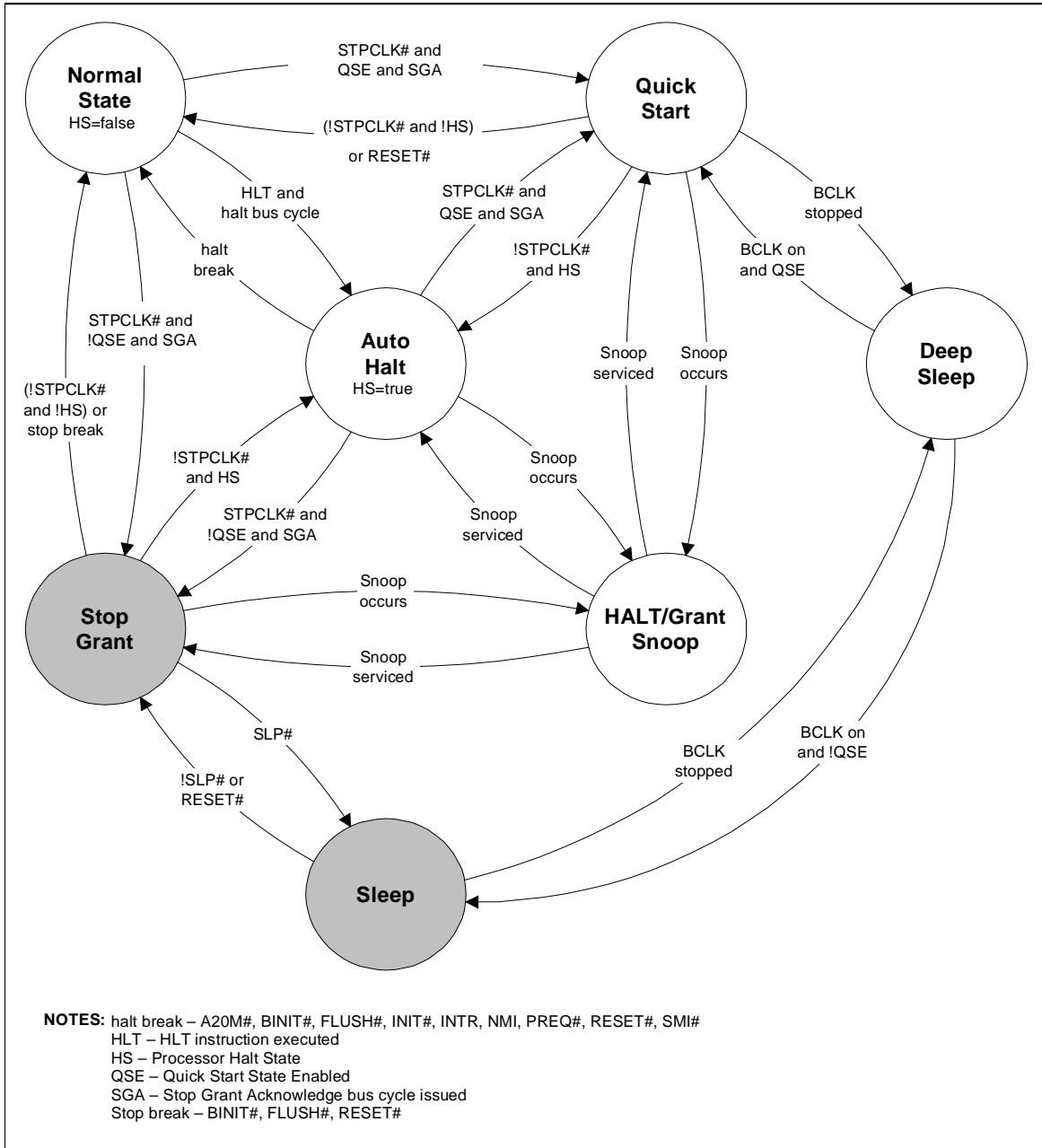


Figure 3. Celeron™ Processor Mobile Module Clock Control States

4.4.2. Normal State

This is the normal operating mode for the mobile Celeron™ processor. The processor's core clock is running and the processor is actively executing instructions.

4.4.3. Auto Halt State

This is a low power mode entered by the processor through the execution of the HLT instruction. The power level of this mode is similar to the Stop Grant state. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH#, or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Stop Grant or Quick Start state, which issues a Stop Grant Acknowledge bus cycle. Deasserting STPCLK# will cause the processor to return to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# (System Management Interrupt) is recognized in the Auto Halt state. The return from SMI handler can be to either the Normal state or the Auto Halt state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information. No Halt bus cycle is issued when returning to the Auto Halt state from System Management Mode (SMM).

The FLUSH# signal is serviced in the Auto Halt state. After flushing the on-chip, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# and PREQ# signals are recognized while in the Auto Halt state.

4.4.4. Stop Grant State

The processor enters this mode with the assertion of the STPCLK# signal when it is configured for Stop Grant state (via the A15# strapping option). The processor is still able to respond to snoop requests and latch interrupts. Latched interrupts will be serviced when the processor returns to the Normal state. Only one occurrence of each interrupt event will be latched. A transition back to the Normal state can be made by the deassertion of the STPCLK# signal or the occurrence of a stop break event (a BINIT#, FLUSH#, or RESET# assertion).

The processor will return to the Stop Grant state after the completion of a BINIT# bus initialization unless STPCLK# has been deasserted. RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Stop Grant state after initialization until STPCLK# is deasserted. If the FLUSH# signal is asserted, the processor will flush the on-chip caches and return to the Stop Grant state. A transition to the Sleep state can be made by the assertion of the SLP# signal.

While in the Stop Grant state, assertions of SMI#, INIT#, INTR, and NMI (or LINT[1:0]) will be latched by the processor. These latched events will not be serviced until the

processor returns to the Normal state. Only one of each event will be recognized upon return to the Normal state.

Intel mobile modules do not support the Stop Grant state.

4.4.5. Quick Start State

This is a mode entered by the processor with the assertion of the STPCLK# signal when it is configured for the Quick Start state (via the A15# strapping option). In the Quick Start state the processor is only capable of acting on snoop transactions generated by the system bus priority device. Because of its snooping behavior, Quick Start can only be used in UP configuration. A transition to the Deep Sleep state can be made by stopping the clock input to the processor. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupts, servicing snoop transactions from symmetric bus masters, or responding to FLUSH# or BINIT# assertions. While the processor is in the Quick Start state, it will not respond properly to any input signal other than STPCLK#, RESET#, or BPRt#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

4.4.6. HALT/Grant Snoop State

The processor will respond to snoop transactions on the system bus while in the Auto Halt, Stop Grant, or Quick Start state. When a snoop transaction is presented on the system bus the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop has been serviced and the system bus is quiet. After the snoop has been serviced, the processor will return to its previous state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state, except for those signal transitions that are required to perform the snoop.

4.4.7. Sleep State

The Sleep state is a very low power state in which the processor maintains its context and the phase-locked loop (PLL) maintains phase lock. The Sleep state can only be entered from the Stop Grant state. After entering the Stop Grant state the SLP# signal can be asserted, causing the processor to enter the Sleep state. The SLP# signal is not recognized in the Normal or Auto Halt states.

The processor can be reset by the RESET# signal while in the Sleep state. If RESET# is driven active while the processor is in the Sleep state then SLP# and STPCLK# must immediately be driven inactive to ensure that the processor correctly initializes itself.

Input signals (other than RESET#) may not change while the processor is in the Sleep state or transitioning into or out of the Sleep state. Input signal changes at these times will cause unpredictable behavior. Thus, the processor is incapable of snooping or latching any events in the Sleep state.

While in the Sleep state the processor can enter its lowest power state, the Deep Sleep state. Removing the processor's input clock puts the processor in the Deep Sleep state. PICCLK may be removed in the Sleep state.

Intel mobile modules do not support the Sleep state.

processor can enter while maintaining its context. The Deep Stopping the BCLK input to the processor enters sleep state, while it is in the Sleep state or Quick Start state. For proper operation, the BCLK input should be stopped in the low state.

The processor will return to the Sleep state or Quick Start state from the Deep Sleep state when the BCLK input is restarted. Due to the PLL lock latency, there is a 30-msec delay after the clocks have started before this state transition happens. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK turns on when transitioning out of the Deep Sleep state.

The input signal restrictions for the Deep Sleep state are the same as for the Sleep state, except that RESET# assertion will result in unpredictable behavior.

4.4.8. Deep Sleep State

The Deep Sleep state is the lowest power mode the

Table 13. Mobile Celeron™ Processor Clock State Characteristics

Clock State	Exit Latency	Processor Power	Snooping ?	System Uses
Normal	N/A	Varies	Yes	Normal program execution.
Auto Halt	Approximately 10 bus clocks	1.2 W	Yes	S/W controlled entry idle mode.
Stop Grant	10 bus clocks	1.2 W	Yes	H/W controlled entry/exit mobile throttling.
Quick Start	Through snoop, to HALT/Grant Snoop state: immediate Through STPCLK#, to Normal state: 10 bus clocks	0.5 W	Yes	H/W controlled entry/exit mobile throttling.
HALT/Grant Snoop	A few bus clocks after the end of snoop activity.	Not specified	Yes	Supports snooping in the low power states.
Sleep	To Stop Grant state 10 bus clocks	0.5 W	No	H/W controlled entry/exit desktop idle mode support.
Deep Sleep	30 msec	150 mW	No	H/W controlled entry/exit mobile powered-on suspend support.

NOTE:

Not 100% tested. Specified at 50°C by design/characterization.

4.5. Typical POS/STR Power

Table 14 shows the POS/STR Typical power.

Table 14. Mobile Celeron Processor POS/STR Power

State	Typical MMC1 Power
POS	0.475A
STR	0.018A

NOTE:

These are average values of measurement on several typical modules and are guidelines only.

4.6. Electrical Requirement

ensure compliance with the Celeron™ processor mobile module DC power requirements.

The following section provides information on the DC requirements for the Celeron™ processor mobile module.

4.6.1. DC Requirements

Please refer to Table 15 for power supply design criteria to

Table 15. Celeron™ Processor Mobile Module Power Specifications 1

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V _{DC}	DC Input Voltage	5.0	12.0	21.0	V	
I _{DC}	DC Input Current	0.1	0.9	3.5	A	2,3
I _{DC-Surge}	Maximum Surge Current for V _{DC}			17.3	A	
I _{DC-Leakage}	Typical Leakage Current for V _{DC}		4.0		μA	(at 25°C), 4
V ₅	Power Managed 5V Voltage Supply	4.75	5.0	5.25	V	
I ₅	Power Managed 5V Current	17	32	60	mA	
I _{5-Surge}	Maximum Surge Current for V ₅			0.6	mA	
I _{5-Leakage}	Typical Leakage Current for V ₅		1.0		μA	
V ₃	Power Managed 3.3V Voltage Supply	3.135	3.3	3.465	V	
I ₃	Power Managed 3.3V Current	0.8	1.2	2.0	A	
I _{3-Surge}	Maximum Surge Current for V ₃			2.8	A	
I _{3-Leakage}	Typical Leakage Current for V ₃		1.1		mA	
V _{CPUPU}	Processor I/O Ring Voltage	2.375	2.5	2.625	V	±0.125
I _{CPUPU}	Processor I/O Ring Current	0	10	20	mA	5
V _{CLK}	Processor Clock Rail Voltage	2.375	2.5	2.625	V	±0.125
I _{CLK}	Processor Clock Rail Current	24.0	35.0	80.0	mA	5

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel mobile module frequencies.
2. V_{DC} is set for 12V in order to determine typical V_{DC} current.
3. V_{DC} is set for 5V in order to determine maximum V_{DC} current.
4. Leakage current that can be expected when VR_ON is deactivated and V_{DC} is still applied.
5. These values are system dependent.

4.6.2 AC Requirements

Please refer to Table 16 for the BCLK AC requirements for the Celeron™ processor mobile module.

Table 16. Celeron™ Processor Mobile Module AC Specifications (BCLK) at the Processor Core Pins 1, 2, 3

T#	Parameter	Min	Nom	Max	Unit	Figure	Notes
	System Bus Frequency		66.67		MHz		All processor core frequencies ⁴
T1:	BCLK Period		15.0		ns		4, 5
T2:	BCLK Period Stability			±250	ps		6, 7, 8
T3:	BCLK High Time	5.3			ns		At >1.8V
T4:	BCLK Low Time	5.3			ns		At <0.7V
T5:	BCLK Rise Time	0.175		0.875	ns		(0.9V-1.6V) ⁸
T6:	BCLK Fall Time	0.175		0.875	ns		(1.6V-0.9V) ⁸

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel mobile modules.
2. All AC timings for the GTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25V at the processor core pins.
4. The internal core clock frequency is derived from the system bus clock. The system bus clock to core clock ratio is determined during initialization as described and is predetermined by the Dixon processor [.18 micron] mobile module.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation. See the *CK97 Clock Synthesizer/Driver Specification* for further information.
6. Measured on the rising edge of adjacent BCLKs at 1.25V. The jitter present must be accounted for as a component of BCLK skew between devices.
7. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The -20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the *CK97 Clock Synthesizer/Driver Specification* for further details.
8. Not 100% tested. Specified by design characterization as a clock driver requirement.

4.6.2.1. System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines

Table 17 describes the signal quality specifications at the processor core for the system bus clock (BCLK) signal.

Figure 4 describes the signal quality waveform for the BCLK at the processor core pins.

Table 17. BCLK Signal Quality Specifications at the Processor Core

T#	Parameter	Min	Nom	Max	Unit	Figure	Notes
V1:	BCLK V_{IL}			0.7	V	4	2
V2:	BCLK V_{IH}	1.8			V	4	2
V3:	V_{IN} Absolute Voltage Range	-0.8		3.5	V	4	3
V4:	Rising Edge Ringback	1.8			V	4	4
V5:	Falling Edge Ringback			0.7	V	4	4
	BCLK rising/falling slew rate	0.8		4	V/ns		

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel mobile modules.
2. BCLK must rise/fall monotonically between $V_{IL,BCLK}$ and $V_{IH,BCLK}$.
3. This is the mobile Celeron™ processor system bus clock overshoot and undershoot specification for 66-MHz system bus operation.
4. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits.
5. For proper signal termination, refer to the Clocking Guidelines in the Mobile Pentium II Processor / 440BX PCISet Advanced Platform Recommend Design and Debug Practices.

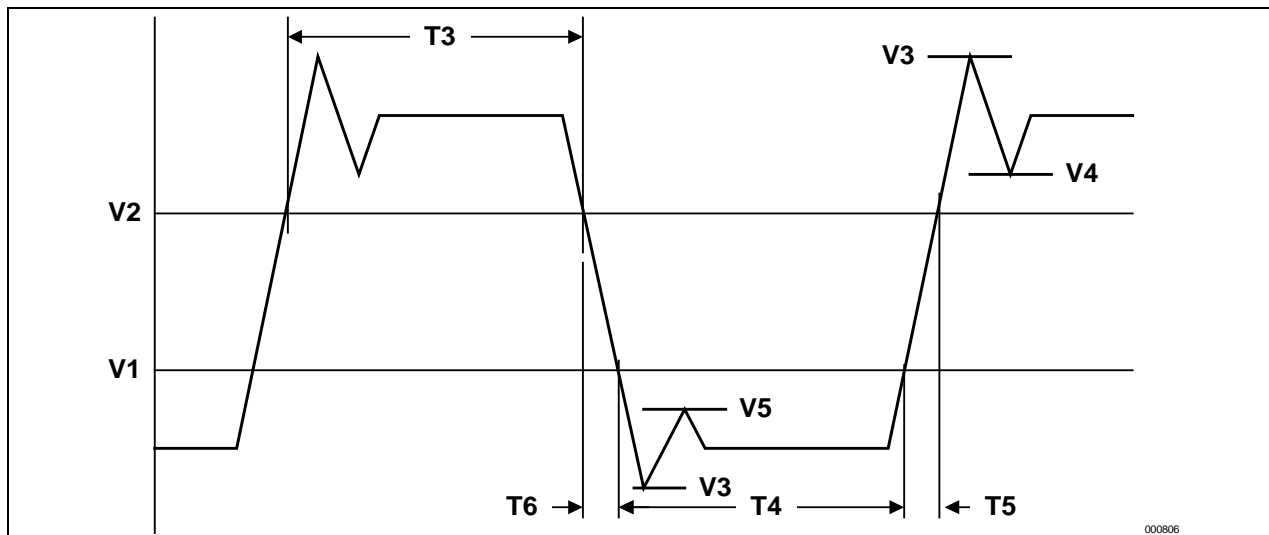


Figure 4. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pin

sideband signal pullup voltage for the Celeron™ processor mobile module. The voltage range is 5V – 21V.

4.7. The Voltage Regulator

The DC voltage regulator (DC/DC converter) provides the appropriate core voltage, the I/O ring voltage, and the

4.7.1. Voltage Regulator Efficiency

Table 18 lists the voltage regulator efficiencies.

Table 18. Typical Voltage Regulator Efficiency

I _{core} , A ³	V _{DC} , V	I _{DC} , A ²	Efficiency ¹
1	5.0	0.370	82.8%
2	5.0	0.702	88.8%
3	5.0	1.044	89.8%
4	5.0	1.404	89.7%
5	5.0	1.762	88.1%
6	5.0	2.144	86.4%
7	5.0	2.528	85.0%
1	12.0	0.159	79.7%
2	12.0	0.295	87.0%
3	12.0	0.438	87.8%
4	12.0	0.584	87.3%
5	12.0	0.736	86.1%
6	12.0	0.890	84.9%
7	12.0	1.043	83.8%
1	21.0	0.091	79.3%
2	21.0	0.170	86.0%
3	21.0	0.253	87.3%
4	21.0	0.340	85.3%
5	21.0	0.429	84.1%
6	21.0	0.519	82.9%
7	21.0	0.617	80.7%

NOTES:

1. These efficiencies will change with future voltage regulators that accommodate wider ranges of input voltages.
2. With V_{DC} applied and the voltage regulator off, typical leakage is 0.3 mA with a maximum of 0.7 mA.
3. I_{core} indicates the CPU core current being drawn during test and measurement.

4.7.2. Control of the Voltage Regulator

The VR_ON pin turns the DC voltage regulator on or off. The VR_ON pin should be controlled as a function of the SUSB#, which controls the system's power planes. VR_ON should switch high only when the following conditions are met: V_{5(s)} => 4.5V and V_{DC} => 4.75V.

CAUTION- Turning on VR_ON prior to meeting these conditions will severely damage the Celeron™ processor mobile module.

The VR_PWRGD signal indicates that the voltage regulator power is operating at a stable voltage level. Use VR_PWRGD on the system electronics to control power inputs and to gate PWROK to the PIIX4E/M.

Table 19 lists the voltage signal definitions and sequences, and Figure 5 shows the signal sequencing and the voltage planes sequencing required for normal operation of the Celeron processor mobile module.

4.7.2.1. Voltage Signal Definition and Sequencing
Table 19. Voltage Signal Definitions and Sequences

Signal	Source	Definitions and Sequences
V_DC	System Electronics	DC voltage is driven from the power supply and is required to be between 5V and 21V DC. V_DC powers the Celeron™ processor mobile module's DC-to-DC converter for processor core and I/O voltages. It cannot be hot inserted or removed while V_DC is powered on.
V_3	System Electronics	V_3 is supplied by the system electronics for the 443BX.
V_5	System Electronics	V_5 is supplied by the system electronics for the 443BX's 5V-reference voltage and the voltage regulator.
V_3S	System Electronics	V_3S is supplied by the system electronics for the L2 cache devices. Each must be powered off during system STR and STD states.
VR_ON	System Electronics	Enables the voltage regulator circuit. When driven active high (3.3V) the voltage regulator circuit on the Mobile Module is activated. The signal driving VR_ON should be a digital signal with a rise/fall time of less than or equal to 1 μ s. (VIL (max)=0.4V, VIH (min)=3.0V). See notes below
V_CORE (also used as host bus GTL+ termination voltage VTT)	Celeron processor mobile module Only; not on module interface.	A result of VR_ON being asserted, V_CORE is an output of the DC-DC regulator on the Mobile Module and is driven to the core voltage of the processor. It is also used as the host bus GTL+ termination voltage, known as VTT.
V_BSB_IO	Celeron processor mobile module	V_BSB_IO is 1.8V. The system electronics uses this voltage to power the L2 cache-to-processor interface circuitry.
VR_PWRGD	Celeron processor mobile module	Upon sampling the voltage level of V_CORE (minus tolerances for ripple), VR_PWRGD is driven active high. If VR_PWRGD is not sampled active within 1 sec. of the assertion of VR_ON, then the system electronics should deassert VR_ON. After Vcore is stabilized, VR_PWRGD will assert to logic high (3.3V). This signal <i>must not be pulled up</i> by the system electronics. VR_PWRGD should be "ANDed" with V_3s to generate the PIIX4E/M input signal, PWROK. The system electronics should monitor VR_PWRGD to verify it is asserted high prior to the active high assertion of PIIX4E/M PWROK.
V_CPUIO	Celeron processor mobile module	V_CPUIO is 2.5V. The system electronics uses this voltage to power the PIIX4E/M-to-processor interface circuitry, as well as the HCLK(0:1) drivers for the processor clock.

NOTES:

1. The VR_ON signal may only be asserted to a logical high by a digital signal only after V_DC \geq 4.7V, V_5 \geq 4.5V, and V_3 \geq 3.0V.
2. The rise time and fall time of VR_ON must be less than or equal to 1 μ s when it goes through its Vil to Vih.
3. VR_ON has its Vil (max) = +0.4V and Vih (min) = + 3.0V.
4. VR_ON needs to rise monotonically through its Vil to Vih points.
5. VR_ON needs to provide an instantaneous in-rush current to the module with the following values: an instantaneous max. of 41 mA with a typical of 0.2 mA; a DC operating max. of 0.1 μ A with a typical of 0.0.
6. In going from a valid on to valid off and then back on, VR_ON must be low for 1 ms. In addition, the original voltage level requirements for turn-on always need to be met before assertion of VR_ON (i.e. V_DC \geq 4.7V, V5 \geq 4.5V, V_3 \geq 3.0V).

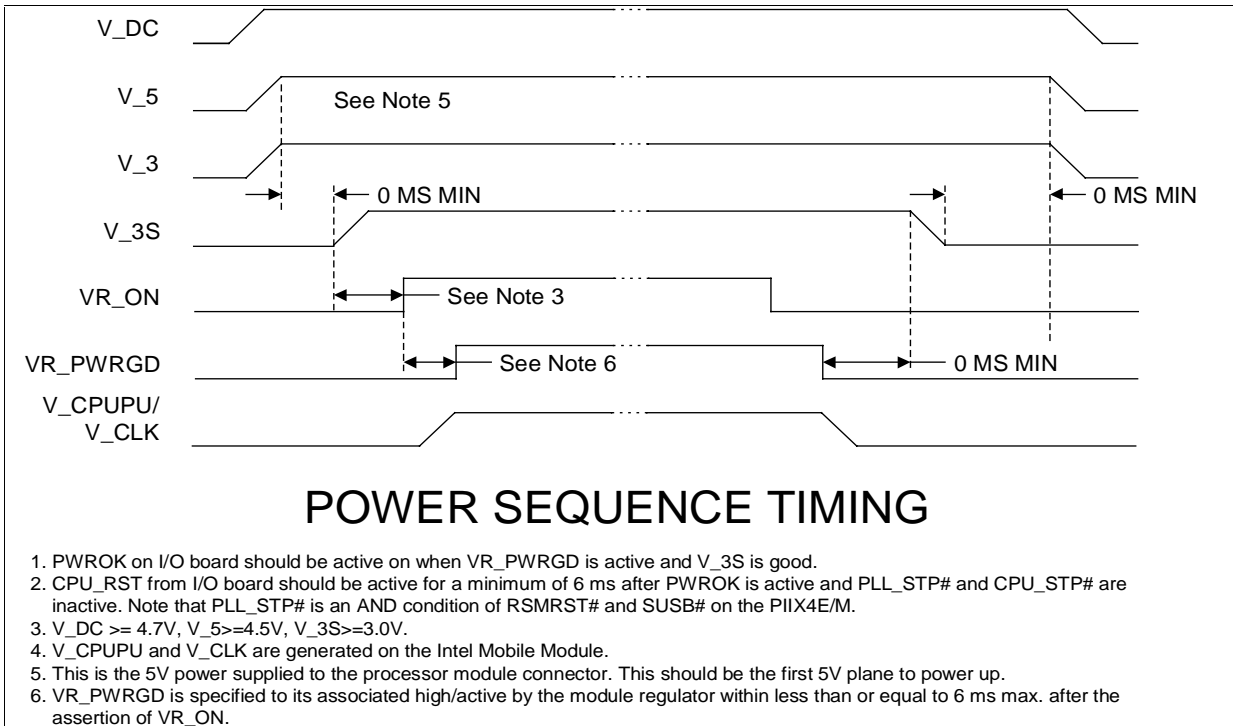


Figure 5. Power-On Sequence Timing

In the power-on process, Intel recommends that the higher voltage power plane is raised first (V_DC), followed by the lower power planes (V_5 and V_3), and finally the assertion of VR_ON after above voltage levels are met on all rails. In the power-off process, the reverse applies so that first VR_ON is deasserted, followed by the lower power planes, and finally the higher power plane.

required. A small amount of bulk capacitance is supplied on the Celeron™ processor mobile module. However, in order to achieve proper filtering additional capacitance should be placed on the system electronics.

Table 20 details the bulk capacitance requirements for the system electronics when using the Celeron processor mobile module.

4.7.3. Power Planes: Bulk Capacitance Requirements

In order to provide adequate filtering and in-rush current protection for any system design, bulk capacitance is

Table 20. Capacitance Requirements per Power Plane

Power Plane	Capacitance Requirements	ESR	Ripple Current	Rating
V_DC	100 uf, 0.1 uf, 0.01 uf ¹	20 mΩ	1-3.5A ³	20% tolerance at 35V
V_5	100 uf, 0.1 uf, 0.01 uf ¹	100 mΩ	1A	20% tolerance at 10V
V_3	470 uf, 0.1 uf, 0.01 uf ¹	100 mΩ	1A	20% tolerance at 6V
V_3S	100 uf, 0.1 uf, 0.01 uf ¹	100 mΩ	N/A	20% tolerance at 6V
V_CPUIO	2.2 uf, 8200 pf ¹	n/a	n/a	20% tolerance at 6V

NOTES:

1. Placement of above capacitance requirements should be located near the MMC-1.
2. V_CPUIO filtering should be located next to the system clock synthesizer.
3. Ripple current specification depends on V_DC input. For 5.0V V_DC, a 3.5A device is required. For V_DC at 18V or higher, 1A is sufficient.

4.7.4. Surge Current Guidelines

This section provides the results of a worst case, surge current analysis. The analysis determines the maximum amount of surge current that the Celeron™ processor mobile module can manage.

In the analysis, the Celeron processor mobile module has two 4.7 μf with an ESR of 0.15Ω total. The MMC-1 is approximately 30 mΩ of series resistance, for a total series resistance of .18Ω. If the user powers the system with the

A/C adapter (18V), the amount of surge current on the module would be approximately 100A.

This information is also used to develop I/O bulk capacitance requirements (See Table 20).

NOTE: Depending on the system electronics design, different impedances may yield different results. The OEM should perform a thorough analysis to understand the implications of surge current on their system.

Figure 6 shows an electrical model used when analyzing instantaneous power-on conditions and figure 7 illustrates the results with a SPICE simulation.

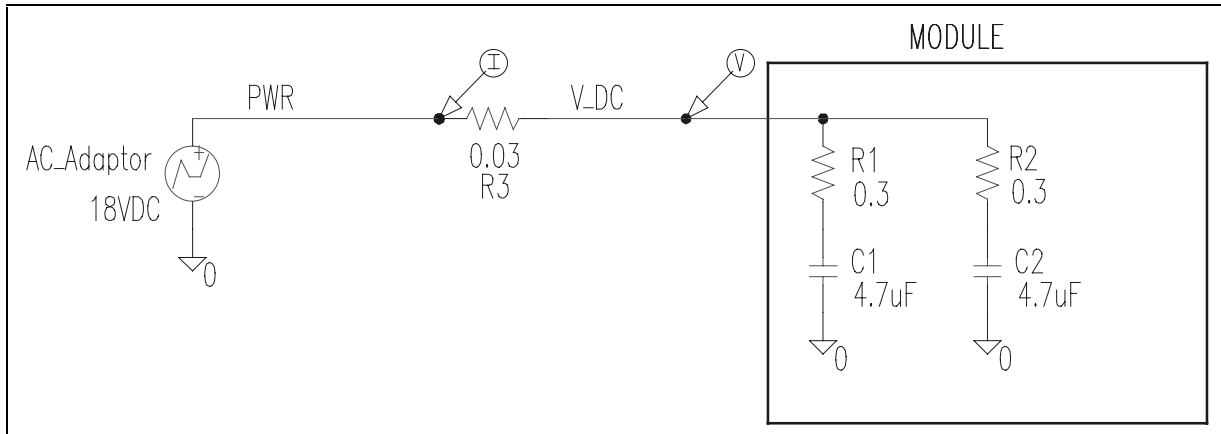


Figure 6. Instantaneous In-Rush Current Model

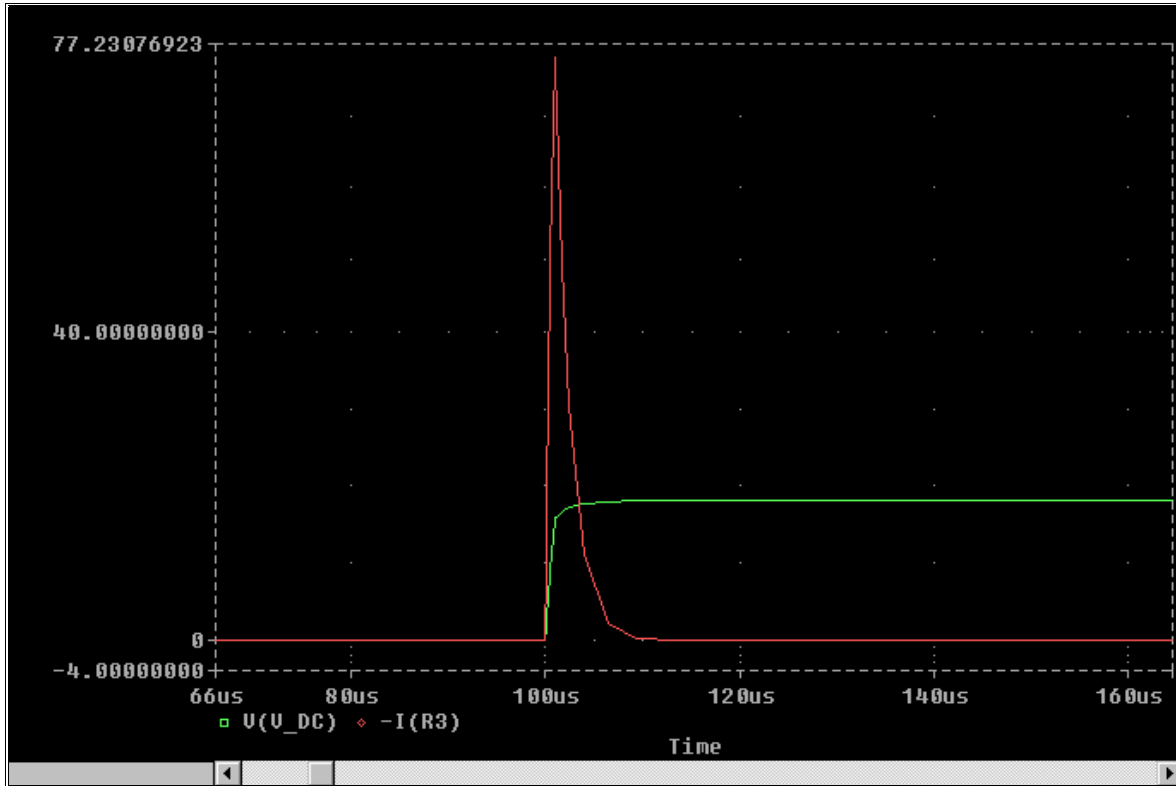


Figure 7. Instantaneous In-Rush Current

Due to the stringent component height requirements of the Celeron™ processor mobile module, Polymerized Organic Semiconductor capacitors must be used as input bulk capacitance in the voltage regulator circuit. Because of the capacitor's susceptibility to high in-rush current, special care

must be taken. One way to soften the in-rush current and provide over-voltage and over-current protection is to ramp up V_{DC} slowly using a circuit similar to the one shown in Figure 8.

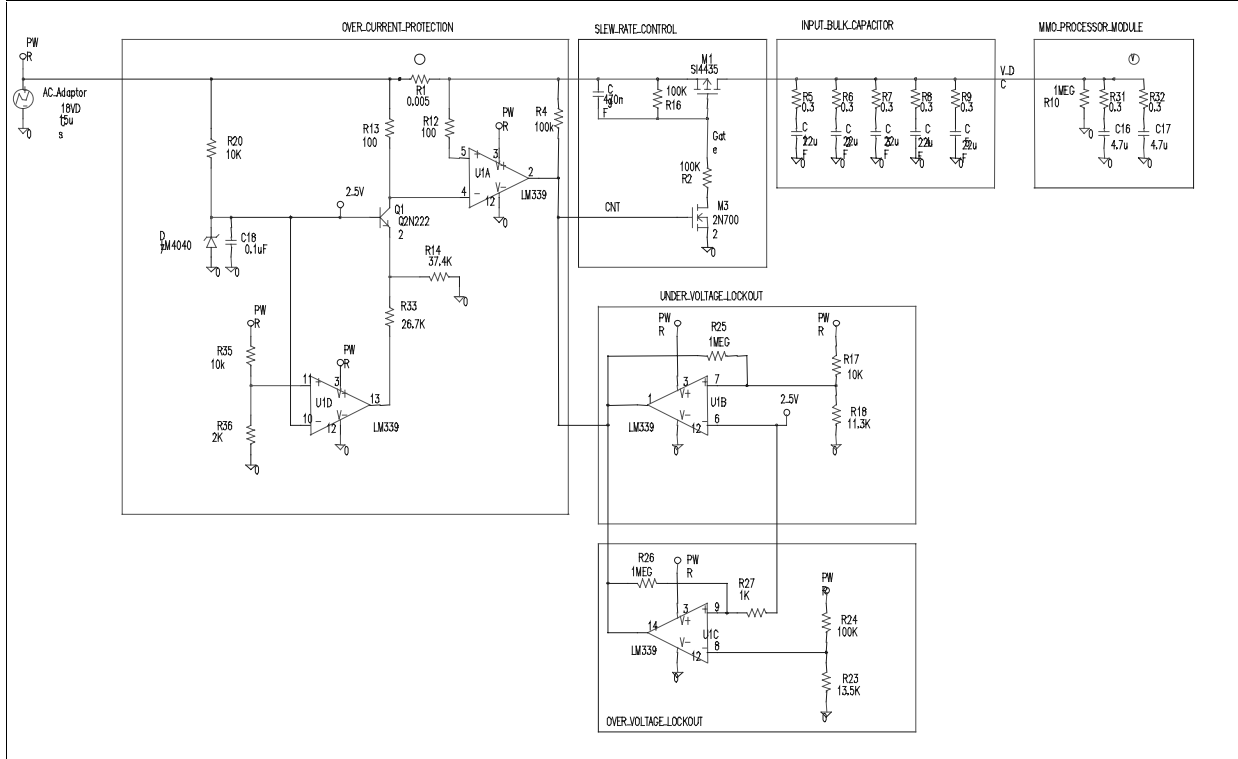


Figure 8. Over-Current Protection Circuit

NOTE:

Values shown are for reference only.

4.7.4.1. Slew-Rate Control: Circuit Description

In Figure 8, PWR is the voltage generated by applying the AC Adaptor or Battery. M1 is a low RDS (on) P-Channel MOSFET such as a Siliconix® Si4435DY. When the voltage on PWR is applied and increased to over 4.75V, the

UNDER_VOLTAGE_LOCKOUT circuit allows R4 to pull up the gate of M3 to start a turn-on sequence. M3 pulls its drain toward ground, forcing current to flow through R2. M1 will not start to source any current until after t_delay with t_delay defined as:

$$t_delay := -R2 \cdot C9 \cdot \ln\left(1 - \frac{Vt}{Vpwr - Vgs_max}\right)$$

$$Vgs_max = \frac{R16}{R16 + R2} \cdot Vpwr$$

The manufacturer's Vgs_max specification of 20V must never be exceeded. However, Vgs_max must be high enough to keep the RDS (on) of the device as low as

possible. After the initial t_delay, M1 will begin to source current and V_DC will start to ramp up. The ramp up time, t_ramp, is defined as:

$$t_ramp := -R2 \cdot C9 \cdot \ln\left(1 - \frac{Vsat}{Vgs_max}\right) - t_delay$$

Maximum current during the voltage ramping is:

$$I = Ctotal \cdot \frac{Vpwr}{t_ramp}$$

With the circuit shown in Figure 8, t_delay = 5.53 ms, t_ran = 14.0 ms and I_max = 146 mA. Figure 9 shows a SPICE simulation of the circuit in Figure 8. To increase the reliability

of Tantalum capacitors, use a slew rate control circuit as described in Figure 8 and voltage-derate the capacitor about 50 percent. That is, for a maximum input voltage of 18V, use

a 35V, low ESR capacitor with high ripple current capability. Place five, 22 µF/35V capacitors on the baseboard directly at the V_{DC} pins of the Celeron™ processor MMC-1.

The slew rate control circuit should also be applied to every input power source to the system V_{DC} to provide the most protection. If all power is OR'ed together at the PWR node,

there is still a potential problem. For example, if a 3X3 Li-Ion battery pack is powering the system (12V at PWR), and the AC Adaptor (18V) is plugged into the system, it will immediately source current to the PWR node and V_{DC} rapidly. This is because the slew rate control is already ON. Therefore, the slew rate control must be applied to every input power source to provide the most protection.

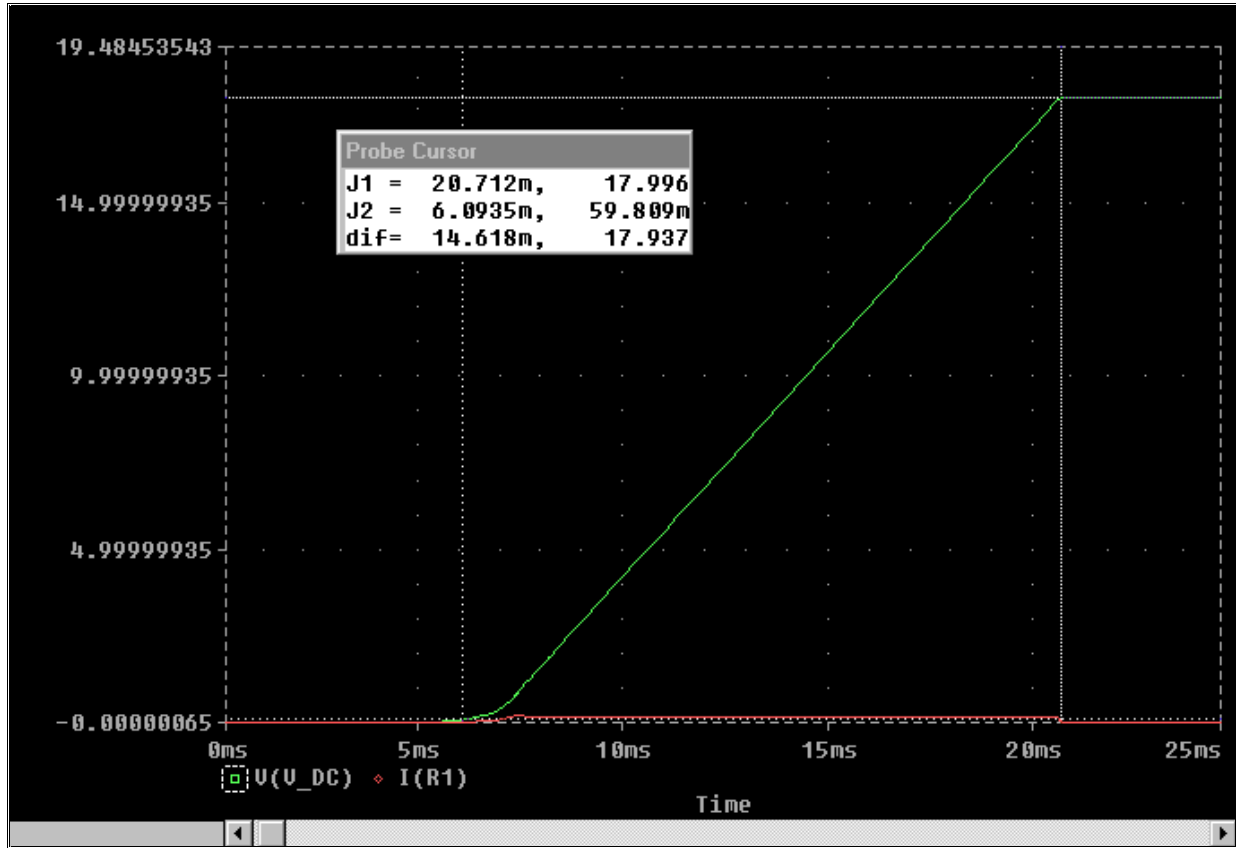


Figure 9. Spice Simulation Using In-Rush Protection (Example Only)

4.7.4.2. Under-Voltage Lockout: Circuit Description (V_{uv_lockout})

The circuit shown in Figure 8 provides an under-voltage protection and locks out the applied voltage to the Celeron™ processor mobile module to prevent an accidental turn-on at low voltage. The output of this circuit, pin 1 of the LM339

comparator, is an open-collector output. It is low when the applied voltage at PWR is less than 4.75V. This voltage can be calculated with the following equation with the voltage across D7 as 2.5V. (D7 is a 2.5-V reference generator).

$$V_{uv_lockout} := V_{ref} \left[1 + \frac{R17}{\left(\frac{R18 \cdot R25}{R18 + R25} \right)} \right]$$

$$V_{uv_lockout} = 4.757 \text{ volt}$$

4.7.4.3. Over-Voltage Lockout: Circuit Description (V_ov_lockout)

The Celeron™ processor mobile module is specified to operate with a maximum input voltage of 21V. This circuit locks out the input voltage if it exceeds the maximum 21V. The output

of this circuit, Pin 14 of the LM339 comparator, is an open-collector output. It is low when the applied voltage at PWR is more than 21V. This voltage can be calculated with the following equation:

$$V_{ov_lockout} := V_{ref} \left(\frac{R26}{R26 + R27} \right) \cdot \left(1 + \frac{R24}{R23} \right)$$

$$V_{ov_lockout} = 20.998 \cdot \text{volt}$$

4.7.4.4. Over-Current Protection: Circuit Description

Figure 8 shows that the circuit detects an over-current condition and cuts off the input voltage applied to the Celeron™ processor mobile module. This circuit has two different current limit trip points. This takes into account the different maximum current drain by the Celeron processor

mobile module at different input voltages. Assuming the AC Adaptor voltage is 18V and the battery is a 3x3 Li-Ion configuration with a minimum of 7.5V, the maximum current for the above circuit can be calculated using the following expression:

With AC Adaptor (I_wAdaptor):

$$I_{wAdaptor} := \frac{V_{ref} - V_{be_Q1}}{R14} \cdot \frac{R13}{R1}$$

$$I_{wAdaptor} = 0.989 \cdot \text{amp}$$

Without AC Adaptor (I_woAdaptor):

$$I_{woAdaptor} := \frac{V_{ref} - V_{be_Q1}}{\left(\frac{R14 \cdot R33}{R14 + R33} \right)} \cdot \frac{R13}{R1}$$

$$I_{woAdaptor} = 2.375 \cdot \text{amp}$$

4.8. Active Thermal Feedback

Table 21 identifies the addresses allocated for the SMBus thermal sensor.

Table 21. Thermal Sensor SMBus Address Table

Function	Fixed Address AD Bits (6:4)	Selectable Address AD Bits (3:0)
Thermal Sensor	100	1110
Reserved	010	1010
Reserved	010	1011

NOTE:

The thermal sensor used is compliant with SMBus addressing. Please refer to the *Pentium® II processor Thermal Sensor Interface Specification*.

4.9 Thermal Sensor Configuration Register

The configuration register of the thermal sensor controls the operating mode (Auto-convert vs. Standby) of the device. Since the processor temperature varies dynamically during normal operation, auto-convert mode should be used exclusively to monitor processor temperature. Table 22 shows the format of the configuration register. If the RUN/STOP bit is low, then the thermal sensor enters auto-conversion mode. If the RUN/STOP bit is set high, then the thermal sensor immediately stops converting and enters

Standby mode. The thermal sensor will still perform temperature conversions in Standby mode when it receives a one-shot command. However, the result of a one-shot command during auto-convert mode is not guaranteed. Intel does not recommend using the one-shot command to monitor temperature when the processor is active, only auto-convert mode should be used. Refer to *Mobile Pentium® II Processor and Pentium® II Processor Mobile Module Thermal Sensor Interface Specifications, Rev.1.0.*

Table 22. Thermal Sensor Configuration Register

Bit	Name	Reset State	Function
7 MSB	MASK	0	Masks SMBALERT# when high.
6	RUN/STOP	0	Standby mode control bit. If low, the device enters auto-convert mode. If high, the device immediately stops converting, and enters standby mode where the one-shot command can be performed.
5 – 0	RFU	0	Reserved for future use.

NOTE:

All RFU bits should be written as "0" and read as "don't care" for programming purposes.

5.0. MECHANICAL SPECIFICATION

5.1. Module Dimensions

This section provides the physical dimensions for the Celeron™ processor MMC-1.

5.1.1. Board Area

Figure 10 shows the board dimensions and the orientation for the Celeron™ processor MMC-1. These dimensions are necessary to accommodate the next generation of Intel mobile modules and PCI 443BX chipset controllers.



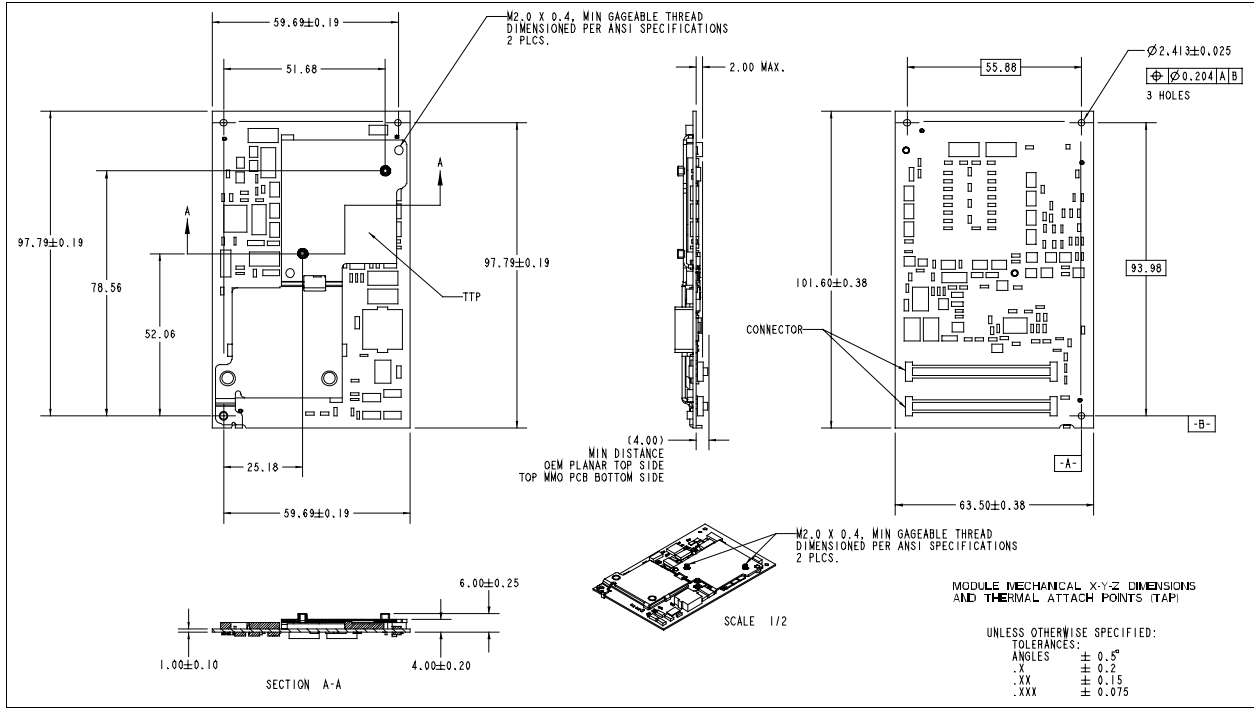


Figure 10. Celeron™ Processor MMC-1 Board Dimensions with 280-Pin Connector Orientation

5.1.2. MMC-1 Pin 1 Location

Figure 11 shows the location of pin 1 of the 280-pin MMC-1 as referenced to the adjacent mounting hole.

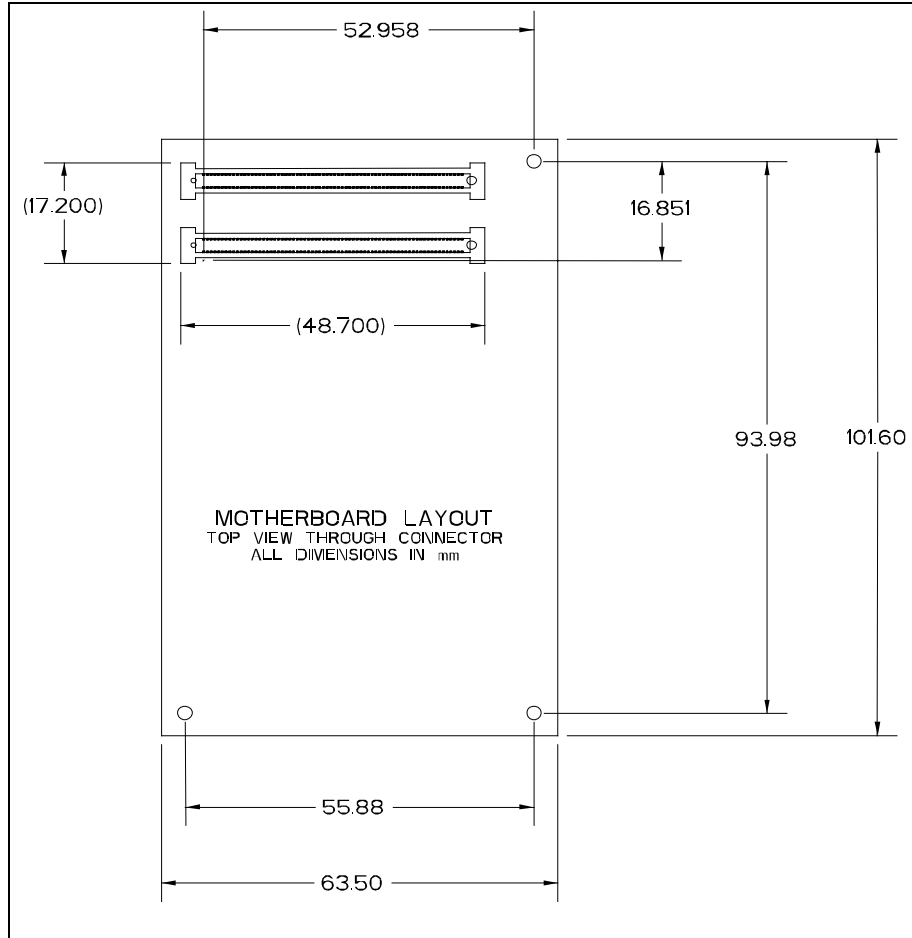


Figure 11. Celeron™ Processor Mobile Module Board Dimensions with 280-Pin Connector - Pin 1 Orientation

5.1.3. Printed Circuit Board Thickness

Figure 12 shows the Celeron™ processor mobile module profile and the associated minimum and maximum thickness of the printed circuit board (PCB). The range of PCB thickness allows for different PCB technologies to be used with current and future Intel mobile modules.

NOTE: The system manufacturer must ensure that the mechanical restraining method or system-level EMI contacts are able to support this range of PCB thickness, to ensure compatibility with future Intel mobile modules.

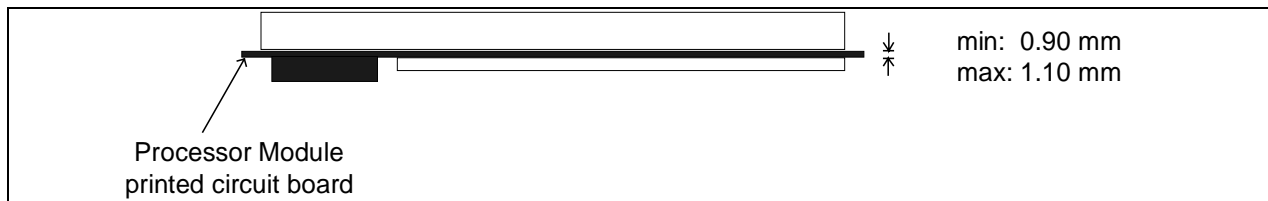


Figure 12. Printed Circuit Board Thickness

5.1.4. Height Restrictions

Figure 13 shows the mechanical stackup and associated component clearance requirements. This is referred to as the module keep-out zone and should not be entered or altered.

The system manufacturer establishes the board-to-board clearance between the Celeron™ processor mobile module and the system electronics by selecting one of three possible mating connectors. The mating connectors are 4 mm, 6 mm, or 8 mm. These three options provide the system manufacturer with flexibility in choosing components between the two boards. Information on these connectors can be obtained from your local Intel representative.

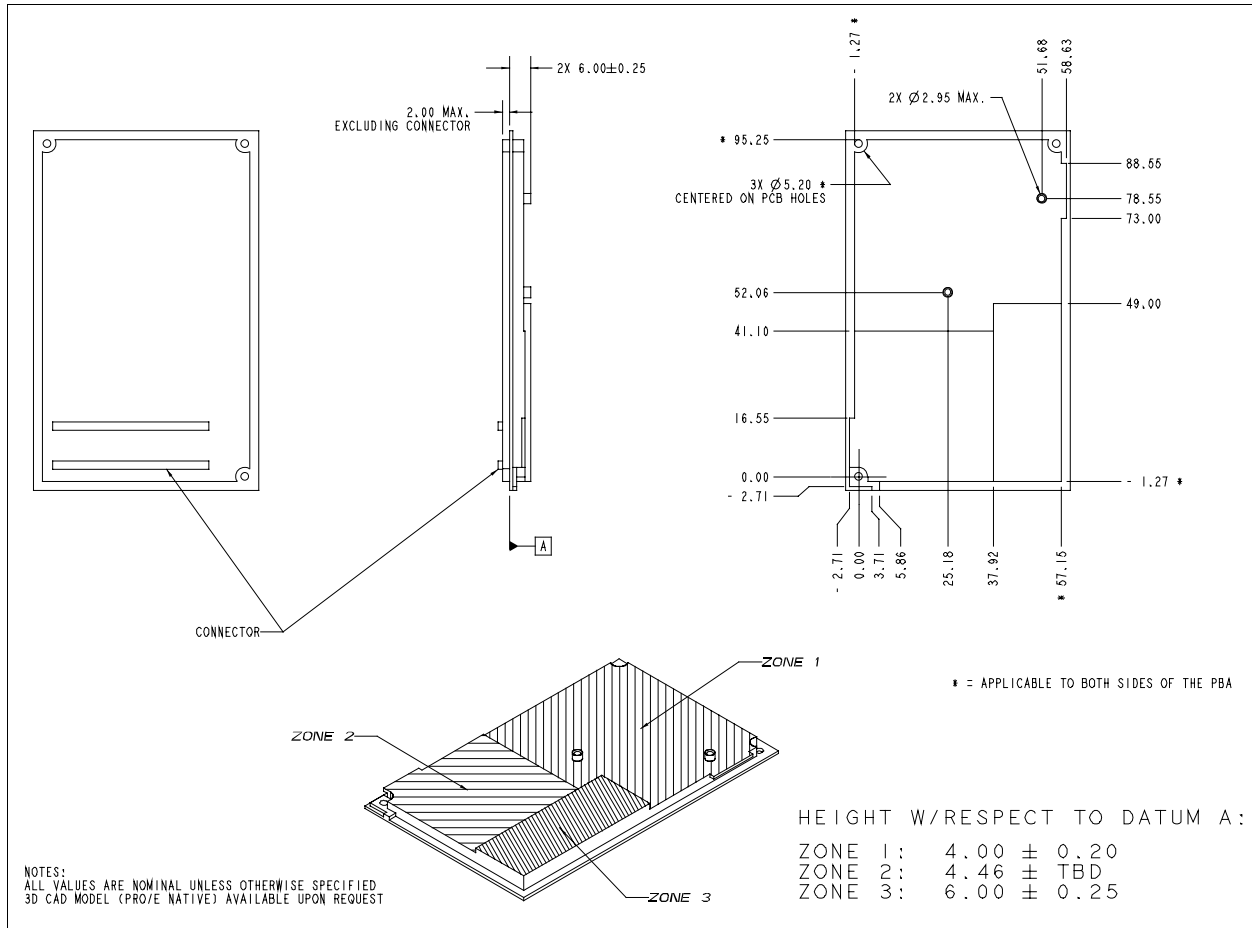


Figure 13. Celeron™ Processor Mobile Module 3-D Keep-out Zone

NOTE:

The topside component clearance is independent of the PCB thickness.

5.2. Thermal Transfer Plate

A thermal transfer plate (TTP) on the mobile Celeron™ processor and the 443BX provides for heat dissipation. The TTP may vary on different generations of Intel mobile modules. The TTP provides the thermal attach point, where a system manufacturer can use a heat pipe, a heat spreader plate, or a thermal solution to transfer heat through the notebook system. Attachment dimensions for the OEM thermal interface block to the TTP are provided in the following figures 14 and 15. The system manufacturer should use the exact dimensions for maximum contact area

to the TTP while ensuring that no warpage of the TTP occurs. If warpage occurs, the thermal resistance of the Celeron processor mobile module could be adversely affected.

When attaching the mating block to the module TTP, a thermal elastimer or thermal grease should be used. This material reduces the thermal resistance. The OEM thermal interface block should be secured with 2.0 mm screws using a maximum torque of 1.5 – 2.0 Kg*cm (equivalent to 0.147 - .197 N*m). The thread length of the 2.00 mm screws should

be 2.25 mm gageable thread (2.25 mm minimum to 2.80 mm maximum).
 The TTP thermal resistance between the processor core to the system interface (top of the TTP) is less than 1°C per Watt.

The following figures 14 and 15 detail the mechanical dimensions of the TTP and the thermal attach point.

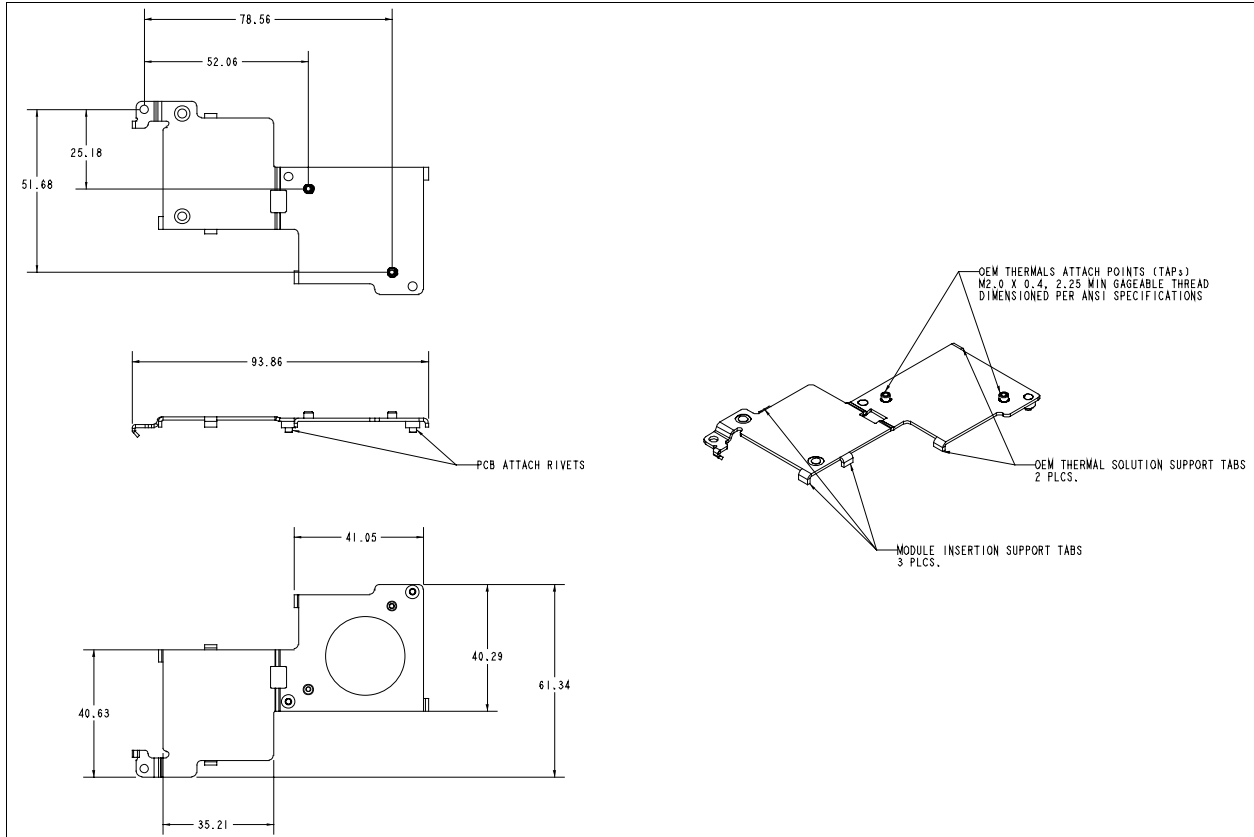


Figure 14. Celeron™ Processor Mobile Module Thermal Transfer Plate

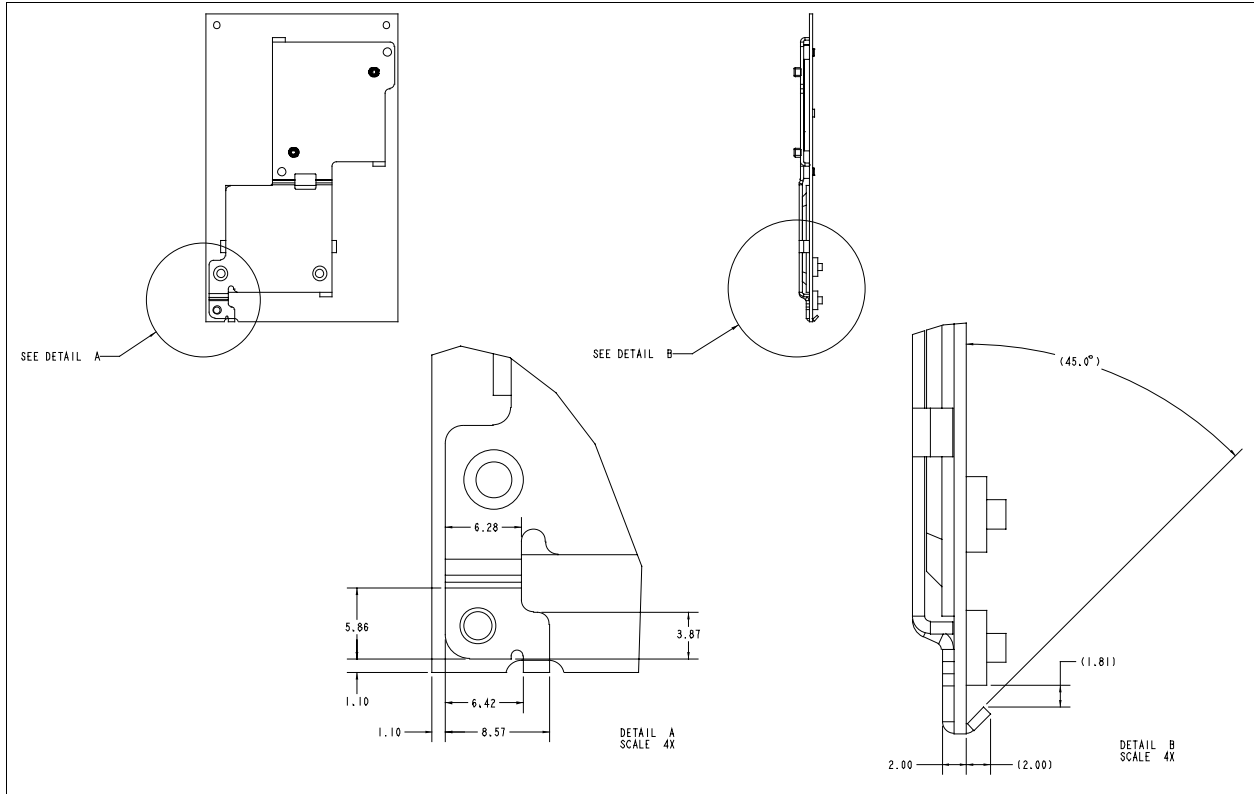


Figure 15. Celeron™ Processor Mobile Module Thermal Transfer Plate

5.3. Module Physical Support

Figure 16 shows the standoff support hole patterns, the board edge clearance, the dimensions of the EMI containment ring, and the keep-out area. These hole locations and board edge clearances will remain fixed for all Intel mobile modules. The hole patterns and board edge clearance lets the system manufacturer develop several methods for mechanically supporting different Intel mobile modules within a particular notebook system.

5.3.1 Module Mounting Requirements

Three mounting holes are available for securing the module to the system base or the system electronics. See Figure 11 for mounting hole locations. It is strongly recommended that the OEM utilize mounting screws through all three of the mounting holes to ensure long term reliability of the mechanical and EMI integrity of the system.

The board edge clearance includes a 0.762 mm (0.030 in) width EMI containment ring around the perimeter of the module. This ring is on each layer of the module PCB and is grounded. On the surface of the module, the metal is

exposed for EMI shielding purposes. The hole patterns placed on the module also have a plated surrounding ring, which can be used with a metal standoff for EMI shielding purposes.

Standoffs should be used to provide support for the installed Celeron™ processor mobile module. The distance from the bottom of the module PCB to the top of the OEM system electronics board with the connectors mated is 4.0 mm +0.16 mm / -0.13 mm. However the warpage of the baseboard can vary and should be calculated into the final dimensions of the standoffs used. All calculations can be made with the *Intel MMC-1 Standoff/Receptacle Height Spreadsheet*. Information on this spreadsheet can be obtained from your local Intel representative.

5.3.2 Module Weight

The weight of the Celeron™ processor mobile module is approximately 50g.

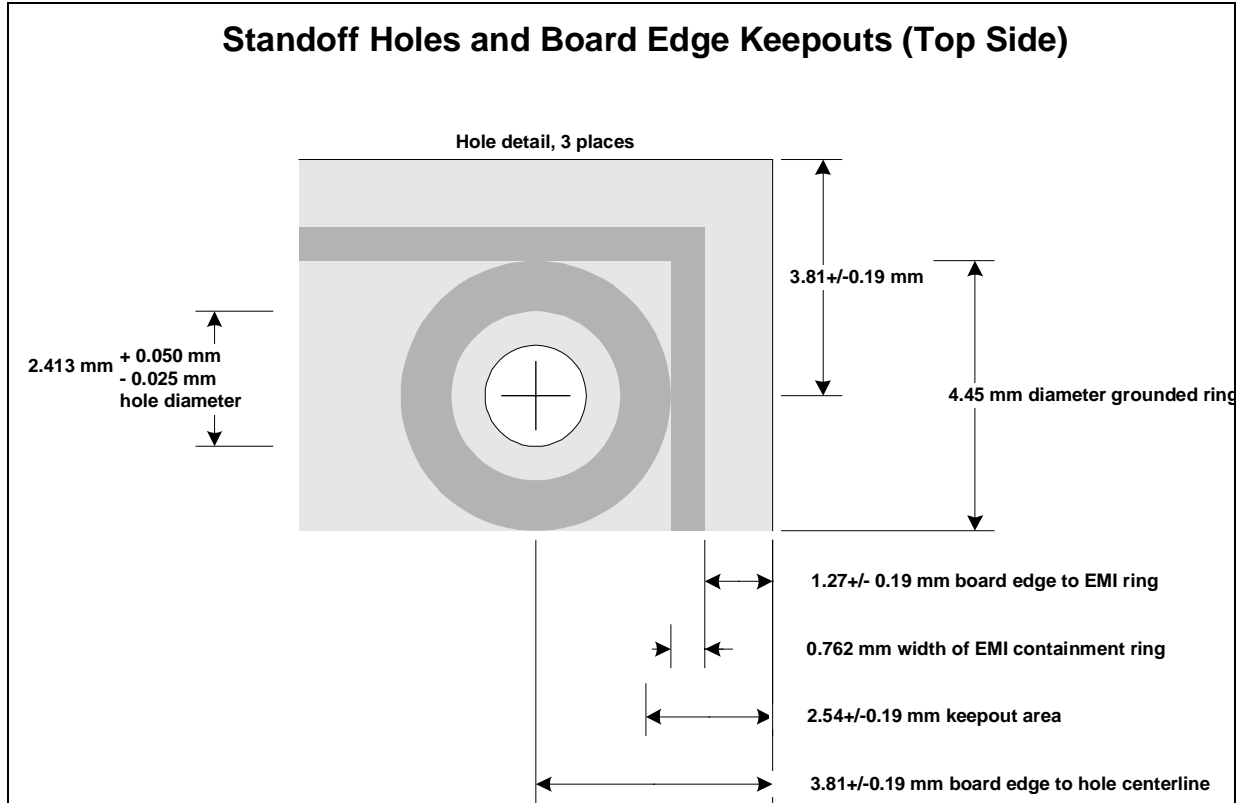


Figure 16. Standoff Holes, Board Edge Clearance, and EMI Containment Ring

6.0. THERMAL SPECIFICATION

6.1. Thermal Design Power

If a notebook system does not incorporate a thermal feedback fail-safe mechanism to keep the component temperatures within specification, the OEM should design the system to the maximum thermal design power as shown in Table 22. The maximum thermal design power is the maximum total power dissipation under normal operating conditions at nominal Vcc while executing the worst case power instruction mix. This includes the power dissipated by *all* of the relevant components of the Celeron™ processor mobile module. System thermal designs do not need the capability to dissipate this level of power if they incorporate some type of thermal feedback fail-safe system.

The use of nominal Vcc in this measurement accounts for the thermal time constant of the package/system. The power supply must be centered at nominal Vcc such that during transients the Vcc levels stay within the Vcc ± Vcc_Delta (%)

range. The duration of surges to Vcc + Vcc_Delta (%) are less than the thermal time constant.

During all operating environments, the processor case temperature, T_{PROC}, must be within the specified range of 0°C to 100°C.

6.2 Thermal Sensor Setpoint

The thermal sensor in the Celeron™ processor mobile module implements the SMBALERT# signal described in the SMBus specification. SMBALERT# is always asserted when the temperature of the processor core thermal diode or the thermal sensor internal temperature exceeds either the upper or lower temperature thresholds. SMBALERT# may also be asserted if the measured temperature equals either the upper or the lower threshold.

Table 23. Celeron™ Processor Mobile Module (MMC-1) Maximum Power Specifications

Symbol	Parameter	Min	Typ	Max ¹	Unit	Notes
TDP _{MMC-2}	Thermal Design Power (MMC-2 module)		—	TBD	W	Module (core, 443BX, and voltage regulator)
T _{PROC}	Processor Case Temperature	0		100	°C	

NOTE:

TDP_{max} is a specification of the total power dissipation of the worst case processor, worst case 443BX, and worst case voltage regulator while executing a worst case instruction mix under normal operating conditions at nominal voltages. Not 100% tested. Specified by design/characterization.

7.0. LABELING INFORMATION

The Celeron™ processor mobile module is tracked in two ways. The first is by the Product Tracking Code (PTC). Intel uses the PTC label to determine the assembly level of the

module. The PTC label is on the secondary side of the module as shown in Figure 17 and provides the following information.

- The Product Tracking code will consist of 13 characters as identified in the above example and can be broken down as follows:

Example: **PMH30001001AA**

- Definition:
 - AA - Processor Module = PM
 - B - Celeron™ processor mobile module = H
 - CCC - Speed Identity = 300 and 266
 - DD - Cache Size = 01 (128K)
 - EEE - Notifiable Design Revision (Start at 001)
 - FF - Notifiable Processor Revision (Start at AA)
- Note: For other Intel mobile modules, the second field (B) is defined as:
 - Celeron™ processor mobile module (MMC-2) = I
 - Pentium® II processor mobile module (MMC-1) = F
 - Pentium® II processor mobile module (MMC-2) = G

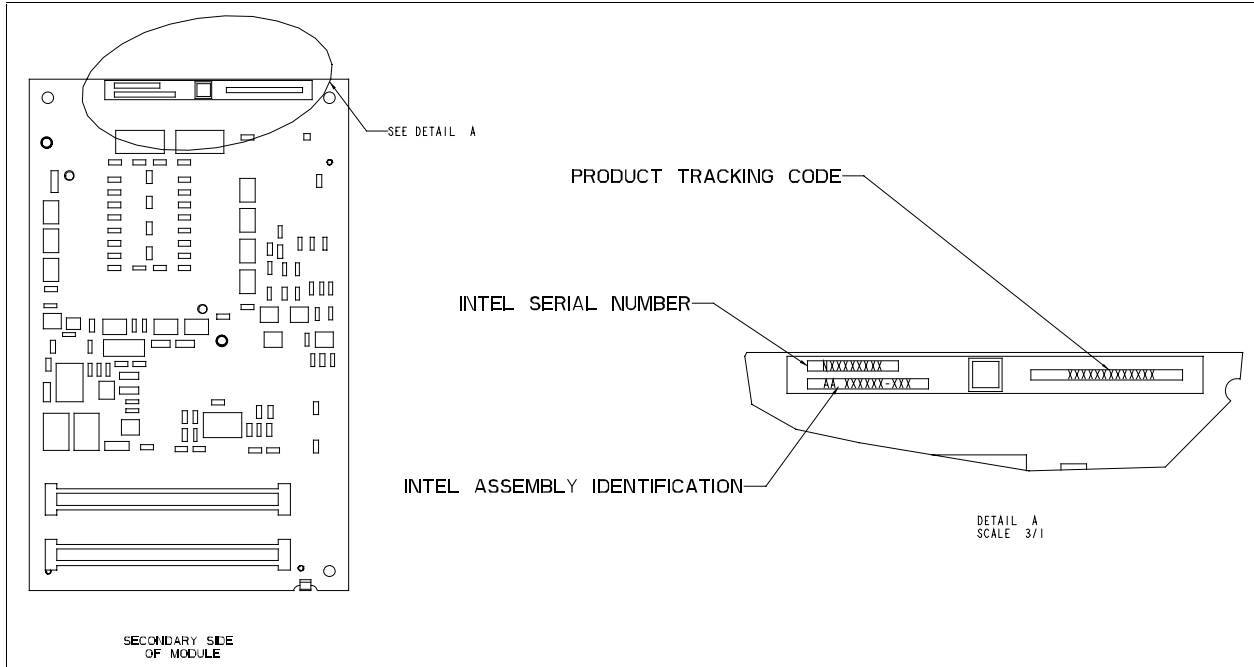


Figure 17. Celeron™ Processor Mobile Module Product Tracking Code

The second tracking method is by OEM generated software utility. Four strapping resistors located on the Celeron™ processor mobile module determine its production level. If connected and terminated properly, up to 16-module revision levels can be determined. An OEM generated software utility can then read these ID bits with CPU IDs and stepping IDs to provide a complete module manufacturing revision level. For current PTC and module ID bit information, please refer to the latest Celeron processor mobile module Product

Change Notification letter which can be obtained from your local Intel sales representative.

8.0. ENVIRONMENTAL STANDARDS

The environmental standards for the Celeron™ processor mobile module are defined in Table 24.

Table 24. Environmental Standards

Parameter	Condition	Specification
Temperature	Non-Operating	-40°C to 85°C
	Cycle	Operating
Humidity	Unbiased	85% relative humidity at 55 °C
Voltage	V_5	5V +/- 5%
	V_3	3.3V +/- 5%
Shock	Non-Operating	Half Sine, 2G, 11 msec
	Unpackaged	Trapezoidal, 50G, 11 msec
	Packaged	Inclined Impact at 5.7 ft/s
	Packaged	Half Sine, 2 msec at 36 in. Simulated Free Fall
Vibration	Unpackaged	5 Hz to 500 Hz 2.2 gRMS random
	Packaged	10 Hz to 500 Hz 1.0 gRMS

Parameter	Condition	Specification
	Packaged	11,800 impacts 2 Hz to 5 Hz (low frequency)
ESD	Human Body Model	0 to 2 kV (no detectable err)





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