Pentium® II Processor at 350 MHz, 400 MHz, and 450 MHz

Datasheet

Product Features

- Available at 350 MHz, 400 MHz, and 450 MHz frequencies
- System bus frequency at 100 MHz
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Dynamic execution micro architecture
- Dual Independent Bus architecture: Separate dedicated external System Bus and dedicated internal high-speed cache bus
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Single Edge Contact Cartridge (S.E.C.C.) and S.E.C.C.2 packaging technology; the S.E.C. cartridges deliver high performance with improved handling protection and socketability
- Integrated high performance 16 KB instruction and 16 KB data, nonblocking, level one cache
- Available with integrated 512 KB unified, nonblocking, level two cache
- Enables systems which are scaleable up to two processors
- Error-correcting code for System Bus data

The Intel Pentium® II processor is designed for high-performance desktops and for workstations and servers. It is binary compatible with previous Intel Architecture processors. The Pentium II processor provides the best performance available for applications running on advanced operating systems such as Windows* 95, Windows NT and UNIX*. This is achieved by integrating the best attributes of Intel processors—the dynamic execution, Dual Independent Bus architecture plus Intel MMX™ technology—bringing a new level of performance for systems buyers. The Pentium II processor is scaleable to two processors in a multiprocessor system and extends the power of today's Pentium II processor with performance headroom for business media, communication and internet capabilities. Systems based on Pentium II processors also include the latest features to simplify system management and lower the cost of ownership for large and small business environments. The Pentium II processor offers great performance for today's and tomorrow's applications.

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1.0 Introduction

The Pentium II 350 MHz/400 MHz/450 MHz processor is the next in the Pentium II processor line of Intel processors. The Pentium II processor, like the Pentium Pro processor, implements a Dynamic Execution microarchitecture—a unique combination of multiple branch prediction, data flow analysis, and speculative execution. This enables these processors to deliver higher performance than the Pentium processor, while maintaining binary compatibility with all previous Intel Architecture processors. The Pentium II processor also executes MMX technology instructions for enhanced media and communication performance. The Pentium II processor utilizes multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

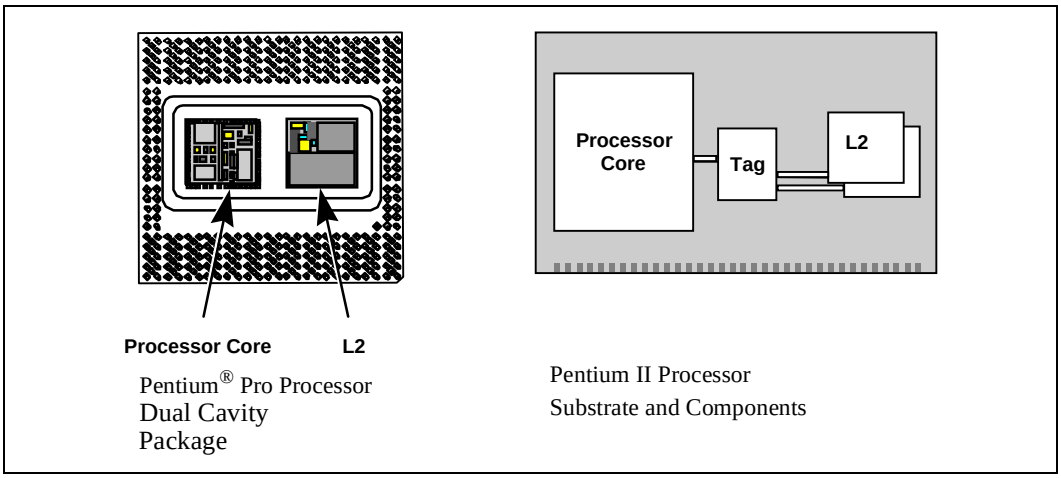
The Pentium II processor utilizes the same multiprocessing system bus technology as the Pentium Pro processor. This allows for a higher level of performance for both uni-processor and two-way multiprocessor (2-way MP) systems. Memory is cacheable for up to 4 GB of addressable memory space, allowing significant headroom for business desktop systems. Please refer to the Intel Specification Update document's S-spec number table to determine the cacheability for a given processor.

The Pentium II processor system bus operates in the same manner as the Pentium Pro processor system bus. The Pentium II processor system bus uses a variant of GTL+ signal technology called AGTL+ signal technology. The Pentium II processor deviates from the Pentium Pro processor by using commercially available die for the second level (L2) cache. The L2 cache (the TagRAM and burst pipelined synchronous static RAM (BSRAM) memories) are now multiple die. Transfer rates between a Pentium II processor's core and L2 cache are one-half the processor core clock frequency and scale with the processor core frequency. Both the TagRAM and BSRAM receive clocked data directly from the Pentium II processor core. As with the Pentium Pro, the Pentium II processor has a dedicated L2 cache bus, thus maintaining the dual independent bus architecture to deliver high bus bandwidth and high performance (see Figure 1).

Pentium II processors use either a Single Edge Contact Cartridge (S.E.C.C.) or a Single Edge Contact Cartridge 2 (S.E.C.C.2) packaging technology. These packaging technologies allow the L2 cache to remain tightly coupled to the processor, while enabling use of high volume commercial SRAM components. The L2 cache is performance optimized and tested at the package level. The S.E.C.C. and S.E.C.C.2 packages utilize surface mounted technology and a substrate with an edge finger connection. Pentium II processors at 350, 400 and 450 MHz, while available at higher core frequencies than the previously released Pentium II processors at 233, 266, 300 and 333 MHz, also provide additional features while utilizing either a compatible S.E.C.C. package or the follow-on S.E.C.C.2 package.

The S.E.C.C. package has the following features: an extended thermal plate, a cover, and a substrate with an edge finger connection. The extended thermal plate allows heatsink attachment or customized thermal solutions. The S.E.C.C.2 package has a cover and a substrate with an edge finger conenction. This allows the thermal solutions to be placed directly onto the processor core package. The edge finger connection maintains socketability for system configuration. The edge finger connector is called the 'SC 242 connector' in this and other documentation.

Figure 1. Second Level (L2) Cache Implementations



1.1 Terminology

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D#[3:0] = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "system bus" refers to the interface between the processor, system core logic (a.k.a. the AGPset components), and other bus agents. The system bus is a multiprocessing interface to processors, memory, and I/O. The term "cache bus" refers to the interface between the processor and the L2 cache components (TagRAM and BSRAMs). The cache bus does NOT connect to the system bus, and is not visible to other agents on the system bus.

1.1.1 S.E.C. Cartridge Terminology

The following terms are used often in this document and are explained here for clarification:

- **Pentium® II processor**—The entire product including internal components, substrate, extended thermal plate, and cover.
- **S.E.C.C.**—The processor packaging technology is called a "Single Edge Contact Cartridge." Initial releases of the Pentium II processor are based upon this packaging technology.
- **S.E.C.C.2**—The follow-on to S.E.C.C. processor packaging technology. The biggest difference from its predecessor is that it has no extended thermal plate, thus reducing thermal resistance.
- **Processor substrate**—The structure on which components are mounted inside the S.E.C.C. or S.E.C.C.2 package technology (with or without components attached).
- **Processor core**—The processor's execution engine.

- **Extended Thermal Plate**—This S.E.C.C. 100 MHz processor feature is the surface used to attach a heatsink or other thermal solution to the processor. The extended thermal plate has an extended skirt as compared to the 66 MHz Pentium II processors for increased thermal capabilities.
- **Cover**—The plastic casing that covers the backsire of the substrate and holds processor branding and marking information.
- **Latch arms**—An S.E.C.C. processor feature which can be used as a means for securing the processor in the retention mechanism(s).
- **PLGA** - Plastic Land Grid Array. This package technology incorporates a heat slug within the package that contacts the extended thermal plate.
- **OLGA** - Organic Land Grid Array. This package technology permits attaching the heatsink directly to the die.

Additional terms referred to in this and other related documentation:

- **SC 242**—The 242-contact slot connector (previously referred to as Slot 1 connector) that the S.E.C.C. and S.E.C.C.2 plug into, just as the Pentium® Pro processor uses Socket 8.
- **Retention mechanism**—An enabled mechanical piece which holds the S.E.C. cartridge in the SC 242 connector.
- **Heatsink support**—The support pieces that are mounted on the motherboard to provide added support for heatsinks.

The L2 cache (TagRAM, BSRAM) die keep industry names.

1.2 References

The reader of this specification should also be familiar with material and concepts presented in the following documents:

- AP-485, *Intel Processor Identification and the CPUID Instruction* (Order Number 241618)
- AP-827, *100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel® 440BX AGPset* (Order Number 243735)
- AP-586, *Pentium® II Processor Thermal Design Guidelines* (Order Number 243331)
- AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332)
- AP-588, *Mechanical and Assembly Technology for S.E.C. Cartridge Processors* (Order Number 243333)
- AP-589, *Pentium® II Processor Electro-Magnetic Interference* (Order Number 243334)
- *Pentium® II Processor at 233, 266, 300, 333 MHz* (Order Number 243335)
- *Pentium® II Processor Specification Update* (Order Number 243337)
- *Slot 1 Connector Specification* (Order Number 243397)
- *Slot 1 Bus Terminator Card Design Guidelines* (Order Number 243409)
- *Intel Architecture Software Developer's Manual* (Order Number 243193)
  - *Volume I: Basic Architecture* (Order Number 243190)
  - *Volume II: Instruction Set Reference* (Order Number 243191)

— *Volume III: System Programming Guide* (Order Number 243192)

- *P6 Family of Processors Hardware Developer's Manual* (Order Number 244001)
- *Pentium® II Processor I/O Buffer Models*, Quad Format (developer.intel.com)

2.0 Electrical Specifications

2.1 Processor System Bus and V_{REF}

Most Pentium II processor signals use a **variation** of the low voltage Gunning Transceiver Logic (GTL) signaling technology.

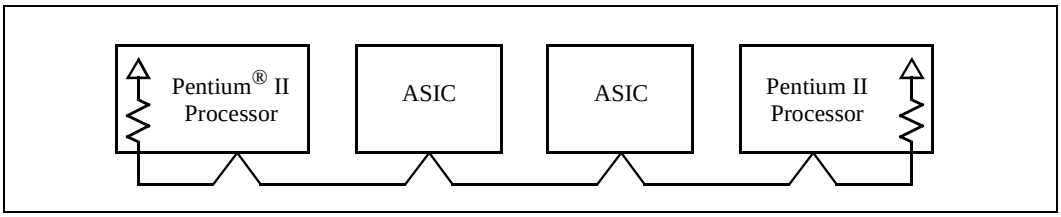
The Pentium II processor system bus specification is similar to the GTL specification, but has been enhanced to provide larger noise margins and reduced ringing. The improvements are accomplished by increasing the termination voltage level and controlling the edge rates. This specification is different from the standard GTL specification, and is referred to as **GTL+**. For more information on GTL+ specifications, see AP-827, *100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel® 440BX AGPset* (Order Number 243735).

The Pentium II processor varies from the Pentium Pro processor in its output buffer implementation. The buffers that drive most of the system bus signals on the Pentium II processor are actively driven to VCC_{CORE} for one clock cycle after the low to high transition to improve its rise times and reduce noise. These signals should still be considered open-drain and require termination to a supply that provides the high signal level. Because this specification is different from the standard GTL+ specification, it is referred to as Assisted Gunning Transitistor Logic (AGTL+) in this document. AGTL+ logic and GTL+ logic are compatible with each other and may both be used on the same system bus.

AGTL+ signals are open-drain and require termination to a supply that provides the high signal level. AGTL+ inputs use differential receivers which require a reference signal (V_{REF}). V_{REF} is used by the receivers to determine if a signal is a logical 0 or a logical 1, and is generated on the S.E.C cartridges for the processor core. Local V_{REF} copies should be generated on the motherboard for all other devices on the AGTL+ system bus. Termination (usually a resistor at each end of the signal trace) is used to pull the bus up to the high voltage level and to control reflections on the transmission line. The processor contains termination resistors that provide termination for one end of the Pentium II processor system bus. These specifications assume another resistor at the end of each signal trace to ensure adequate signal quality for the AGTL+ signals; see Table 8 for the bus termination voltage specifications for AGTL+ and the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the GTL+ bus specification. Solutions exist for single-ended termination as well, though solution space is affected. Figure 2 is a schematic representation of AGTL+ bus topology with Pentium II processors.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the Pentium II processor system bus including trace lengths is highly recommended when designing a system with a heavily loaded AGTL+ bus, especially for systems using a single set of termination resistors (i.e., those on the processor substrate) with the Intel® 440BX AGPset. Such designs will not match the solution space allowed for by installation of termination resistors on the motherboard. See Intel's World Wide Web page (http://developer.intel.com) to download the buffer models: *Pentium® II Processor I/O Buffer Models*, Quad Format (Electronic Form).

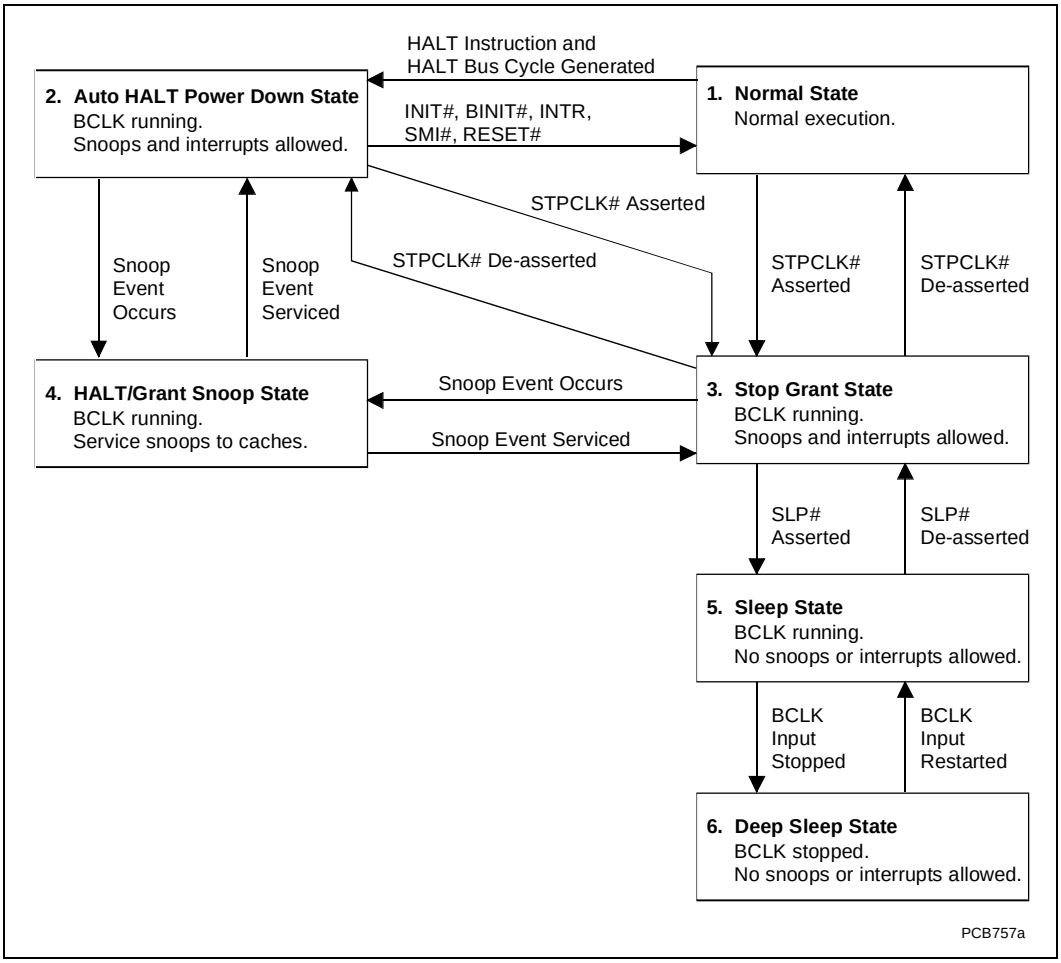
Figure 2. AGTL+ Bus Topology



2.2 Clock Control and Low Power States

Pentium II processors allow the use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 3 for a visual representation of the Pentium II processor low power states.

Figure 3. Stop Clock State Machine



For the processor to fully realize the low current consumption of the Stop-Grant, Sleep, and Deep Sleep states, a Model Specific Register (MSR) bit must be set. For the MSR at 02AH (Hex), bit 26 must be set to a '1' (this is the power on default setting) for the processor to stop all internal clocks during these modes. For more information, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

Due to the inability of processors to recognize bus transactions during the Sleep and Deep Sleep states, two-way MP systems are not allowed to have one processor in Sleep/Deep Sleep state and the other processor in Normal or Stop-Grant state simultaneously.

2.2.1 Normal State—State 1

This is the normal operating state for the processor.

2.2.2 AutoHALT Powerdown State—State 2

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* (Order Number 243192) for more information.

FLUSH# will be serviced during the AutoHALT state, and the procesor will return to the AutoHALT state.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

2.2.3 Stop-Grant State—State 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will be recognized while the processor is in Stop-Grant state. If STPCLK# is still asserted at the completion of the BINIT# bus initialization, the processor will remain in Stop-Grant mode. If the STPCLK# is not asserted at the completion of the BINIT# bus initialization, the processor will return to Normal state.

FLUSH# will not be serviced during Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 2.2.4). A transition to the Sleep state (see Section 2.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

2.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the Pentium II processor system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the Pentium II processor system bus has been serviced (whether by the processor or another agent on the Pentium II processor system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK input (see Section 2.2.6). Once in the Sleep or Deep Sleep states, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin has a minimum assertion of one BCLK period.

2.2.6 Deep Sleep State—State 6

The Deep Sleep state is the lowest power state the processor can enter while maintaining context. The Deep Sleep state is entered by stopping the BCLK input (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BLCK is stopped. It is recommended that the BLCK input be held low during the Deep Sleep State. Stopping of the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BLCK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.2.7 Clock Control

The processor provides the clock signal to the L2 cache. During AutoHALT Power Down and Stop-Grant states, the processor will process a system bus snoop. The processor will not stop the clock to the L2 cache during AutoHALT Power Down or Stop-Grant states. Entrance into the Halt/ Grant Snoop state will allow the L2 cache to be snooped, similar to the Normal state.

When the processor is in Sleep and Deep Sleep states, it will not respond to interrupts or snoop transactions. During the Sleep state, the clock to the L2 cache is not stopped. During the Deep Sleep state, the clock to the L2 cache is stopped. The clock to the L2 cache will be restarted only after the internal clocking mechanism for the processor is stable (i.e., the processor has re-entered Sleep state).

PICCLK should not be removed during the AutoHALT Power Down or Stop-Grant states. PICCLK can be removed during the Sleep or Deep Sleep states. When transitioning from the Deep Sleep state to the Sleep state, PICCLK must be restarted with BCLK.

2.3 Power and Ground Pins

The operating voltage of the processor die and of the L2 cache die differ from each other. There are two groups of power inputs on the Pentium II processor package to support this voltage difference between the components in the package. There are also five pins defined on the package for voltage identification (VID). These pins specify the voltage required by the processor core. These have been added to cleanly support voltage specification variations on current and future Pentium II processors.

For clean on-chip power distribution, Pentium II processors have 27 V_{CC} (power) and 30 V_{SS} (ground) inputs. The 27 V_{CC} pins are further divided to provide the different voltage levels to the components. $V_{CC_{CORE}}$ inputs for the processor core and some L2 cache components account for 19 of the V_{CC} pins, while 4 V_{TT} inputs (1.5 V) are used to provide an AGTL+ termination voltage to the processor and 3 $V_{CC_{L2}}$ inputs (3.3 V) are for use by the L2 cache TagRAM and BSRAMs. One V_{CC5} pin is provided for use by the Slot 1 Test Kit. V_{CC5}, V_{CCL2}, and $V_{CC_{CORE}}$ must remain electrically separated from each other. On the circuit board, all $V_{CC_{CORE}}$ pins must be connected to a voltage island and all V_{CCL2} pins must be connected to a separate voltage island (an island is a portion of a power plane that has been divided, or an entire plane). Similarly, all V_{SS} pins must be connected to a system ground plane.

2.4 Decoupling Guidelines

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This causes voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 5. Failure to do so can result in timing violations or a reduced lifetime of the component.

2.4.1 Processor VCC_{CORE} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep an interconnect resistance from the regulator (or VRM pins) to the SC 242 connector of less than 0.3 mΩ. This can be accomplished by keeping a maximum distance of 1.0 inches between the regulator output and SC 242 connector. The recommended $V_{CC_{CORE}}$ interconnect is a 2.0 inch wide (the width of the VRM 8.2 connector) by 1.0 inch long (maximum distance between the SC 242 connector and the VRM 8.2 connector) plane segment with a 1-ounce plating. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, is provided on the voltage regulation module (VRM). The $V_{CC_{CORE}}$ input should be capable of delivering a recommended minimum $dI_{CC_{CORE}}/dt$ (defined in Table 5) while maintaining the required tolerances (also defined in Table 5).

2.4.2 Processor System Bus AGTL+ Decoupling

The Pentium II processor contains high frequency decoupling capacitance on the processor substrate; bulk decoupling must be provided for by the system motherboard for proper AGTL+ bus operation. See AP-827, *100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel® 440BX AGPset* (Order Number 243735), AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332), and the *Pentium® II Processor Developer's Manual* (Order Number 243502) for more information.

2.5 Processor System Bus Clock and Processor Clocking

The BCLK input directly controls the operating speed of the Pentium II processor system bus interface. All Pentium II processor system bus timing parameters are specified with respect to the rising edge of the BCLK input. See the *Pentium® II Processor Developer's Manual* (Order Number 243502) for further details.

2.5.1 Mixing Processors of Different Frequencies

Mixing processors of different internal clock frequencies is not supported and has not been validated by Intel. One should also note that when attempting to mix processors rated at different frequencies in a two-way MP system, a common bus clock frequency and a set of multipliers must be found that is acceptable to both processors in the system. A processor may run at a core frequency as low as its minimum rating.

2.6 Voltage Identification

There are five voltage identification pins on the SC 242 connector. These pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor core. The VID pins are needed to cleanly support voltage specification variations on current and future Pentium II processors. These pins (VID[0] through VID[4]) are defined in Table 1. A ‘1’ in this table refers to an open pin and a ‘0’ refers to a short to ground. The definition provided in Table 1 is a superset of the definition previously defined for the Pentium Pro processor. The power supply must supply the voltage that is requested or disable itself.

To ensure the system is ready for current and future Pentium II processors, the range of values in **bold** in Table 1 must be supported. A smaller range will risk the ability of the system to migrate to a higher performance Pentium II processor and/or maintain compatibility with current Pentium II processors.

Table 1. Voltage Identification Definition [1, 2, 3]

Processor Pins					
VID4	**VID3**	**VID2**	**VID1**	**VID0**	**$V_{CC_{CORE}}$**
01111 - 00110					Reserved
0	0	1	0	1	**1.80** [4]
0	0	1	0	0	**1.85** [4]
0	0	0	1	1	**1.90** [4]
0	0	0	1	0	**1.95** [4]
0	0	0	0	1	**2.00** [4]
0	0	0	0	0	**2.05** [4]
1	1	1	1	1	No Core
1	1	1	1	0	**2.1** [4]
1	1	1	0	1	**2.2** [4]
1	1	1	0	0	**2.3** [4]
1	1	0	1	1	**2.4** [4]
1	1	0	1	0	**2.5** [4]
1	1	0	0	1	**2.6** [4]
1	1	0	0	0	**2.7** [4]
1	0	1	1	1	**2.8** [4]
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

NOTES:
1. 0 = Processor pin connected to V_{SS}.
2. 1 = Open on processor; may be pulled up to TTL V_{IH} on motherboard.
3. VRM output should be disabled for $V_{CC_{CORE}}$ values less than 1.80 V.
4. To ensure the system is ready for the Pentium® II processors, the values in **BOLD** in Table 1 must be supported.

Note that the '11111' (all opens) ID can be used to detect the absence of a processor core in a given slot as long as the power supply used does not affect these lines. Detection logic and pull-ups should not affect VID inputs at the power source (see Section 7.0).

The VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator only if required by the regulator or external logic monitoring the VID[4:0] signals. The power source chosen must be guaranteed to be stable whenever the supply to the voltage regulator is stable. This will prevent the possibility of the processor supply going above the specified $V_{CC_{CORE}}$ in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line

pull-ups. A resistor of greater than or equal to 10 kΩ may be used to connect the VID signals to the converter input. Note that no changes have been made to the physical connector between the VRM 8.1 and VRM 8.2 specifications, though pin definitions have changed.

2.7 Processor System Bus Unused Pins

All RESERVED pins must remain unconnected. Connection of these pins to $V_{CC_{CORE}}$, V_{CCL2}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Pentium II processors. See Section 5.4 for a pin listing of the processor and the location of each RESERVED pin.

All TESTHI pins must be connected to 2.5 V via a pull-up resistor of between 1 and 100 kΩ value.

PICCLK must be driven with a valid clock input and the PICD[1:0] lines must be pulled-up to 2.5 V even when the APIC will not be used. A separate pull-up resistor must be provided for each PICD line (see Table 2 for recommended values).

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused AGTL+ inputs should be left as no connects; AGTL+ termination is provided on the processor. Unused active low CMOS inputs should be connected to 2.5 V. Unused active high inputs should be connected to ground (V_{SS}). Unused outputs can be left unconnected. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused pins, it is suggested that ~10 kΩ resistors be used for pull-ups (except for PICD[1:0] discussed above), and ~1 kΩ resistors be used as pull-downs.

2.8 Processor System Bus Signal Groups

In order to simplify the following discussion, the Pentium II processor system bus signals have been combined into groups by buffer type. **All Pentium II processor system bus outputs are open drain** and require a high-level source provided externally by the termination or pull-up resistor.

AGTL+ input signals have differential input buffers, which use V_{REF} as a reference signal. AGTL+ output signals require termination to 1.5 V. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0Ω) resistors. The 0Ω resistors should be placed in close proximity to the SC 242 connector. The path to chassis ground should be short in length and have a low impedance.

The CMOS, Clock, APIC, and TAP inputs can each be driven from ground to 2.5 V. The CMOS, APIC, and TAP outputs are open drain and should be pulled high to 2.5 V. This ensures not only correct operation for current Pentium II processors, but compatibility for future Pentium II products as well. See Table 2 for recommended pull-up resistor values on each CMOS signal. ~150Ω resistors are expected on the PICD[1:0] lines; other values in Table 2 are specified for proper logic analyzer and test mode operation only.

Table 2. Recommended Pull-up Resistor Values (Approximate) for CMOS Signals [1, 2, 3]

Recommended Resistor Value (Approximate)	CMOS Signal
150Ω	TDI, TDO, TMS, PICD[0], PICD[1]
150Ω – 220Ω	FERR#, IERR#, THERMTRIP#
150Ω – 330Ω	A20M#, IGNNE#, INIT#, LINT[1]/NMI, LINT[0]/INTR, PWRGOOD, SLP#, PREQ#
410Ω	STPCLK#, SMI#
500Ω	FLUSH#
1KΩ–100KΩ	TESTHI[4]

NOTES:
1. These resistor values are recommended for system implementations using open-drain CMOS buffers.
2. ~150Ω resistors are expected for these signals. This value may vary by system and should be correlated with the output drive characteristics of the devices generating the input signals. Other approximate values are recommended for proper operation with the Pentium® II processor Logic Analyzer Interface.
3. **TRST# must be pulled to ground via a 680Ω resistor or driven low at power on with the assertion of RESET#** (see Table 19).
4. 1K–10KΩ pullup to 2.0 V ($V_{CC_{CORE}}$) or, if 2.5 V ramps after core, pull up TESTHI to 2.5V ($V_{CC2.5}$) with a 100 kΩ resistor.

The groups and the signals contained within each group are shown in Table 3. Refer to Section 7.0 for descriptions of these signals.

Table 3. System Bus Signal Groups

Group Name	Signals
AGTL+ Input	BPRI#, BR1#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
AGTL+ Output	PRDY#
AGTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#[1], D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
CMOS Input[5]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD[2], SMI#, SLP#[3], STPCLK#
CMOS Output[5]	FERR#, IERR#, THERMTRIP#[4]
System Bus Clock	BCLK
APIC Clock	PICCLK
APIC I/O[5]	PICD[1:0]
TAP Input[5]	TCK, TDI, TMS, TRST#
TAP Output[5]	TDO
Power/Other[6]	$V_{CC_{CORE}}$, V_{CCL2}, V_{CC5}, VID[4:0], V_{TT}, V_{SS}, SLOTOCC#, THERMDP, THERMDN, 100/66#, EMI

NOTES:
1. The BR0# pin is the only BREQ# signal that is bidirectional. The internal BREQ# signals are mapped onto BR# pins after the agent ID is determined. See Section 7.0 for more information.
2. See Section 7.0 for information on the PWRGOOD signal.
3. See Section 7.0 for information on the SLP# signal.
4. See Section 7.0 for information on the THERMTRIP# signal.
5. These signals are specified for 2.5 V operation. See Table 2 for recommended pull-up resistor values.
6. $V_{CC_{CORE}}$ is the power supply for the processor core and L2 cache I/O logic.
   V_{CCL2} is the power supply for the L2 cache component core logic.
   VID[4:0] is described in Section 2.6.
   V_{TT} is used to terminate the system bus and generate VREF on the processor substrate.
   V_{SS} is system ground.
   TESTHI should be connected to 2.5 V with a 1–100 kΩ resistor.
   V_{CC5} is not connected to the Pentium® II processors. This supply is used for the Slot 1 Test Kit.
   SLOTOCC# is described in Section 7.0.
   100/66# is described in Section 2.8.2 and Section 7.0.
   EMI pins are described in Section 7.0.
   THERMDP, THERMDN are described in Section 7.0.

2.8.1 Asynchronous vs. Synchronous for System Bus Signals

All AGTL+ signals are synchronous to BCLK. All of the CMOS, Clock, APIC, and TAP signals can be applied asynchronously to BCLK.

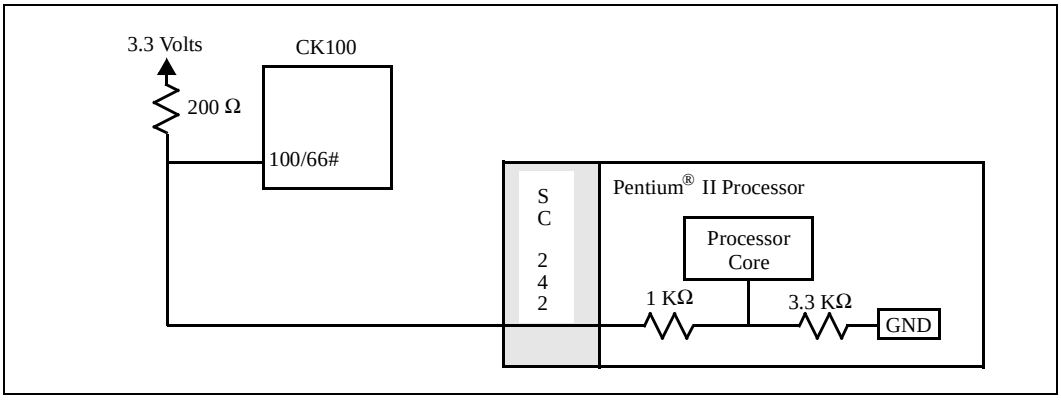
All APIC signals are synchronous to PICCLK. All TAP signals are synchronous to TCK.

2.8.2 System Bus Frequency Select Signal (100/66#)

This bidirectional signal is used to select the system bus frequency. A logic low will select a 66 MHz system bus frequency and a logic high (3.3 V) will select a 100 MHz system bus frequency. The frequency is determined by the processor(s), AGPset and frequency synthesizer. All system bus agents must operate at the same frequency; in a two-way MP Pentium II processor configuration, this signal must connect the pins of both Pentium II processors. This signal will be grounded by processors that are only capable of operating at a host frequency of 66 MHz. On

motherboards which support operation at either 66 or 100 MHz, this signal must be pulled up to 3.3 V with a 1/4 W, 200Ω resistor (as shown in Figure 4) and provided as a frequency selection signal to the clock driver/synthesizer. If the system motherboard is not capable of operating at 100 MHz (e.g., Intel 440FX PCIset and 440LX AGPset-based systems), it should ground this signal and generate a 66 MHz system bus frequency. This signal can also be incorporated into RESET# logic on the motherboard if only 100 MHz operation is supported (thus forcing the RESET# signal to remain active as long as the 100/66# signal is low).

Figure 4. 100/66# Pin Example



2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Pentium II processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting a 2.5 V input. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

The Debug Port will have to be placed at the start and end of the TAP chain with the TDI of the first component coming from the Debug Port and the TDO from the last component going to the Debug Port. In a two-way MP system, be cautious when including an empty SC 242 connector in the scan chain. All connectors in the scan chain must have a processor installed to complete the chain or the system must support a method to bypass the empty connectors; SC 242 terminator substrates should not connect TDI to TDO in order to avoid placing the TDO pull-up resistors in parallel. (See *Slot 1 Bus Terminator Card Design Guidelines* (Order Number 243409) for more details.)

2.10 Maximum Ratings

Table 4 contains Pentium II processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables in Section 2.11 and Section 2.13. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
$V_{CC(All)}$	Any processor supply voltage with respect to V_{SS}	–0.5	Operating voltage + 1.0	V	1, 2
V_{inAGTL}	AGTL+ buffer DC input voltage with respect to V_{SS}	–0.3	$V_{CC_{CORE}}$ + 0.7	V	
V_{inCMOS}	CMOS buffer DC input voltage with respect to V_{SS}	–0.3	3.3	V	3
I_{VID}	Max VID pin current		5	mA	
$I_{SLOTOCC}$	Max SLOTOCC# pin current		5	mA	
Mech Max Latch Arms	Mechanical integrity of latch arms		50	Cycles	4
Mech Max Edge Fingers	Mechanical integrity of processor edge fingers		50	Insertions/ Extractions	5, 6

NOTES:
1. Operating voltage is the voltage to which the component is designed to operate. See Table 5.
2. This rating applies to the $V_{CC_{CORE}}$, V_{CCL2}, V_{CC5}, and any input (except as noted below) to the processor.
3. Parameter applies to CMOS, APIC, and TAP bus signal groups only.
4. The mechanical integrity of the latch arms is specified to last a maximum of 50 cycles.
5. The electrical and mechanical integrity of the processor edge fingers are specified to last for 50 insertion/extraction cycles.
6. While insertion/extraction cycling above 50 insertions will cause an increase in the contact resistance (above 0.1Ω) and a degradation in the material integrity of the edge finger gold plating, it is possible to have processor functionality above the specified limit. The actual number of insertions before processor failure will vary based upon system configuration and environmental conditions.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the Pentium II processor edge fingers. See Section 7.0 for the processor edge finger signal definitions and Section 5.0 for the signal listing.

Most of the signals on the Pentium II processor system bus are in the AGTL+ signal group. These signals are specified to be terminated to 1.5 V. The DC specifications for these signals are listed in Table 6.

To allow connection with other devices, the Clock, CMOS, APIC, and TAP signals are designed to interface at non-AGTL+ levels. The DC specifications for these pins are listed in Table 7.

Table 5 through Table 8 list the DC specifications for Pentium II processors operating at 100 MHz processor system bus frequencies. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 5. Voltage and Current Specifications [1]

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes
$V_{CC_{CORE}}$	V_{CC} for processor core		1.9	2.00	2.1	V	2, 4, 5, 6
V_{CCL2}	V_{CC} for second level cache		3.135	3.30	3.465	V	3.3 V ±5% [7]
V_{TT}	AGTL+ bus termination voltage		1.365	1.50	1.635	V	1.5 ±9% [8]
Baseboard Tolerance, Static	Processor core voltage static tolerance level at SC 242 pins		–0.070		0.070	V	4, 9
Baseboard Tolerance, Transient	Processor core voltage transient tolerance level at SC 242 pins		–0.110		0.110	V	4, 9
$V_{CC_{CORE}}$ Tolerance, Static	Processor core voltage static tolerance level at edge fingers		–0.085		0.085	V	4, 10
$V_{CC_{CORE}}$ Tolerance, Transient	Processor core voltage transient tolerance level at edge fingers		–0.140		0.140	V	4, 10
$I_{CC_{CORE}}$	I_{CC} for processor core	350 MHz 400 MHz 450 MHz			10.8 12.0 13.6	A A A	2, 4, 12, 13 2, 4, 12, 13 2, 4, 12, 13
$I_{CC_{L2}}$	I_{CC} for second level cache	350 MHz 400 MHz 450 MHz			0.7 0.9 1.0	A A A	4, 7, 12 4, 7, 12 4, 7, 12
I_{VTT}	Termination voltage supply current				2.7	A	14
I_{SGnt}	I_{CC} Stop-Grant for processor core	350 MHz 400 MHz 450 MHz			0.8 0.9 1.0	A A A	4, 11, 12, 15 4, 11, 12, 15 4, 11, 12, 15
$I_{SG_{ntL2}}$	I_{CC} Stop-Grant for second level cache				0.1	A	4, 7, 12
I_{SLP}	I_{CC} Sleep for processor core	350 MHz 400 MHz 450 MHz			0.8 0.9 1.0	A A A	4, 11, 12 4, 11, 12 4, 11, 12
$I_{SL_{PL2}}$	I_{CC} Sleep for second level cache				0.1	A	4, 7, 12
I_{DSLP}	I_{CC} Deep Sleep for processor core				0.35	A	12
$I_{DSL_{PL2}}$	I_{CC} Deep Sleep for second level cache				0.1	A	
$dI_{CC_{CORE}}/dt$	Power supply current slew rate				20	A/µs	3, 16, 17, 18
$dI_{CC_{L2}}/dt$	L2 cache power supply current slew rate				1	A/µs	16, 17, 18
$dI_{CC_{VTT}}/dt$	Termination current slew rate				8	A/µs	See Table 8 [17, 18]
V_{CC5}	5 V supply voltage		4.75	5.00	5.25	V	5 V ±5% [19]
I_{CC5}	I_{CC} for 5 V supply voltage			1.0		A	19

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. Vcc_{CORE} and Icc_{CORE} supply the processor core and the TagRAM and BSRAM I/O buffers.
3. This specification applies only to the Pentium® II processor. Unless otherwise noted, this specification applies to all Pentium II processor frequencies and cache sizes.
4. This specification applies only to the Pentium II processor when operating with a 100 MHz Pentium II processor system bus. Unless otherwise noted, this specification applies to all Pentium II processor cache sizes.
5. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.5 and Table 1 for more information.
6. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
7. V_{CCL2} and I_{CCL2} supply the second level cache. Unless otherwise noted, this specification applies to all Pentium II processor cache sizes. Systems should be designed for these specifications, even if a smaller cache size is used.
8. V_{TT} must be held to 1.5 V ±9%. It is recommended that V_{TT} be held to 1.5 V ±3% while the Pentium II processor system bus is idle. This is measured at the processor edge fingers.
9. These are the tolerance requirements, across a 20 MHz bandwidth, at the SC 242 connector pin on the bottom side of the baseboard. The requirements at the SC 242 connector pins account for voltage drops (and impedance discontinuities) across the connector, processor edge fingers, and to the processor core. Vcc_{CORE} must return to within the static voltage specification within 100 µs after a transient event.
10. These are the tolerance requirements, across a 20 MHz bandwidth, at the processor edge fingers. The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. Vcc_{CORE} must return to within the static voltage specification within 2 µs after a transient event.
11. These are estimated values not actual measurements.
12. Max I_{CC} measurements are measured at V_{CC} max voltage, 95 °C ±2 °C, under maximum signal loading conditions. The Max Icc currents specified do not occur simultaneously under the stress measurement condition.
13. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of Vcc_{CORE} (Vcc_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:

$$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times Vcc_{CORE\_TYP} / (Vcc_{CORE\_TYP} + Vcc_{CORE} \text{ Tolerance, Transient})$$

14. The current specified is the current required for a single Pentium II processor. A similar amount of current is drawn through the termination resistors on the opposite end of the AGTL+ bus, unless single-ended termination is used (see Section 2.1).
15. The current specified is also for AutoHALT state.
16. Maximum values are specified by design/characterization at nominal Vcc_{CORE} and nominal V_{CCL2}.
17. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
18. dI_{CC}/dt specifications are measured and specified at the SC 242 connector pins.
19. V_{CC5} and I_{CC5} are not used by the Pentium II processors. This supply is used for the SC 242 Test Kit.

Table 6. AGTL+ Signal Groups DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.82	V	
V_{IH}	Input High Voltage	1.22	V_{TT}	V	2, 3, 7, 8
Ron	Buffer On Resistance		16.67	Ω	6
I_L	Leakage Current		±100	µA	4
I_{LO}	Output Leakage Current		±15	µA	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. V_{IH} and V_{OH} for the Pentium II processor may experience excursions of up to 200 mV above V_{TT} for a single system bus clock. However, input signal drivers must comply with the signal quality specifications in Section 3.0.
3. Minimum and maximum V_{TT} are given in Table 8.
4. ($0 \le V_{IN} \le 2.0$ V +5%).
5. ($0 \le V_{OUT} \le 2.0$ V +5%).
6. Refer to the I/O Buffer Models for IV characteristics.
7. Parameter correlated to measure into a 25Ω resistor terminated to 1.5 V.
8. Refer to the IO Buffer Models for IV characteristics.

Table 7. Non-AGTL+ Signal Group DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.5	V	
V_{IH}	Input High Voltage	2.0	2.625	V	2.5 V +5% maximum
V_{OL}	Output Low Voltage		0.4	V	2
V_{OH}	Output High Voltage	N/A	2.625	V	All outputs are open-drain to 2.5 V +5%
I_{OL}	Output Low Current	14		mA	
I_{LI}	Input Leakage Current		±100	µA	3
I_{LO}	Output Leakage Current		±15	µA	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. Parameter measured at 14 mA (for use with TTL inputs).
3. ($0 \le V_{IN} \le 2.5$ V +5%).
4. ($0 \le V_{OUT} \le 2.5$ V +5%).

2.12 AGTL+ System Bus Specifications

It is recommended that the AGTL+ bus be routed in a daisy-chain fashion with termination resistors to V_{TT} at each end of the signal trace. These termination resistors are placed electrically between the ends of the signal traces and the V_{TT} voltage supply and generally are chosen to approximate the substrate impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}.

Table 8 lists the nominal specification for the AGTL+ termination voltage (V_{TT}). The AGTL+ reference voltage (V_{REF}) is generated on the processor substrate for the processor core, but should be set to 2/3 V_{TT} for other AGTL+ logic using a voltage divider on the motherboard. It is important that the motherboard impedance be specified and held to a 65Ω±15% tolerance, and that the

intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on GTL+, see the *Pentium® II Processor Developer's Manual* (Order Number 243502) and AP-827, *100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel® 440BX AGPset* (Order Number 243735).

Table 8. AGTL+ Bus Specifications [1, 2]

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{TT}	Bus Termination Voltage	1.365	1.50	1.635	V	1.5 V ±9% [3]
R_{TT}	Termination Resistor		56		Ω	±5%
V_{REF}	Bus Reference Voltage		2/3 V_{TT}		V	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. Pentium II processors contain AGTL+ termination resistors at the end of each signal trace on the processor substrate. Pentium II processors generate V_{REF} on the processor substrate by using a voltage divider on V_{TT} supplied through the SC 242 connector.
3. V_{TT} must be held to 1.5 V ±9%; $dI_{CC_{VTT}}/dt$ is specified in Table 5. It is recommended that V_{TT} be held to 1.5 V ±3% while the Pentium II processor system bus is idle. This is measured at the processor edge fingers.
4. V_{REF} is generated on the processor substrate to be 2/3 V_{TT} nominally.

2.13 System Bus AC Specifications

The Pentium II processor system bus timings specified in this section are defined at the Pentium II processor edge fingers and the processor core pads. Unless otherwise specified, timings are tested at the processor core during manufacturing. Timings at the processor edge fingers are specified by design characterization. See Section 7.0 for the Pentium II processor edge connector signal definitions. See the *Pentium® II Processor at 233, 266, 300, and 333 MHz* (Order Number 243335) for more detail.

Table 9 through Table 20 list the AC specifications associated with the Pentium II processor system bus. These specifications are broken into the following categories: Table 9 through Table 11 contain the system bus clock core frequency and cache bus frequencies, Table 12 and Table 13 contain the AGTL+ specifications, Table 14 and Table 15 are the CMOS signal group specifications, Table 16 contains timings for the Reset conditions, Table 17 and Table 18 cover APIC bus timing, and Table 19 and Table 20 cover TAP timing. For each pair of tables, the first table contains timing specifications for measurement or simulation at the processor edge fingers. The second table contains specifications for simulation at the processor core pads.

All Pentium II processor system bus AC specifications for the AGTL+ signal group are relative to the rising edge of the BCLK input. All AGTL+ timings are referenced to V_{REF} for both ‘0’ and ‘1’ logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium II processor in Quad format as the *Pentium® II Processor I/O Buffer Models*, Quad Format (Electronic Form) on Intel’s website: “http://www.intel.com.” GTL+ layout guidelines are also available in AP-827, *100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel® 440BX AGPset* (Order Number 243735).

Care should be taken to read all notes associated with a particular timing parameter.

Table 9. System Bus AC Specifications (Clock) at the Processor Edge Fingers [1, 2, 3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency			100.00	MHz		All processor core frequencies [4]
T1': BCLK Period	10.0			ns	6	4, 5
T1B': SC 242 to Core Logic BCLK Offset		0.78		ns	6	Absolute Value [7, 8]
T2': BCLK Period Stability						See Table 10
T3': BCLK High Time	2.1			ns	6	@>2.0 V [6]
T4': BCLK Low Time	1.97			ns	6	@<0.5 V [6]
T5': BCLK Rise Time	0.88		2.37	ns	6	(0.5 V–2.0 V) [6, 9]
T6': BCLK Fall Time	1.13		2.94	ns	6	(2.0 V–0.5 V) [6, 9]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.7 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
4. The internal core clock frequency is derived from the Pentium II processor system bus clock. The system bus clock to core clock ratio is determined during initialization as described in Section 2.5. Table 11 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns -0.0ns tolerance for clock driver variation.
6. This specification applies to Pentium II processors when operating with a Pentium II processor system bus frequency of 100 MHz.
7. The BCLK offset time is the absolute difference needed between the BCLK signal arriving at the Pentium II processor edge finger at 0.5 V vs. arriving at the core logic at 1.25 V. The positive offset is needed to account for the delay between the SC 242 connector and processor core. The positive offset ensures both the processor core and the core logic receive the BCLK edge concurrently.
8. See Section 3.1 for Pentium II processor system bus clock signal quality specifications.
9. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 10. System Bus AC Specifications (Clock) at Processor Core Pins [1, 2, 3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency			100.00	MHz		All processor core frequencies [4]
T1: BCLK Period	10.0			ns	6	4, 5, 6, 10
T2: BCLK Period Stability			±250	ps	6	6, 7, 8, 10
T3: BCLK High Time	2.6			ns	6	@>2.0 V [6]
T4: BCLK Low Time	2.47			ns	6	@<0.5 V [6]
T5: BCLK Rise Time	0.38		1.25	ns	6	(0.5 V–2.0 V) [6, 9]
T6: BCLK Fall Time	0.38		1.5	ns	6	(2.0 V–0.5 V) [6, 9]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor core pins.
4. The internal core clock frequency is derived from the Pentium II processor system bus clock. The system bus clock to core clock ratio is determined during initialization as described in Section 2.5. Table 11 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to the Pentium II processor when operating with a Pentium II processor system bus frequency of 100 MHz.
7. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25 V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
8. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
9. Not 100% tested. Specified by design characterization as a clock driver requirement.
10. The average period over a 1uS period of time must be greater than the minimum specified period.

Table 11. Valid System Bus, Core Frequency, and Cache Bus Frequencies [1, 2]

Core Frequency (MHz)	BCLK Frequency (MHz)	Frequency Multiplier	L2 Cache (MHz)
350.00	100.00	7/2	175.00
400.00	100.00	4/1	200.00
450.00	100.00	9/2	225.00

NOTES:
1. Contact your local Intel representative for the latest information on processor frequencies and/or frequency multipliers.
2. While other bus ratios are defined, operation at frequencies other than those listed are not supported.

Table 12. System Bus AC Specifications (AGTL+ Signal Group)at the Processor Edge Fingers [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T7': AGTL+ Output Valid Delay	0.71	4.66	ns	7	4
T8': AGTL+ Input Setup Time	1.97		ns	8	5, 6, 7
T9': AGTL+ Input Hold Time	1.61		ns	8	8
T10': RESET# Pulse Width	1.00		ms	10	9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for AGTL+ signals are referenced to the BCLK rising edge at 0. 7 V at the processor edge fingers. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor edge fingers.
4. Valid delay timings for these signals are specified into 50Ω to 1.5 V and with V_{REF} at 1.0 V.
5. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
6. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
7. Specification is for a minimum 0.40 V swing.
8. Specification is for a maximum 1.0 V swing.
9. After $V_{CC_{CORE}}$, $V_{CC_{L2}}$, and BCLK become stable.

Table 13. System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	-0.20	3.45	ns	7	4
T8: AGTL+ Input Setup Time	2.10		ns	8	5, 6, 7
T9: AGTL+ Input Hold Time	0.85		ns	8	8
T10: RESET# Pulse Width	1.00		ms	10	6, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor core pins.
4. Valid delay timings for these signals are specified into 25Ω to 1.5 V and with VREF at 1.0 V.
5. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
6. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
7. Specification is for a minimum 0.40 V swing.
8. Specification is for a maximum 1.0 V swing.
9. This should be measured after $V_{CC_{CORE}}$, V_{CCL2}, and BCLK become stable.

Table 14. System Bus AC Specifications (CMOS Signal Group) at the Processor Edge Fingers [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T11': CMOS Output Valid Delay	1.00	10.5	ns	7	5
T12': CMOS Input Setup Time	4.50		ns	8	6, 7, 8
T13': CMOS Input Hold Time	1.50		ns	8	6, 7
T14': CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	7	Active and Inactive states
T15': PWRGOOD Inactive Pulse Width	10		BCLKs	7, 10	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.5 V at the processor edge fingers. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. Valid delay timings for these signals are specified to 2.5 V +5%. See Table 2 for pull-up resistor values.
6. To ensure recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
7. INTR and NMI are only valid when the local APIC is disabled. LINT[1:0] are only valid when the local APIC is enabled.
8. When driven inactive or after $V_{CC_{CORE}}$, V_{CCL2}, and BCLK become stable.

Table 15. System Bus AC Specifications (CMOS Signal Group)at the Processor Core Pins [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T11: CMOS Output Valid Delay	0.00	8.00	ns	7	5
T12: CMOS Input Setup Time	4.00		ns	8	6, 7, 8
T13: CMOS Input Hold Time	1.30		ns	8	6, 7
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	7	Active and Inactive states
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	7, 10	9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. These specifications are tested during manufacturing.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pins. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. Valid delay timings for these signals are specified to 2.5 V +5%. See Table 2 for pull-up resistor values.
6. This specification applies to Pentium II processors operating with a 100-MHz Pentium II processor system bus only.
7. To ensure recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
8. INTR and NMI are only valid when the local APIC is disabled. LINT[1:0] are only valid when the local APIC is enabled.
9. When driven inactive or after $V_{CC_{CORE}}$, V_{CCL2}, and BCLK become stable.

Table 16. System Bus AC Specifications (Reset Conditions) [1]

T# Parameter	Min	Max	Unit	Figure	Notes
T16: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	9	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	9	After clock that deasserts RESET#
T18: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Setup Time	1		ms	9	Before deassertion of RESET#
T19: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Delay Time		5	BCLKs	9	After assertion of RESET# [2]
T20: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Hold Time	2	20	BCLKs	9, 10	After clock that deasserts RESET#

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. For a Reset, the clock ratio defined by these signals must be a safe value (their final or a lower multiplier) within this delay unless PWRGOOD is being driven inactive.

Table 17. System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Edge Fingers [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T21': PICCLK Frequency	2.0	33.3	MHz		
T22': PICCLK Period	30.0	500.0	ns	6	
T23': PICCLK High Time	12.0		ns	6	
T24': PICCLK Low Time	12.0		ns	6	
T25': PICCLK Rise Time	1.0	5.0	ns	6	
T26': PICCLK Fall Time	1.0	5.0	ns	6	
T27': PICD[1:0] Setup Time	8.5		ns	8	4
T28': PICD[1:0] Hold Time	3.0		ns	8	4
T29': PICD[1:0] Valid Delay	3.0	12.0	ns	7	4, 5, 6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 0.7 V at the processor edge fingers. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
4. Referenced to PICCLK rising edge.
5. For open drain signals, valid delay is synonymous with float delay.
6. Valid delay timings for these signals are specified to 2.5 V +5%. See Table 2 for recommended pull-up resistor values.

Table 18. System Bus AC Specifications (APIC Clock and APIC I/O)at the Processor Core Pins [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	6	
T23: PICCLK High Time	12.0		ns	6	
T24: PICCLK Low Time	12.0		ns	6	
T25: PICCLK Rise Time	1.0	5.0	ns	6	
T26: PICCLK Fall Time	1.0	5.0	ns	6	
T27: PICD[1:0] Setup Time	8.0		ns	8	4
T28: PICD[1:0] Hold Time	2.5		ns	8	4
T29: PICD[1:0] Valid Delay	1.5	10.0	ns	7	4, 5, 6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor core pins. All APIC I/O signal timings are referenced at 1.25 V at the processor core pins.
4. Referenced to PICCLK rising edge.
5. For open drain signals, valid delay is synonymous with float delay.
6. Valid delay timings for these signals are specified to 2.5 V +5%. See Table 2 for recommended pull-up resistor values.

Table 19. System Bus AC Specifications (TAP Connection)at the Processor Edge Fingers [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T30': TCK Frequency		16.667	MHz		
T31': TCK Period	60.0		ns	6	
T32': TCK High Time	25.0		ns	6	@1.7 V
T33': TCK Low Time	25.0		ns	6	@0.7 V
T34': TCK Rise Time		5.0	ns	6	(0.7 V–1.7 V) [4]
T35': TCK Fall Time		5.0	ns	6	(1.7 V–0.7 V) [4]
T36': TRST# Pulse Width	40.0		ns	12	Asynchronous
T37': TDI, TMS Setup Time	5.5		ns	11	5
T38': TDI, TMS Hold Time	14.5		ns	11	5
T39': TDO Valid Delay	2.0	13.5	ns	11	6, 7
T40': TDO Float Delay		28.5	ns	11	6, 7
T41': All Non-Test Outputs Valid Delay	2.0	27.5	ns	11	6, 8, 9
T42': All Non-Test Inputs Setup Time		27.5	ns	11	6, 8, 9
T43': All Non-Test Inputs Setup Time	5.5		ns	11	5, 8, 9
T44': All Non-Test Inputs Hold Time	14.5		ns	11	5, 8, 9

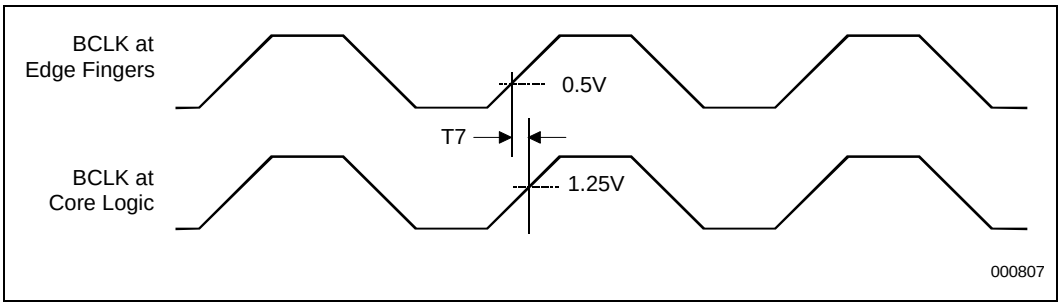
NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 0.7 V at the processor edge fingers. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.
3. Not 100% tested. Specified by design characterization.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%. See Table 2 for pull-up resistor values.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.

Table 20. System Bus AC Specifications (TAP Connection)at the Processor Core Pins [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T30: TCK Frequency		16.667	MHz		
T31: TCK Period	60.0		ns	6	
T32: TCK High Time	25.0		ns	6	@1.7 V [10]
T33: TCK Low Time	25.0		ns	6	@0.7 V [10]
T34: TCK Rise Time		5.0	ns	6	(0.7 V–1.7 V) [4, 10]
T35: TCK Fall Time		5.0	ns	6	(1.7 V–0.7 V) [4, 10]
T36: TRST# Pulse Width	40.0		ns	12	Asynchronous [10]
T37: TDI, TMS Setup Time	5.0		ns	11	5
T38: TDI, TMS Hold Time	14.0		ns	11	5
T39: TDO Valid Delay	1.0	10.0	ns	11	6, 7
T40: TDO Float Delay		25.0	ns	11	6, 7, 10
T41: All Non-Test Outputs Valid Delay	2.0	25.0	ns	11	6, 8, 9
T42: All Non-Test Inputs Setup Time		25.0	ns	11	6, 8, 9, 10
T43: All Non-Test Inputs Setup Time	5.0		ns	11	5, 8, 9
T44: All Non-Test Inputs Hold Time	13.0		ns	11	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 1.25 V at the processor core pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor core pins.
3. These specifications are tested during manufacturing, unless otherwise noted.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%. See Table 2 for pull-up resistor values.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.
10. Not 100% tested. Specified by design characterization.

Figure 5. BCLK to Core Logic Offset



Note: For Figure 6 through Figure 12, the following apply:

1. Figure 6 through Figure 12 are to be used in conjunction with Table 9 through Table 20.
2. All AC timings for the AGTL+ signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the AGTL+ signals at the processor core pins are referenced to the BCLK rising edge at 1.25 V. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
4. All AC timings for the CMOS signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
5. All AC timings for the APIC I/O signals at the processor edge fingers are referenced to the PICCLK rising edge at 0.7 V. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
6. All AC timings for the TAP signals at the processor edge fingers are referenced to the TCK rising edge at 0.70 V. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.

Figure 6. BCLK, PICCLK, and TCK Generic Clock Waveform

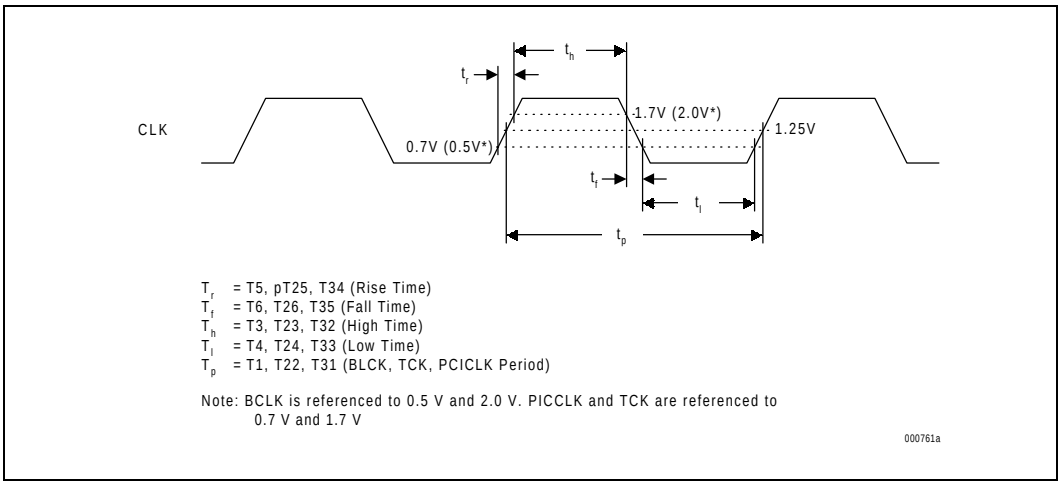


Figure 7. System Bus Valid Delay Timings

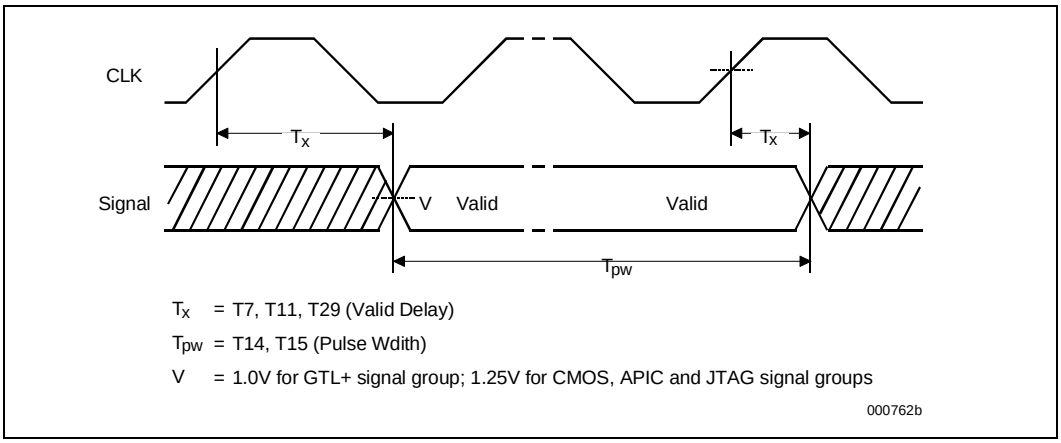


Figure 8. System Bus Setup and Hold Timings

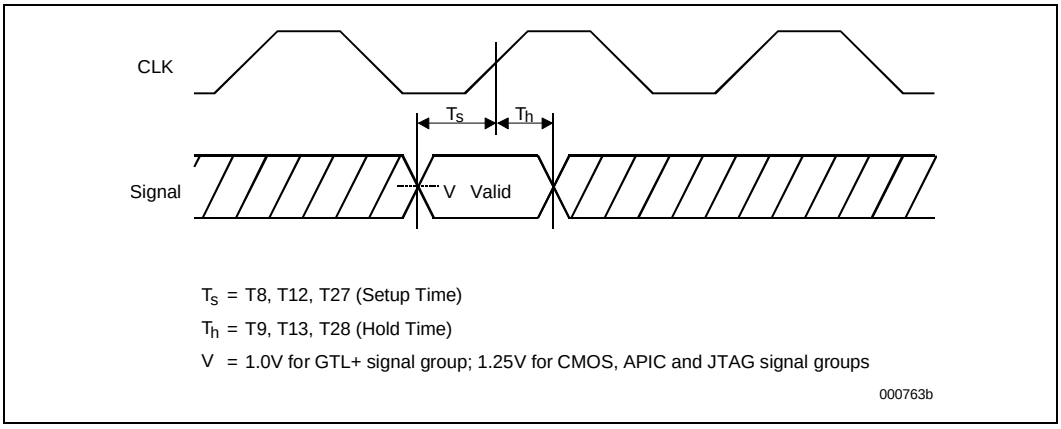


Figure 9. System Bus Reset and Configuration Timings

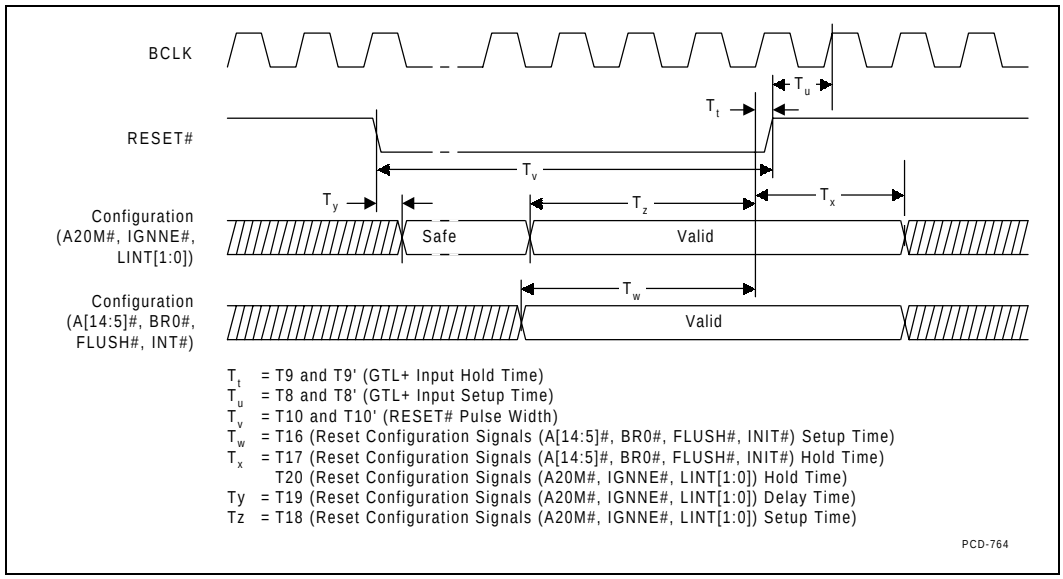


Figure 10. Power-On Reset and Configuration Timings

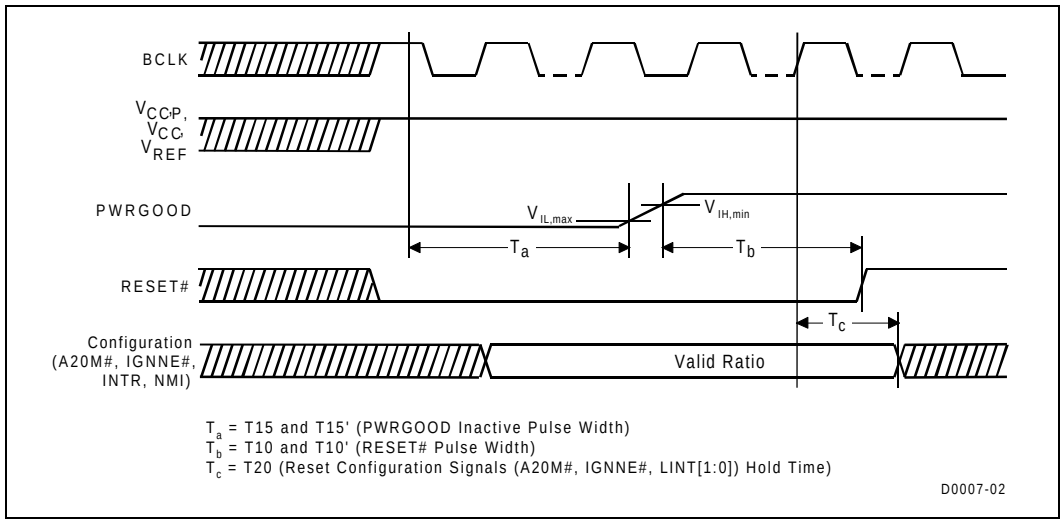


Figure 11. Test Timings (TAP Connection)

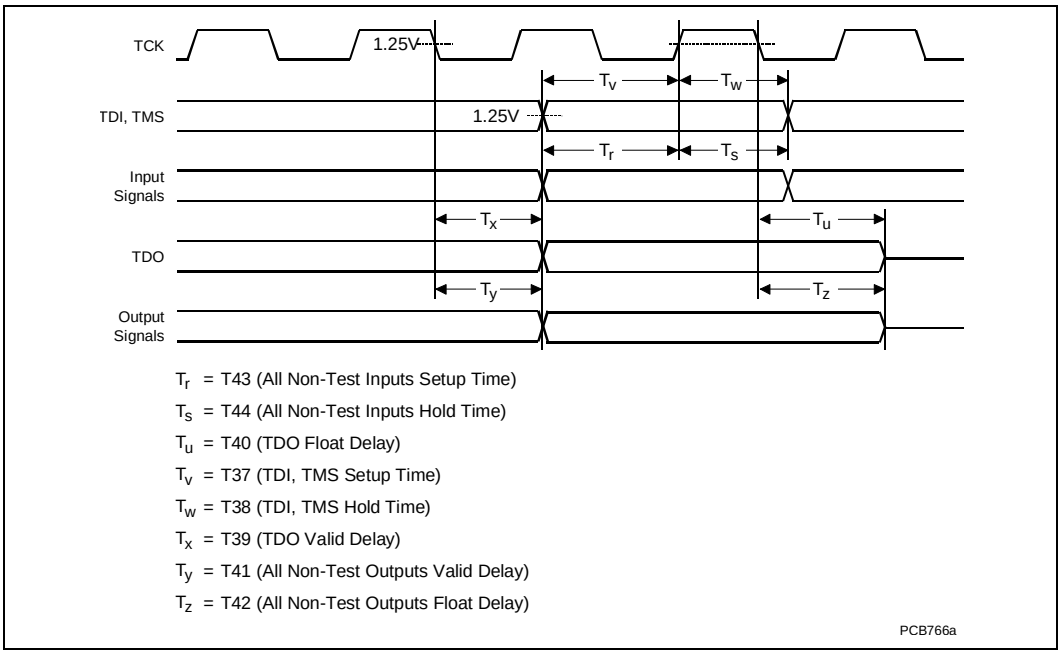
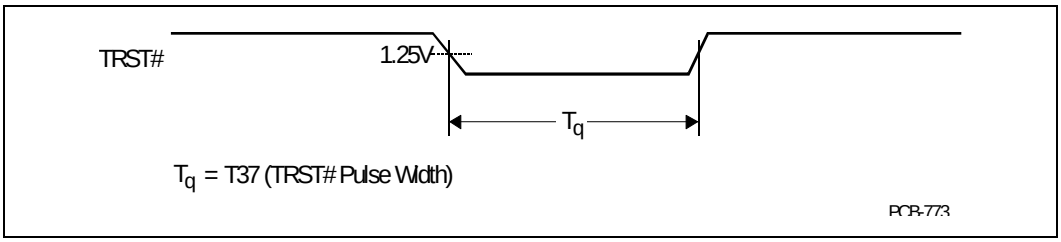


Figure 12. Test Reset Timings



3.0 System Bus Signal Simulations

Signals driven on the Pentium II processor system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. Specifications are provided for simulation at the processor core; guidelines are provided for correlation to the processor edge fingers. These edge finger guidelines are intended for use during testing and measurement of system signal integrity. Violations of these guidelines are permitted, but if they occur, simulation of signal quality at the processor core should be performed to ensure that no violations of signal quality specifications occur. Meeting the specifications at the processor core in Table 21, Table 23, and Table 25 ensures that signal quality effects will not adversely affect processor operation, but does not necessarily guarantee that the guidelines in Table 22, Table 24, and Table 26 will be met.

3.1 System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines

Table 21 describes the signal quality specifications at the processor core for the Pentium II processor system bus clock (BCLK) signal. Table 22 describes guidelines for signal quality measurement at the processor edge fingers. Figure 13 describes the signal quality waveform for the system bus clock at the processor core pins. Figure 14 describes the signal quality waveform for the system bus clock at the processor edge fingers.

Table 21. BCLK Signal Quality Specifications for Simulation at the Processor Core [1]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: BCLK V_{IL}			0.5	V	13	
V2: BCLK V_{IH}	2.0			V	13	2
V3: V_{IN} Absolute Voltage Range	–0.7		3.3	V	13	2
V4: Rising Edge Ringback	1.7			V	13	3
V5: Falling Edge Ringback			0.7	V	13	3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. This is the Pentium II processor system bus clock overshoot and undershoot specification for 100-MHz system bus operation.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 13. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pins

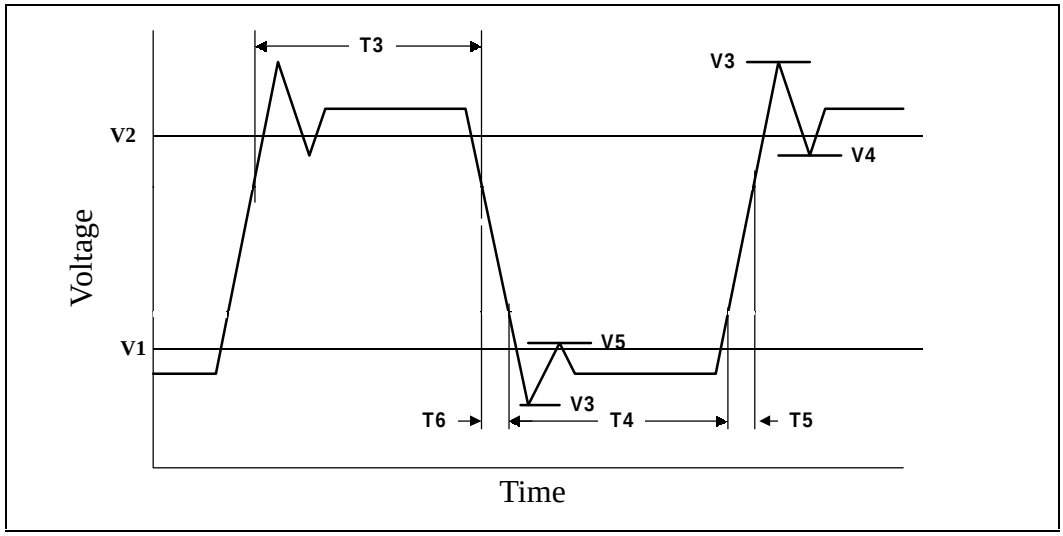
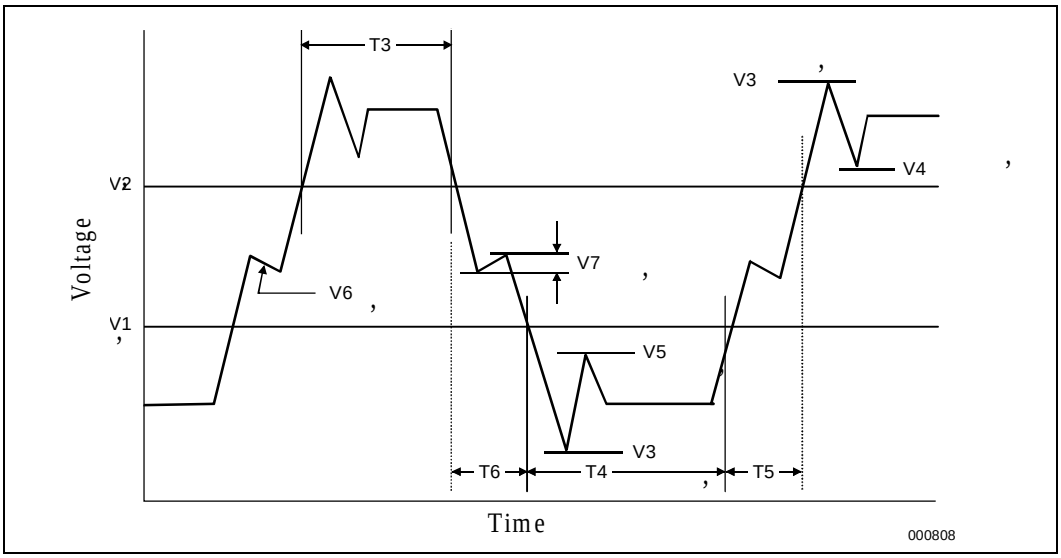


Table 22. BCLK Signal Quality Guidelines for Edge Finger Measurement [1]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1': BCLK V_{IL}			0.5	V	14	
V2': BCLK V_{IH}	2.0			V	14	
V3': V_{IN} Absolute Voltage Range	–0.5		3.3	V	14	2
V4': Rising Edge Ringback	2.0			V	14	3
V5': Falling Edge Ringback			0.5	V	14	3
V6': T_{line} Ledge Voltage	1.0		1.7	V	14	At Ledge Midpoint [4]
V7': T_{line} Ledge Oscillation			0.2	V	14	Peak-to-Peak [5]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. This is the Pentium II processor system bus clock overshoot and undershoot measurement guideline.
3. The rising and falling edge ringback voltage guideline is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal may dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This guideline is an absolute value.
4. The BCLK at the processor edge fingers may have a dip or ledge midway on the rising or falling edge. The midpoint voltage level of this ledge should be within the range of the guideline.
5. The ledge (V7') is allowed to have peak-to-peak oscillation as given in the guideline.

Figure 14. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Edge Fingers



3.2 AGTL+ Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of GTL+ layout guidelines which are available in AP-827, *100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel® 440BX AGPset* (Order Number 243735). Refer to the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the GTL+ buffer specification.

Table 23 provides the AGTL+ signal quality specifications for Pentium II processors for use in simulating signal quality at the processor core. Table 24 provides AGTL+ signal quality guidelines for measuring and testing signal quality at the processor edge fingers. Figure 15 describes the signal quality waveform for AGTL+ signals at the processor core and edge fingers. For more information on the AGTL+ interface, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

Table 23. AGTL+ Signal Groups Ringback Tolerance Specifications at the Processor Core [1, 2, 3]

T# Parameter	Min	Unit	Figure	Notes
α: Overshoot	100	mV	15	4
τ: Minimum Time at High	0.50	ns	15	4
ρ: Amplitude of Ringback	–20	mV	15	4, 5, 6
ϕ: Final Settling Voltage	20	mV	15	4
δ: Duration of Squarewave Ringback	N/A	ns	15	

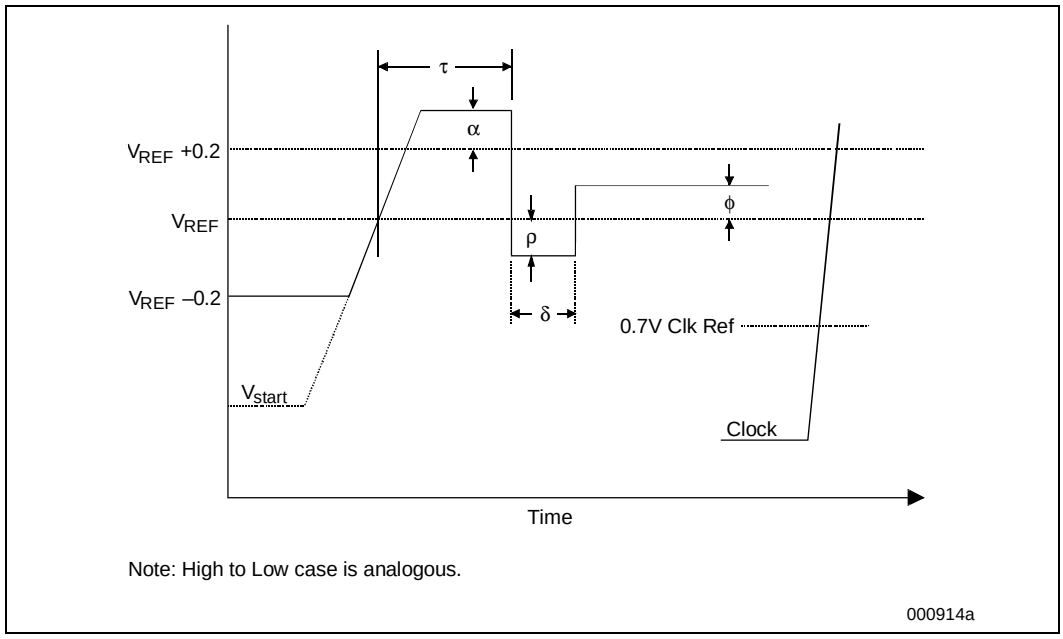
NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.
2. Specifications are for the edge rate of 0.3 - 0.8 V/ns. See Figure 15 for the generic waveform.
3. All values specified by design characterization.
4. This specification applies to Pentium II processors operating with a 100-MHz Pentium II processor system bus only.
5. Ringback below V_{REF} + 20 mV is not supported.
6. Intel recommends performing simulations using an amplitude of -120 mV to allow margin for other sources of system noise.

Table 24. AGTL+ Signal Groups Ringback Tolerance Guidelines for Edge Finger Measurement [1, 2, 3]

T# Parameter	Min	Unit	Figure	Notes
α': Overshoot	100	mV	15	
τ': Minimum Time at High	0.5	ns	15	4
ρ': Amplitude of Ringback	–210	mV	15	4,5
ϕ': Final Settling Voltage	210	mV	15	4
δ': Duration of Squarewave Ringback	N/A	ns	15	

NOTES:
1. Unless otherwise noted, all guidelines in this table apply to all Pentium® II processor frequencies and cache sizes.
2. Guidelines are for the edge rate of 0.3 - 0.8 V/ns. See Figure 15 for the generic waveform.
3. All values specified by design characterization.
4. This guideline applies to Pentium II processors operating with a 100-MHz Pentium II processor system bus only.
5. Ringback below V_{REF} + 210 mV is not supported.

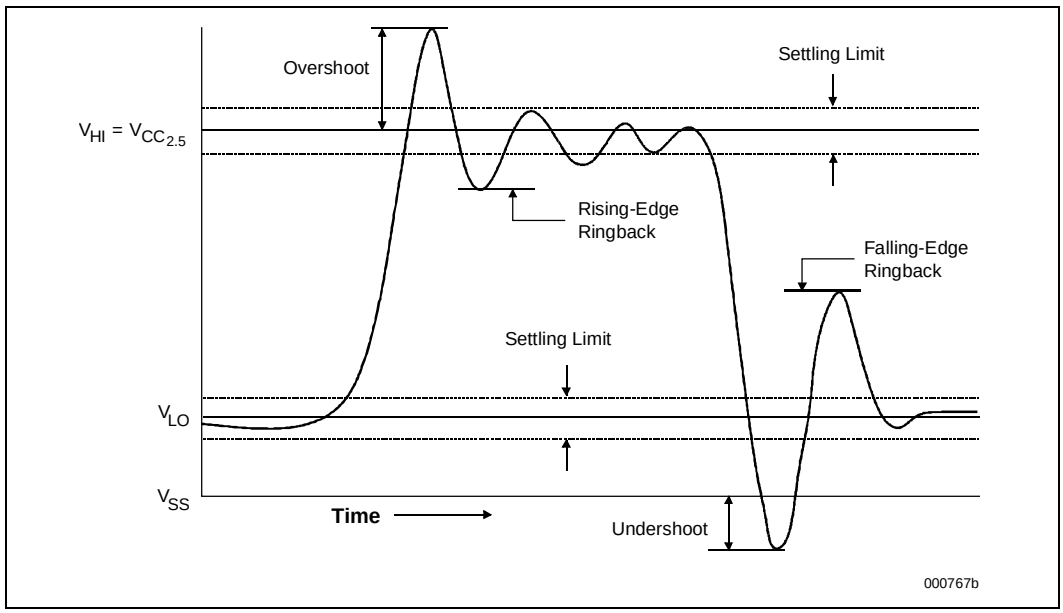
Figure 15. Low to High AGTL+ Receiver Ringback Tolerance



3.3 Non-AGTL+ Signal Quality Specifications and Measurement Guidelines

There are three signal quality parameters defined for non-AGTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Figure 16 for the non-AGTL+ signal group.

Figure 16. Non-AGTL+ Overshoot/Undershoot, Settling Limit, and Ringback



3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS}. The overshoot/undershoot guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. (See Figure 16 for non-AGTL+ signals.) The processor can be damaged by repeated overshoot events on 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). However, excessive ringback is the dominant detrimental system timing effect resulting from overshoot/undershoot (i.e., violating the overshoot/undershoot guideline will make satisfying the ringback specification difficult). **The overshoot/undershoot guideline is 0.7 V** and assumes the absence of diodes on the input. These guidelines should be verified in simulations **without the on-chip ESD protection diodes present** because the diodes will begin clamping the 2.5 V tolerant signals beginning at approximately 0.7 V above the 2.5 V supply and 0.7 V below V_{SS}. If signals are not reaching the clamping voltage, this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

3.3.2 Ringback Specification

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is **the voltage that the signal rings back to after achieving its maximum absolute value**. (See Figure 16 for an illustration of ringback.) Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for non-AGTL+ signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 25 for the signal ringback specifications for non-AGTL+ signals for simulations at the processor core, and Table 26 for guidelines on measuring ringback at the edge fingers.

Table 25. Signal Ringback Specifications for Non-AGTL+ Signal Simulation at the Processor Core [1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure
Non-AGTL+ Signals	0 → 1	1.7	V	16
Non-AGTL+ Signals	1 → 0	0.7	V	16

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.

Table 26. Signal Ringback Guidelines for Non-AGTL+ Signal Edge Finger Measurement [1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure
Non-AGTL+ Signals	0 → 1	2.0	V	16
Non-AGTL+ Signals	1 → 0	0.7	V	16

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all Pentium® II processor frequencies and cache sizes.

3.3.3 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10% of the total signal swing ($V_{HI}-V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again.

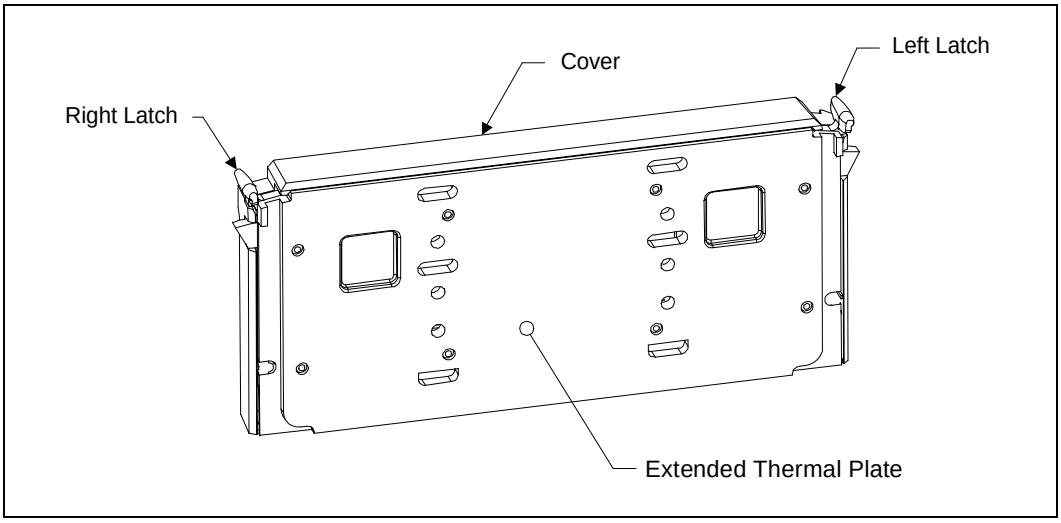
Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

4.0 Thermal Specifications and Design Considerations

Initial Pentium II processors take advatange of S.E.C.C. package technology. This technology uses an extended thermal plate for heatsink attachment. The extended thermal plate interface is intended to provide accessiblity for multiple types of thermal solutions. Follow-on releases of the Pentium II processor use S.E.C.C.2 packaging technology. This pakaging technology doesn't incorporate an extended thermal plate. Processors which use S.E.C.C.2 packaging technology have either a PLGA or an OLGA processor core that is surface mounted onto the substrate. All three of these package variations require unique thermal measuring processes. This chapter provides needed data for designing a thermal solution. However, for the correct thermal measuring processes please refer to AP-586, *Pentium® II Processor Thermal Design Guidelines* (Order Number 243331).

Figure 17 provides a side view of an S.E.C.C. package. This figure provides the thermal plate location.

Figure 17. Pentium® II Processor S.E.C.C. - Side View



4.1 Thermal Specifications

Table 27 and Table 28 provide the thermal design power dissipation and maximum and minimum temperatures for Pentium II processors with S.E.C.C. and S.E.C.C.2 package technologies, respectively. While the processor core dissipates the majority of the thermal power, thermal power dissipated by the L2 cache also impacts the overall processor power specification. Systems should design for the highest possible thermal power, even if a processor with a lower thermal dissipation is planned.

Table 27. Thermal Specifications for S.E.C.C. Packaged Processors [1]

Processor Core Frequency (MHz)	L2 Cache Size (Kbytes)	Processor Power [2] (W)	Extended Thermal Plate Power [3] (W)	Min T_{PLATE} (°C)	Max T_{PLATE} (°C)	Min T_{COVER} (°C)	Max T_{COVER} (°C)
450 [4]	512	27.1	26.4	5	70	5	75
400 [4]	512	24.3	23.6	5	75	5	75
350 [4]	512	21.5	20.8	5	75	5	75

NOTES:
1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor core and nominal V_{CCL2} for the L2 cache.
2. Processor power includes the power dissipated by the processor core, the L2 cache, and the AGTL + bus termination. The maximum power for each of these components does not occur simultaneously.
3. Extended Thermal Plate power is the processor power that is dissipated through the extended thermal plate.
4. These processors use the extended thermal plate for the Pentium® II processor (see Figure 17).

Table 28. Thermal Specifications for S.E.C.C.2 Packaged Processors[1]

Processor Core Frequency (MHz)	L2 Cache Size (Kbytes)	Processor Power [2] (W)	Min PLGA T_{CASE} (°C)	Max PLGA T_{CASE} (°C)	Min OLGA T_{JUNC} (°C)	Max OLGA T_{JUNC} (°C)	L2 Cache Min T_{CASE} (°C)	L2 Cache Max T_{CASE} (°C)	Min T_{COVER} (°C)	Max T_{COVER} (°C)
450	512	27.1	N/A	N/A	5	90	5	105	5	75
400	512	24.3	N/A	N/A	5	90	5	105	5	75
350	512	21.5	5	80	N/A	N/A	5	105	5	75

NOTES:
1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor core and nominal V_{CCL2} for the L2 cache.
2. Processor power includes the power dissipated by the processor core, the L2 cache, and the AGTL + bus termination. The maximum power for each of these components does not occur simultaneously.

For S.E.C.C. packaged processors, the extended thermal plate is the attach location for all thermal solutions. The maximum and minimum extended thermal plate temperatures are specified in Table 27. For S.E.C.C.2 packaged processors, thermal solutions attach to the processor by connecting through the substrate to the cover. The maximum and minimum temperatures of the pertinent locations are specified in Table 28. A thermal solution should be designed to ensure the temperature of the specified locations never exceeds these temperatures.

The total processor power is a result of heat dissipation that is a combination of heat from both the processor core and L2 cache. The overall system chassis thermal design must comprehend the entire processor power. In S.E.C.C. packaged processors, the extended thermal plate power is a component of this power, and is composed of a combination of the processor core and the L2 cache dissipating heat through the extended thermal plate. The heatsink need only be designed to dissipate the extended thermal plate power. See Table 27 for current Pentium II processor thermal design specifications.

For S.E.C.C.2 packaged processors, no extended thermal plate exists and thermal solutions need to contact the core package directly and attach through the substrate to the cover. The total processor power that must be dissipated for S.E.C.C.2 processors can be thought of just as it is for S.E.C.C. packaged processors: a combination of both the processor core and L2 cache. In regards to the core, thermal specifications depend on the packaging technology used. Pentium II processors in S.E.C.C.2 utilizing PLGA core packaging technology have a **case** temperature specified. Pentium II processors in S.E.C.C.2 utilizing OLGA core packaging technology have a **junction** temperature specified. Specifics on how to measure these two paramaters are outlined in AP-586, *Pentium® II Processor Thermal Design Guidelines* (Order Number 243331). In addition, there are surface mounted SRAM components for the L2 Cache on the substrate that have a separate T_{CASE} specification in Table 28.

4.1.1 Thermal Diode

The Pentium II processor incorporates an on-die diode that must be used to monitor the die temperature (junction temperature). A thermal sensor located on the motherboard, or a stand-alone measurement kit, may monitor the die temperature of the Pentium II processor for thermal management or instrumentation purposes.Table 29 and Table 30 provide the diode parameter and interface specifications.

Table 29. Thermal Diode Parameters[1]

Symbol	Min	Typ	Max	Unit	Notes
$I_{forward\ bias}$	5		500	uA	2
n_ideality	1.0000	1.0065	1.0173		3,4

NOTES:
1. Not 100% tested. Specified by design characterization.
2. Intel does not support or recommend operation of the thermal diode under reverse bias.
3. At room temperature with a forward bias of 630 mV.
4. n_ideality is the diode ideality factor parameter, as represented by the diode equation: I-Io(e (Vd*q)/(nkT) - 1).

Table 30. Thermal Diode Interface

Pin Name	SC 242 Connector Signal #	Pin Description
THERMDP	B14	diode anode
THERMDN	B15	diode cathode

5.0 S.E.C.C. and S.E.C.C.2 Mechanical Specifications

Pentium II processors use either S.E.C.C. or S.E.C.C.2 package technology. Both package types contain the processor core, L2 cache, and other passive components. The cartridges connect to the motherboard through an edge connector. Mechanical specifications for the processor are given in this section. See Section 1.1.1 for a complete terminology listing.

5.1 S.E.C.C. Mechnical Specifications

S.E.C.C. package drawings and dimension details are provided in Figure 18 through Figure 27. Figure 18 shows all views of the Pentium II processor in an S.E.C.C. package; Figure 19 through Figure 22 show the S.E.C.C. package dimensions; Figure 23 and Figure 24 show the extended thermal plate dimensions; and Figure 25 and Figure 26 provide details of the processor substrate edge finger contacts. Figure 27 and Table 31 contain processor marking information.

The processor edge connector defined in this document is referred to as the "SC 242 connector." See the *Slot 1 Connector Specification* (Order Number 243397) for further details on the SC 242 connector.

Note: For Figure 18 through Figure 35, the following apply:

1. Unless otherwise specified, the following drawings are dimensioned in inches.
2. All dimensions provided with tolerances are guaranteed to be met for all normal production product.
3. Figures and drawings labeled as "Reference Dimensions" are provided for informational purposes only. Reference Dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference Dimensions are NOT checked as part of the processor manufacturing. Dimensions in parentheses without tolerances are Reference Dimensions.
4. Drawings are not to scale.

Figure 18. Pentium® II Processor (S.E.C.C. Package)—Top and Side View

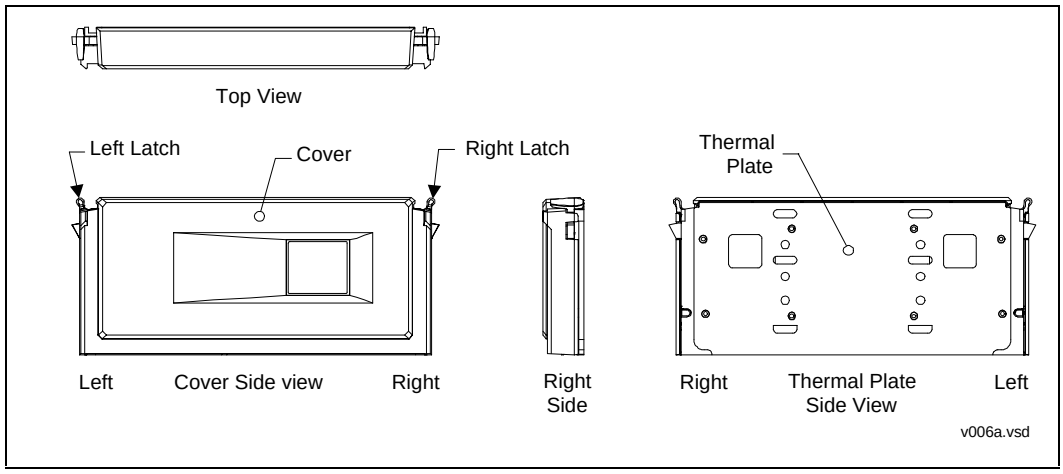


Figure 19. Pentium® II Processor (S.E.C.C. Package)—Extended Thermal Plate Side Dimensions

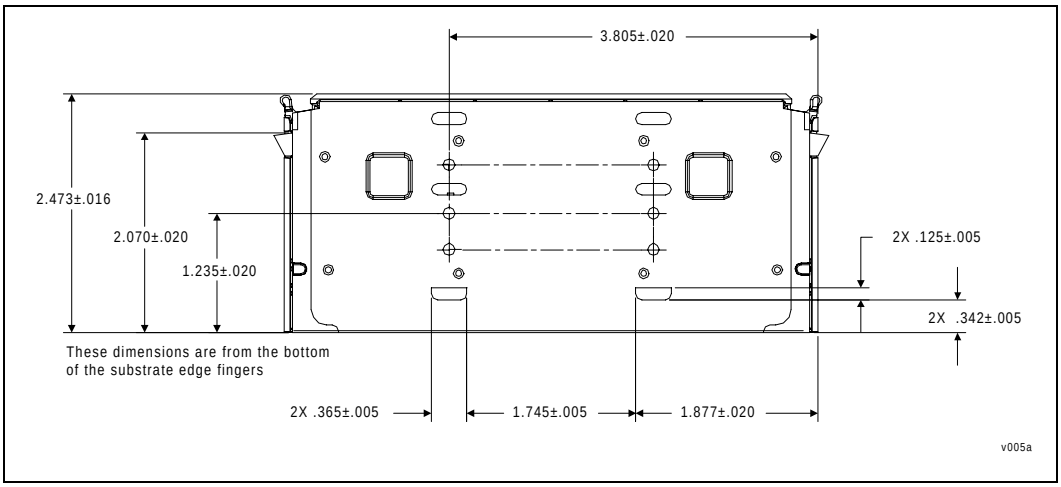


Figure 20. Pentium® II Processor (S.E.C.C. Package)—Bottom View Dimensions

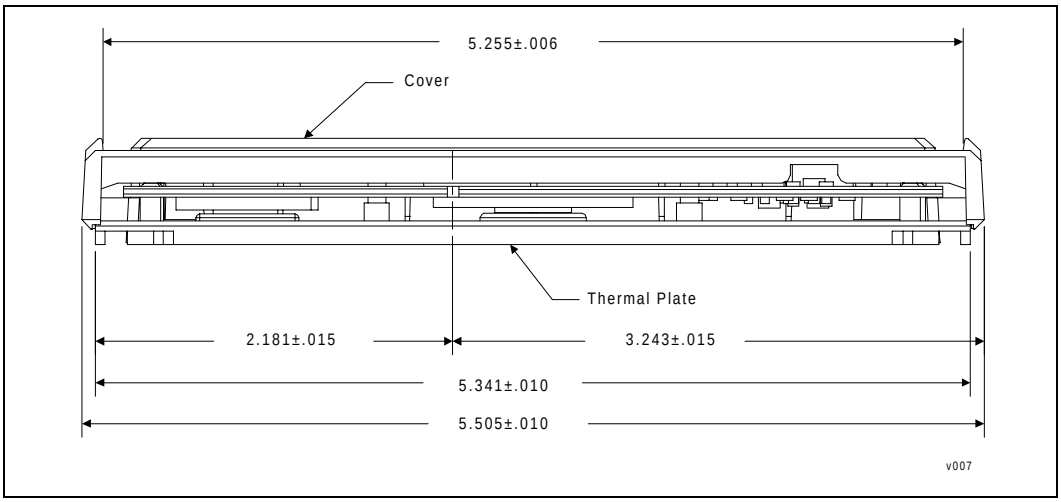


Figure 21. Pentium® II Processor (S.E.C.C. Package)—Latch Arm, Extended Thermal Plate Lug, and Cover Lug Dimensions

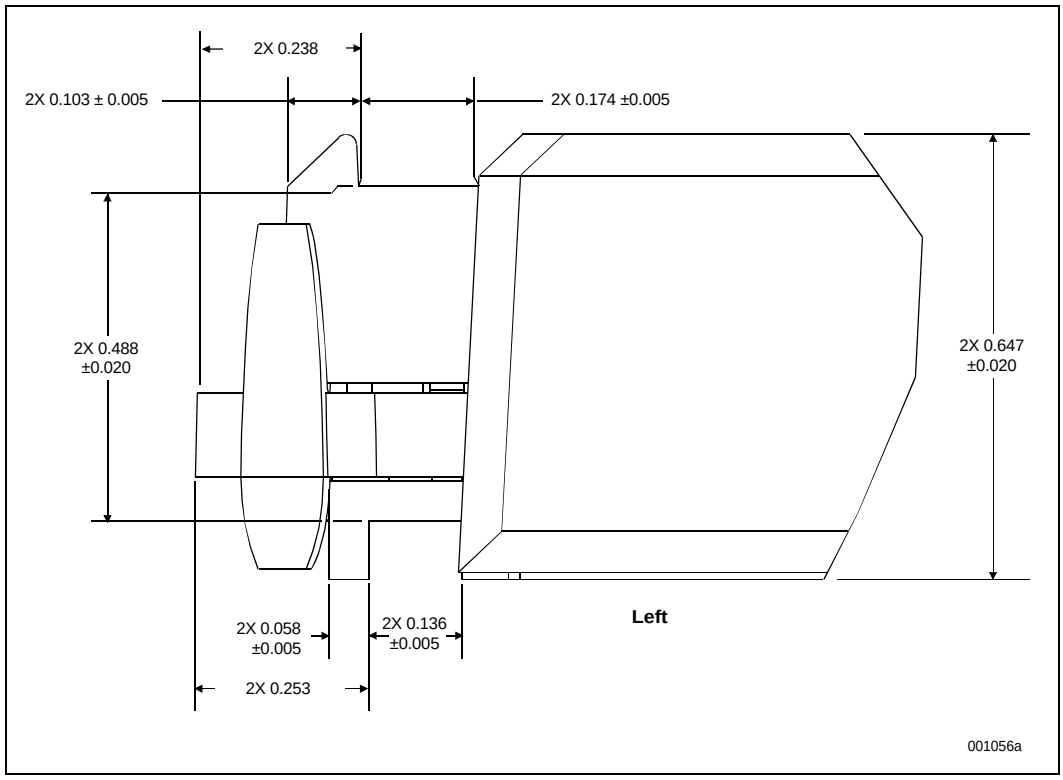


Figure 22. Pentium® II Processor (S.E.C.C. Package)—Latch Arm, Extended Thermal Plate, and Cover Detail Dimensions (Reference Dimensions Only)

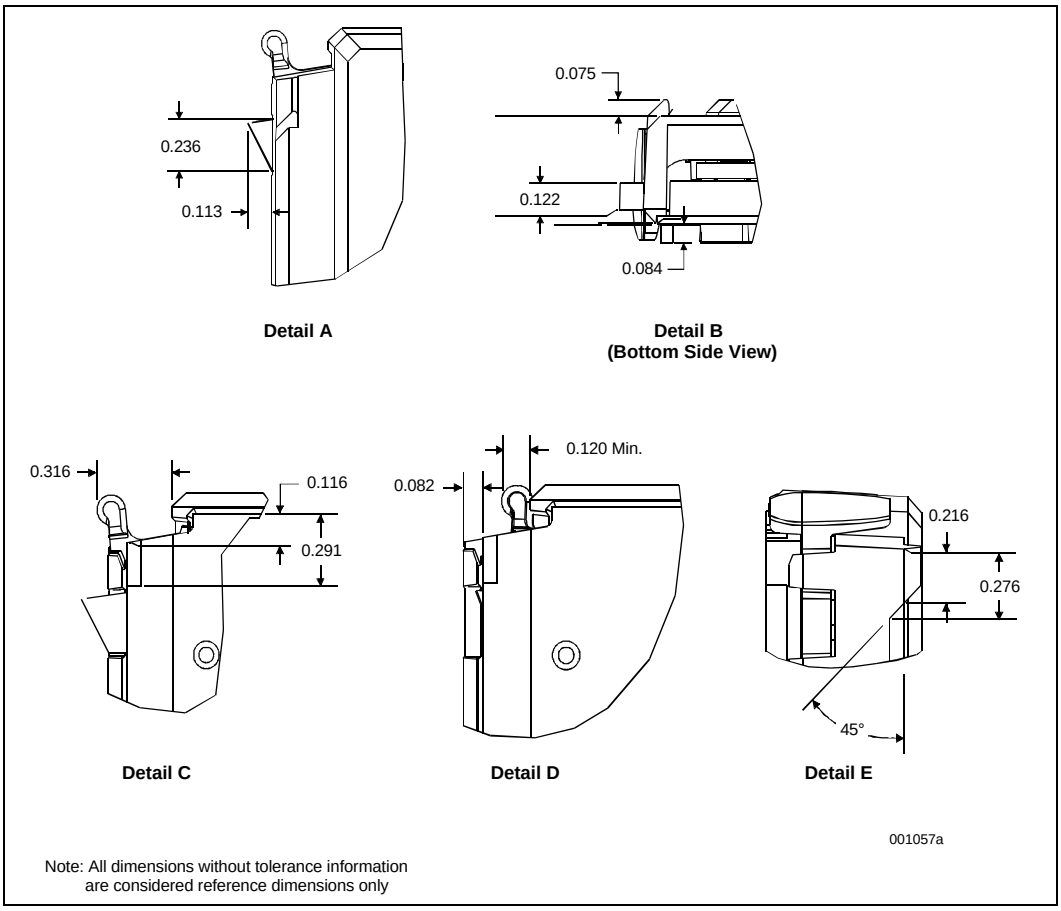


Figure 23. Pentium® II Processor (S.E.C.C. Package)—Extended Thermal Plate Attachment Detail Dimensions

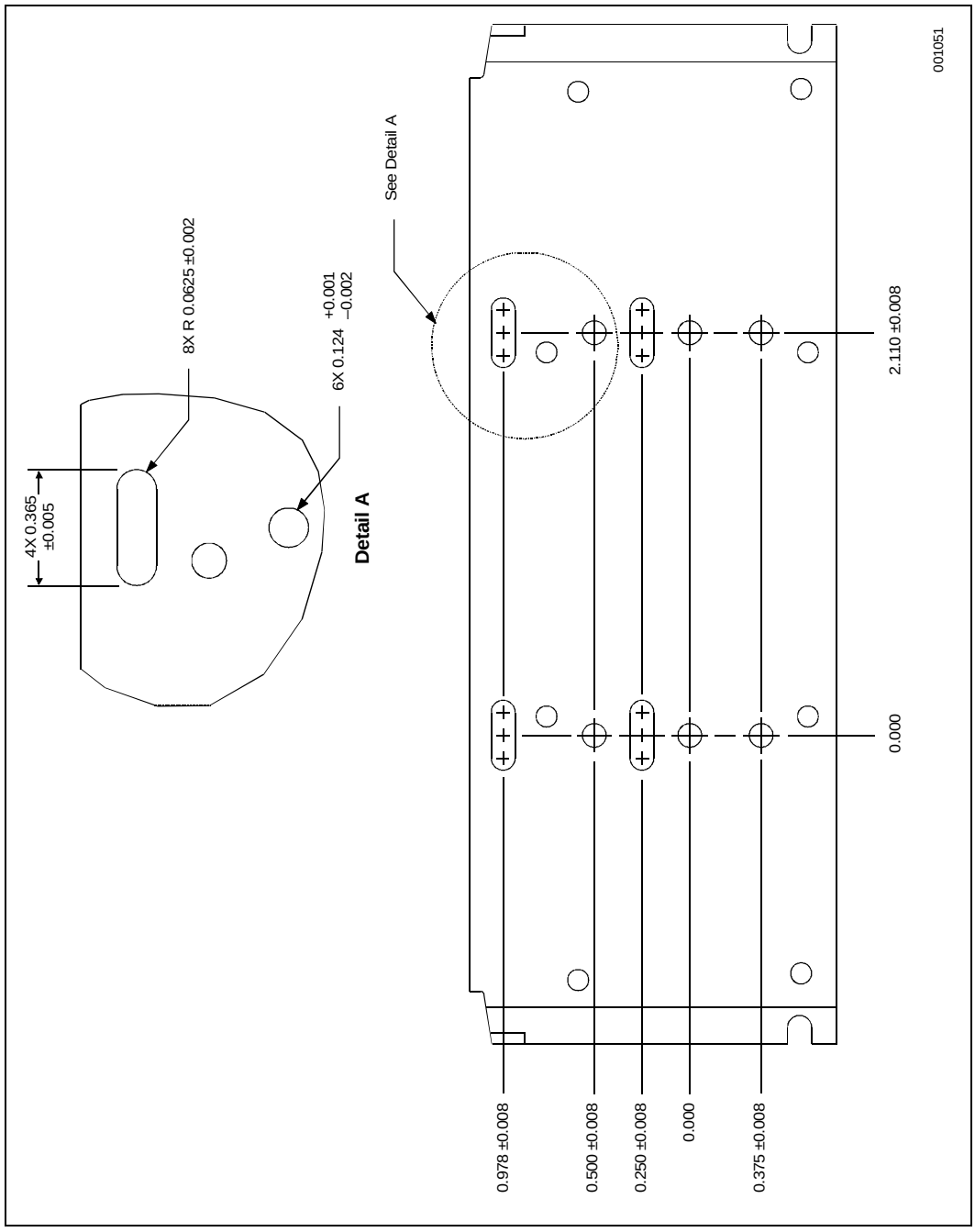


Figure 24. Pentium® II Processor (S.E.C.C. Package)—Extended Thermal Plate Attachment Detail Dimensions, Continued

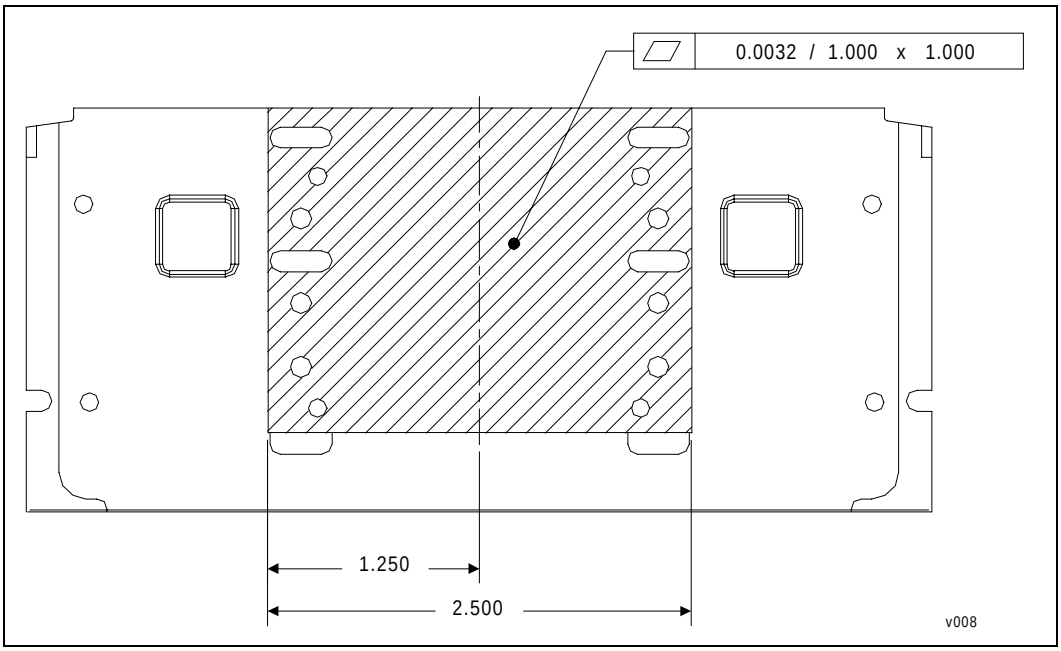


Figure 25. Pentium® II Processor Substrate (S.E.C.C. Package)—Edge Finger Contact Dimensions

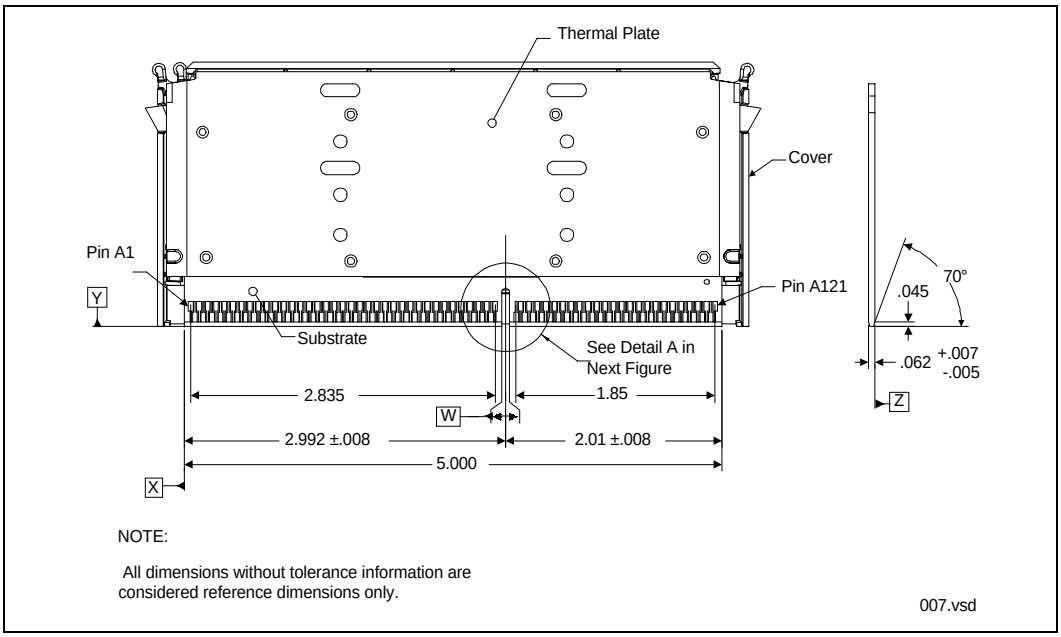


Figure 26. Pentium® II Processor Substrate (S.E.C.C. Package)—Edge Finger Contact Dimensions, Detail A

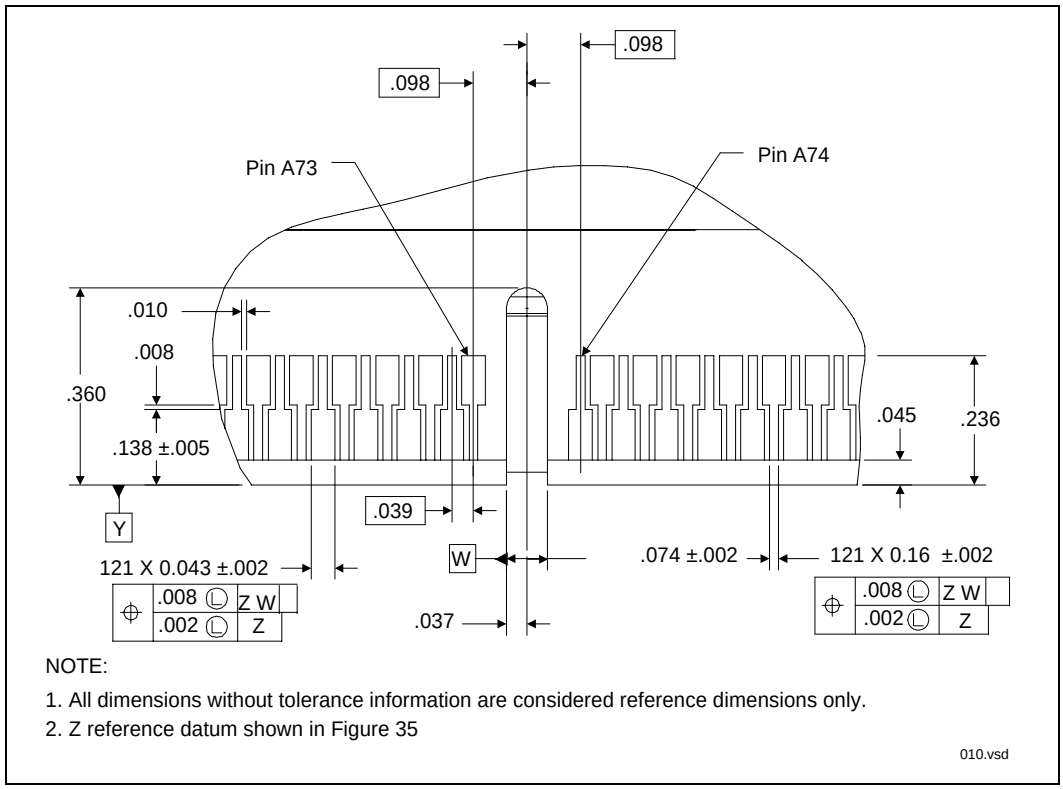


Figure 27. Pentium® II Processor Markings (S.E.C.C. Package)

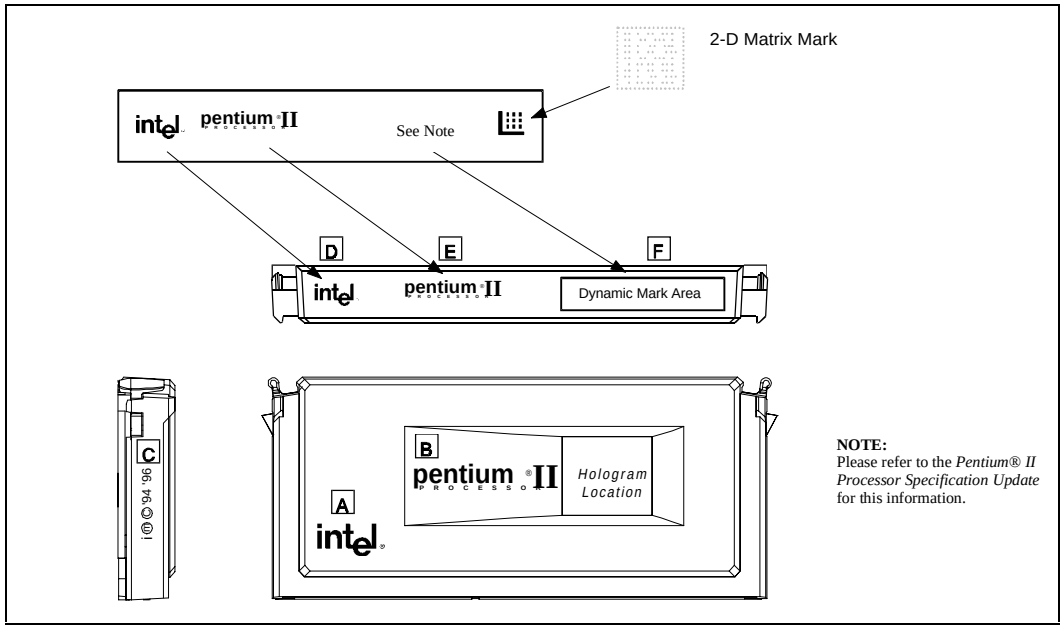


Table 31. Description Table for Processor Markings (S.E.C.C. Packaged Processor)

Code Letter	Description
A	Logo
B	Product Name
C	Trademark
D	Logo
E	Product Name
F	Dynamic Mark Area – with 2-D matrix

5.2 S.E.C.C.2 Mechanical Specification

S.E.C.C.2 packaged drawings and dimension details are provided in Figure 28 through Figure 35. Figure 28 shows all views of the Pentium II processor in an S.E.C.C.2 package using an OLGA packaged processor core; Figure 29 shows all views of a Pentium II processor in an S.E.C.C.2 package using a PLGA packaged processor core; Figure 30 through Figure 34 show the S.E.C.C.2 package dimensions; Figure 35 provides dimensions of the processor substrate edge finger contacts; and Figure 36 and Table 32 contain processor marking information.

Figure 28. Pentium® II Processor (S.E.C.C.2 Package) Top and Side Views—OLGA Processor Core

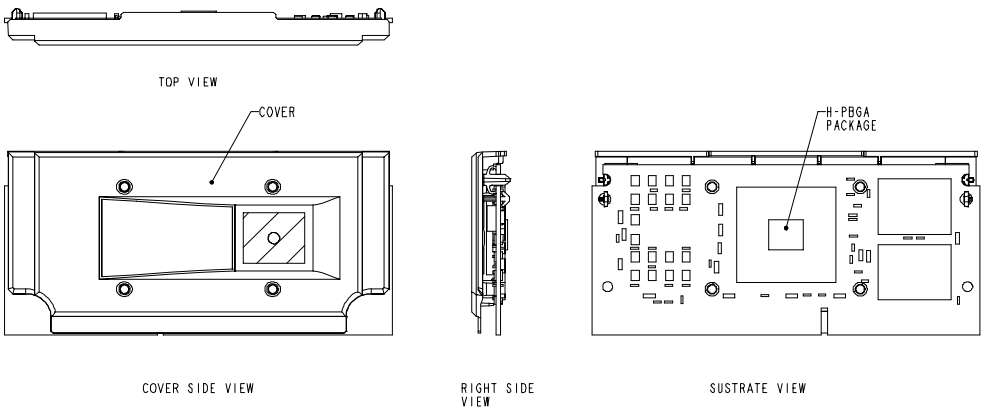


Figure 29. Pentium® II Processor (S.E.C.C.2 Package) Top and Side Views—PLGA Processor Core

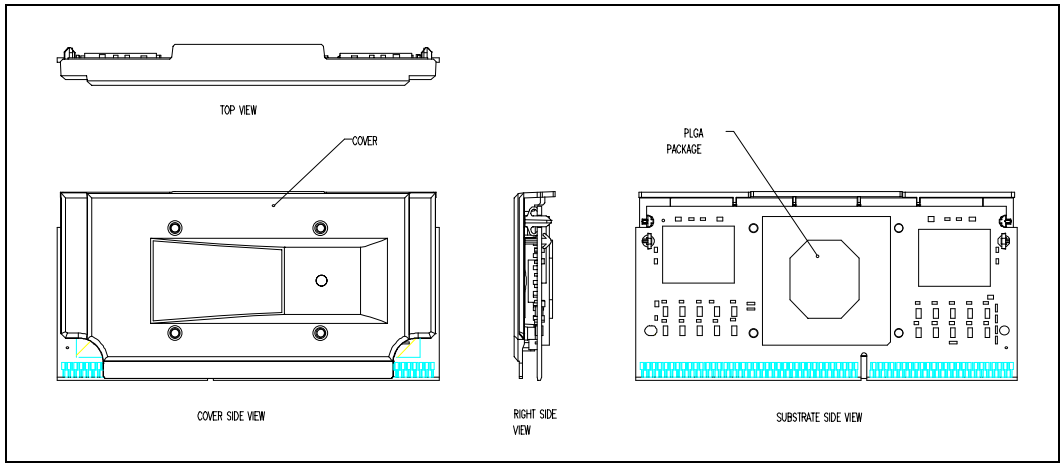


Figure 30. Pentium® II Processor Assembly (S.E.C.C.2 Package)—Primary View

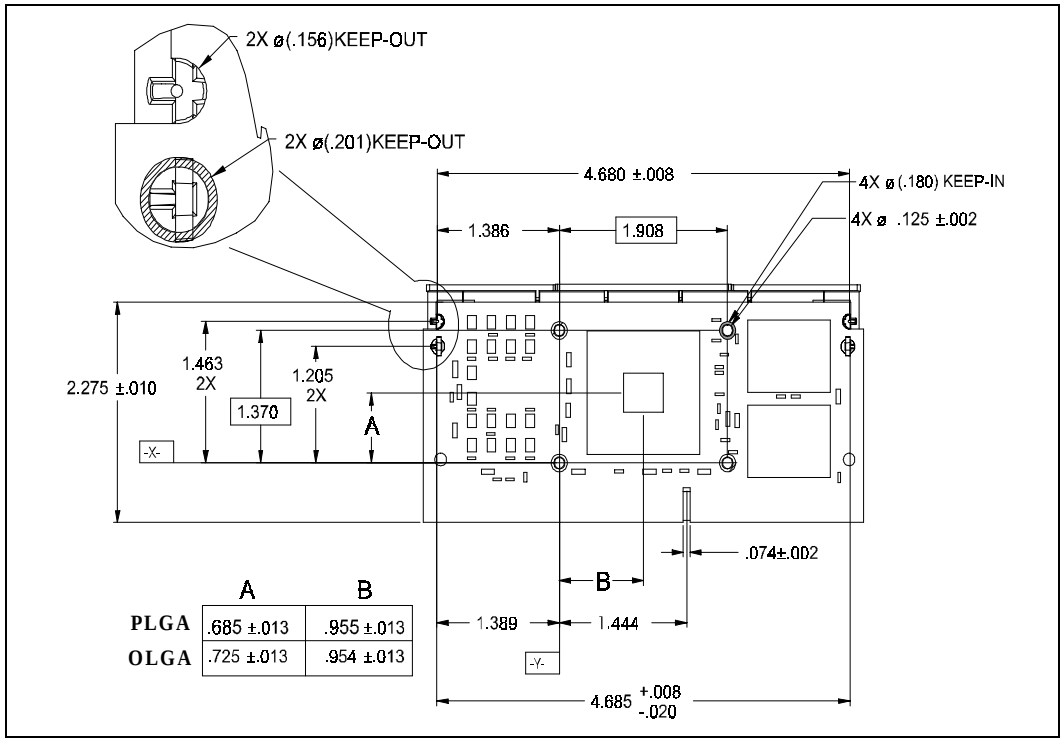


Figure 31. Pentium® II Processor Assembly (S.E.C.C.2 Package)—Cover View with Dimensions

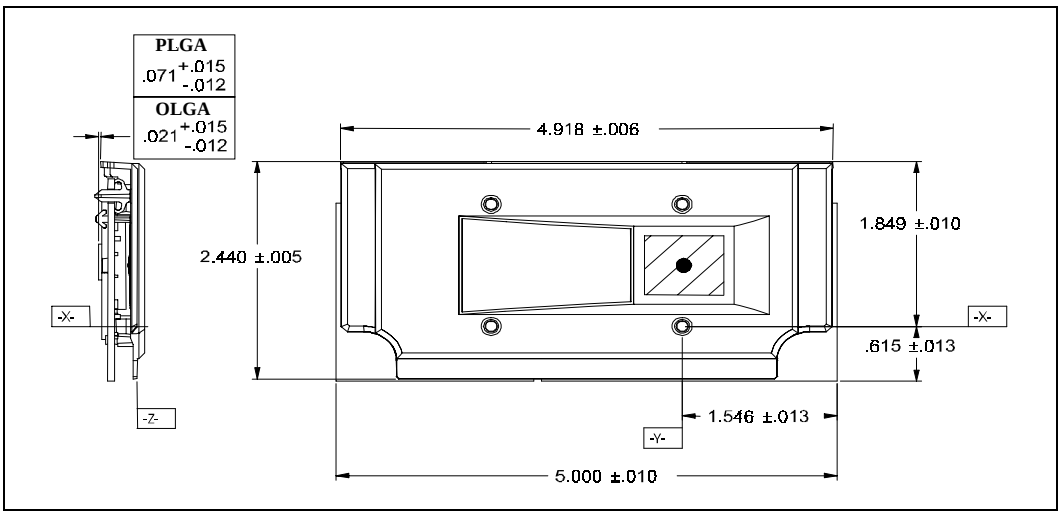


Figure 32. Pentium® II Processor Assembly (S.E.C.C.2 Package)—Heat Sink Attach Boss Section

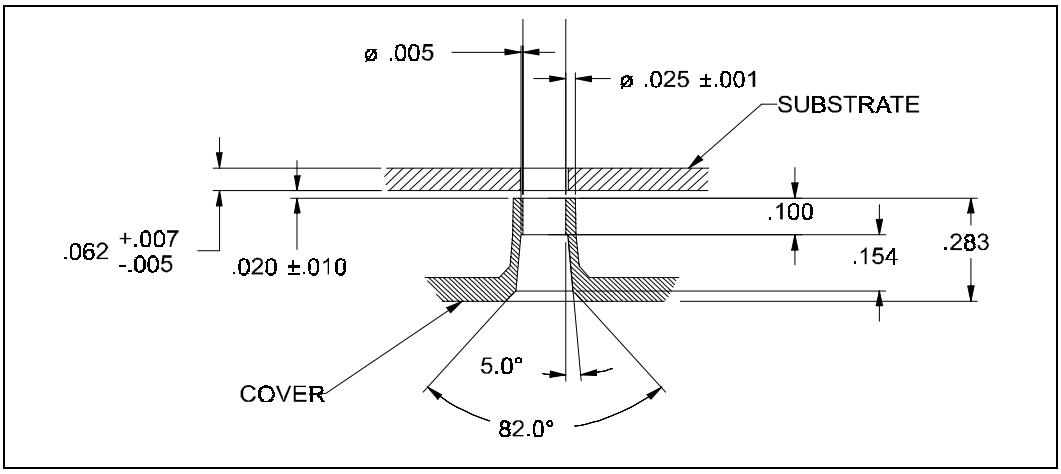


Figure 33. Pentium® II Processor Assembly (S.E.C.C.2 Package), Side View—OLGA Substrate Shown

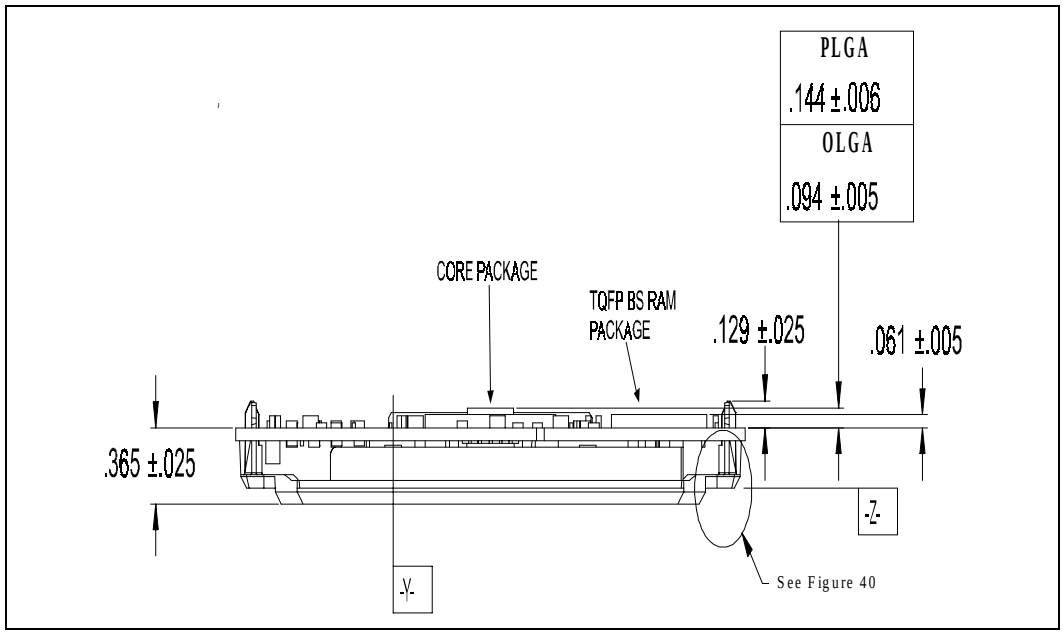


Figure 34. Detail View of Cover in the Vicinity of the Substrate Attach Features

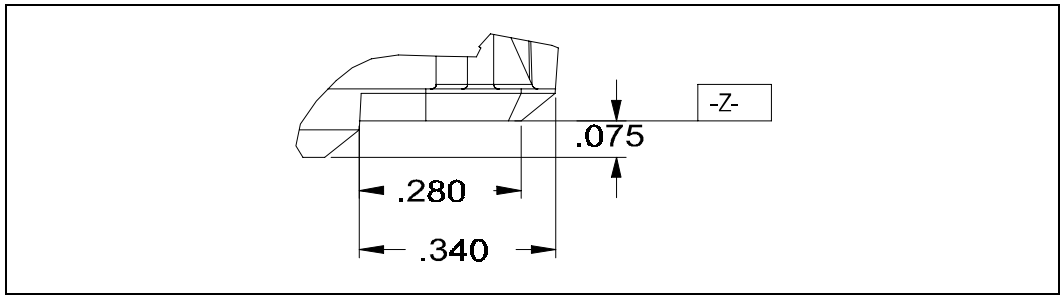


Figure 35. Pentium® II Processor Substrate (S.E.C.C.2 Package), Edge Finger Contact Dimensions

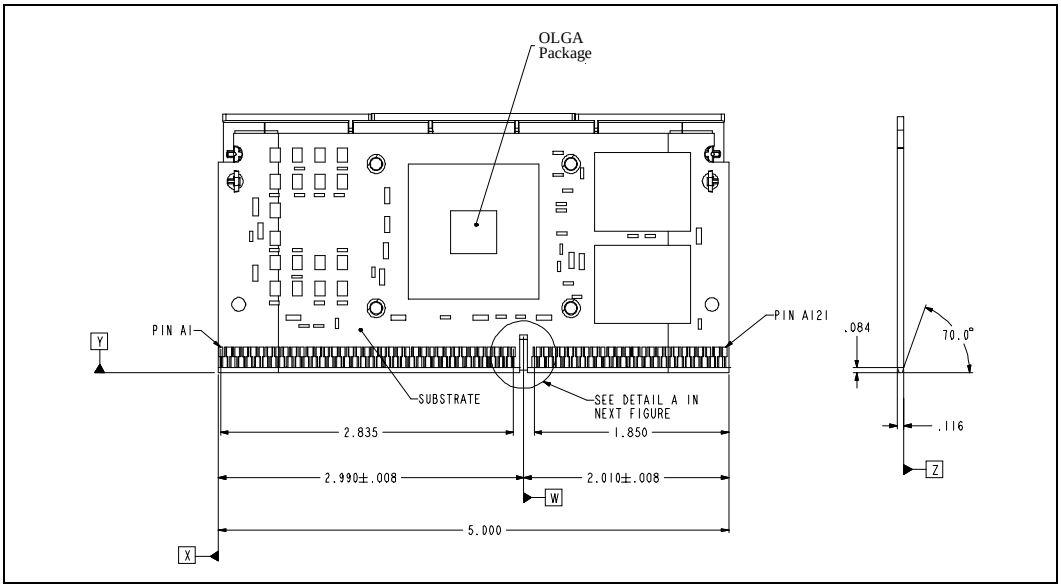
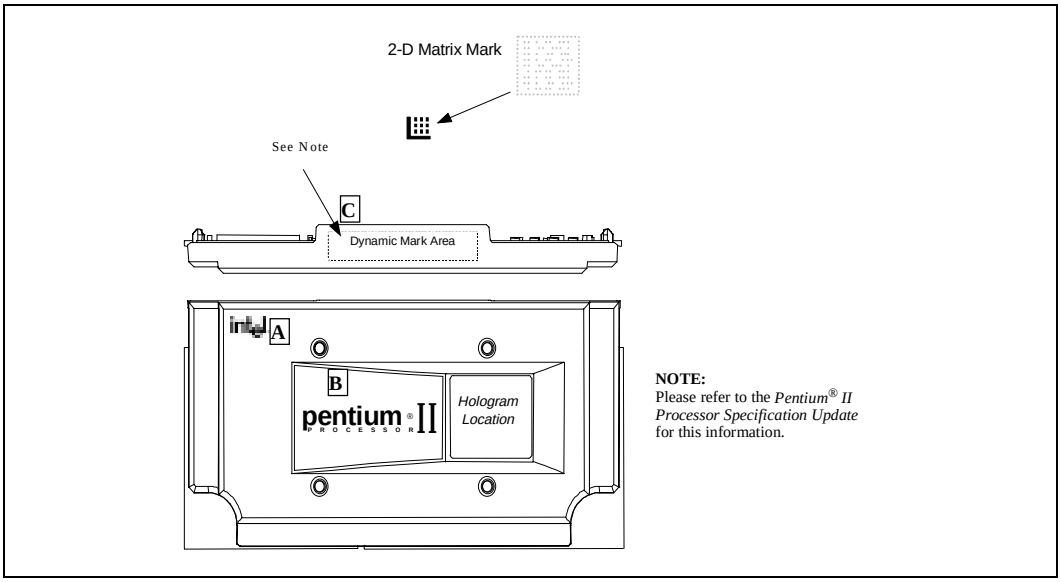


Figure 36. Pentium® II Processor Markings (S.E.C.C.2 Package)



NOTE:
Please refer to the *Pentium® II Processor Specification Update* for this information.

Table 32. Description Table for Processor Markings (S.E.C.C.2 Packaged Processor)

Code Letter	Description
A	Logo
B	Product Name
C	Trademark
D	Logo
E	Product Name
F	Dynamic Mark Area – with 2-D matrix

5.3 Processor Package Materials Information

Both the the S.E.C.C. and S.E.C.C.2 processor cartridges are comprised of multiple pieces to make the complete assembly. This section provides information relevant to the use and acceptance of the package. Table 33 and Section 34 contain piece-part information of the S.E.C.C. and S.E.C.C.2 processor packages, respectively.

Table 33. S.E.C.C. Materials [1]

S.E.C.C. Piece	Piece Material	Maximum Piece Weight (Grams)
Extended Thermal Plate	Aluminum 6063-T6	84.0
Latch Arms	GE Lexan 940-V0, 30% glass filled	Less than 2.0 per latch arm
Cover	GE Lexan 940-V0	24.0
Total Pentium® II Processor		150

NOTE:
1. Unless otherwise noted, these specifications apply to all S.E.C.C. packaged Pentium® II processor frequencies and cache sizes.

Table 34. S.E.C.C.2 Materials [1]

S.E.C.C.2 Piece	Piece Material	Maximum Piece Weight (Grams)
Cover	GE Lexan 940-V0	18.0
Total Pentium® II Processor		57.0

NOTE:
1. Unless otherwise noted, these specifications apply to all S.E.C.C.2 packaged Pentium® II processor frequencies and cache sizes.

5.4 Pentium® II Processor Signal Listing

Table 35 and Table 36 provide the processor edge finger and Pentium II processor connector signal definitions for Pentium II processors. The signal locations on the SC 242 edge connector are to be used for signal routing, simulation, and component placement on the motherboard.

Table 35 is the Pentium II processor substrate edge finger listing in order by pin number.

Table 35. Signal Listing in Order by Pin Number (Sheet 1 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A1	VCC_VTT	AGTL+ VTT Supply	B1	EMI	EMI Management
A2	GND	VSS	B2	FLUSH#	CMOS Input
A3	VCC_VTT	AGTL+ VTT Supply	B3	SMI#	CMOS Input
A4	IERR#	CMOS Output	B4	INIT#	CMOS Input
A5	A20M#	CMOS Input	B5	VCC_VTT	AGTL+ VTT Supply
A6	GND	VSS	B6	STPCLK#	CMOS Input
A7	FERR#	CMOS Output	B7	TCK	JTAG Input
A8	IGNNE#	CMOS Input	B8	SLP#	CMOS Input
A9	TDI	JTAG Input	B9	VCC_VTT	AGTL+ VTT Supply
A10	GND	VSS	B10	TMS	JTAG Input
A11	TDO	JTAG Output	B11	TRST#	JTAG Input
A12	PWRGOOD	CMOS Input	B12	Reserved	Reserved for Future Use
A13	TESTHI	CMOS Test Input	B13	VCC_CORE	Processor core VCC
A14	GND	VSS	B14	THERMDP	Diode Anode
A15	THERMTRIP#	CMOS Output	B15	THERMDN	Diode Cathode
A16	Reserved	Reserved for Future Use	B16	LINT[1]/NMI	CMOS Input
A17	LINT[0]/INTR	CMOS Input	B17	VCC_CORE	Processor core VCC
A18	GND	VSS	B18	PICCLK	APIC Clock Input
A19	PICD[0]	CMOS I/O	B19	BP#[2]	AGTL+ I/O
A20	PREQ#	CMOS Input	B20	Reserved	Reserved for Future Use
A21	BP#[3]	AGTL+ I/O	B21	100/66#	BCLK Frequency Select
A22	GND	VSS	B22	PICD[1]	CMOS I/O
A23	BPM#[0]	AGTL+ I/O	B23	PRDY#	AGTL+ Output
A24	BINIT#	AGTL+ I/O	B24	BPM#[1]	AGTL+ I/O
A25	DEP#[0]	AGTL+ I/O	B25	VCC_CORE	Processor core VCC
A26	GND	VSS	B26	DEP#[2]	AGTL+ I/O
A27	DEP#[1]	AGTL+ I/O	B27	DEP#[4]	AGTL+ I/O
A28	DEP#[3]	AGTL+ I/O	B28	DEP#[7]	AGTL+ I/O
A29	DEP#[5]	AGTL+ I/O	B29	VCC_CORE	Processor core VCC
A30	GND	VSS	B30	D#[62]	AGTL+ I/O
A31	DEP#[6]	AGTL+ I/O	B31	D#[58]	AGTL+ I/O

Table 35. Signal Listing in Order by Pin Number (Sheet 2 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A32	D#[61]	AGTL+ I/O	B32	D#[63]	AGTL+ I/O
A33	D#[55]	AGTL+ I/O	B33	VCC_CORE	Processor core VCC
A34	GND	VSS	B34	D#[56]	AGTL+ I/O
A35	D#[60]	AGTL+ I/O	B35	D#[50]	AGTL+ I/O
A36	D#[53]	AGTL+ I/O	B36	D#[54]	AGTL+ I/O
A37	D#[57]	AGTL+ I/O	B37	VCC_CORE	Processor core VCC
A38	GND	VSS	B38	D#[59]	AGTL+ I/O
A39	D#[46]	AGTL+ I/O	B39	D#[48]	AGTL+ I/O
A40	D#[49]	AGTL+ I/O	B40	D#[52]	AGTL+ I/O
A41	D#[51]	AGTL+ I/O	B41	EMI	EMI Management
A42	GND	VSS	B42	D#[41]	AGTL+ I/O
A43	D#[42]	AGTL+ I/O	B43	D#[47]	AGTL+ I/O
A44	D#[45]	AGTL+ I/O	B44	D#[44]	AGTL+ I/O
A45	D#[39]	AGTL+ I/O	B45	VCC_CORE	Processor core VCC
A46	GND	VSS	B46	D#[36]	AGTL+ I/O
A47	Reserved	Reserved for Future Use	B47	D#[40]	AGTL+ I/O
A48	D#[43]	AGTL+ I/O	B48	D#[34]	AGTL+ I/O
A49	D#[37]	AGTL+ I/O	B49	VCC_CORE	Processor core VCC
A50	GND	VSS	B50	D#[38]	AGTL+ I/O
A51	D#[33]	AGTL+ I/O	B51	D#[32]	AGTL+ I/O
A52	D#[35]	AGTL+ I/O	B52	D#[28]	AGTL+ I/O
A53	D#[31]	AGTL+ I/O	B53	VCC_CORE	Processor core VCC
A54	GND	VSS	B54	D#[29]	AGTL+ I/O
A55	D#[30]	AGTL+ I/O	B55	D#[26]	AGTL+ I/O
A56	D#[27]	AGTL+ I/O	B56	D#[25]	AGTL+ I/O
A57	D#[24]	AGTL+ I/O	B57	VCC_CORE	Processor core VCC
A58	GND	VSS	B58	D#[22]	AGTL+ I/O
A59	D#[23]	AGTL+ I/O	B59	D#[19]	AGTL+ I/O
A60	D#[21]	AGTL+ I/O	B60	D#[18]	AGTL+ I/O
A61	D#[16]	AGTL+ I/O	B61	EMI	EMI Management
A62	GND	VSS	B62	D#[20]	AGTL+ I/O
A63	D#[13]	AGTL+ I/O	B63	D#[17]	AGTL+ I/O
A64	D#[11]	AGTL+ I/O	B64	D#[15]	AGTL+ I/O
A65	D#[10]	AGTL+ I/O	B65	VCC_CORE	Processor core VCC
A66	GND	VSS	B66	D#[12]	AGTL+ I/O
A67	D#[14]	AGTL+ I/O	B67	D#[7]	AGTL+ I/O
A68	D#[9]	AGTL+ I/O	B68	D#[6]	AGTL+ I/O
A69	D#[8]	AGTL+ I/O	B69	VCC_CORE	Processor core VCC

Table 35. Signal Listing in Order by Pin Number (Sheet 3 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A70	GND	VSS	B70	D#[4]	AGTL+ I/O
A71	D#[5]	AGTL+ I/O	B71	D#[2]	AGTL+ I/O
A72	D#[3]	AGTL+ I/O	B72	D#[0]	AGTL+ I/O
A73	D#[1]	AGTL+ I/O	B73	VCC_CORE	Processor core VCC
A74	GND	VSS	B74	RESET#	AGTL+ Input
A75	BCLK	Processor Clock Input	B75	BR1#	AGTL+ Input
A76	BR0#	AGTL+ I/O	B76	Reserved	Reserved for Future Use.
A77	BERR#	AGTL+ I/O	B77	VCC_CORE	Processor core VCC
A78	GND	VSS	B78	A#[35]	AGTL+ I/O
A79	A#[33]	AGTL+ I/O	B79	A#[32]	AGTL+ I/O
A80	A#[34]	AGTL+ I/O	B80	A#[29]	AGTL+ I/O
A81	A#[30]	AGTL+ I/O	B81	EMI	EMI Management
A82	GND	VSS	B82	A#[26]	AGTL+ I/O
A83	A#[31]	AGTL+ I/O	B83	A#[24]	AGTL+ I/O
A84	A#[27]	AGTL+ I/O	B84	A#[28]	AGTL+ I/O
A85	A#[22]	AGTL+ I/O	B85	VCC_CORE	Processor core VCC
A86	GND	VSS	B86	A#[20]	AGTL+ I/O
A87	A#[23]	AGTL+ I/O	B87	A#[21]	AGTL+ I/O
A88	Reserved	Reserved for Future Use	B88	A#[25]	AGTL+ I/O
A89	A#[19]	AGTL+ I/O	B89	VCC_CORE	Processor core VCC
A90	GND	VSS	B90	A#[15]	AGTL+ I/O
A91	A#[18]	AGTL+ I/O	B91	A#[17]	AGTL+ I/O
A92	A#[16]	AGTL+ I/O	B92	A#[11]	AGTL+ I/O
A93	A#[13]	AGTL+ I/O	B93	VCC_CORE	Processor core VCC
A94	GND	VSS	B94	A#[12]	AGTL+ I/O
A95	A#[14]	AGTL+ I/O	B95	A#[8]	AGTL+ I/O
A96	A#[10]	AGTL+ I/O	B96	A#[7]	AGTL+ I/O
A97	A#[5]	AGTL+ I/O	B97	VCC_CORE	Processor core VCC
A98	GND	VSS	B98	A#[3]	AGTL+ I/O
A99	A#[9]	AGTL+ I/O	B99	A#[6]	AGTL+ I/O
A100	A#[4]	AGTL+ I/O	B100	EMI	EMI Management
A101	BNR#	AGTL+ I/O	B101	SLOTOCC#	SC 242 Occupied
A102	GND	VSS	B102	REQ#[0]	AGTL+ I/O
A103	BPRI#	AGTL+ Input	B103	REQ#[1]	AGTL+ I/O
A104	TRDY#	AGTL+ Input	B104	REQ#[4]	AGTL+ I/O
A105	DEFER#	AGTL+ Input	B105	VCC_CORE	Processor core VCC
A106	GND	VSS	B106	LOCK#	AGTL+ I/O
A107	REQ#[2]	AGTL+ I/O	B107	DRDY#	AGTL+ I/O

Table 35. Signal Listing in Order by Pin Number (Sheet 4 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A108	REQ#[3]	AGTL+ I/O	B108	RS#[0]	AGTL+ Input
A109	HITM#	AGTL+ I/O	B109	VCC5	Other VCC
A110	GND	VSS	B110	HIT#	AGTL+ I/O
A111	DBSY#	AGTL+ I/O	B111	RS#[2]	AGTL+ Input
A112	RS#[1]	AGTL+ Input	B112	Reserved	Reserved for Future Use
A113	Reserved	Reserved for Future Use	B113	VCC_L2	Other VCC
A114	GND	VSS	B114	RP#	AGTL+ I/O
A115	ADS#	AGTL+ I/O	B115	RSP#	AGTL+ Input
A116	Reserved	Reserved for Future Use	B116	AP#[1]	AGTL+ I/O
A117	AP#[0]	AGTL+ I/O	B117	VCC_L2	Other VCC
A118	GND	VSS	B118	AERR#	AGTL+ I/O
A119	VID[2]	Voltage Identification	B119	VID[3]	Voltage Identification
A120	VID[1]	Voltage Identification	B120	VID[0]	Voltage Identification
A121	VID[4]	Voltage Identification	B121	VCC_L2	Other VCC

Table 36 is the Pentium II processor substrate edge connector listing in order by signal name.

Table 36. Signal Listing in Order by Signal Name (Sheet 1 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B21	100/66#	BCLK Frequency Select	A29	DEP#[5]	AGTL+ I/O
B98	A#[3]	AGTL+ I/O	A31	DEP#[6]	AGTL+ I/O
A100	A#[4]	AGTL+ I/O	B28	DEP#[7]	AGTL+ I/O
A97	A#[5]	AGTL+ I/O	B107	DRDY#	AGTL+ I/O
B99	A#[6]	AGTL+ I/O	B1	EMI	EMI Management
B96	A#[7]	AGTL+ I/O	B41	EMI	EMI Management
B95	A#[8]	AGTL+ I/O	B61	EMI	EMI Management
A99	A#[9]	AGTL+ I/O	B81	EMI	EMI Management
A96	A#[10]	AGTL+ I/O	B100	EMI	EMI Management
B92	A#[11]	AGTL+ I/O	A7	FERR#	CMOS Output
B94	A#[12]	AGTL+ I/O	B2	FLUSH#	CMOS Input
A93	A#[13]	AGTL+ I/O	B76	Reserved	Reserved for Future Use
A95	A#[14]	AGTL+ I/O	A2	GND	VSS
B90	A#[15]	AGTL+ I/O	A6	GND	VSS
A92	A#[16]	AGTL+ I/O	A10	GND	VSS
B91	A#[17]	AGTL+ I/O	A14	GND	VSS
A91	A#[18]	AGTL+ I/O	A18	GND	VSS
A89	A#[19]	AGTL+ I/O	A22	GND	VSS
B86	A#[20]	AGTL+ I/O	A26	GND	VSS

Table 36. Signal Listing in Order by Signal Name (Sheet 2 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B87	A#[21]	AGTL+ I/O	A30	GND	VSS
A85	A#[22]	AGTL+ I/O	A34	GND	VSS
A87	A#[23]	AGTL+ I/O	A38	GND	VSS
B83	A#[24]	AGTL+ I/O	A42	GND	VSS
B88	A#[25]	AGTL+ I/O	A46	GND	VSS
B82	A#[26]	AGTL+ I/O	A50	GND	VSS
A84	A#[27]	AGTL+ I/O	A54	GND	VSS
B84	A#[28]	AGTL+ I/O	A58	GND	VSS
B80	A#[29]	AGTL+ I/O	A62	GND	VSS
A81	A#[30]	AGTL+ I/O	A66	GND	VSS
A83	A#[31]	AGTL+ I/O	A70	GND	VSS
B79	A#[32]	AGTL+ I/O	A74	GND	VSS
A79	A#[33]	AGTL+ I/O	A78	GND	VSS
A80	A#[34]	AGTL+ I/O	A82	GND	VSS
B78	A#[35]	AGTL+ I/O	A86	GND	VSS
A5	A20M#	CMOS Input	A90	GND	VSS
A115	ADS#	AGTL+ I/O	A94	GND	VSS
B118	AERR#	AGTL+ I/O	A98	GND	VSS
A117	AP#[0]	AGTL+ I/O	A102	GND	VSS
B116	AP#[1]	AGTL+ I/O	A106	GND	VSS
A75	BCLK	Processor Clock Input	A110	GND	VSS
A77	BERR#	AGTL+ I/O	A114	GND	VSS
A24	BINIT#	AGTL+ I/O	A118	GND	VSS
A101	BNR#	AGTL+ I/O	B110	HIT#	AGTL+ I/O
B19	BP#[2]	AGTL+ I/O	A109	HITM#	AGTL+ I/O
A21	BP#[3]	AGTL+ I/O	A4	IERR#	CMOS Output
A23	BPM#[0]	AGTL+ I/O	A8	IGNNE#	CMOS Input
B24	BPM#[1]	AGTL+ I/O	B4	INIT#	CMOS Input
A103	BPRI#	AGTL+ Input	A17	LINT[0]/INTR	CMOS Input
A76	BR0#	AGTL+ I/O	B16	LINT[1]/NMI	CMOS Input
B75	BR1#	AGTL+ Input	B106	LOCK#	AGTL+ I/O
B72	D#[0]	AGTL+ I/O	B18	PICCLK	APIC Clock Input
A73	D#[1]	AGTL+ I/O	A19	PICD[0]	CMOS I/O
B71	D#[2]	AGTL+ I/O	B22	PICD[1]	CMOS I/O
A72	D#[3]	AGTL+ I/O	B23	PRDY#	AGTL+ Output
B70	D#[4]	AGTL+ I/O	A20	PREQ#	CMOS Input
A71	D#[5]	AGTL+ I/O	A12	PWRGOOD	CMOS Input
B68	D#[6]	AGTL+ I/O	B102	REQ#[0]	AGTL+ I/O

Table 36. Signal Listing in Order by Signal Name (Sheet 3 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B67	D#[7]	AGTL+ I/O	B103	REQ#[1]	AGTL+ I/O
A69	D#[8]	AGTL+ I/O	A107	REQ#[2]	AGTL+ I/O
A68	D#[9]	AGTL+ I/O	A108	REQ#[3]	AGTL+ I/O
A65	D#[10]	AGTL+ I/O	B104	REQ#[4]	AGTL+ I/O
A64	D#[11]	AGTL+ I/O	A16	Reserved	Reserved for Future Use
B66	D#[12]	AGTL+ I/O	A47	Reserved	Reserved for Future Use
A63	D#[13]	AGTL+ I/O	A88	Reserved	Reserved for Future Use
A67	D#[14]	AGTL+ I/O	A113	Reserved	Reserved for Future Use
B64	D#[15]	AGTL+ I/O	A116	Reserved	Reserved for Future Use
A61	D#[16]	AGTL+ I/O	B12	Reserved	Reserved for Future Use
B63	D#[17]	AGTL+ I/O	B14	THERMDP	Diode Anode
B60	D#[18]	AGTL+ I/O	B15	THERMDN	Diode Cathode
B59	D#[19]	AGTL+ I/O	B20	Reserved	Reserved for Future Use
B62	D#[20]	AGTL+ I/O	B112	Reserved	Reserved for Future Use
A60	D#[21]	AGTL+ I/O	B74	RESET#	AGTL+ Input
B58	D#[22]	AGTL+ I/O	B114	RP#	AGTL+ I/O
A59	D#[23]	AGTL+ I/O	B108	RS#[0]	AGTL+ Input
A57	D#[24]	AGTL+ I/O	A112	RS#[1]	AGTL+ Input
B56	D#[25]	AGTL+ I/O	B111	RS#[2]	AGTL+ Input
B55	D#[26]	AGTL+ I/O	B115	RSP#	AGTL+ Input
A56	D#[27]	AGTL+ I/O	B101	SLOTOCC#	SC 242 Occupied
B52	D#[28]	AGTL+ I/O	B8	SLP#	CMOS Input
B54	D#[29]	AGTL+ I/O	B3	SMI#	CMOS Input
A55	D#[30]	AGTL+ I/O	B6	STPCLK#	CMOS Input
A53	D#[31]	AGTL+ I/O	B7	TCK	JTAG Input
B51	D#[32]	AGTL+ I/O	A9	TDI	JTAG Input
A51	D#[33]	AGTL+ I/O	A11	TDO	JTAG Output
B48	D#[34]	AGTL+ I/O	A13	TESTHI	CMOS Test Input
A52	D#[35]	AGTL+ I/O	A15	THERMTRIP#	CMOS Output
B46	D#[36]	AGTL+ I/O	B10	TMS	JTAG Input
A49	D#[37]	AGTL+ I/O	A104	TRDY#	AGTL+ Input
B50	D#[38]	AGTL+ I/O	B11	TRST#	JTAG Input
A45	D#[39]	AGTL+ I/O	B13	VCC_CORE	Processor core V_{CC}
B47	D#[40]	AGTL+ I/O	B17	VCC_CORE	Processor core V_{CC}
B42	D#[41]	AGTL+ I/O	B25	VCC_CORE	Processor core V_{CC}
A43	D#[42]	AGTL+ I/O	B29	VCC_CORE	Processor core V_{CC}
A48	D#[43]	AGTL+ I/O	B33	VCC_CORE	Processor core V_{CC}
B44	D#[44]	AGTL+ I/O	B37	VCC_CORE	Processor core V_{CC}

Table 36. Signal Listing in Order by Signal Name (Sheet 4 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A44	D#[45]	AGTL+ I/O	B45	VCC_CORE	Processor core VCC
A39	D#[46]	AGTL+ I/O	B49	VCC_CORE	Processor core VCC
B43	D#[47]	AGTL+ I/O	B53	VCC_CORE	Processor core VCC
B39	D#[48]	AGTL+ I/O	B57	VCC_CORE	Processor core VCC
A40	D#[49]	AGTL+ I/O	B65	VCC_CORE	Processor core VCC
B35	D#[50]	AGTL+ I/O	B69	VCC_CORE	Processor core VCC
A41	D#[51]	AGTL+ I/O	B73	VCC_CORE	Processor core VCC
B40	D#[52]	AGTL+ I/O	B77	VCC_CORE	Processor core VCC
A36	D#[53]	AGTL+ I/O	B85	VCC_CORE	Processor core VCC
B36	D#[54]	AGTL+ I/O	B89	VCC_CORE	Processor core VCC
A33	D#[55]	AGTL+ I/O	B93	VCC_CORE	Processor core VCC
B34	D#[56]	AGTL+ I/O	B97	VCC_CORE	Processor core VCC
A37	D#[57]	AGTL+ I/O	B105	VCC_CORE	Processor core VCC
B31	D#[58]	AGTL+ I/O	B113	VCC_L2	Other VCC
B38	D#[59]	AGTL+ I/O	B117	VCC_L2	Other VCC
A35	D#[60]	AGTL+ I/O	B121	VCC_L2	Other VCC
A32	D#[61]	AGTL+ I/O	A1	VCC_VTT	AGTL+ VTT Supply
B30	D#[62]	AGTL+ I/O	A3	VCC_VTT	AGTL+ VTT Supply
B32	D#[63]	AGTL+ I/O	B5	VCC_VTT	AGTL+ VTT Supply
A111	DBSY#	AGTL+ I/O	B9	VCC_VTT	AGTL+ VTT Supply
A105	DEFER#	AGTL+ Input	B109	VCC5	Other VCC
A25	DEP#[0]	AGTL+ I/O	B120	VID[0]	Voltage Identification
A27	DEP#[1]	AGTL+ I/O	A120	VID[1]	Voltage Identification
B26	DEP#[2]	AGTL+ I/O	A119	VID[2]	Voltage Identification
A28	DEP#[3]	AGTL+ I/O	B119	VID[3]	Voltage Identification
B27	DEP#[4]	AGTL+ I/O	A121	VID[4]	Voltage Identification

6.0 Boxed Processor Specifications

6.1 Introduction

The Pentium II processor is also offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from motherboards and components. Boxed Pentium II processors are supplied with an attached fan heatsink. This section documents motherboard and system requirements for the fan heatsink that will be supplied with the boxed Pentium II processor. This section is particularly important for OEM's that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches. Figure 37 shows a mechanical representation of a boxed Pentium II

processor in the Single Edge Contact Cartridge (S.E.C.C.) package in its retention mechanism with heatsink supports installed. Figure 38 shows a mechanical representation of a boxed Pentium II processor in the S.E.C.C.2 package.

Note: The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. The large arrows in Figure 37 denote the direction of airflow.

Figure 37. Boxed Pentium® II Processor in the S.E.C.C. Packaging Installed in Retention Mechanism (Fan Power Cable Not Shown)

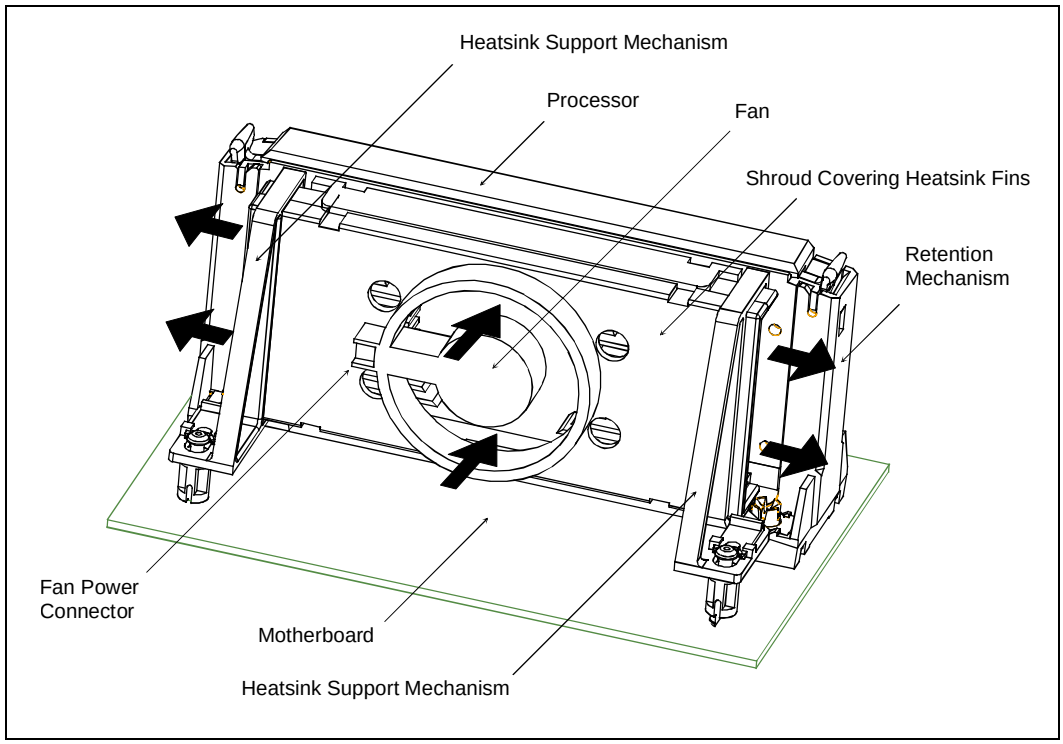
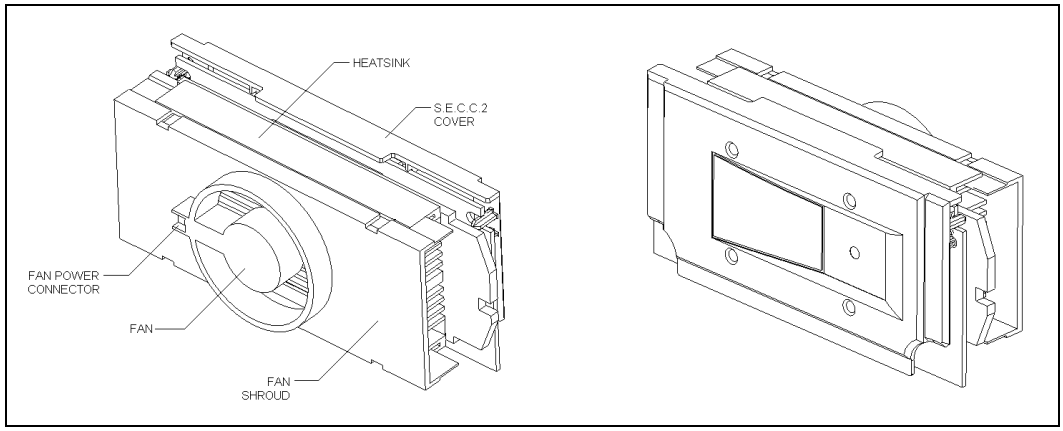


Figure 38. Boxed Pentium® II Processor in the S.E.C.C.2 Packaging (Fan Power Cable Not Shown)



6.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed Pentium II processor fan heatsinks. Motherboard manufacturers and system designers should take into account the spacial requirement for both the boxed Pentium II processor in the S.E.C.C. package and the boxed Pentium II processor in the S.E.C.C.2 package.

6.2.1 Boxed Processor Fan Heatsink Dimensions

The boxed processor is shipped with an attached fan heatsink. Clearance is required around the fan heatsink to ensure unimpeded air flow for proper cooling. The space requirements and dimensions for the boxed processor in the S.E.C.C. package are shown in Figure 39 (Side View), Figure 40 (Front View), and Figure 43 (Top View). Spacial requirements and dimensions for the boxed processor in the S.E.C.C.2 package are shown in Figure 41 (Side View), Figure 42 (Front View), and Figure 43 (Top View). All dimensions are in inches.

Figure 39. Side View Space Requirements for the Boxed Processor with S.E.C.C. Packaging

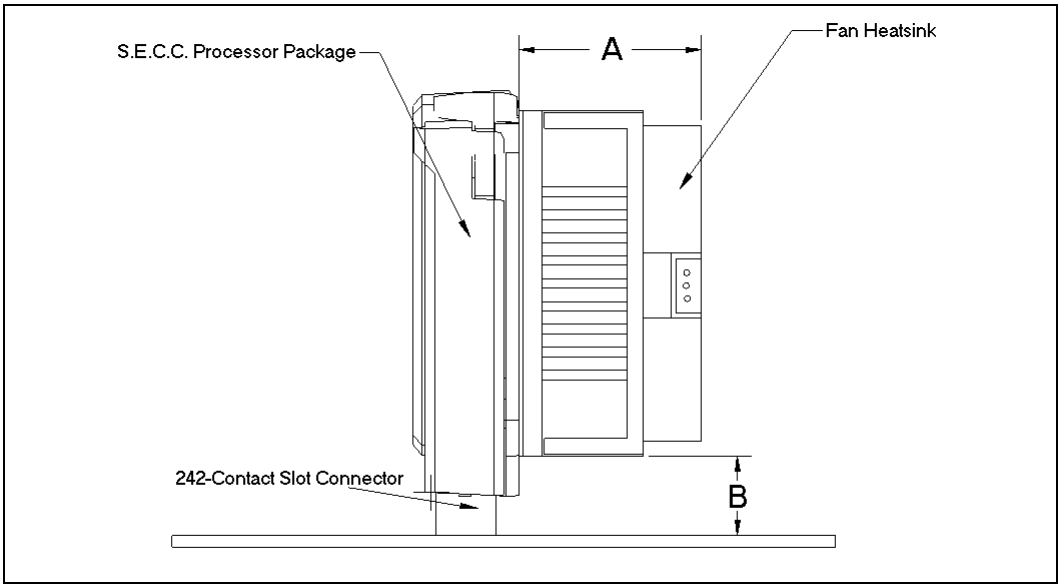


Figure 40. Front View Space Requirements for the Boxed Processor with S.E.C.C. Packaging

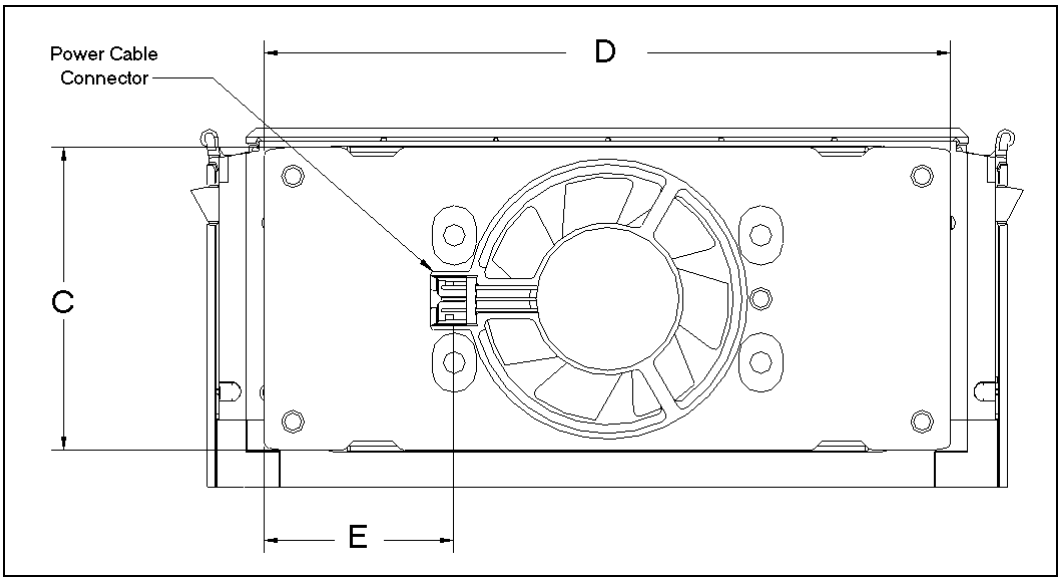


Figure 41. Side View Space Requirements for the Boxed Processor with S.E.C.C.2 Packaging

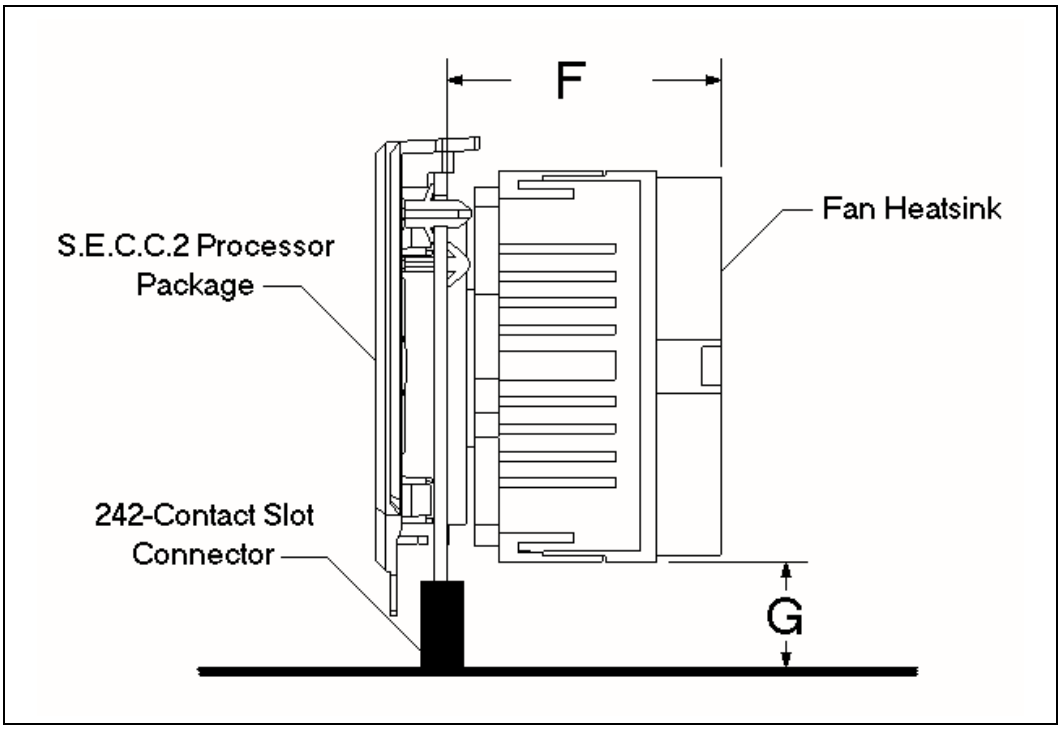


Figure 42. Front View Space Requirements for the Boxed Processor with S.E.C.C.2 Packaging

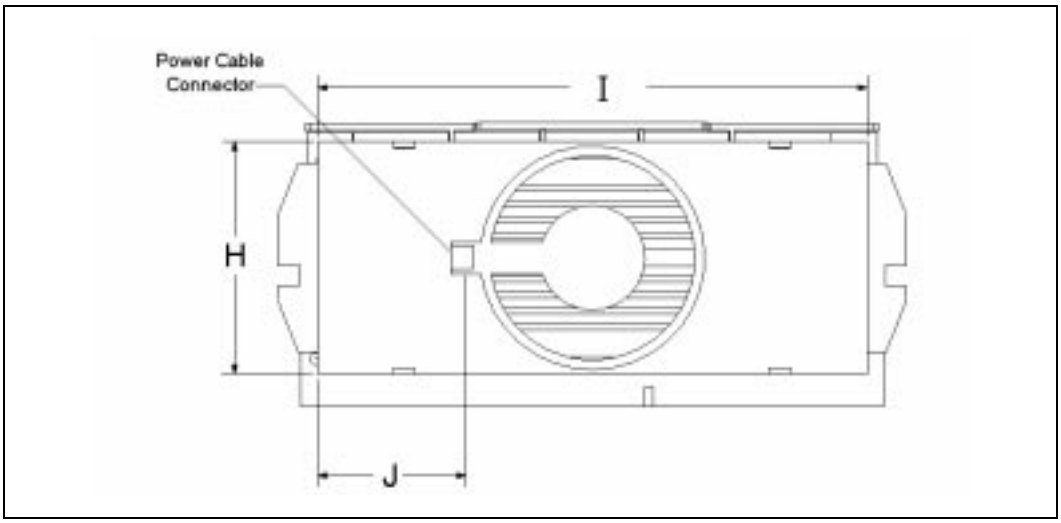


Figure 43. Top View Air Space Requirements for the Boxed Processor

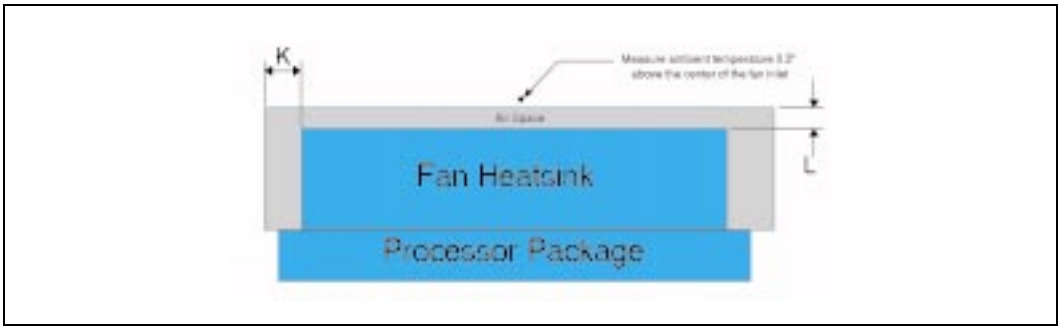


Table 37. Boxed Processor Fan Heatsink Spatial Dimensions

Fig. Ref. Label	Refers to Figure	Dimensions (Inches)	Min	Typ	Max
A	Figure 39	S.E.C.C. Fan Heatsink Depth (off processor extended thermal plate)	-	1.1	1.3
B	Figure 39	S.E.C.C. Fan Heatsink Height Above Motherboard	Note 1	0.5	-
C	Figure 40	S.E.C.C. Fan Heatsink Height	-	2.1	2.2
D	Figure 40	S.E.C.C. Fan Heatsink Width (plastic shroud only)	-	4.8	4.9
E	Figure 40	S.E.C.C. Power Cable Connector Location From Edge of Fan Heatsink Shroud	1.3	-	1.45
F	Figure 41	S.E.C.C.2 Fan Heatsink Depth (off processor substrate)	-	1.3	1.4
G	Figure 41	S.E.C.C.2 Fan Heatsink Height Above Motherboard	0.4	0.6	-
H	Figure 42	S.E.C.C.2 Fan Heatsink Height	-	2.0	2.2
I	Figure 42	S.E.C.C.2 Fan Heatsink Width (plastic shroud only)	-	4.7	4.8
J	Figure 42	S.E.C.C.2 Power Cable Connector Location From Edge of Fan Heatsink Shroud	1.4	-	1.45
K	Figure 43	Airflow keep out zones from end of fan heatsink	0.40	-	-
L	Figure 43	Airflow keepout zones from face of fan heatsink	0.20	-	-

NOTE:
1. See Figure 45, label N.

6.2.2 Boxed Processor Fan Heatsink Weight

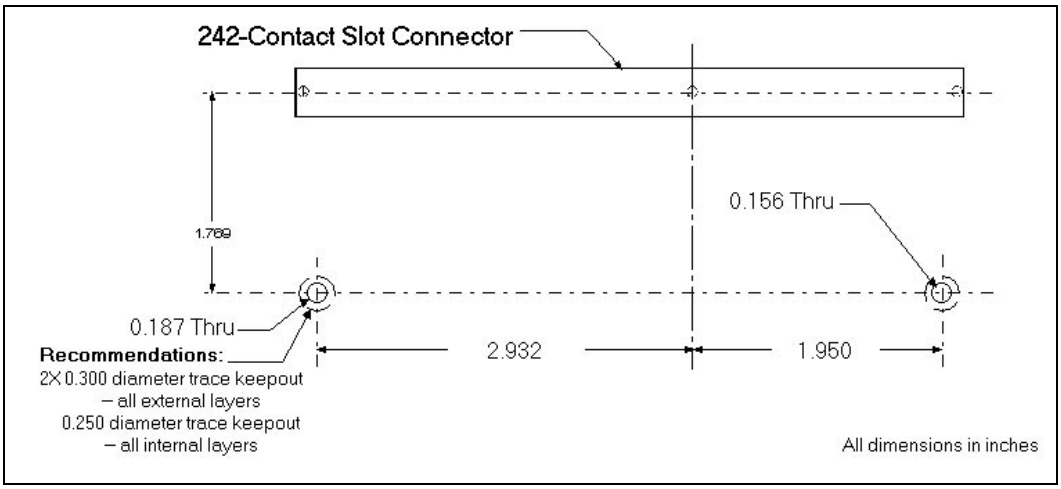
The boxed processor fan heatsink will not weigh more than 225 grams. See Section 4.0 and Section 5.0 for details on the heatsink preformance requirements and processor weight.

6.2.3 Boxed Processor Retention Mechanism and Fan Heatsink Supports

The boxed processor requires processor retention mechanism(s) to secure the processor in the 242-contact slot connector. S.E.C.C. processors must use either the retention mechanism described in AP-588, *Mechanical and Assembly Technology for S.E.C. Cartridge Processors* (Order Number 243333), or retention mechanisms that have been designed to support S.E.C.C., S.E.C.C.2, and Single Edge Processor Package (S.E.P.P.) form factors (also known as universal retention mechanisms). S.E.C.C.2 processors must use either retention mechanisms described in AP-826, *Mechanical Assembly and Customer Manufacturing Technology for S.E.P. Packages* (Order Number 243748). The boxed processor will **not** ship with a retention mechanism. Motherboards designed for use by system integrators **must** include retention mechanisms that support the S.E.C.C. and S.E.C.C.2 form factors and the appropriate installation instructions.

Some boxed Pentium II processors using the S.E.C.C. packaging technology were shipped with fan heatsink supports. These supports differ from supports for passive heatsinks. The boxed processor fan heatsink support requires heatsink support holes in the motherboard. Location and size of these holes are given in Figure 44.

Figure 44. Heatsink Support Hole Locations and Size



Any motherboard components placed in the area beneath the fan heatsink supports must recognize the clearance given in Table 38. Component height restrictions for passive heatsink support designs, as described in AP-588, *Mechanical and Assembly Technology for S.E.C. Cartridge Processors* (Order Number 243333), still apply.

Motherboards designed for use by system integrators should not have objects installed in the heatsink support holes. Otherwise, removal instructions for objects preinstalled in the heatsink support holes should be included in the motherboard documentation.

Table 38. Boxed Processor Fan Heatsink Support Dimensions[1]

Fig. Ref. Label	Refers to Figure	Dimensions (Inches)	Min	Typ	Max
M	Figure 45	Fan Heatsink support height		2.261	
N	Figure 45	Fan Heatsink support clearance above motherboard		0.430	
O	Figure 45	Fan Heatsink support standoff diameter		0.275	0.300
P	Figure 45	Fan Heatsink support front edge to heatsink support hole center		0.240	
Q	Figure 45	Fan Heatsink support standoff protrusion beneath motherboard		0.06	
R	Figure 45	Motherboard thickness	0.05	0.06	0.075
S	Figure 46	Spacing between FHS Supports		4.084	
T	Figure 46	Fan Heatsink support width		0.600	
U	Figure 46	Fan Heatsink support inner edge to heatsink support hole		0.400	

NOTE:
1. All dimensions are in inches. Unless otherwise specified, all dimensions with three significant digits have a tolerance of ±0.005 inches. All dimensions with two significant digits have a tolerance of ±0.01 inches.

Figure 45. Side View Space Requirements for Boxed Processor Fan Heatsink Supports

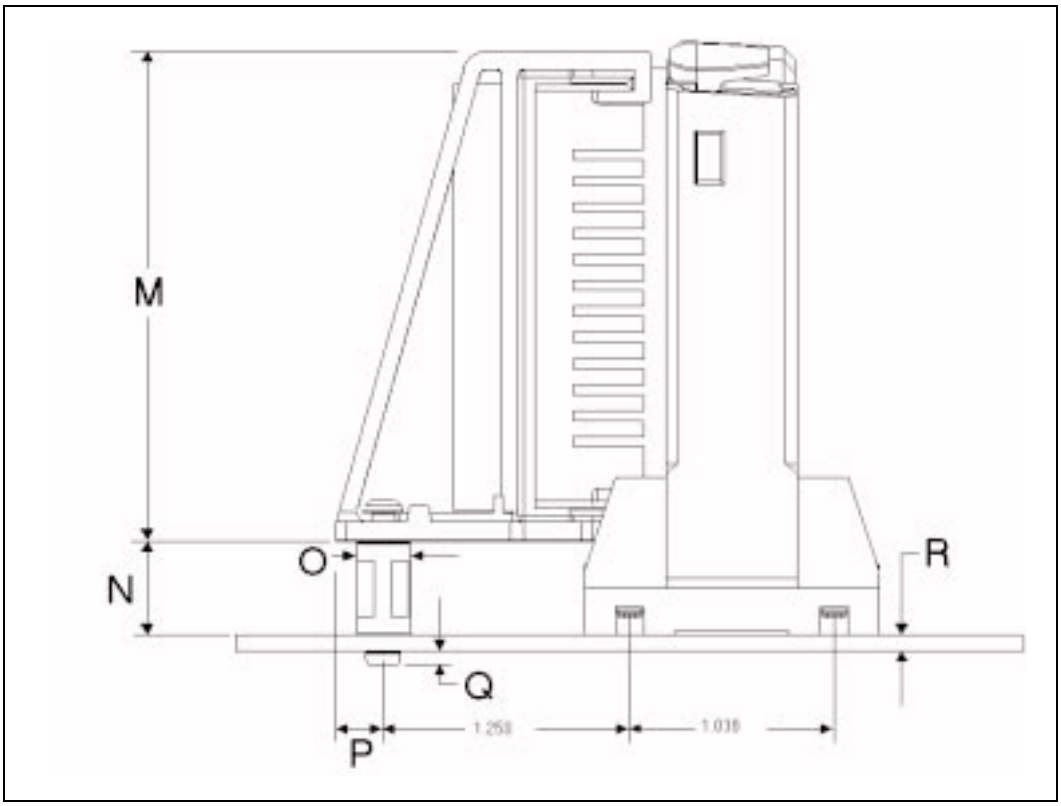
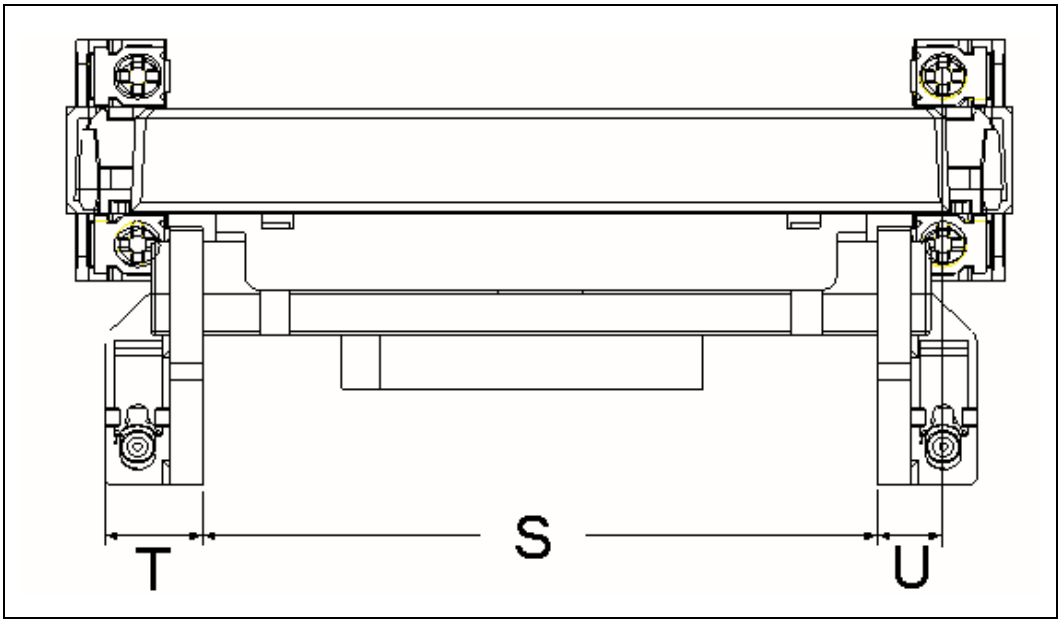


Figure 46. Top View Space Requirements for Boxed Processor Fan Heatsink Supports



6.3 Boxed Processor Requirements

6.3.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 47. Motherboards must provide a matched power header to support the boxed processor. Table 39 contains specifications for the input and output signals at the fan heatsink connector. The cable length will be 7.0 ±0.25 inches. The fan heatsink outputs a SENSE signal, which is an open-collector output, that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides V_{OH} to match the motherboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the motherboard documentation, or on the motherboard itself. Figure 48 shows the location of the fan power connector relative to the 242-contact slot connector. The motherboard power header should be positioned within 4.75 inches (lateral) of the fan power connector.

Figure 47. Boxed Processor Fan Heatsink Power Cable Connector Description

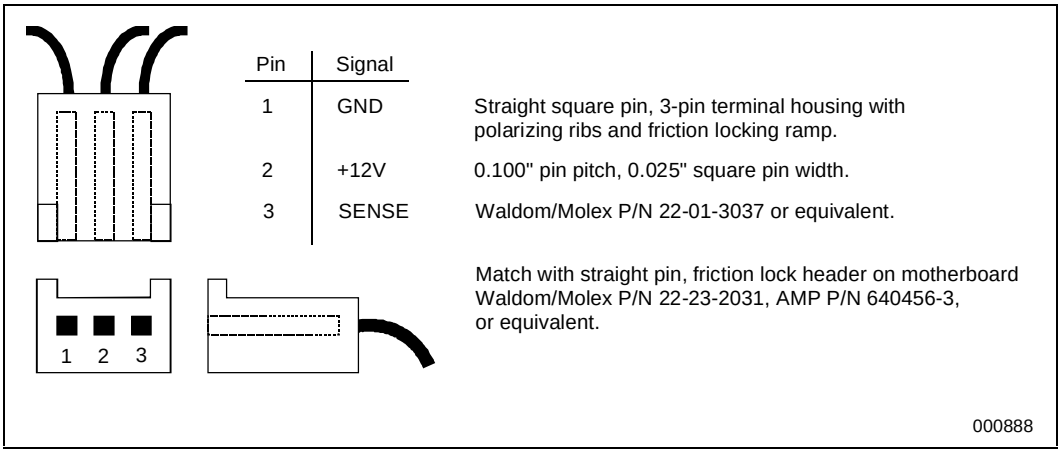


Table 39. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	9 V	12 V	13.8 V
I_C: Fan current draw			100 mA
SENSE: SENSE frequency (motherboard should pull this pin up to appropriate V_{CC} with resistor)		2 pulses per fan revolution	

Figure 48. Recommended Motherboard Power Header Placement Relative to Fan Power Connector and Pentium® II Processor

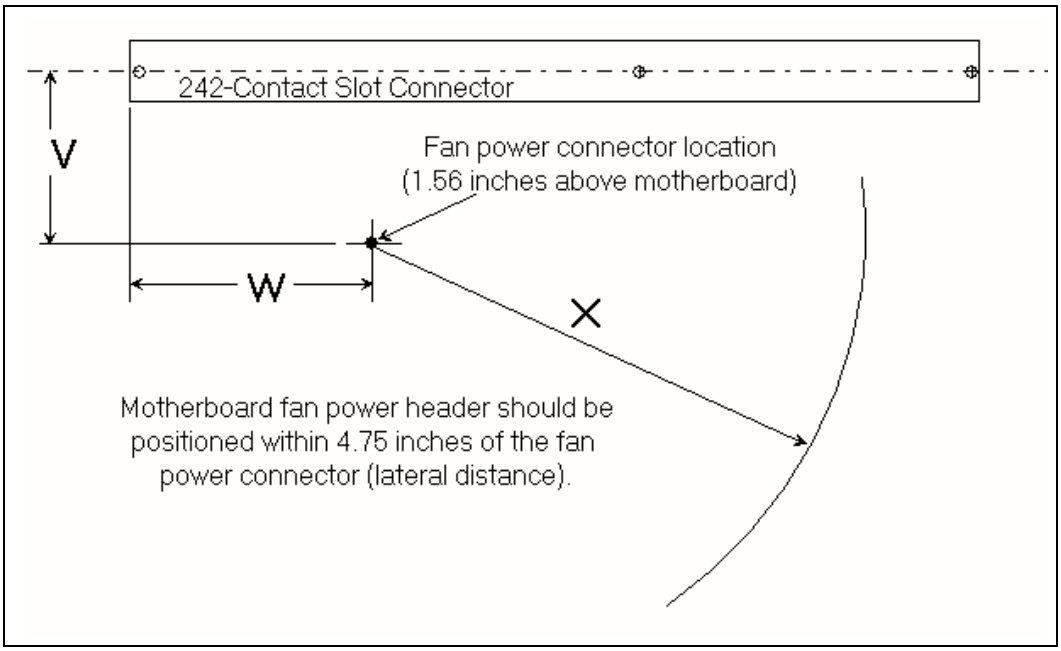


Table 40. Motherboard Fan Power Connector Location

Fig. Ref. Labels	Dimensions (Inches)	Min	Typ	Max
V	Aproximate perpendicular distance of the fan power connector from the center of the 242-contact slot connector		1.44	
W	Aproximate parallel distance of the fan power connector from the edge of the 242-contact slot connector		1.45	
X	Lateral distance of the motherboard fan power header location from the fan power connector			4.75

6.4 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

6.4.1 Boxed Processor Cooling Requirements

The boxed processor will be cooled with a fan heatsink. The boxed processor fan heatsink will keep the processor temperature, within the specifications (see Section 4.0), provided airflow through the fan heatsink is unimpeded and the air temperature entering the fan is below 45 °C (see Figure 43 for measurement location).

Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 43 illustrates an acceptable airspace clearance for the fan heatsink.

7.0 Pentium® II Processor Signal Description

This section provides an alphabetical listing of all Pentium II processor signals. The tables at the end of this section summarize the signals by direction: output, input, and I/O.

7.1 Alphabetical Signals Reference

Table 41. Signal Description (Sheet 1 of 8)

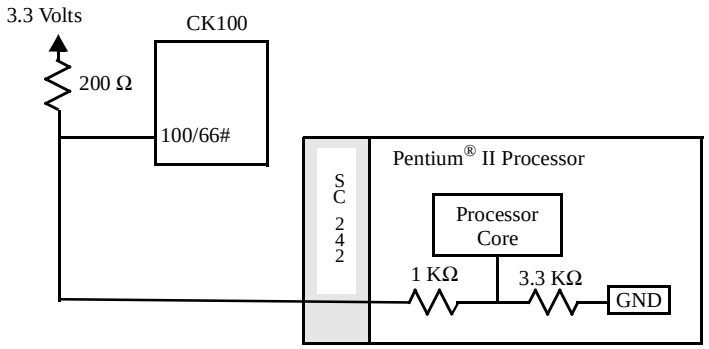
Name	Type	Description
100/66#	I/O	This bidirectional signal is used to select the system bus frequency. A logic low will select a 66 MHz system bus frequency and a logic high (3.3 V) will select a 100 MHz system bus frequency. The frequency is determined by the processor(s), PCIset, and frequency synthesizer. All system bus agents must operate at the same frequency; in a two-way MP Pentium® II procesor configuration, this signal must connect the pins of both Pentium II processors. This signal will be grounded by processors that are only capable of operating at a host frequency of 66 MHz. On motherboards which support operation at either 66- or 100 MHz, this signal must be pulled up to 3.3 V with a 200Ω resistor (as shown in the figure below) and provided as a frequency selection signal to the clock driver/synthesizer. If the system motherboard is not capable of operating at 100 MHz (e.g., Intel® 440FX and 440LX PCIset-based systems), it should ground this signal and generate a 66 MHz system bus frequency. This signal can also be incorporated into RESET# logic on the motherboard if only 100 MHz operation is supported (thus forcing the RESET# signal to remain active as long as the 100/66# signal is low). **100/66# Pin Example** 
A[35:3]#	I/O	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Pentium II processor system bus. The A[35:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[35:3]# pins to determine their power-on configuration. See the *Pentium® II Processor Developer's Manual* (Order Number 243502) for details.

Table 41. Signal Description (Sheet 2 of 8)

Name	Type	Description
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the Pentium II processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. During active RESET#, each processor begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 9. On the active-to-inactive transition of RESET#, each processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all Pentium II processor system bus agents.
AERR#	I/O	The AERR# (Address Parity Error) signal is observed and driven by all Pentium II processor system bus agents, and if used, must connect the appropriate pins on all Pentium II processor system bus agents. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]#, and RP#. AP1# covers A[35:24]#, and AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium II processor system bus agents.
BCLK	I	The BCLK (Bus Clock) signal determines the bus frequency. All Pentium II processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.
BERR#	I/O	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all Pentium II processor system bus agents, and must connect the appropriate pins of all such agents, if used. However, Pentium II processors do not observe assertions of the BERR# signal. BERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted optionally for internal errors along with IERR#. • Asserted optionally by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction.

Table 41. Signal Description (Sheet 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BINIT#</td><td>I/O</td><td>The BINIT# (Bus Initialization) signal may be observed and driven by all Pentium II processor system bus agents, and if used must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.
If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after Reset, and internal count information is lost. The L1 and L2 caches are not affected.
If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.</td></tr>
<tr><td>BNR#</td><td>I/O</td><td>The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all Pentium II processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.</td></tr>
<tr><td>BP[3:2]#</td><td>I/O</td><td>The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.</td></tr>
<tr><td>BPM[1:0]#</td><td>I/O</td><td>The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.</td></tr>
<tr><td>BPRI#</td><td>I</td><td>The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the Pentium II processor system bus. It must connect the appropriate pins of all Pentium II processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</td></tr>
<tr><td>BR0#
BR1#</td><td>I/O
I</td><td>The BR0# and BR1# (Bus Request) pins drive the BREQ[1:0]# signals in the system. The BREQ[1:0]# signals are interconnected in a rotating manner to individual processor pins. The table below gives the rotating interconnect between the processor and bus signals.
BR0# (I/O) and BR1# Signals Rotating Interconnect
<table>
<tr><th>Bus Signal</th><th>Agent 0 Pins</th><th>Agent 1 Pins</th></tr>
<tr><td>BREQ0#</td><td>BR0#</td><td>BR1#</td></tr>
<tr><td>BREQ1#</td><td>BR1#</td><td>BR0#</td></tr>
</table>
During power-up configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[1:0]# pins on active-to-inactive transition of RESET#. Th pin on which the agent samples an active level determines its agent ID. All agents then configure their pins to match the appropriate bus signal protocol, as shown below.
BR[1:0]# Signal Agent IDs
<table>
<tr><th>Pin Sampled Active in RESET#</th><th>Agent ID</th></tr>
<tr><td>BR0#</td><td>0</td></tr>
<tr><td>BR1#</td><td>1</td></tr>
</table></td></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the Pentium II processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</td></tr>
</table>

Table 41. Signal Description (Sheet 4 of 8)

Name	Type	Description
DBSY#	I/O	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the Pentium II processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all Pentium II processor system bus agents.
DEFER#	I	The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all Pentium II processor system bus agents.
DEP[7:0]#	I/O	The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium II processor system bus agents which use them. The DEP[7:0]# signals are enabled or disabled for ECC protection during power on configuration.
DRDY#	I/O	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all Pentium II processor system bus agents.
EMI	I	EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0Ω) resistors. The zero ohm resistors should be placed in close proximity to the Pentium II processor connector. The path to chassis ground should be short in length and have a low impedance. These pins are used for EMI management purposes.
FERR#	O	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When the FLUSH# input signal is asserted, processors write back all data in the Modified state from their internal caches and invalidate all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, each processor samples FLUSH# to determine its power-on configuration. See *P6 Family of Processors Hardware Developer's Manual* (Order Number 244001) for details.
HIT# HITM#	I/O I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all Pentium II processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Pentium II processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.

Table 41. Signal Description (Sheet 5 of 8)

Name	Type	Description
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. During active RESET#, the Pentium II processor begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 9. On the active-to-inactive transition of RESET#, the Pentium II processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1 or L2) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all Pentium II processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration. During active RESET#, the Pentium II processor begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 9. On the active-to-inactive transition of RESET#, the Pentium II processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all Pentium II processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the Pentium II processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the Pentium II processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of all processors and core logic or I/O APIC components on the APIC bus.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.

Table 41. Signal Description (Sheet 6 of 8)

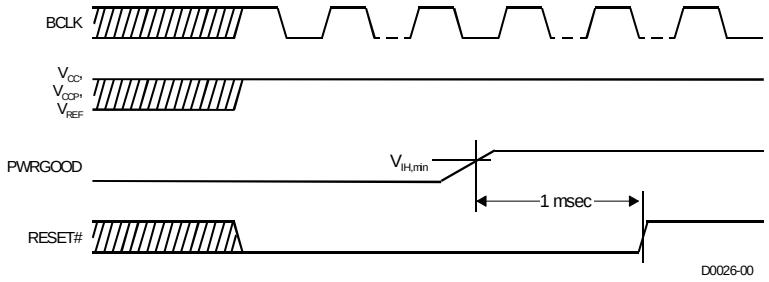
Name	Type	Description
PWRGOOD	I	The PWRGOOD (Power Good) signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies (VCC_{CORE}, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state. The figure below illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 14 and Table 15, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. **PWRGOOD Relationship at Power-On** 
REQ[4:0]#	I/O	The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all Pentium II processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their L1 and L2 caches without writing back any of their contents. RESET# must remain active for one microsecond for a “warm” Reset; for a power-on Reset, RESET# must stay active for at least one millisecond after VCC_{CORE} and CLK have reached their proper specifications. On observing active RESET#, all Pentium II processor system bus agents will deassert their outputs within two clocks. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the *P6 Family of Processors Hardware Developer’s Manual* (Order Number 244001) for details. The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all Pentium II processor system bus agents.
RP#	I/O	The RP# (Request Parity) signal is driven by the request initiator, and provides parity protection on ADS# and REQ[4:0]#. It must connect the appropriate pins of all Pentium II processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all Pentium II processor system bus agents.

Table 41. Signal Description (Sheet 7 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RSP#</td><td>I</td><td>The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect the appropriate pins of all Pentium II processor system bus agents.
A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.</td></tr>
<tr><td>SLOTOCC#</td><td>O</td><td>The SLOTOCC# signal is defined to allow a system design to detect the presence of a terminator card or processor in a SC 242 connector. Combined with the VID combination of VID[4:0]= 11111 (see Section 2.6), a system can determine if a SC 242 connector is occupied, and whether a processor core is present. See the table below for states and values for determining the type of cartridge in the SC 242 connector.
SC 242 Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
Anything other than ‘11111’</td><td>Processor with core in SC 242 connector.</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
11111</td><td>Terminator cartridge in SC 242 connector (i.e., no core present).</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>1
Any value</td><td>SC 242 connector not occupied.</td></tr>
</table></td></tr>
<tr><td>SLP#</td><td>I</td><td>The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.</td></tr>
<tr><td>SMI#</td><td>I</td><td>The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.</td></tr>
<tr><td>STPCLK#</td><td>I</td><td>The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.</td></tr>
<tr><td>TCK</td><td>I</td><td>The TCK (Test Clock) signal provides the clock input for the Pentium II processor Test Bus (also known as the Test Access Port).</td></tr>
<tr><td>TDI</td><td>I</td><td>The TDI (Test Data In) signal transfers serial test data into the Pentium II processor. TDI provides the serial input needed for JTAG specification support.</td></tr>
<tr><td>TDO</td><td>O</td><td>The TDO (Test Data Out) signal transfers serial test data out of the Pentium II processor. TDO provides the serial output needed for JTAG specification support.</td></tr>
<tr><td>TESTHI</td><td>I</td><td>The TESTHI signal must be connected to a 2.5 V power source through a 1-100 kΩ resistor for proper processor operation.</td></tr>
<tr><td>THERMDN</td><td>O</td><td>Thermal Diode Cathode. Used to calculate core temperature. See Section 4.1.</td></tr>
<tr><td>THERMDP</td><td>I</td><td>Thermal Diode Anode. Used to calculate core temperature. See Section 4.1.</td></tr>
</table>

Table 41. Signal Description (Sheet 8 of 8)

Name	Type	Description
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP# and remain stopped.
TMS	I	The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all Pentium II processor system bus agents.
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 ohm pull-down resistor.
VID[4:0]	O	The VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on Pentium II processors. See Table 1 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.

7.2 Signal Summaries

Table 42 through Table 45 list attributes of the Pentium II processor output, input, and I/O signals.

Table 42. Output Signals

Name	Active Level	Clock	Signal Group
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	AGTL+ Output
SLOTOCC#	Low	Asynch	Power/Other
TDO	High	TCK	JTAG Output
THERMTRIP#	Low	Asynch	CMOS Output
VID[4:0]	High	Asynch	Power/Other

Table 43. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always[1]
BPRI#	Low	BCLK	AGTL+ Input	Always
BR1#	Low	BCLK	AGTL+ Input	Always
BCLK	High	—	Clock	Always
DEFER#	Low	BCLK	AGTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always[1]
IGNNE#	Low	Asynch	CMOS Input	Always[1]
INIT#	Low	Asynch	CMOS Input	Always[1]
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGOOD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	AGTL+ Input	Always
RS[2:0]#	Low	BCLK	AGTL+ Input	Always
RSP#	Low	BCLK	AGTL+ Input	Always
SLP#	Low	Asynch	CMOS Input	During Stop-Grant state
SMI#	Low	Asynch	CMOS Input	
STPCLK#	Low	Asynch	CMOS Input	
TCK	High	—	JTAG Input	
TDI	High	TCK	JTAG Input	
TESTHI	High	Asynch	Power/Other	Always
TMS	High	TCK	JTAG Input	
TRST#	Low	Asynch	JTAG Input	
TRDY#	Low	BCLK	AGTL+ Input	

NOTE:
1. Synchronous assertion with active TDRY# ensures synchronization.

Table 44. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
100/66#	Low	Asynch	Power/Other	Always
A[35:3]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	AGTL+ I/O	Always
AP[1:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
BR0#	Low	BCLK	AGTL+ I/O	Always
BP[3:2]#	Low	BCLK	AGTL+ I/O	Always
BPM[1:0]#	Low	BCLK	AGTL+ I/O	Always
D[63:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DBSY#	Low	BCLK	AGTL+ I/O	Always
DEP[7:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DRDY#	Low	BCLK	AGTL+ I/O	Always
LOCK#	Low	BCLK	AGTL+ I/O	Always
REQ[4:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
RP#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1

Table 45. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	AGTL+ I/O	ADS#+3
BERR#	Low	BCLK	AGTL+ I/O	Always
BNR#	Low	BCLK	AGTL+ I/O	Always
BINIT#	Low	BCLK	AGTL+ I/O	Always
HIT#	Low	BCLK	AGTL+ I/O	Always
HITM#	Low	BCLK	AGTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always