AP-906
APPLICATION
NOTE

100 MHz AGTL+ Layout Guidelines for the Pentium® III Processor and Intel® 440BX AGPset

FEBRUARY 1999

Order Number: 245086-001

CG-041493

CONTENTS

List of Figures

1.0. INTRODUCTION

The Pentium® III processor is the latest processor in the family of Intel Architecture microprocessors. This processor extends the power of the Pentium II processor and adds the capability of the Streaming SIMD instructions to enhance multimedia technology. The Pentium III Processor maintains binary compatibility with the Pentium II processors. The design of the Pentium II processor, at the system bus speed of 100MHz, enables the Pentium III Processor to be plugged into the existing hardware platforms and bring "multiprocessor ready" capability to such platforms. The Pentium III Processor implements a synchronous, latched bus protocol that allows a full clock cycle for signal transmission and a full clock cycle for signal interpretation and generation. The Pentium III Processor bus, like the Pentium II processor with 100MHz system bus, uses low-voltage-swing AGTL+ I/O buffers, making high frequency signal communication between multiple loads easier.

The goal of this layout guideline is to provide a system designer with the necessary information for designing the printed circuit board layout of a 100 MHz AGTL+ system bus using the Intel® Pentium III Processor and the Intel 440BX AGPset. This document provides methodologies and guidelines that are to be used with good engineering practices in designing your system. It does not provide hard and fast rules. See the Pentium III Processor datasheet, as well as the applicable chipset specification for component specific electrical details. Intel strongly recommends running analog simulations using the available I/O buffer models together with layout information extracted from your specific design, especially if the design deviates from the layout recommendations of section 4. In addition, for designs that are based on the layout recommendations, simulation will confirm adherence to the guidelines.

2.0. ABOUT THIS DOCUMENT

2.1. How to Use This Document

This document is aimed at system designers. It assumes that the reader is familiar with transmission line and synchronous timing concepts. No attempt is made to teach either subject.
This layout guideline is intended to

- describe the operation of AGTL+ and identify the areas of sensitivity to focus on when designing a 100 MHz system bus.
- describe the AGTL+ timing and signal quality metrics.
- provide the necessary information to develop system timing targets.
- describe a comprehensive design methodology that shrinks the design cycle time and delivers high confidence in the resulting solution.
- provide trace length recommendations for single and dual processor designs.

The layout guidelines outlined in this document are intended for all Pentium® III Processors that run at 100MHz system bus.

2.2. Document Organization

This section describes the intent of the document, and outlines the contents.

Section 3 provides a description of AGTL+ technology. Timing and signal quality metrics are also described in Section 3. The operation of AGTL+ is presented, along with a discussion of the key design variables that affect AGTL+ performance.

Section 4 provides layout guidelines for the 100 MHz AGTL+ host bus. It includes a summary of results from extensive interconnect analysis performed at Intel during the development of the 100 MHz timing specifications and layout guidelines.

Section 5 provides layout guidelines for the host bus clock signals, including a summary of simulation results.

Section 6 provides a step-by-step design methodology that Intel has successfully used to design Pentium® II processor systems using the 440BX AGPset components for validation and feasibility. Section 7 contains a description of the timing analysis that was used to determine the recommended 100 MHz system timings.

2.3. References

- Pentium® II Processor at 333MHz, 300MHz, 266MHz and 233MHz (Order Number 2433353)
- Pentium® II Processor at 350MHz, 400MMHz and 450MHz (Order Number 243657)
- Pentium® III Processor at 450MHz and 500MHz (Order Number 244452)
- Pentium® III Processor I/O Buffer Models (Electronic Form at http://developer.intel.com/design)
- CK97 Clock Synthesizer/Driver Specification (Order Number OR-0963)
- AP-907, Pentium® III Processor Power Distribution Guidelines (Order Number 245085)
- Slot 1 Bus Termination Card Design Guidelines (Order Number 243409)

3.0. AGTL+ DESCRIPTION

AGTL+ is the electrical bus technology used for Pentium® III Processors at 100 MHz system bus. AGTL+, or Assisted Gunning Transistor Logic, is a low output swing, incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at the end of the bus. The AGTL+ drivers have an additional PMOS pull-up transistor to assist the pull-up resistors during the first clock of a low to high voltage transition.

The specification defines:

- Termination voltage, V_{TT}
- Termination resistance, R_{TT}
- Maximum output low voltage, V_{OL}, and output low current, I_{OL}
- Output driver edge rate when driving the AGTL+ reference load
- Receiver high and low voltage level, V_{IL} and V_{IH}
- Receiver reference voltage, V_{REF}, as a function of the termination voltage
- Receiver ringback tolerance

The following material provides an overview of AGTL+ operation, and discusses the primary factors that affect signal quality and timings in a AGTL+ bus.

3.1. AGTL+ Operation

3.1.1. OVERVIEW

As stated above, AGTL+ uses open drain output buffers with external pull-up resistors, as shown in Figure 1. The pull-up resistors provide two functions. First, they provide a current path for the rising edge when the open drain device turns off. The high logic level for AGTL+ is equal to the termination voltage, V_{TT}. Second, the resistors provide termination for the interconnect transmission lines. At high switching frequencies it is critical that the network be properly terminated to minimize reflections that could otherwise impact the performance of the system. Typically, the termination resistor value is chosen to match the effective impedance of the network. For the Pentium® III Processor, in a Dual Processor configuration, and Intel® 440BX AGPset, the recommended value for R_{TT} is 56Ω (+/- 5%). The Pentium III Processor contains one of the termination resistors on the processor substrate.

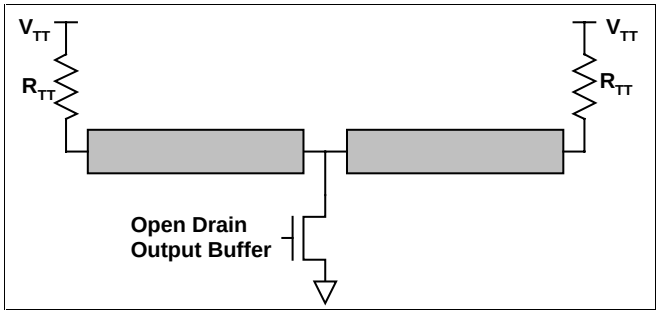


Figure 1. AGTL+ open drain buffer with external pull-up to V_{TT}.

To achieve high speed operation, AGTL+ is defined as an incident wave switching interface. The initial signal wave is driven with sufficient amplitude to switch the receivers. Incident wave switching requires that the open drain output buffers have low output impedance, maximum 16.67Ω.

3.1.2. AGTL+ SENSITIVITIES

Pull-up resistance

As noted above, the pull-up resistors provide a path for current flow when the signal on the network is less than the termination voltage. As a result, the value of R_{TT} affects the rise and fall times of the signals. The impact of this effect is that the system flight time is dependent on the pull-up resistance, as illustrated by Figure 2. Higher values for R_{TT} result in slower rising edges and faster falling edges. Lower values for R_{TT} cause faster rising edges and slower falling edges.

The processor substrate contains a 56Ω resistor at the end of the network. Intel recommends that an additional 56Ω resistor be placed on the system board at the other end of the network for a single processor design. This value represents the optimum balance between rising and falling edges.
In addition to flight times, the pull-up value affects the ringback characteristics of a AGTL+ network (see section 3.2 for a description of ringback). Lower values for R_{TT} generally result in decreased ringback on the rising edge. Ringback is not typically a problem on the falling edge.

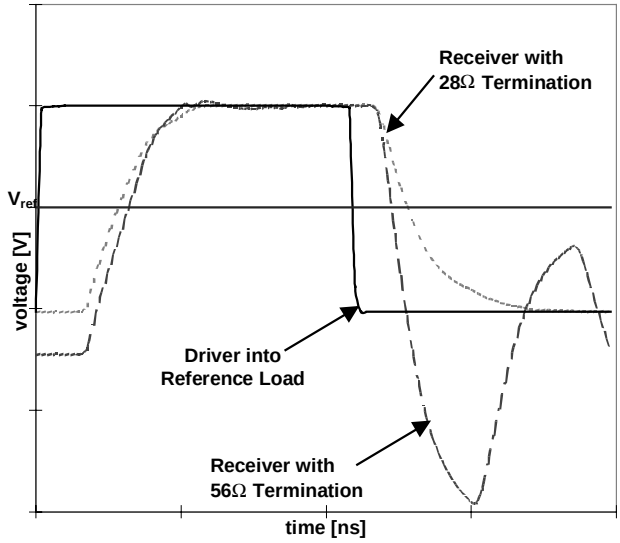
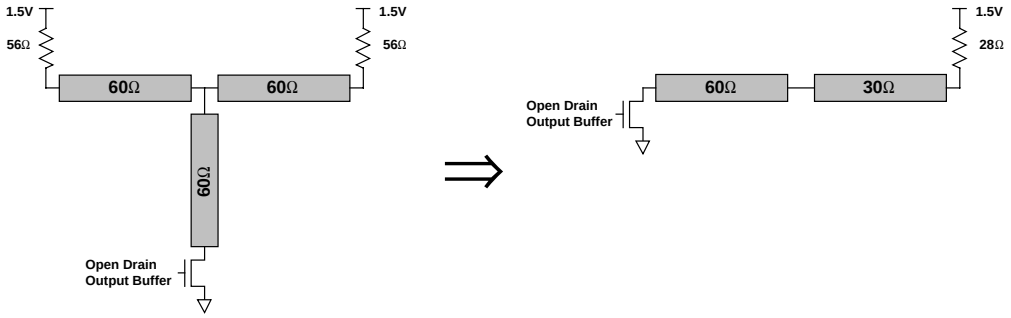


Figure 2. AGTL+ flight time dependence on R_{TT}.

Overshoot and Ringing

Open drain buffers have a tendency to overshoot and ring on the rising edge. The source of the overshoot and ringing can be understood with some simple analysis. Consider the example network shown in Figure 3. The network can be simplified by recognizing the parallel impedance, as shown in the figure. In Figure 3, when the open drain device is turned on, the network will transition from high to low and reach a steady state level, V_{OL}. The equivalent circuit for the low state is shown in Figure 4. At V_{OL}, the current flowing in the network is 37.5 mA.



EXAMPLE NETWORK

SIMPLIFIED NETWORK

Figure 3. Example AGTL+ network.

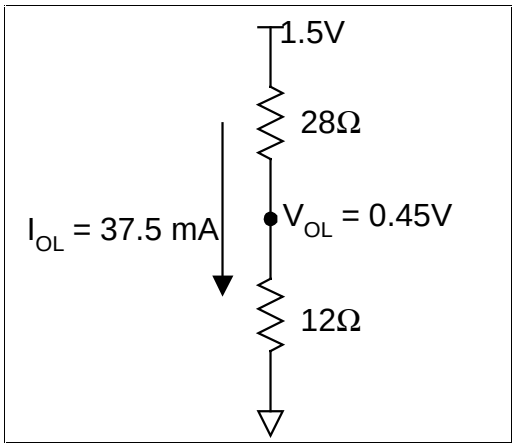


Figure 4. Equivalent circuit for output low state.

When the open drain device turns off, a 37.5 milliamp current wave is launched on the network in the opposite direction, originating at the driver (Figure 5). The amplitude of the corresponding voltage waveform (2.25V) is the product of the current (37.5 mA) and the impedance of the interconnect trace (60Ω). The voltage amplitude at the output of the driver (2.70V) is equal to sum of the steady state V_{OL} (0.45V) and the voltage waveform (2.25V).

When the wave reaches the branch point of the network, part of the wave will be reflected back to the source, according to the following:

$$V_{reflected} = \frac{Z_{02} - Z_{01}}{Z_{02} + Z_{01}} V_{incident} = \frac{30\Omega - 60\Omega}{30\Omega + 60\Omega} 2.25V = -0.75V$$

In the off state, the open drain output buffer behaves like an open circuit. Therefore, the -0.75V reflected wave will be fully reflected. The resulting voltage at the driver will be the sum of the initial voltage plus all wave components:

$$V_{driver} = 0.45V + 2.25V - 0.75V - 0.75V = 1.20V$$

The waveform in Figure 6 illustrates this behavior. The voltage at the driver has an initial overshoot to 2.7V, followed by ringback to 1.20V. Since the network is well terminated at the receiver end of the network, the ringing subsides quickly.

Notice from Figure 6 that the waveform at the far end of the line also exhibits ringing, even though the termination is nearly ideal. This occurs because of the initial overshoot and the reflections at the point where the trace branches off from the main transmission line network.

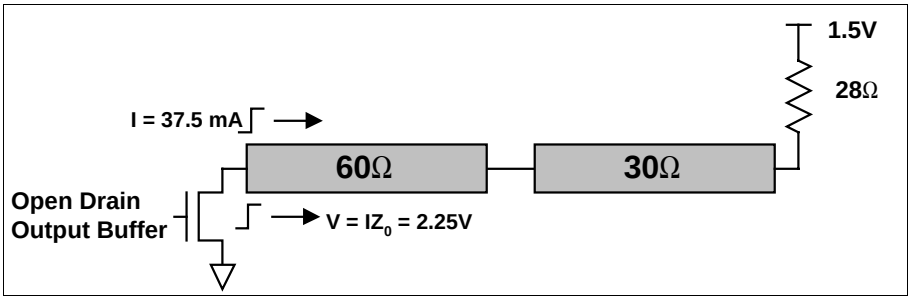


Figure 5. Waveform launch for low-high signal transition.

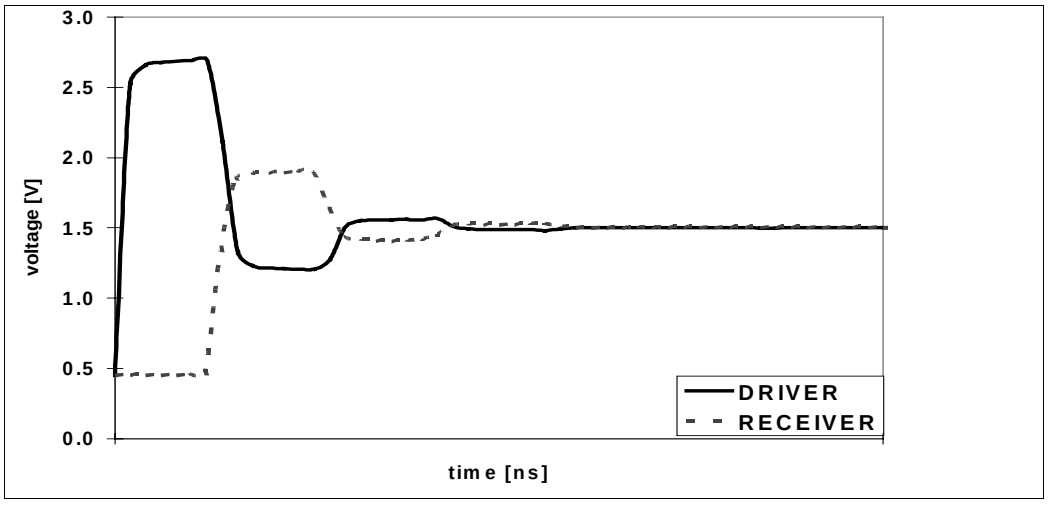


Figure 6. Waveform at the driver for the network in Figure 3.

As this example shows, the combination of the high output impedance of the open drain driver and transmission line stubs creates overshoot and ringing on the rising edge. Controlling the length of transmission line stubs, therefore, is critical in the design of a high speed AGTL+ bus. Figure 7 shows how ringing at the driver and the receivers increases as a function of stub length for the network in Figure 3. Section 4 provides recommendations for maximum transmission line stub lengths in single and dual processor designs.

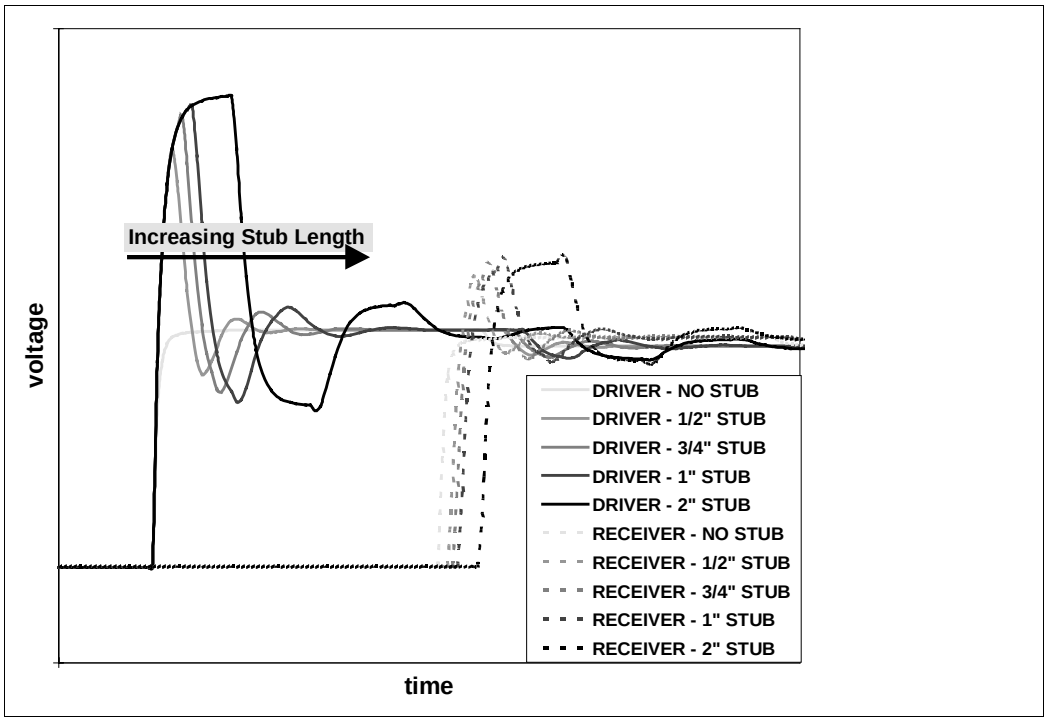


Figure 7. Ringing as a function of stub length for the network in Figure 3.

Pentium® III Processor AGTL+ I/O Buffers

In practice, it is nearly impossible to completely eliminate transmission line stubs from the bus. To reduce the amount of ringing at the driver, Intel has added a weak pull-up device to the output buffer. This device turns on at the beginning of a low-to-high signal transition, substantially reducing the impedance mismatch between the output buffer and the transmission line. As a result, the amount of overshoot and ringback is significantly reduced. The source terminal of pull-up device is connected to the core supply (typically 2.0V). This causes the logic high voltage to rise above the AGTL+ termination voltage for one cycle. After one bus cycle, the pull-up device is turned-off and the output will stabilize at V_{TT} if the output remains in the logic high state.

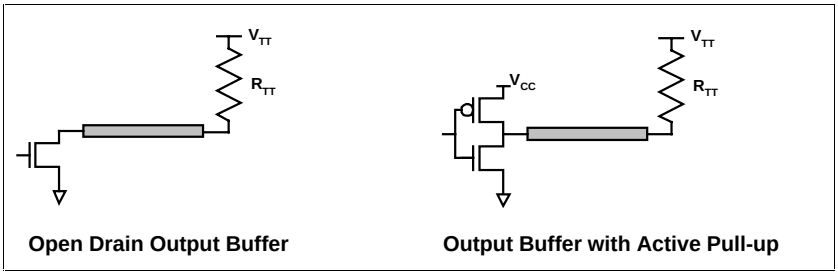


Figure 8. AGTL+ buffer types - open drain and active pull-up

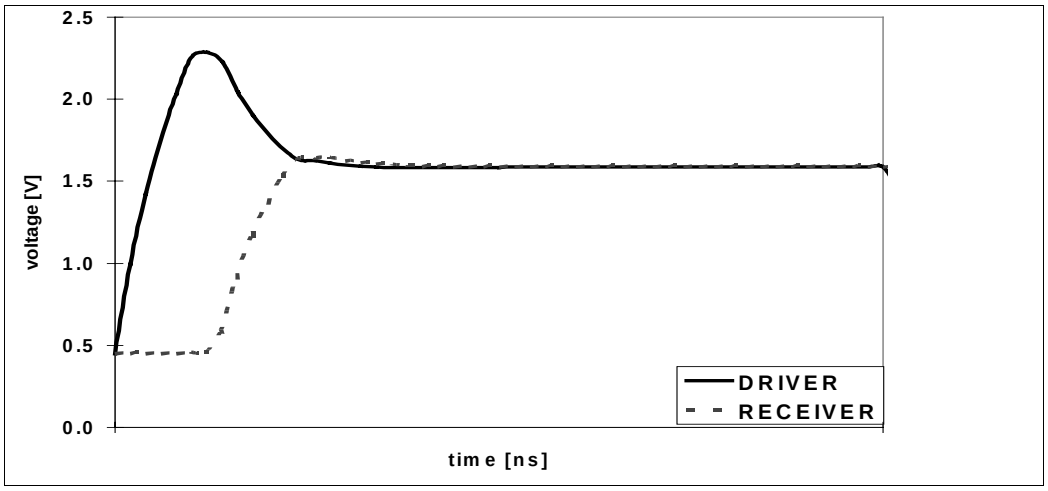


Figure 9. Waveform for the network in Figure 3 when driven with active pull-up

3.2. AGTL+ Simulation Metrics

The complete AGTL+ specification is contained in each processor's datasheet. A description of the simulation metrics is included below.

Flight Time

Interconnect delay on the AGTL+ bus is determined in terms of the interconnect "flight time". The definition of flight time is illustrated in Figure 10. Flight time simulations include two simulations – one of the system under analysis, and one with the driver connected to a test load. (The test or "reference" load is a 25Ω resistor connected to 1.5V). Output buffer delays are guaranteed when driving the reference load.

Delays in AGTL+ systems are measured with respect to the reference voltage V_{REF}. This voltage is usually set to a nominal value of 1.0V. (AGTL+ inputs are differential, therefore the value of V_{REF} may be varied).

In addition to the nominal value of V_{REF}, the "Overdrive Region", at a receiver, from V_{REF} + 200 mV for a low to high going signal and V_{REF} - 200 mV for a high to low going signal must be factored into the determination of flight time.

Flight time is determined as follows: for a nominal waveform, flight time is measured from the time at which the driver crosses V_{REF} when driving a test or "reference" load, to the time at which the receiver's voltage crosses V_{REF}, as shown in Figure 10.

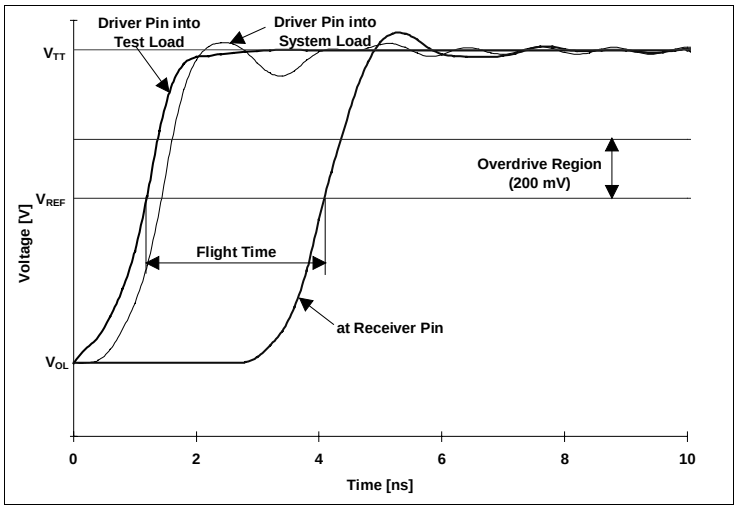


Figure 10. Nominal flight time measurement

If the waveform at the receiver has an edge rate slower than specified for the receiver, then additional time must be allowed for the receiver to recognize the signal as a valid logic level. Specifically, if the receiver's edge rate is slower than 0.3 V/ns, the crossing is calculated at the point which the receiver's voltage crosses V_{REF} + 200 mV (V_{REF} - 200 mV), and then extrapolated back to 1.0V using a slope of 0.3 V/ns. (In other words, 0.67 ns is subtracted from the time of the $V_{REF} \pm 200$ mV crossing.) This form of flight time calculation is shown in Figure 11.

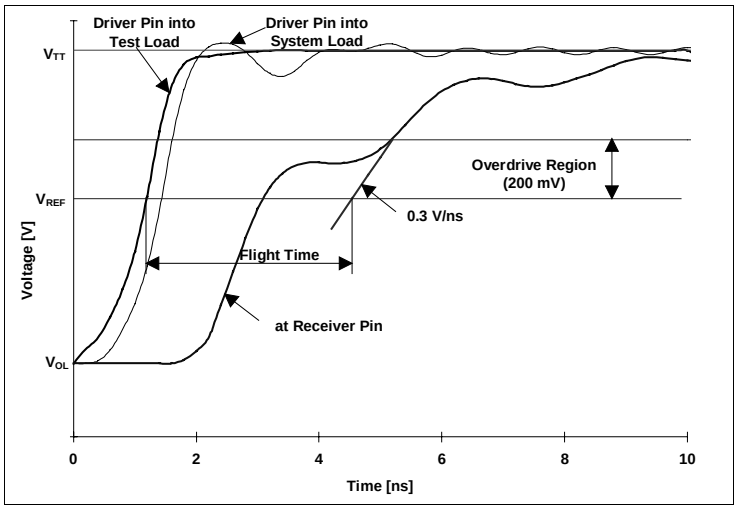


Figure 11. Flight time measurement with edge slower than 0.3 V/ns

A third and final situation must be considered, and that is the case of a non-monotonic waveform, where the receiver's voltage crosses through the "Overdrive Region", and then returns back into the "Overdrive Region", beyond the ringback threshold. In this case the crossing must be measured to the *last* V_{REF} + 200 mV (V_{REF} - 200 mV) crossing at the receiver and extrapolated back to V_{REF}, but in this case an extrapolation slope of 0.8 V/ns is used. (In other words, 0.25 ns is subtracted from the time of the $V_{REF} \pm 200$ mV crossing). This form of flight time calculation is shown in Figure 12.

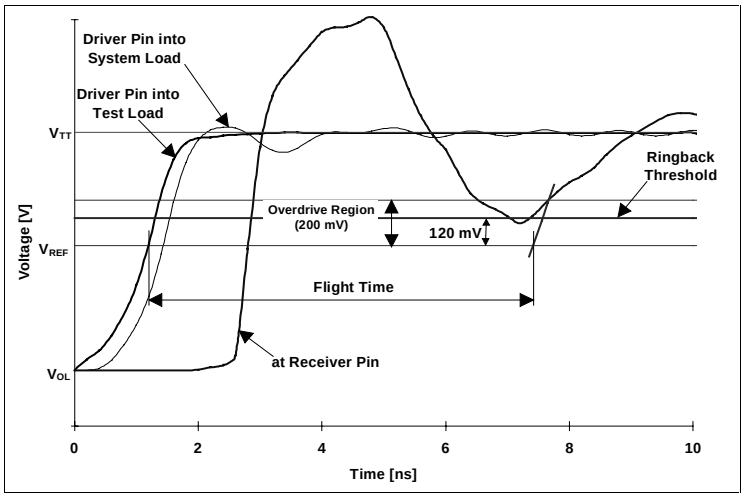


Figure 12. Flight time measurement with non-monotonic rising edge

The methods for measuring flight time on the falling edge are identical to those shown in Figure 10 through Figure 12 for the rising edge. An example is shown in Figure 13.

In all cases, flight time is measured with respect to the edge fingers of the processor and the package pins of the Intel® 440BX AGPset.

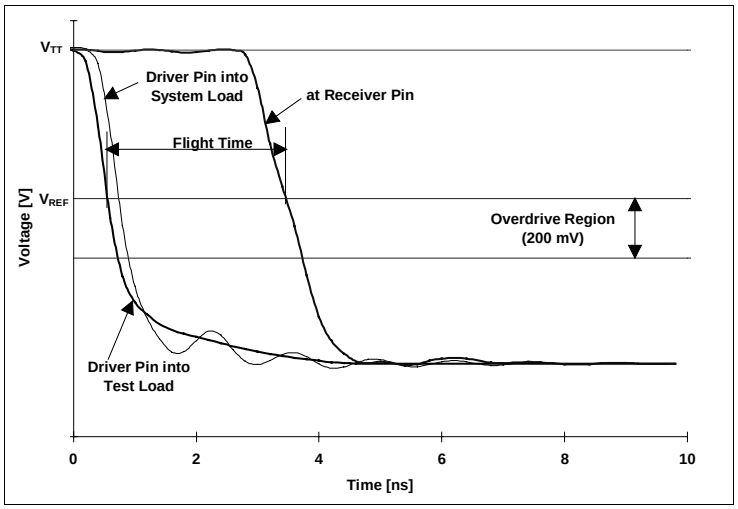


Figure 13. Example falling edge flight time measurement

Signal Quality

In addition to trace delay, waveforms on the AGTL+ bus must conform to signal quality requirements to ensure that system performance is not limited by interconnect noise. The overshoot, ringback, and settling time parameters are illustrated in Figure 14. All signal quality metrics are specified at the processor core.

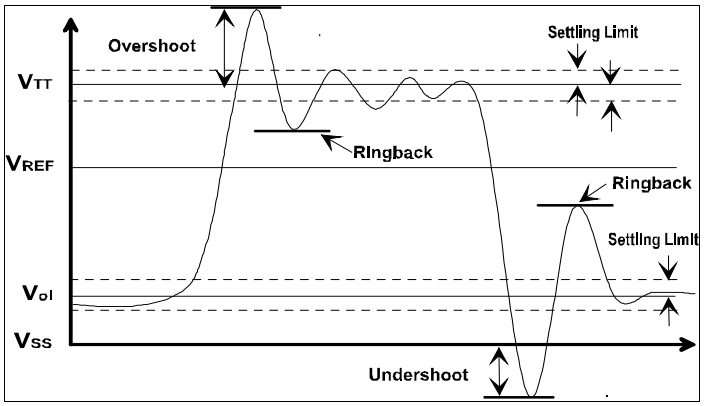


Figure 14. Overshoot, ringback, and settling time

Overshoot

Overshoot (sometimes referred to as undershoot for falling transitions), is the amount by which the signal's voltage level extends above or below the final V_{OH} or V_{OL} level. In this document, overshoot is stated in absolute voltages, rather than its value relative to V_{OH} or V_{OL}. (This convention is chosen since V_{OH} and V_{OL} may vary on AGTL+ busses, thus causing possible confusion).

Limiting overshoot is usually necessary to insure the flight time meets the design requirements and to avoid damaging the components connected on the AGTL+ bus.

Ringback

Ringback is the amount by which a signal rebounds below V_{OH} (or above V_{OL}) after an overshoot event has occurred. As with overshoot, the convention used in this document states ringback in absolute voltages rather than relative to V_{OH} or V_{OL}.

Ringback must be limited to prevent inadvertent false switching of these digital signals. Refer to processor datasheets for the ringback threshold specifications for the processor and Intel® 440BX AGPset. The ringback specifications adhere to the methodology described in chapter 3 of the processor datasheet.

Settling Time

Settling time is a measurement of oscillations on the AGTL+ waveform (usually caused by reflections on the transmission line traces). This term measures the amount of time required for oscillations to dampen to a level that will not increase the flight time of the next transition.

Settling time for the processor bus is limited to 10 ns when operating at 100 MHz. This ensures that oscillations have dampened to amplitude within ±10% of the signal swing before the next cycle. (±10% equates to approximately ±100 mV for AGTL+ signals. This value has been chosen based on analysis of AGTL+ sensitivity to these oscillations.)

4.0. AGTL+ LAYOUT RECOMMENDATIONS

This section contains the layout recommendations for the AGTL+ signals. The layout recommendations are derived from pre-layout simulations Intel has run using the methodology described in Section 6. Results from the pre-layout simulations are included in this section.

4.1. Single Processor Design

4.1.1. SINGLE PROCESSOR NETWORK TOPOLOGY & CONDITIONS

The recommended topology for single processor systems is shown in Figure 15. In addition to the termination resistor on the processor substrate, a termination resistor is placed on the system board. The recommended value for the termination resistor is 56Ω ± 5%.

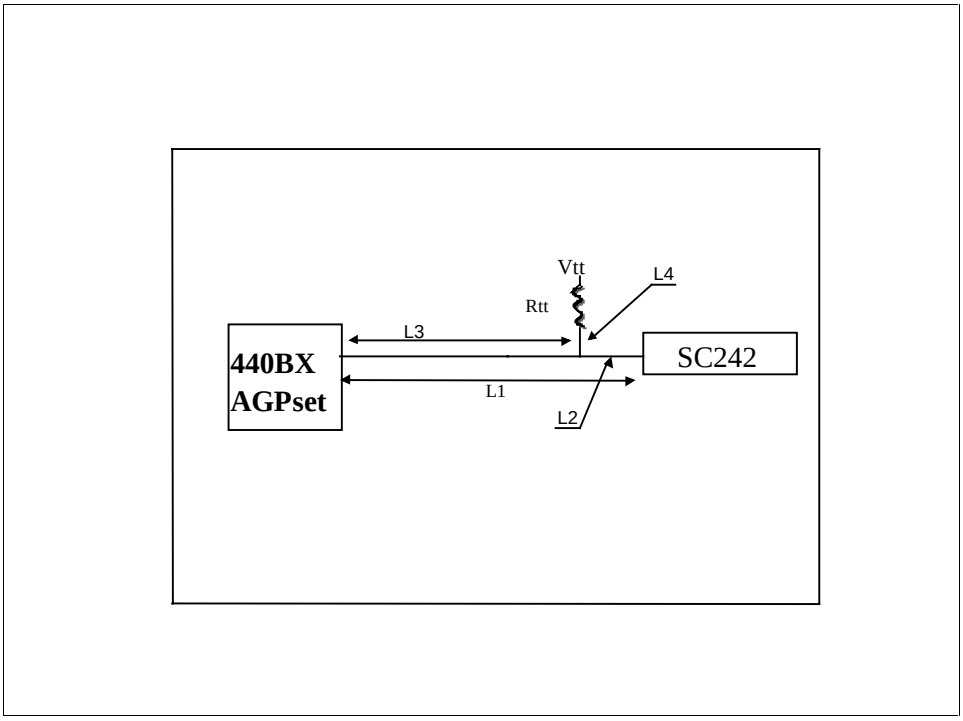


Figure 15. Recommended topology for single processor design

4.1.2. SINGLE PROCESSOR RECOMMENDED TRACE LENGTHS

Single processor trace length recommendations are summarized in Table 1. The recommended lengths are derived from the parametric sweeps and Monte Carlo analysis described in the following section.

Table 1. Recommended trace lengths for single processor design

Trace	Minimum Length	Maximum Length
L1	1.50"	6.75" [1]
L3	0.00"	1.50"
L4	0.00"	2.50" [2]

Notes:
1. L1=4.5" maximum for processor stepping affected by erratum #42. Please refer to the appropriate Processor Specification Update for details.
2. L4 can be increased to 5.00" if the L1 is restricted to 4.5" maximum (see note 1).

Intel strongly recommends running analog simulations using the available I/O buffer models together with layout information extracted from your specific design. Simulation will confirm that the design adheres to the signal quality and timing requirements.

4.1.3. SINGLE PROCESSOR SIMULATION RESULTS

Parametric Sweeps

Section 6.3.2 defines the parametric sweeps analysis methodology. The values for interconnect parameter values that were used in all parametric sweeps are summarized in Table 2. Three distinct cases were analyzed: minimum flight time, maximum flight time, and signal quality. In each case, the lengths for the L2 and L3 trace segments were varied, while all other parameters were held constant at the values listed in the table. The processor substrate, package, termination, SC242 connector and buffer corner parameters are all defined in the appropriate I/O model for the processor. Following provides the simulation data around the Pentium® II processor at 100MHz system bus. The data is applicable to the Pentium III Processor at 100MHz system bus.

Table 2. Model Parameter Values for Interconnect Simulations

Parameter	Minimum Flight Time	Maximum Flight Time	Signal Quality
System Board Impedance	75Ω	55Ω	75Ω
System Board Delay per Unit Length	1.6 ns/ft (microstrip) 1.8 ns/ft (stripline)	2.0 ns/ft (microstrip) 2.2 ns/ft (stripline)	1.6 ns/ft (microstrip) 1.8 ns/ft (stripline)
System Board Trace Length (L2)	0.00”-12.00”	0.00”-12.00”	0.00”-12.00”
System Board Trace Length (L3)	0.00”-2.00”	0.00”-2.00”	0.00”-2.00”
System Board Trace Length (L4)	0.00”	2.50”	2.50”
Termination Resistor	56Ω ± 5%	56Ω ± 5%	56Ω ± 5%
Processor Substrate Impedance	75Ω	55Ω	55Ω
Processor Substrate Delay per Unit Length	1.6 ns/ft	2.2 ns/ft	2.2 ns/ft
Processor Substrate Trace Length	2.5”	1.50”	1.50”
SC242 Connector Impedance	80Ω	35Ω	35Ω
SC242 Connector Delay	110 ps	150 ps	150 ps
Processor Core Package Impedance	111.7Ω (microstrip) 56.4Ω (stripline)	111.7Ω (microstrip) 56.4Ω (stripline)	111.7Ω (microstrip) 56.4Ω (stripline)
Processor Core Package Delay per Unit Length	2.2 ns/ft	2.2 ns/ft	2.2 ns/ft
Processor Core Package Trace Length	0.079” (microstrip) 0.146” (stripline)	0.681” (microstrip) 0.276” (stripline)	0.681” (microstrip) 0.276” (stripline)
440BX AGPset Package Impedance	64.2Ω	64.2Ω	64.2Ω
440BX AGPset Package Delay per Unit Length	1.93 ns/ft	1.93 ns/ft	1.93 ns/ft
440BX AGPset Package Trace Length	0.417”	0.540”	0.540”
Buffer Model Corner	Fast	Slow	Fast

Figure 16 summarizes minimum flight time results for both rising and falling edges with each agent driving. Figure 17 summarizes maximum flight time results.

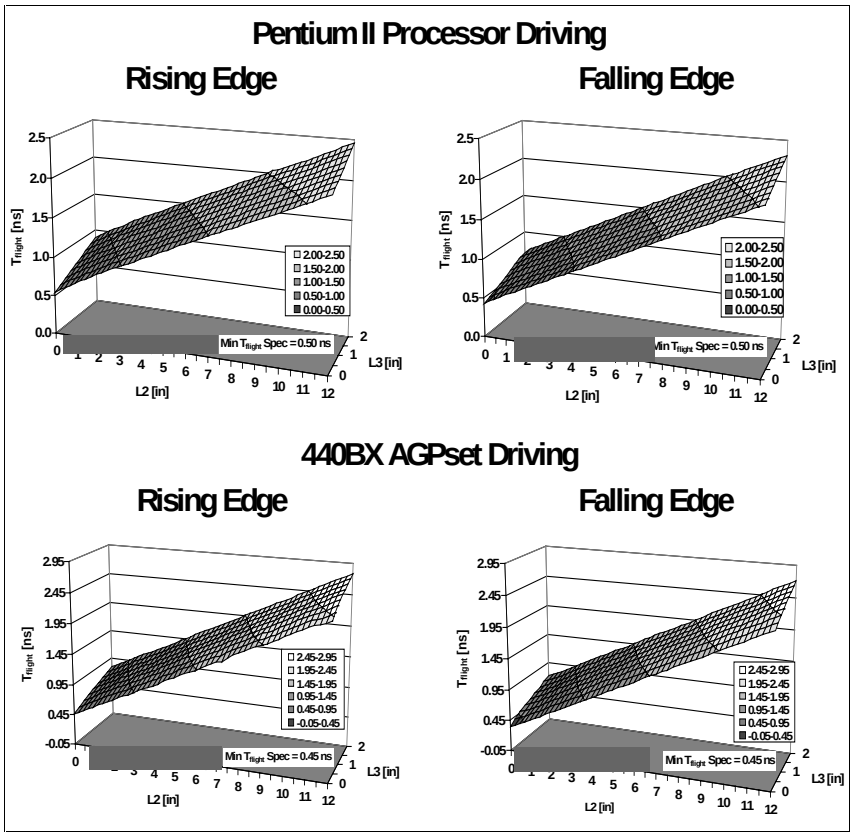


Figure 16. Parametric sweep minimum flight times for single processor design

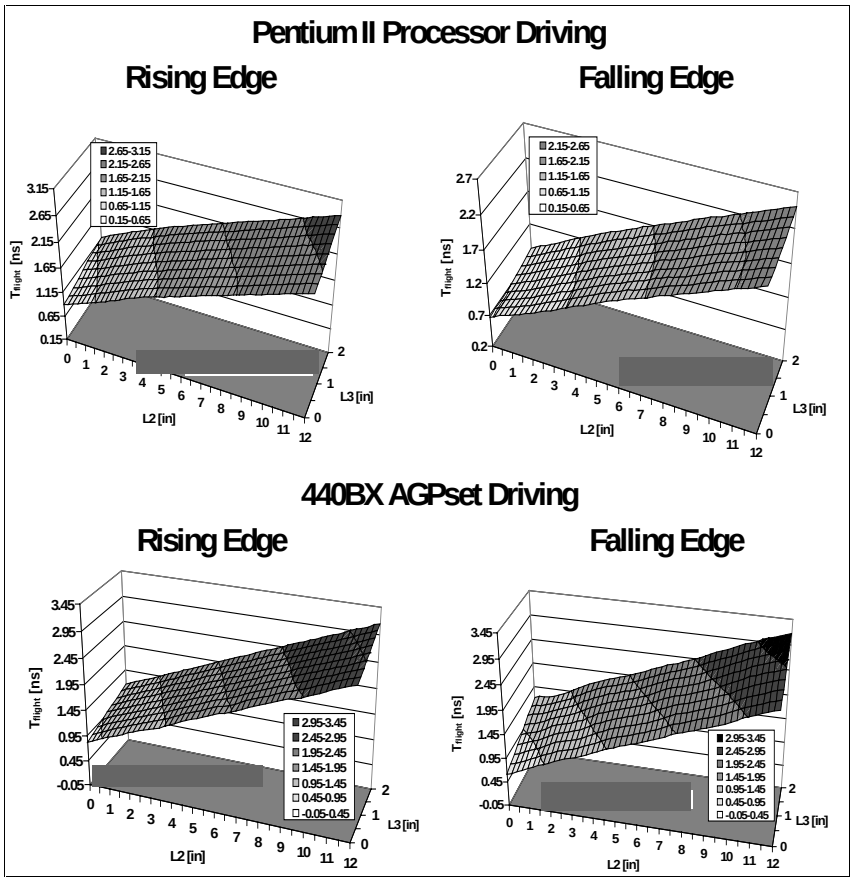


Figure 17. Parametric sweep maximum flight times for single processor design

Overshoot and ringback are not shown here, as the single processor design with dual termination is very robust with respect to signal quality. The solution space in Figure 18 was constructed using the surfaces in Figure 16 and Figure 17. Section 6 describes the method for calculating the solution space from the response surfaces. Figure 18 shows that the parametric sweeps support a range of trace lengths from 1.5 inches to 6.75 inches.

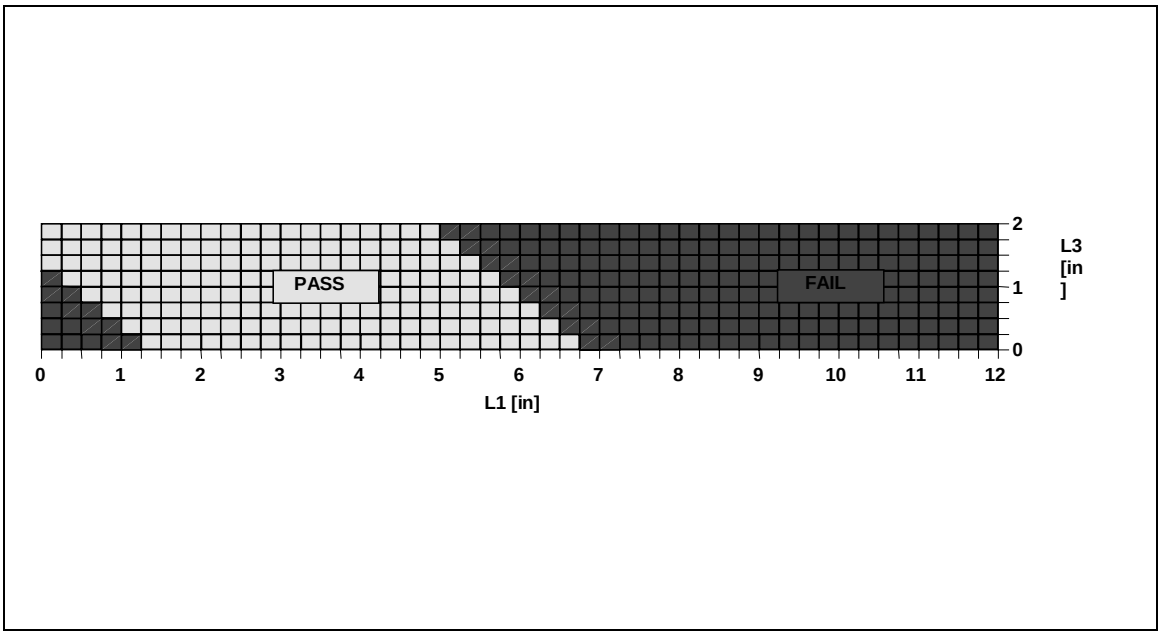


Figure 18. Solution space for single processor design, based on results of parametric sweeps

Monte Carlo Analysis

Figure 19 summarizes the flight time results from Monte Carlo simulations for the single processor topology, section 6.3.3 defines the Monte Carlo analysis methodology. For the Monte Carlo simulations the following parameters were allowed to vary uniformly within the ranges defined in Table 2:

- Processor substrate impedance, velocity, and trace length
- Termination resistance
- System board impedance, velocity, and trace length
- Processor core package impedance, velocity, and trace length
- 440BX AGPset package impedance, velocity, and trace length
- SC242 connector impedance and propagation delay

In Figure 19, the minimum and maximum trace lengths were determined by defining the range of lengths for which all flight times met the minimum and maximum specs. As the figure shows, the trace lengths are limited by the case where the processor drives the network. The Monte Carlo simulations also support trace lengths from 1.5 inches to 6.75 inches.

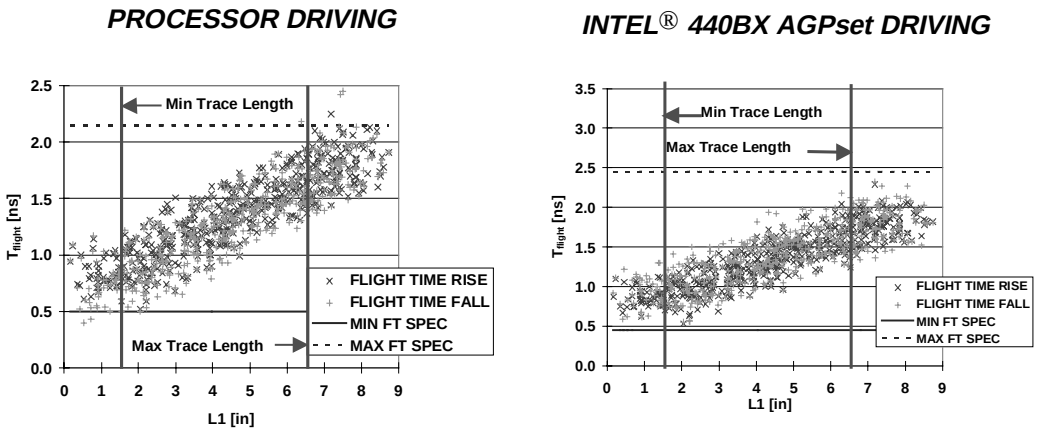


Figure 19. Monte Carlo flight times for Uni-processor, based on parametric sweeps results

Figure 20 shows Monte Carlo ringback results for the rising edge. The single processor design shows very little ringback when the processor drives the network. Some ringback is present when the 440BX AGPset drives, but there is more than 100 mV of margin to the ringback spec. The falling edge shows minimal ringback, and the results are not shown here.

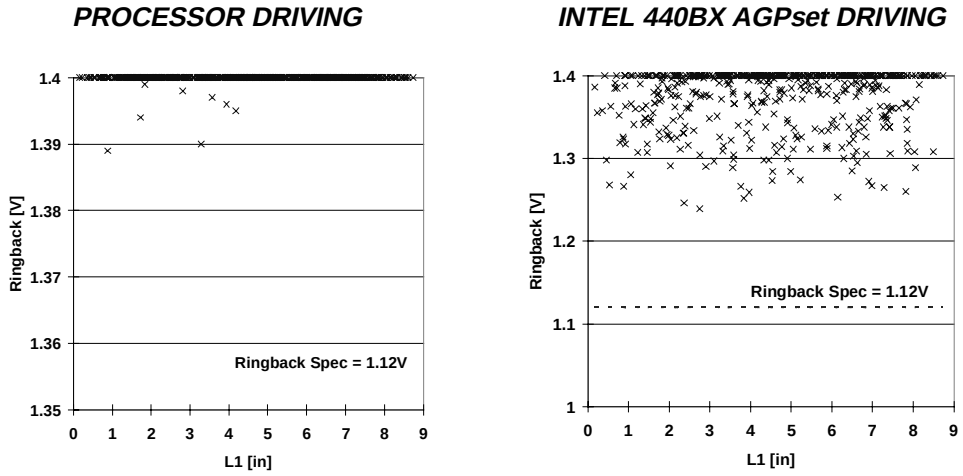


Figure 20. Monte Carlo signal quality for Uni-processor, based on parametric sweeps results

4.2. Dual Processor Systems

4.2.1. DUAL PROCESSOR NETWORK TOPOLOGY & CONDITIONS

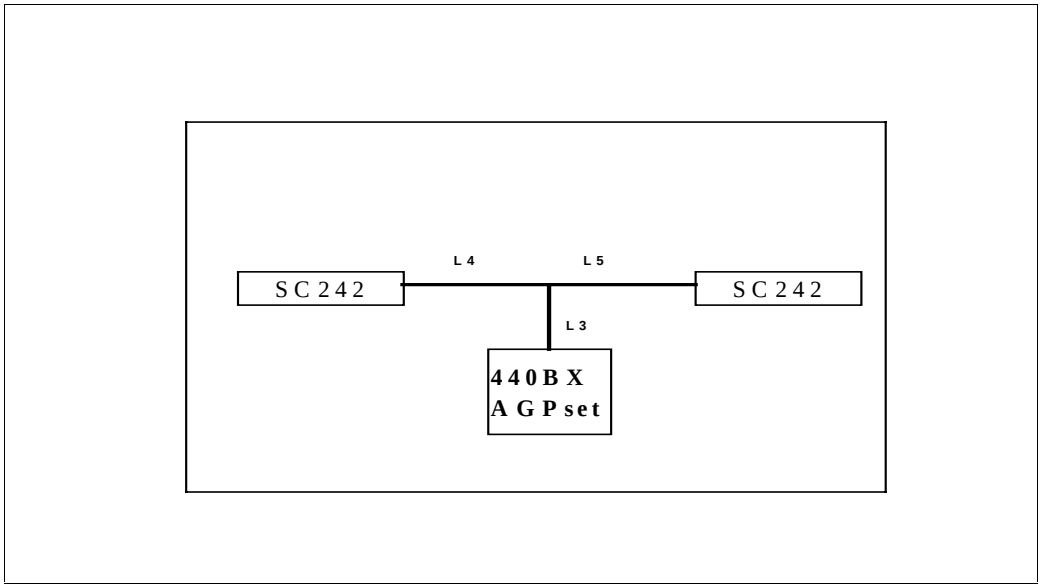


Figure 21. Recommended topology for dual processor design

4.2.2. DUAL PROCESSOR RECOMMENDED TRACE LENGTHS

The recommended trace lengths for dual processor designs are summarized in Table 3. Intel's simulations have shown that it is desirable to control the amount of imbalance in the network in order to meet ringback specifications at the processor when the Intel® 440BX AGPset drives the bus. This control is reflected in the recommendations of Table 3.

Table 3. Recommended trace lengths for dual processor designs[2,3]

Trace	Minimum Length	Maximum Length
L3	0.50”	1.50”
L4[1]	1.50”	4.00”
L5[2]	L4 - 1.00”, but L4+L5 must be at least 4.00”	L4 + 1.00”, but not greater than 5.00”

Notes:

1. L4 and L5 are interchangeable (see Figure 22).
2. It is possible to find working solutions outside the recommendations of Table 3, as the solution space plot shows. Intel strongly recommends that any traces that fall outside the recommended lengths be simulated to ensure they meet timing and signal quality specs.
3. For dual processor platforms with one processor installed, the termination card should be placed in the longer leg.

4.2.3. DUAL PROCESSOR SIMULATION RESULTS

The dual processor trace length recommendations in Table 3 are based on the intersection of the solution spaces created by parametric sweeps and Monte Carlo analysis. The solution space is contained in Figure 22. The solution space was constructed from surface plots for minimum flight time, maximum flight time, and signal quality using the method described in section 6.

For the Monte Carlo simulations, the parameters in Table 2 were allowed to vary uniformly between the extremes listed in the table.

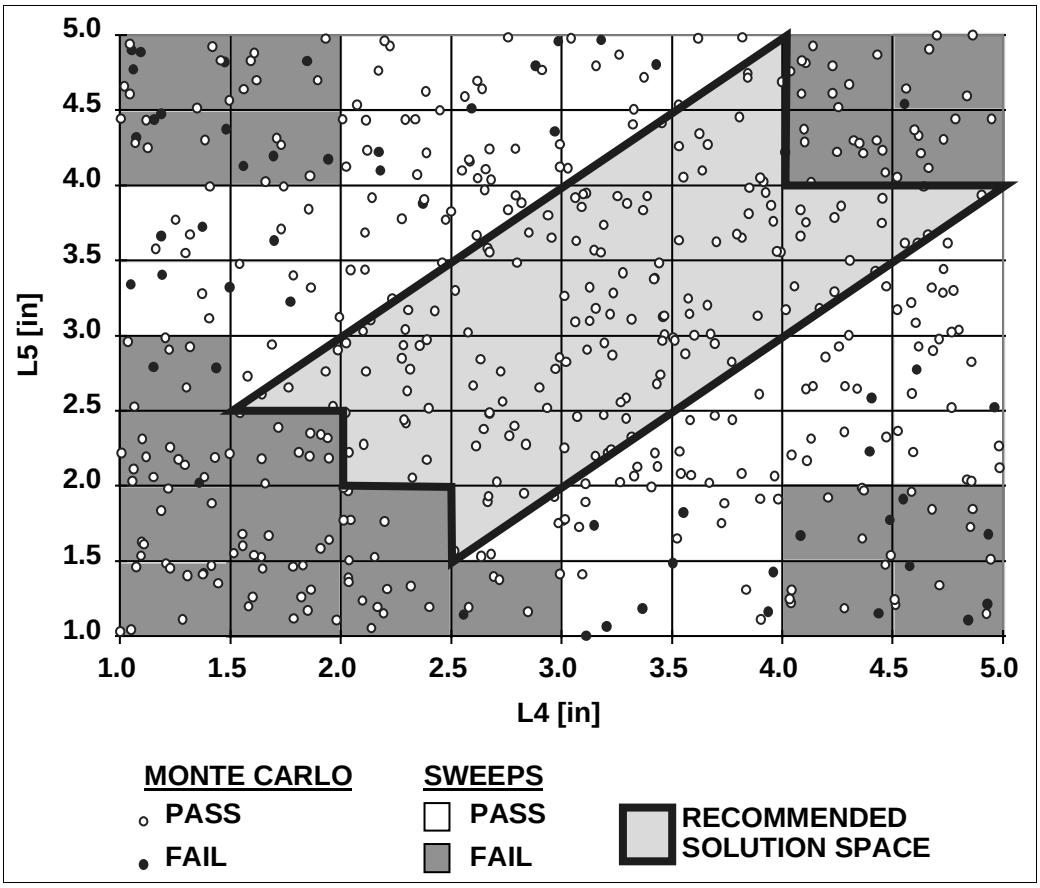


Figure 22. Dual processor solution space based on sweeps & Monte Carlo analysis

Lossy transmission line effects have been included in the solution spaces. Intel has found that including the DC resistance of the processor substrate and system board can reduce the amount of ringback on the rising edge by as much as 50 mV. Interconnect losses were included in the simulations to allow as much flexibility as possible in the solution space, while still meeting signal quality specs.

4.3. Single Processor Systems - Single-End Termination (SET)

4.3.1. SET NETWORK TOPOLOGY & CONDITIONS

Removal of the termination resistors from the system board can reduce system cost, at the expense of increased ringing and reduced solution space. Intel has simulated this topology, known as single end termination (SET), and found that it can be made to work. However, the topology has some limitations which are discussed below.

In the SET topology, the only termination is on the processor substrate. There is no termination present at the other end of the network. Due to the lack of termination, SET exhibits much more ringback than the dual terminated topology. Extra care is required in SET simulations to make sure that the ringback specs are met under the worst case signal quality conditions.

In addition, since there is only one pull-up resistor per net the rising edge response is substantially degraded when using slow corner buffers. This effect manifests itself as a degraded flight time, which results in a reduced maximum trace length that meets the 100 MHz timing requirements. This loss of design flexibility must be carefully weighed against the cost savings from removing resistors.

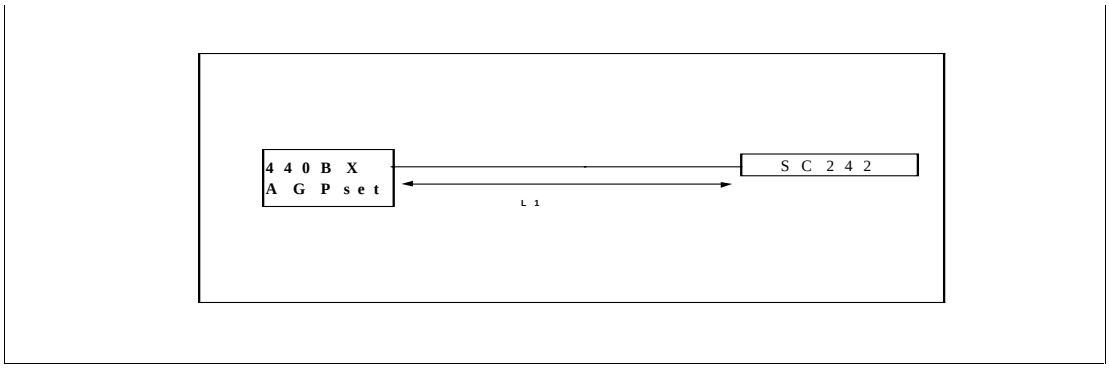


Figure 23. Topology for single processor designs with single end termination (SET)

4.3.2. SET TRACE LENGTH REQUIREMENTS

Intel has performed sensitivity analysis on the SET topology. The required trace lengths for operation at 100 MHz with the SET topology are based on the sensitivity analysis results, and are listed in Table 4. Intel's SET simulations were performed assuming a four layer system board, so that all traces used the microstrip propagation velocity range from Table 2. The slower propagation of stripline transmission line structures is not included in the recommendations of Table 4.

Table 4. SET trace length requirements

Trace	Minimum Length	Maximum Length
L1	1.50"	4.00"

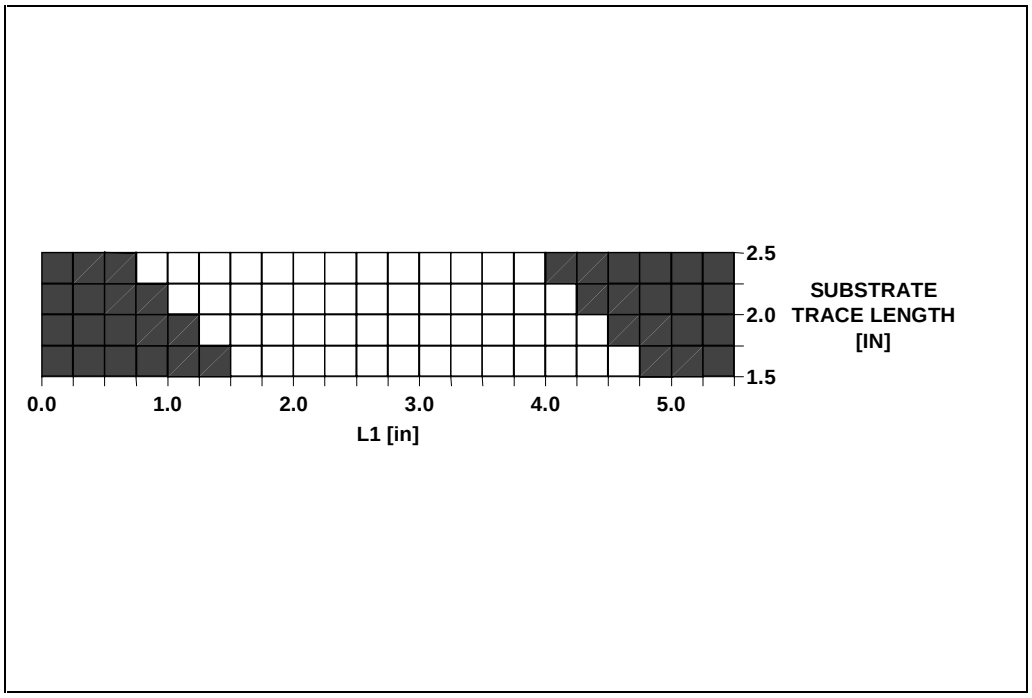


Figure 24. Solution space for single processor designs with single end termination (SET)

4.4. Additional Guidelines

4.4.1. MINIMIZING CROSSTALK

The following general rules will minimize the impact of crosstalk in the high speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 0.010" between traces wherever possible. It may be necessary to use tighter spacing when routing between component pins.

- Avoid parallelism between signals on adjacent layers.

- Since AGTL+ is a slow signal swing technology, it is important to isolate AGTL+ signals from other signals by at least 0.025". This will avoid coupling from signals that have larger voltage swings, such as 5V PCI.

- Select a board stack-up that minimizes the coupling between adjacent signals.

- Route AGTL+ address, data and control signals in separate groups to minimize crosstalk between groups. The Pentium® III Processor uses a split transaction bus. In a given clock cycle, the address lines and corresponding control lines could be driven by a different agent than the data lines and their corresponding control lines.

4.4.2. PRACTICAL CONSIDERATIONS

- Distribute V_{TT} with a wide trace. A 0.050" minimum trace is recommended to minimize DC losses. Route the V_{TT} trace to all components on the host bus. Be sure to include de-coupling capacitors. Guidelines for V_{TT} distribution and de-coupling are contained in AP-907 *Pentium® III Processor Power Distribution Guidelines*.

- Place resistor divider pairs for V_{REF} generation at the Intel® 440BX AGPset component. No V_{REF} generation is needed at the processor(s). V_{REF} is generated locally on the processor. Be sure to include de-coupling capacitors. Guidelines for V_{REF} distribution and de-coupling are contained in AP-907 *Pentium® III Processor Power Distribution Guidelines.*

- There are six AGTL+ signals that can be driven by more than one agent simultaneously. These signals may require extra attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two agents on the same clock edge, the two falling wave fronts will meet at some point on the bus. This can create a large undershoot, followed by ringback which may violate the ringback specifications. This "wired-OR" situation should be simulated for the following signals: AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

- Loss-less simulations can overstate the amount of ringing on AGTL+ signals. Lossy simulations may help to make your results less pessimistic if ringing is a problem. Intel has found the resistivity of copper in printed circuit board signal layers higher than the value of 0.662 $\Omega \cdot mil^2/in$ that has been published for annealed copper. Intel recommends using a value of 1.0 $\Omega \cdot mil^2/in$ for lossy simulations.

- Higher R_{TT} values tend to increase the amount of ringback on the rising edge, while smaller values tend to increase the amount of ringback on the falling edge. It is not necessary to budget for R_{TT} variation if your simulations comprehend the expected manufacturing variation.

- I/O Buffer models for the fast corner correspond to the minimum T_{co}. Slow corner buffers will be at least 500 ps slower. Therefore, it is only necessary to ensure that the minimum flight time is met when fast buffer models drive the network.

- I/O Buffer models for the slow corner correspond to the maximum T_{co}. Fast corner buffers will be at least 500 ps faster. It is only necessary to ensure that the maximum flight time is met when slow buffer models drive the network, as long as no ringback problems exist.

5.0. CLOCK LAYOUT RECOMMENDATIONS

5.1. Clock Design Approach

- All of the Host clocks are referenced to the Host clock signal that is routed to the SC242 connector.

- The 440BX PCI clock is referenced to the 440BX Host clock. The layout of the PCI clock for the Intel® 440BX AGPset is established to ensure that the PCI clock lags the Host clock by 1.5 to 5 ns (Figure 25). The analysis assumes that the clock driver for the PCI clock lags the host clock by 1.5 to 4 ns, consistent with the CK97 clock specification.

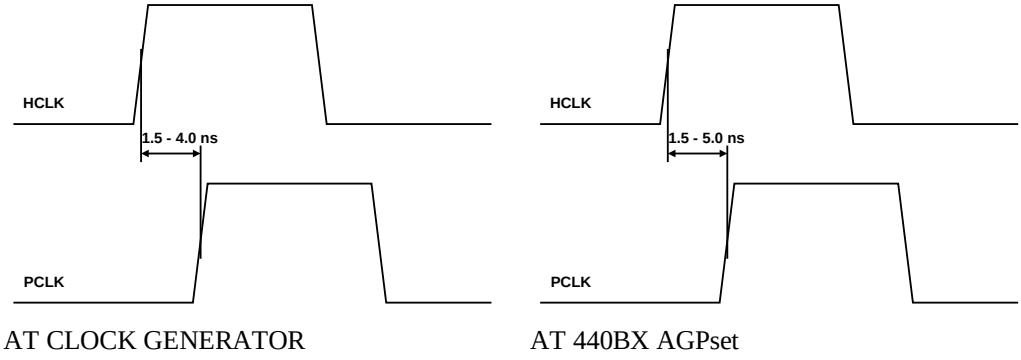


Figure 25. Host-to-PCI clock lag spec

- The remaining PCI clocks should be referenced to the 440BX PCI clock, and routed to meet the clock skew specifications contained in revision 2.1 of PCI bus specification.

5.2. Recommended Topology

Host clock nets should be routed as point-to-point connections with a series resistor that closely matches the output impedance of the clock driver, which is normally in the range of 33Ω, to be placed as close to the output pins on the clock driver as possible (<0.5").

PCI clock nets should be routed a point-to-point connections with a 22Ω series resistor that is to be placed as close to the output pins on the clock driver as possible (<0.5").

5.3. Simulation Results

Results from Monte Carlo simulations using buffer models that reflect the CK97 device specifications are summarized in Figure 26. The trace lengths from the clock driver to the SC242 connector were allowed to vary between 3 and 9 inches. In addition, the following parameters were allowed to vary uniformly within expected extremes (see Table 2):

- Processor substrate impedance, velocity
- System board impedance and velocity
- Processor core package impedance, velocity
- AGPset package impedance, velocity, and trace length
- SC242 connector impedance and propagation delay

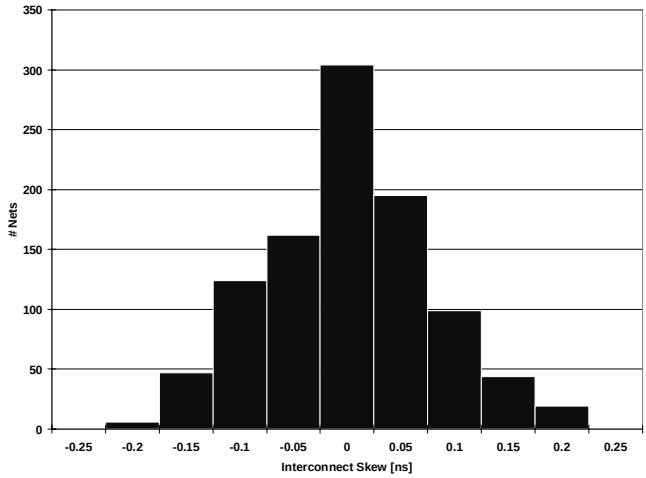


Figure 26. Monte Carlo results for host clock skew.

The simulations support a maximum interconnect skew of 225 ps. The skew budget has been broken into two pieces. Variation in the processor substrate and in the processor core capacitive loading contributes 75 ps of skew that is accounted for in the processor timing specs. The remaining 150 ps is budgeted for variations in the system board, SC242 connector, and AGPset package and loading. Table 5 summarizes the interconnect skew budget.

Table 5. Budget for Clock Skew Due to Interconnect

Signal	Budget
Pentium II processors Skew	75 ps
System Board Skew	150 ps
Total Host Bus Skew	225 ps

5.4. Recommended Host Clock Trace Lengths

Recommended lengths for clock traces are contained in Table 6. All traces should be routed to meet the recommended guidelines within 0.025". The lengths are specified relative to the host clock signal that is connected to the SC242 connector (denoted as "X" in the table).

When measuring clock skew between the processor and Intel® 440BX AGPset, there will be a nominal offset of 780 ps. In other words, for a perfectly designed system with no skew between the processor and AGPset, the delay to the SC242 connector will be 780 ps less than the delay to the AGPset. This is due to the trace delay of the clock signal on the processor substrate. This delay should not be treated as a clock skew, and therefore must be accounted for in the analysis.

Table 6. Layout guidelines for host and PCI clocks

Signal	Guideline
Host Clock to SC242	X
Host Clock to 440BX AGPset	X + 780ps
Host Clock to ITP	X + 4.000"
PCI Clock to 440BX AGPset	X + 6.000"

To minimize the impact of crosstalk, a minimum of 0.014" spacing should be maintained between the clock traces and other traces. A minimum spacing of 0.018" is recommended for serpentines.

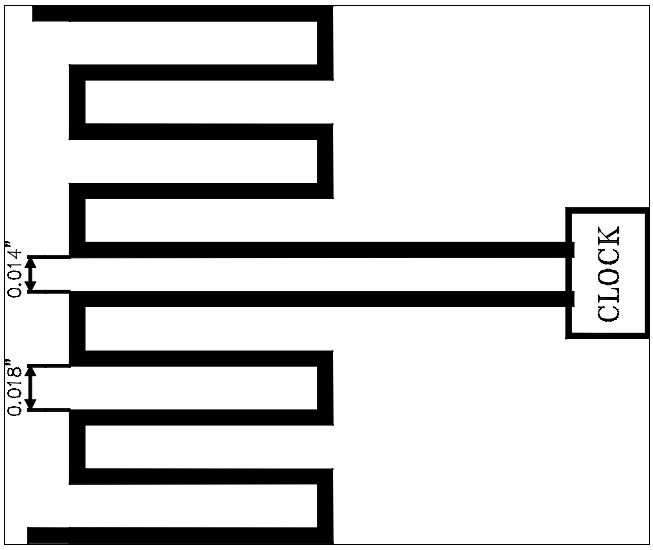


Figure 27. Clock trace spacing guidelines

6.0. DESIGN METHODOLOGY

Intel recommends using the following design methodology when designing systems based on one or two Pentium® III Processors and one 440BX AGPset. The methodology evolved from Intel's experience developing and validating high-speed AGTL+ bus designs for the Pentium Pro and Pentium II processors.

The methodology provides a step-by-step process, which is summarized in Figure 28. The process begins with an initial timing analysis and topology definition. Timing and topology recommendations are included in this section. The heart of the methodology is structured around extensive simulations and analysis prior to board layout. This represents a significant departure from traditional design methods. The pre-layout simulations provide a detail picture of the working "solution space" for the design. By basing the board layout guidelines on the solution space, the need to iterate between layout and post-layout simulation is minimized. The methodology includes specific recommendations for analytical techniques and simulation conditions. Following layout, simulation with the extracted design database is used to verify that the design meets flight time and signal quality requirements prior to building hardware. Finally, validation verifies that the system meets 100 MHz timing and signal quality requirements with actual hardware.

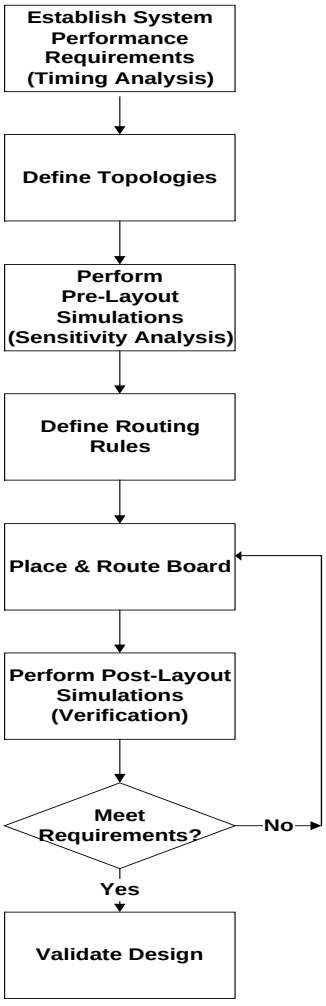


Figure 28. AGTL+ Design Process

6.1. Performance Requirements

Prior to performing interconnect simulations, establish the minimum and maximum flight time requirements. Setup and hold requirements determine the flight time bounds for the host bus. The system contains multiple paths which must be considered:

- Processor driving an AGPset component
- AGPset component driving a processor
- Processor driving a Processor (dual processor systems only)

Section 7 describes the timing analysis for the 100 MHz host bus in more detail. Table 7 provides recommended flight time targets for single and dual processor systems. Flight times are measured at the processor edge fingers, as described in section 3.2. AGTL+ Simulation Metrics

Table 7. Recommended 100 MHz System Flight Time Targets

Driver	Receiver	$T_{flight,min}$ [ns]	$T_{flight,max}$ [ns]
Processor	AGPset	0.36	2.13
AGPset	Processor	0.37	1.76
Processor	Processor	1.23	2.39

6.2. Topology Definition

As described in section 3, AGTL+ is sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. AGTL+ signals should be connected in a daisy chain, keeping transmission line stubs to the Intel® 440BX AGPset under 1.5 inches. The processor should be placed at the end of the bus to properly terminate the AGTL+ signals.

For a single processor design, Intel recommends that termination resistors be placed at the other (AGPset) end of the bus. This provides the most robust signal integrity characteristics and maximizes the range of trace lengths that will meet the flight time requirements. The recommended termination resistor value is $56\Omega \pm 5\%$.

For dual Processor designs, a termination card must be placed in the unused slot when only one processor is populated. This is necessary to ensure that signal integrity requirements are met. Refer to "Slot 1 Bus Termination Card Design Guidelines" for details.

6.3. Pre-Layout Simulation (Sensitivity Analysis)

After an initial timing analysis has been completed, simulations should be performed to determine the bounds on system layout. The layout recommendations in sections 5 and 6 are based on results of pre-layout simulations conducted by Intel.

AGTL+ interconnect simulations using transmission line models are recommended to determine signal quality and flight times for proposed layouts. Recommended parameter values shown in Table 2 on page 17 should be used for simulation.

The recommended values in Table 2 may be replaced if your supplier's specific capabilities are known. The corner values should comprehend the full range of manufacturing variation.

Processor models include the I/O buffer models, core package parasitic, and substrate trace length, impedance and velocity. Intel® 440BX models include the I/O buffers and package traces. Termination resistors should be controlled to within ± 5%.

6.3.1. SIMULATION METHODOLOGY

Pre-layout simulation allows the system "solution space" that meets flight time and signal quality requirements to be understood before any routing is undertaken. Determining the layout restrictions prior to physical design removes iteration cycles between layout & post layout simulation, as shown in Figure 29.

The methodology that Intel recommends is known as "Sensitivity Analysis". In sensitivity analysis, interconnect parameters are varied to understand how they affect system timing and signal integrity. Sensitivity analysis can be further broken into two types of analysis, parametric sweeps and Monte Carlo analysis, which are described below.

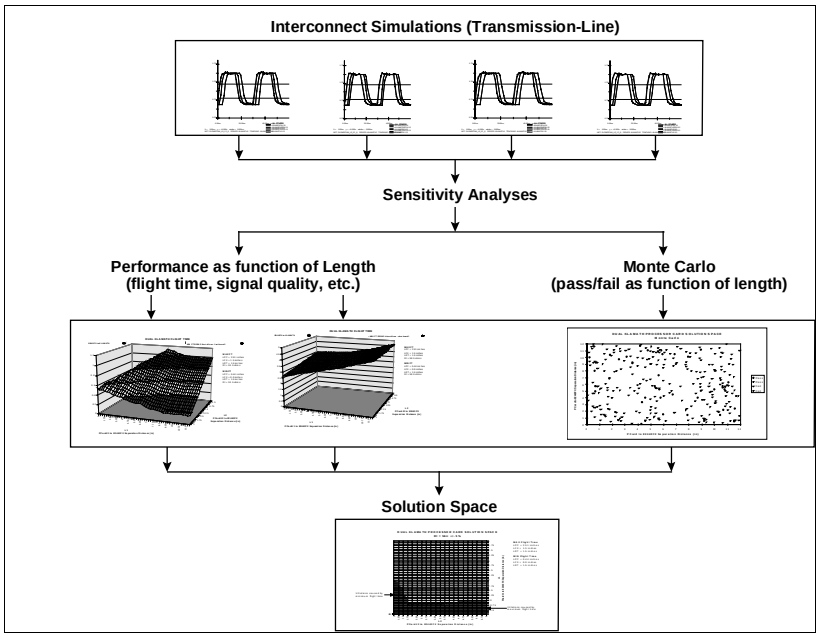


Figure 29. Pre-layout simulation process

6.3.2. PARAMETRIC SWEEP ANALYSIS

In parametric sweep analysis, one or two system parameters are varied while all others are held constant. In this way, the sensitivity of the bus to the varying parameters can be analyzed in a systematic manner. For example, in the simulations that were used to generate the layout guidelines in section 4, the trace lengths between the SC242 connector and the AGPset were varied to establish limits on the system board lengths.

The sweeps should cover all metrics, including minimum flight time, maximum flight time, and signal quality. Recommendations for the cases to cover are contained in Table 2 on page 17. The buffer corner refers to the I/O buffer process, voltage, and temperature conditions, as well as the core package and substrate trace conditions. These are reflected in the I/O models. In general, minimum flight time conditions occur with fast models for the I/O, package, substrate, and PCB. Fast I/O buffers typically supply maximum current and have the fastest rise and fall times. Fast packages and

PCBs correspond to minimum transmission line delay per unit length and maximum characteristic impedance. Conversely, maximum flight time conditions correspond to slow I/O and interconnect. For signal quality, the worst case conditions occur with fast I/O models and the maximum impedance mismatch between the processor substrate and system board.

The recommendations in Table 2 reflect the conditions described above.

The output from the sweeps should be analyzed using surface plots to determine the regions that meet specifications and those that do not. Each simulation case will result in a surface plot. To establish the working solution space, the plots must be logically overlaid to find the common space that meets all timing and signal quality specs. An example is shown in Figure 30

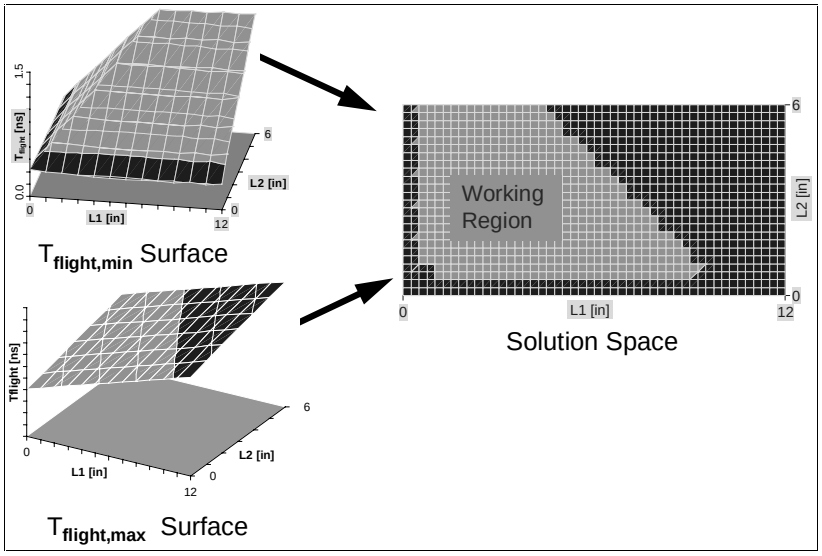


Figure 30. Solution space construction process

This type of analysis is best accomplished using a spreadsheet.

6.3.3. MONTE CARLO ANALYSIS

In Monte Carlo analysis, all system parameters varied at random across pre-established ranges. Monte Carlo analysis is useful for uncovering side effects that are not seen when only one or two parameters are varied. Thus, Monte Carlo analysis is used to refine the solution space, and to uncover any unexpected system behavior that merits additional analysis. Monte Carlo results are also best analyzed using a spreadsheet.

6.4. Placement & Layout

Once the pre-layout simulation is completed, route the board using the solution space resulting from the sensitivity analysis.

6.5. Post-Layout Simulation

Following layout, extract the traces and run simulations to verify that the layout meets timing and noise requirements. A small amount of trace "tuning" may be required, but experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required.

The post layout simulations should take into account the expected variation for all interconnect parameters. For timing simulations, use a V_{REF} of 2/3 V_{TT} ± 2% for both the processor and 440BX AGPset components. Flight times measured from the processor edge fingers to other system components use the standard flight time method.

6.5.1. CROSSTALK AND THE MULTI-BIT ADJUSTMENT FACTOR

Coupled lines should be included in the post-layout simulations. The flight times listed in Table 7 apply to single bit simulations only. They include an allowance for crosstalk. Crosstalk effects are accounted for as part of the multi-bit timing adjustment factor, T_{adj}, that is defined in Table 10. The recommended timing budget includes 400 ps for the adjustment factor.

Use caution in applying T_{adj} to coupled simulations. This adjustment factor encompasses other effects besides board coupling, such as processor and package crosstalk, and ground return inductance. In general, the additional delay introduced by coupled simulations should be less than 200 ps. Therefore multi-bit simulations should not be compared to the recommended flight time targets listed in Table 7. Instead, the system flight time limits should be determined by using the equations in Table 9 where the adjustment factor, T_{adj} is replaced by a separate factor to be determined by the designer to account for effects that are not able to be modeled by the multi-bit simulation.

6.6. Validation

6.6.1. FLIGHT TIME MEASUREMENT

The timings for the processors are specified at the processor edge fingers. In systems, the processor edges fingers are not readily accessible. In most cases, measurements must be taken at the system board solder connection to the SC242 connector. To effectively correlate delay measurements to values at the processor edge fingers, the SC242 connector delay must be incorporated.
Flight time is defined as the difference between the delay of a signal at the input of a receiving agent (measured at V_{REF}), and the delay at the output pin of the driving agent when driving the AGTL+ reference load (see section 4.3.1).

However, the driver delay into the reference load is not readily available, thus making flight time measurement unfeasible. There are three options for dealing with this limitation.

The first option is to subtract the delay of the driver in the system environment (at the SC242 connection to the board) from the delay at the receiver. Such a measurement will introduce uncertainty into the measurement due to differences between the driver delay in the reference and system loads. If simulations indicate that your design has margin to the flight time specifications, this approach will allow you to verify that the design is robust.

The second option is to subtract the simulated reference delay from the delay at the receiver. The limitation of this option is that there may be 1 ns or more of uncertainty between the actual driver delay and the results from a simulation. This approach is less accurate that the first option.

The final option is to simply use the measured delay from driver to receiver ($T_{measured}$) to validate that the system meets the setup and hold requirements. In this approach, the sum of the driver delay and the flight time must fit within the “valid window” for setup and hold. The timing requirements for satisfying the valid window are shown below:

Table 8. System Timing Requirements for Validating Setup/Hold Windows

Driver	Receiver	Equation
Processor	AGPset	$T_{measured} \geq T_{hold} + T_{skew,CLK} + T_{skew,PCB} + T_{clk,\max}$
		$T_{measured} \leq T_{cycle} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{jit} - T_{adj} + T_{clk,\min}$
AGPset	Processor	$T_{measured} \geq T_{hold} + T_{skew,CLK} + T_{skew,PCB} - T_{clk,\min}$
		$T_{measured} \leq T_{cycle} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{jit} - T_{adj} - T_{clk,\max}$
Processor	Processor	$T_{measured} \geq T_{hold} + T_{skew,CLK} + T_{skew,PCB}$
		$T_{measured} \leq T_{cycle} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{jit} - T_{adj}$

See Section 7 for a description of the timing terms and analysis method.

6.6.2. SIGNAL QUALITY MEASUREMENT

Signal integrity is specified at the processor core, which is not accessible. Intel has found that there can be substantial miscorrelation between ringback at the edge finger versus the core. The miscorrelation creates instances where a signal fails to satisfy ringback requirements at the edge finger, but passes the ringback specification at the core. For this reason, signal integrity is specified at the core. Ringback guidelines are supplied at the edge finger, as shown the processor datasheet. Any measurement at the edge finger that violates the guidelines should be simulated to verify that it meets the specification at the core.

7.0. TIMING ANALYSIS

To determine the available flight time window perform an initial timing analysis. Analysis of setup and hold conditions will determine the minimum and maximum flight time bounds for the host bus. Use the following equations to establish the system flight time limits:

Table 9. Processor and Intel 440BX AGPset System Timing Equations

Driver	Receiver	Equation
Processor	AGPset	$T_{flight,\min} \geq T_{hold} - T_{co,\min} + T_{skew,CLK} + T_{skew,PCB} + T_{clk,\max}$
		$T_{flight,\max} \leq T_{cycle} - T_{co,\max} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{jit} - T_{adj} + T_{clk,\min}$
AGPset	Processor	$T_{flight,\min} \geq T_{hold} - T_{co,\min} + T_{skew,CLK} + T_{skew,PCB} - T_{clk,\min}$
		$T_{flight,\max} \leq T_{cycle} - T_{co,\max} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{jit} - T_{adj} - T_{clk,\max}$
Processor	processor	$T_{flight,\min} \geq T_{hold} - T_{co,\min} + T_{skew,CLK} + T_{skew,PCB}$
		$T_{flight,\max} \leq T_{cycle} - T_{co,\max} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{jit} - T_{adj}$

The terms used in the equations are described below:

Table 10. Processors and Intel® 440BX AGPset System Timing Terms

Term	Description
T_{cycle}	System cycle time, defined as the reciprocal of the frequency
$T_{flight,min}$	Minimum system flight time. Flight time is defined in section 4.
$T_{flight,max}$	Maximum system flight time. Flight time is defined in section 4.
$T_{co,max}$	Maximum driver delay from input clock to output data.
$T_{co,min}$	Minimum driver delay from input clock to output data.
T_{su}	Minimum setup time. Defined as the time for which the input data must be valid prior to the input clock.
T_h	Minimum hold time. Defined as the time for which the input data must remain valid after the input clock.
$T_{skew,CLK}$	Clock generator skew. Defined as the maximum delay variation between output clock signals from the system clock generator.
$T_{skew,PCB}$	PCB skew. Defined as the maximum delay variation between clock signals due to system board variation and 440BX AGPset loading variation.
T_{jit}	Clock jitter. Defined as the maximum edge to edge variation in a given clock signal.
T_{adj}	Multi-bit timing adjustment factor. This term accounts for the additional delay that occurs in the network when multiple data bits switch in the same cycle. The adjustment factor includes such mechanisms as package and PCB crosstalk, high inductance current return paths, and simultaneous switching noise.
$T_{clk,min}$	Minimum clock substrate delay. Defined as the minimum adjustment factor that accounts for the delay of the clock trace on the processor substrate.
$T_{clk,max}$	Minimum clock substrate delay. Defined as the maximum adjustment factor that accounts for the delay of the clock trace on the processor substrate.

Notice that the timing equations include an extra term to account for the delay due to routing of the BCLK trace on the processor substrate from the processor edge fingers and the processor core. Adding the BCLK adjustment to the timing calculations between processor and chipset guarantees host clock synchronization between the AGPset and processor core. The minimum and maximum values for this term are contained in Table 11.

Component timings for the Pentium® II processor and 440BX AGPset are contained in Table 12. The timing specifications are contained in the Pentium II and 440BX AGPset datasheets. These timings are for reference only. **Pentium® III Processor timing is subset of the Pentium II processor, at 100MHz system bus.**

Table 11. Pentium® II processors and Intel® 440BX AGPset 100 MHz Timing Specifications

Timing Term	Pentium® II Processor	Intel® 440BX AGPset
$T_{co,max}$ [ns]	4.66	4.45
$T_{co,min}$ [ns]	0.71	0.80
T_{su} [ns]	1.97	3.00
T_{h} [ns]	1.61	-0.10
$T_{clk,min}$ [ns]	0.77	Not applicable
$T_{clk,max}$ [ns]	0.84	No applicable

Recommended values for system timings are contained in Table 12. Skew and jitter values for the clock generator device come from the CK97 clock driver specification. The PCB skew spec is based on the results of extensive simulations at Intel. The T_{adj} value is based on Intel's experience with systems that use the Pentium® Pro and Pentium II Processors.

Table 12. Recommended 100 MHz System Timing Parameters

Timing Term	Value
$T_{skew,CLK}$ [ns]	0.18
$T_{skew,PCB}$ [ns]	0.15
T_{jit} [ns]	0.25
T_{adj} [ns]	0.40

The flight time requirements that result from using the component timing specifications and recommended system timings are summarized in Table 7. All component values should be verified against the current specifications before proceeding with analysis.

8.0 CONCLUSION

GTL + routing requires a significant amount of effort. Planning ahead and leaving the necessary time available for correctly designing a board layout will allow a designer to avoid the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.

UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119
Tel: +1 408 765-8080

JAPAN, Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi, Ibaraki-ken 300-26
Tel: + 81-29847-8522

FRANCE, Intel Corporation S.A.R.L.
1, Quai de Grenelle, 75015 Paris
Tel: +33 1-45717171

UNITED KINGDOM, Intel Corporation (U.K.) Ltd.
Pipers Way, Swindon, Wiltshire, England SN3 1RJ
Tel: +44 1-793-641440

GERMANY, Intel GmbH
Dornacher Strasse 1
85622 Feldkirchen/ Muenchen
Tel: +49 89/99143-0

HONG KONG, Intel Semiconductor Ltd.
32/F Two Pacific Place, 88 Queensway, Central
Tel: +852 2844-4555

CANADA, Intel Semiconductor of Canada, Ltd.
190 Attwell Drive, Suite 500
Rexdale, Ontario M9W 6H8
Tel: +416 675-2438

Printed in USA/96/POD/PMG