Mobile Pentium® Processor with MMX™ Technology (0.25 Micron Process)

SmartDie® Product Specification

Preliminary

Product Features

- Support for MMX™ Technology
- Compatible with Large Software Base
  - MS-DOS*, Windows*, OS/2*, UNIX*
- 32-Bit CPU with 64-Bit Data Bus
- Superscalar Architecture
  - Enhanced pipelines
  - Two Pipelined Integer Units Capable of 2 Instructions/Clock
  - Pipelined MMX Technology
  - Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - 16-Kbyte Code, 16-Kbyte Write Back Data
  - MESI Cache Protocol
- 4-Mbyte Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Advanced Design Features
  - Deeper Write Buffers
  - Enhanced Branch Prediction Feature
  - Virtual Mode Extensions
- 0.25 Micron Process Technology
  - 1.8 V core supply (166/200/233 MHz)
  - 2.5 V I/O Interface (166/200/233 MHz)
- Internal Error Detection Features
- On-Chip Local APIC Controller
- Power Management Features
  - System Management Mode
  - Clock Control
- Fractional Bus Operation
  - 166-MHz Core/66-MHz Bus
  - 200-MHz Core/66-MHz Bus
  - 233-MHz Core/66-MHz Bus

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May, 1998

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1.0 Die Specifications

The die photo in Figure 1 and the plot in Figure 2 indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name "8PTMK" appears on the die. Table 1 describes the bond pad number and pad center data for each signal.

Figure 1. Mobile Pentium® Processor with MMX™ Technology Die Photo

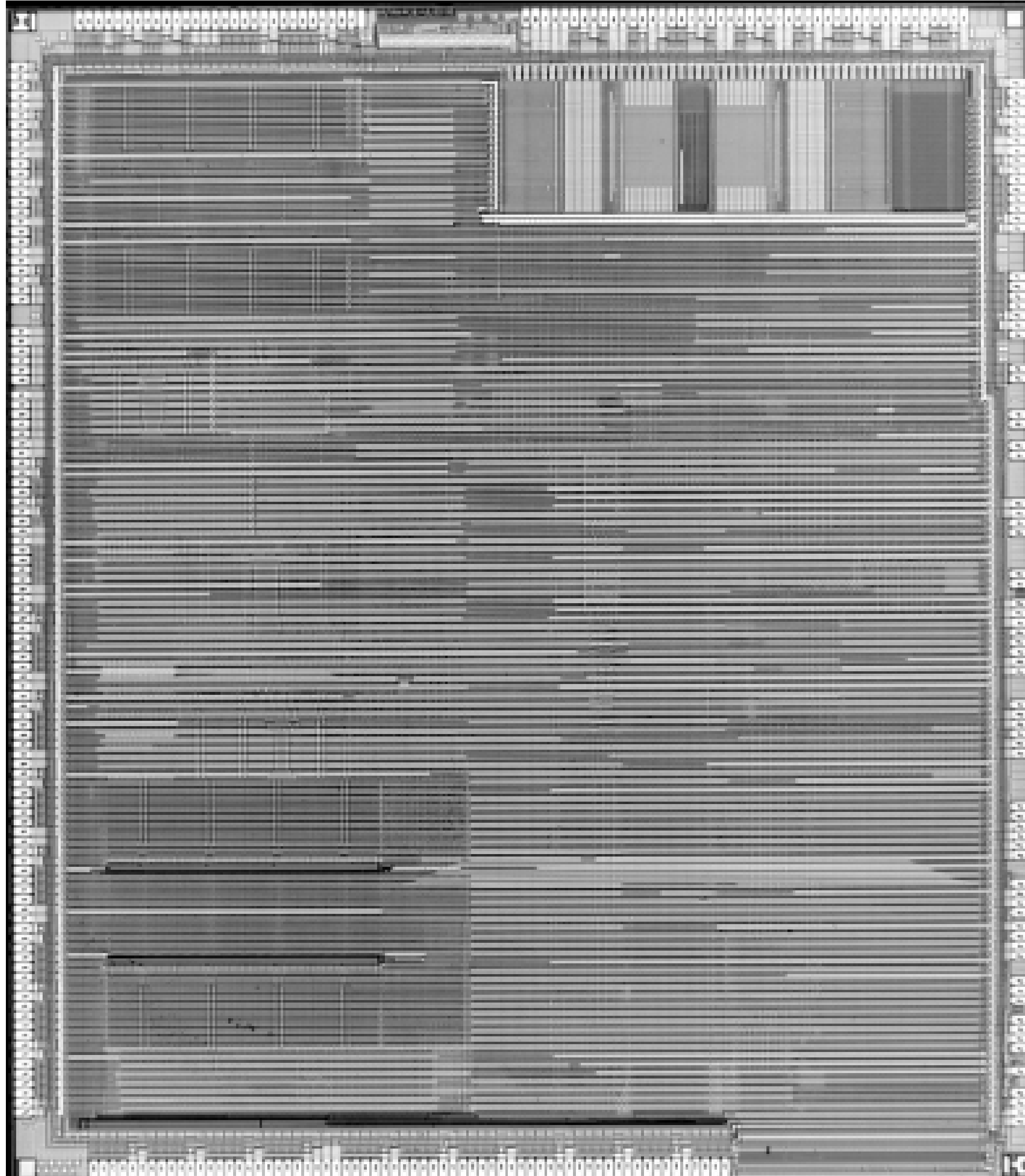

Figure 2. Mobile Pentium® Processor with MMX™ Technology Die/Bond Pad Layout

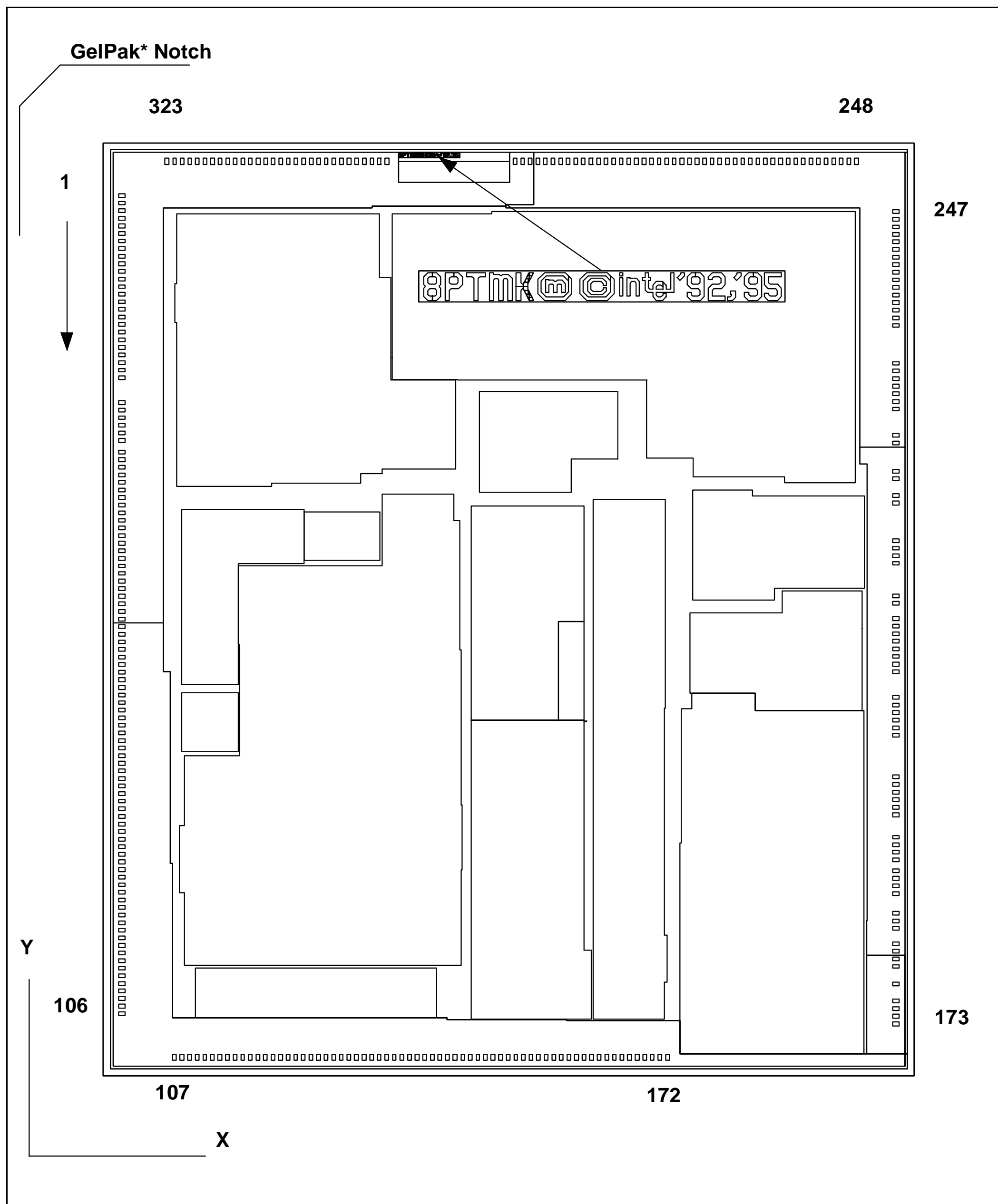

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 1 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
1	V_{CC3}	-171.573	182.490	-4357.97	4635.25
2	V_{SS}	-171.573	179.142	-4357.97	4550.22
3	LOCK#	-171.573	175.795	-4357.97	4465.20
4	V_{CC2}	-171.573	172.448	-4357.97	4380.18
5	V_{SS}	-171.573	169.100	-4357.97	4295.15
6	V_{CC3}	-171.573	165.753	-4357.97	4210.13
7	V_{SS}	-171.573	162.405	-4357.97	4125.10
8	AP	-171.573	159.058	-4357.97	4040.08
9	V_{CC2}	-171.573	155.711	-4357.97	3955.06
10	V_{SS}	-171.573	152.363	-4357.97	3870.03
11	HLDA	-171.573	149.016	-4357.97	3785.01
12	BREQ	-171.573	145.668	-4357.97	3699.98
13	V_{CC3}	-171.573	142.321	-4357.97	3614.96
14	V_{SS}	-171.573	138.974	-4357.97	3529.94
15	APCHK#	-171.573	135.626	-4357.97	3444.91
16	PCHK#	-171.573	132.279	-4357.97	3359.89
17	V_{CC2}	-171.573	128.931	-4357.97	3274.86
18	PRDY	-171.573	125.584	-4357.97	3189.84
19	SMIACT#	-171.573	122.237	-4357.97	3104.82
20	V_{SS}	-171.573	118.889	-4357.97	3019.79
21	V_{CC2}	-171.573	115.542	-4357.97	2934.77
22	V_{CC3}	-171.573	112.194	-4357.97	2849.74
23	V_{SS}	-171.573	108.847	-4357.97	2764.72
24	HOLD	-171.573	105.500	-4357.97	2679.70
25	WB/WT#	-171.573	102.152	-4357.97	2594.67
26	V_{CC2}	-171.573	91.186	-4357.97	2316.14
27	V_{SS}	-171.573	87.839	-4357.97	2231.12
28	NA#	-171.573	84.492	-4357.97	2146.10
29	BOFF#	-171.573	81.144	-4357.97	2061.07

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 2 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
30	BRDY#	-171.573	77.797	-4357.97	1976.05
31	V_{CC2}	-171.573	74.449	-4357.97	1891.02
32	V_{SS}	-171.573	69.328	-4357.97	1760.94
33	KEN#	-171.573	65.981	-4357.97	1675.92
34	AHOLD	-171.573	62.634	-4357.97	1590.90
35	INV	-171.573	59.286	-4357.97	1505.87
36	EWBE#	-171.573	55.939	-4357.97	1420.85
37	V_{CC2}	-171.573	52.591	-4357.97	1335.82
38	V_{SS}	-171.573	49.244	-4357.97	1250.80
39	V_{CC3}	-171.573	45.897	-4357.97	1165.78
40	V_{SS}	-171.573	42.549	-4357.97	1080.75
41	CACHE#	-171.573	39.202	-4357.97	995.73
42	M/IO#	-171.573	35.854	-4357.97	910.70
43	V_{CC3}	-171.573	32.507	-4357.97	825.68
44	V_{SS}	-171.573	29.160	-4357.97	740.66
45	BP3	-171.573	25.812	-4357.97	655.63
46	V_{SS}	-171.573	22.465	-4357.97	570.61
47	V_{CC2}	-171.573	19.117	-4357.97	485.58
48	BP2	-171.573	15.770	-4357.97	400.56
49	PM1/BP1	-171.573	12.423	-4357.97	315.54
50	PM0/BP0	-171.573	9.075	-4357.97	230.51
51	FERR#	-171.573	5.728	-4357.97	145.49
52	V_{SS}	-171.573	2.380	-4357.97	60.46
53	V_{CC2}	-171.573	-0.967	-4357.97	-24.56
54	IERR#	-171.573	-4.314	-4357.97	-109.58
55	V_{CC3}	-171.573	-7.662	-4357.97	-194.61
56	V_{SS}	-171.573	-11.009	-4357.97	-279.63
57	DP7	-171.573	-14.357	-4357.97	-364.66
58	D63	-171.573	-17.704	-4357.97	-449.68
59	D62	-171.573	-21.051	-4357.97	-534.70

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 3 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
60	D61	-171.573	-24.399	-4357.97	-619.73
61	V_{CC2}	-171.573	-27.746	-4357.97	-704.75
62	V_{SS}	-171.573	-31.094	-4357.97	-789.78
63	V_{CC3}	-171.573	-34.441	-4357.97	-874.80
64	V_{SS}	-171.573	-37.788	-4357.97	-959.82
65	D60	-171.573	-41.136	-4357.97	-1044.85
66	D59	-171.573	-44.483	-4357.97	-1129.87
67	D58	-171.573	-47.831	-4357.97	-1214.90
68	D57	-171.573	-51.178	-4357.97	-1299.92
69	V_{CC2}	-171.573	-54.525	-4357.97	-1384.94
70	V_{SS}	-171.573	-57.873	-4357.97	-1469.97
71	V_{CC3}	-171.573	-61.220	-4357.97	-1554.99
72	V_{SS}	-171.573	-64.568	-4357.97	-1640.02
73	D56	-171.573	-67.915	-4357.97	-1725.04
74	DP6	-171.573	-71.262	-4357.97	-1810.06
75	D55	-171.573	-74.610	-4357.97	-1895.09
76	D54	-171.573	-77.957	-4357.97	-1980.11
77	V_{CC2}	-171.573	-81.305	-4357.97	-2065.14
78	V_{SS}	-171.573	-84.652	-4357.97	-2150.16
79	V_{CC3}	-171.573	-87.999	-4357.97	-2235.18
80	V_{SS}	-171.573	-91.347	-4357.97	-2320.21
81	D53	-171.573	-94.694	-4357.97	-2405.23
82	D52	-171.573	-98.042	-4357.97	-2490.26
83	D51	-171.573	-101.389	-4357.97	-2575.28
84	D50	-171.573	-104.736	-4357.97	-2660.30
85	V_{CC2}	-171.573	-108.084	-4357.97	-2745.33
86	V_{SS}	-171.573	-111.431	-4357.97	-2830.35
87	V_{CC3}	-171.573	-114.779	-4357.97	-2915.38
88	V_{SS}	-171.573	-118.126	-4357.97	-3000.40
89	D49	-171.573	-121.473	-4357.97	-3085.42

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads: 181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 4 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
90	D48	-171.573	-124.821	-4357.97	-3170.45
91	DP5	-171.573	-128.168	-4357.97	-3255.47
92	D47	-171.573	-131.515	-4357.97	-3340.50
93	V_{CC3}	-171.573	-134.863	-4357.97	-3425.52
94	V_{SS}	-171.573	-138.210	-4357.97	-3510.54
95	D46	-171.573	-141.558	-4357.97	-3595.57
96	D45	-171.573	-144.905	-4357.97	-3680.59
97	D44	-171.573	-148.252	-4357.97	-3765.62
98	D43	-171.573	-151.600	-4357.97	-3850.64
99	V_{CC3}	-171.573	-154.947	-4357.97	-3935.66
100	V_{SS}	-171.573	-158.295	-4357.97	-4020.69
101	D42	-171.573	-161.642	-4357.97	-4105.71
102	D41	-171.573	-164.989	-4357.97	-4190.74
103	D40	-171.573	-168.337	-4357.97	-4275.76
104	DP4	-171.573	-171.684	-4357.97	-4360.78
105	V_{CC3}	-171.573	-175.032	-4357.97	-4445.81
106	V_{SS}	-171.573	-178.379	-4357.97	-4530.83
107	D39	-147.617	-198.454	-3749.49	-5040.75
108	D38	-144.270	-198.454	-3664.46	-5040.75
109	D37	-140.923	-198.454	-3579.44	-5040.75
110	D36	-137.575	-198.454	-3494.42	-5040.75
111	V_{CC3}	-134.228	-198.454	-3409.39	-5040.75
112	V_{SS}	-130.880	-198.454	-3324.37	-5040.75
113	D35	-127.533	-198.454	-3239.34	-5040.75
114	D34	-124.186	-198.454	-3154.32	-5040.75
115	D33	-120.838	-198.454	-3069.30	-5040.75
116	D32	-117.491	-198.454	-2984.27	-5040.75
117	V_{CC3}	-114.143	-198.454	-2899.25	-5040.75
118	V_{SS}	-110.796	-198.454	-2814.22	-5040.75
119	DP3	-107.449	-198.454	-2729.20	-5040.75

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 5 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
120	D31	-104.101	-198.454	-2644.18	-5040.75
121	D30	-100.754	-198.454	-2559.15	-5040.75
122	D29	-97.406	-198.454	-2474.13	-5040.75
123	V_{CC3}	-94.059	-198.454	-2389.10	-5040.75
124	V_{SS}	-90.712	-198.454	-2304.08	-5040.75
125	D28	-87.364	-198.454	-2219.06	-5040.75
126	D27	-84.017	-198.454	-2134.03	-5040.75
127	D26	-80.670	-198.454	-2049.01	-5040.75
128	D25	-77.322	-198.454	-1963.98	-5040.75
129	V_{CC3}	-73.975	-198.454	-1878.96	-5040.75
130	V_{SS}	-70.627	-198.454	-1793.94	-5040.75
131	V_{CC2}	-67.280	-198.454	-1708.91	-5040.75
132	V_{SS}	-63.933	-198.454	-1623.89	-5040.75
133	D24	-60.585	-198.454	-1538.86	-5040.75
134	DP2	-57.238	-198.454	-1453.84	-5040.75
135	D23	-53.890	-198.454	-1368.82	-5040.75
136	D22	-50.543	-198.454	-1283.79	-5040.75
137	V_{CC3}	-47.196	-198.454	-1198.77	-5040.75
138	V_{SS}	-43.848	-198.454	-1113.74	-5040.75
139	D21	-40.501	-198.454	-1028.72	-5040.75
140	D20	-37.153	-198.454	-943.70	-5040.75
141	D19	-33.806	-198.454	-858.67	-5040.75
142	D18	-30.459	-198.454	-773.65	-5040.75
143	V_{CC3}	-27.111	-198.454	-688.62	-5040.75
144	V_{SS}	-23.764	-198.454	-603.60	-5040.75
145	D17	-20.416	-198.454	-518.58	-5040.75
146	D16	-17.069	-198.454	-433.55	-5040.75
147	DP1	-13.722	-198.454	-348.53	-5040.75
148	D15	-10.374	-198.454	-263.50	-5040.75
149	V_{CC3}	-7.027	-198.454	-178.48	-5040.75

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 6 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
150	V_{SS}	-3.680	-198.454	-93.46	-5040.75
151	D14	-0.332	-198.454	-8.43	-5040.75
152	D13	3.015	-198.454	76.59	-5040.75
153	D12	6.363	-198.454	161.62	-5040.75
154	D11	9.710	-198.454	246.64	-5040.75
155	V_{CC3}	13.057	-198.454	331.66	-5040.75
156	V_{SS}	16.405	-198.454	416.69	-5040.75
157	D10	19.752	-198.454	501.71	-5040.75
158	D9	23.100	-198.454	586.74	-5040.75
159	D8	26.447	-198.454	671.76	-5040.75
160	DP0	29.794	-198.454	756.78	-5040.75
161	V_{CC3}	33.142	-198.454	841.81	-5040.75
162	V_{SS}	36.489	-198.454	926.83	-5040.75
163	D7	39.837	-198.454	1011.86	-5040.75
164	D6	43.184	-198.454	1096.88	-5040.75
165	D5	46.531	-198.454	1181.90	-5040.75
166	D4	49.879	-198.454	1266.93	-5040.75
167	V_{CC3}	53.226	-198.454	1351.95	-5040.75
168	V_{SS}	56.574	-198.454	1436.98	-5040.75
169	D3	59.921	-198.454	1522.00	-5040.75
170	D2	63.268	-198.454	1607.02	-5040.75
171	D1	66.616	-198.454	1692.05	-5040.75
172	D0	69.963	-198.454	1777.07	-5040.75
173	V_{CC2}	171.573	-182.835	4357.97	-4644.02
174	V_{SS}	171.573	-179.487	4357.97	-4558.99
175	PICCLK	171.573	-176.140	4357.97	-4473.97
176	PICD0	171.573	-172.793	4357.97	-4388.94
177	V_{CC2}	171.573	-165.270	4357.97	-4197.87
178	PICD1	171.573	-157.512	4357.97	-4000.82
179	V_{SS}	171.573	-154.165	4357.97	-3915.79

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 7 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
180	V_{CC3}	171.573	-150.817	4357.97	-3830.77
181(4)	TCK	171.573	-147.470	4357.97	-3745.74
182(4)	TDO	171.573	-140.774	4357.97	-3575.66
183(4)	TDI	171.573	-137.426	4357.97	-3490.64
184(4)	TMS	171.573	-134.079	4357.97	-3405.62
185	V_{CC2}	171.573	-125.314	4357.97	-3182.99
186	V_{SS}	171.573	-121.967	4357.97	-3097.97
187(4)	TRST#	171.573	-118.619	4357.97	-3012.94
188	V_{CC2}	171.573	-115.272	4357.97	-2927.92
189	N.C.	171.573	-110.511	4357.97	-2806.99
190	V_{SS}	171.573	-107.164	4357.97	-2721.97
191	V_{CC2}	171.573	-103.816	4357.97	-2636.94
192	N.C.	171.573	-100.469	4357.97	-2551.92
193	V_{SS}	171.573	-90.664	4357.97	-2302.86
194	V_{CC2}	171.573	-87.316	4357.97	-2217.84
195	V_{SS}	171.573	-83.969	4357.97	-2132.82
196	V_{CC2}	171.573	-80.621	4357.97	-2047.79
197	N.C.	171.573	-77.274	4357.97	-1962.77
198	N.C.	171.573	-73.927	4357.97	-1877.74
199	V_{SS}	171.573	-55.605	4357.97	-1412.37
200	V_{CC2}	171.573	-52.257	4357.97	-1327.34
201	V_{CC3}	171.573	-48.910	4357.97	-1242.32
202	V_{SS}	171.573	-45.563	4357.97	-1157.30
203	V_{CC2}	171.573	-42.215	4357.97	-1072.27
204	STPCLK#	171.573	-38.868	4357.97	-987.25
205	V_{SS}	171.573	-27.512	4357.97	-698.80
206	V_{CC2}	171.573	-24.165	4357.97	-613.78
207	BF2	171.573	-20.817	4357.97	-528.75
208	BF1	171.573	-17.470	4357.97	-443.73
209	BF0	171.573	-14.122	4357.97	-358.70

NOTES:

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3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads: 181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 8 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
210	V_{SS}	171.573	-10.775	4357.97	-273.68
211	V_{CC2}	171.573	-7.428	4357.97	-188.66
212	V_{SS}	171.573	-4.080	4357.97	-103.63
213	V_{CC2}	171.573	2.615	4357.97	66.42
214	PEN#	171.573	5.962	4357.97	151.44
215	INIT	171.573	20.270	4357.97	514.86
216	IGNNE#	171.573	23.618	4357.97	599.89
217	V_{SS}	171.573	26.965	4357.97	684.91
218	V_{CC2}	171.573	30.313	4357.97	769.94
219	SMI#	171.573	46.857	4357.97	1190.16
220	INTR/LINT0	171.573	50.204	4357.97	1275.18
221	R/S#	171.573	57.563	4357.97	1462.10
222	NMI/LINT1	171.573	60.910	4357.97	1547.12
223	A21	171.573	73.352	4357.97	1863.15
224	A22	171.573	76.700	4357.97	1948.18
225	A23	171.573	88.367	4357.97	2244.53
226	V_{SS}	171.573	91.714	4357.97	2329.55
227	V_{CC3}	171.573	95.062	4357.97	2414.58
228	A24	171.573	98.409	4357.97	2499.60
229	A25	171.573	101.756	4357.97	2584.62
230	A26	171.573	105.104	4357.97	2669.65
231	A27	171.573	108.451	4357.97	2754.67
232	V_{SS}	171.573	125.195	4357.97	3179.95
233	V_{CC3}	171.573	128.542	4357.97	3264.98
234	A28	171.573	131.890	4357.97	3350.00
235	A29	171.573	135.237	4357.97	3435.02
236	A30	171.573	138.584	4357.97	3520.05
237	A31	171.573	141.932	4357.97	3605.07
238	V_{SS}	171.573	145.279	4357.97	3690.10
239	V_{CC3}	171.573	148.626	4357.97	3775.12

NOTES:

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   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
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Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 9 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
240	V_{CC2}	171.573	151.974	4357.97	3860.14
241	V_{SS}	171.573	155.321	4357.97	3945.17
242	A3	171.573	158.669	4357.97	4030.19
243	V_{SS}	171.573	162.016	4357.97	4115.22
244	V_{CC3}	171.573	165.363	4357.97	4200.24
245	A4	171.573	168.711	4357.97	4285.26
246	A5	171.573	172.058	4357.97	4370.29
247	V_{SS}	171.573	175.406	4357.97	4455.31
248	V_{CC2}	153.315	198.454	3894.22	5040.75
249	V_{CC3}	149.968	198.454	3809.20	5040.75
250	A6	146.621	198.454	3724.18	5040.75
251	A7	143.273	198.454	3639.15	5040.75
252	V_{SS}	139.926	198.454	3554.13	5040.75
253	V_{CC3}	136.578	198.454	3469.10	5040.75
254	A8	133.231	198.454	3384.08	5040.75
255	V_{CC2}	129.884	198.454	3299.06	5040.75
256	V_{SS}	126.536	198.454	3214.03	5040.75
257	A9	123.189	198.454	3129.01	5040.75
258	V_{SS}	119.841	198.454	3043.98	5040.75
259	V_{CC3}	116.494	198.454	2958.96	5040.75
260	A10	113.147	198.454	2873.94	5040.75
261	A11	109.799	198.454	2788.91	5040.75
262	V_{SS}	106.452	198.454	2703.89	5040.75
263	V_{CC2}	103.105	198.454	2618.86	5040.75
264	V_{CC3}	99.757	198.454	2533.84	5040.75
265	A12	96.410	198.454	2448.82	5040.75
266	V_{CC2}	93.062	198.454	2363.79	5040.75
267	V_{SS}	89.715	198.454	2278.77	5040.75
268	A13	86.368	198.454	2193.74	5040.75
269	V_{SS}	83.020	198.454	2108.72	5040.75

NOTES:

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   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
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Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 10 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
270	V_{CC3}	79.673	198.454	2023.70	5040.75
271	A14	76.325	198.454	1938.67	5040.75
272	V_{CC2}	72.978	198.454	1853.65	5040.75
273	V_{SS}	69.631	198.454	1768.62	5040.75
274	A15	66.283	198.454	1683.60	5040.75
275	V_{SS}	62.936	198.454	1598.58	5040.75
276	V_{CC3}	59.588	198.454	1513.55	5040.75
277	A16	56.241	198.454	1428.53	5040.75
278	A17	52.894	198.454	1343.50	5040.75
279	V_{SS}	49.546	198.454	1258.48	5040.75
280	V_{CC2}	46.199	198.454	1173.46	5040.75
281	V_{CC3}	42.851	198.454	1088.43	5040.75
282	A18	39.504	198.454	1003.41	5040.75
283	V_{CC2}	36.157	198.454	918.38	5040.75
284	V_{SS}	32.809	198.454	833.36	5040.75
285	A19	29.462	198.454	748.34	5040.75
286	V_{SS}	26.115	198.454	663.31	5040.75
287	V_{CC3}	22.767	198.454	578.29	5040.75
288	A20	19.420	198.454	493.26	5040.75
289	V_{CC2}	16.072	198.454	408.24	5040.75
290	V_{SS}	12.725	198.454	323.22	5040.75
291	V_{CC2}	9.378	198.454	238.19	5040.75
292	V_{SS}	6.030	198.454	153.17	5040.75
293	RESET	2.683	198.454	68.14	5040.75
294	N.C.	-53.793	198.454	-1366.35	5040.75
295	CLK	-57.141	198.454	-1451.38	5040.75
296	SCYC	-60.488	198.454	-1536.40	5040.75
297	V_{SS}	-63.835	198.454	-1621.42	5040.75
298	V_{CC3}	-67.183	198.454	-1706.45	5040.75
299	BE7#	-70.530	198.454	-1791.47	5040.75

NOTES:

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4. Boundary Scan (JTAG) is implemented through the following pads:
   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

Table 1. Mobile Pentium® Processor with MMX™ Technology Bond Pad Center Data (Sheet 11 of 11)

PAD#	SIGNAL(2,3,5)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
300	BE6#	-73.878	198.454	-1876.50	5040.75
301	BE5#	-77.225	198.454	-1961.52	5040.75
302	BE4#	-80.572	198.454	-2046.54	5040.75
303	V_{SS}	-83.920	198.454	-2131.57	5040.75
304	V_{CC3}	-87.267	198.454	-2216.59	5040.75
305	BE3#	-90.615	198.454	-2301.62	5040.75
306	BE2#	-93.962	198.454	-2386.64	5040.75
307	BE1#	-97.309	198.454	-2471.66	5040.75
308	BE0#	-100.657	198.454	-2556.69	5040.75
309	A20M#	-104.004	198.454	-2641.71	5040.75
310	FLUSH#	-107.352	198.454	-2726.74	5040.75
311	BUSCHK#	-110.699	198.454	-2811.76	5040.75
312	W/R#	-114.046	198.454	-2896.78	5040.75
313	V_{SS}	-117.394	198.454	-2981.81	5040.75
314	V_{CC3}	-120.741	198.454	-3066.83	5040.75
315	HIT#	-124.089	198.454	-3151.86	5040.75
316	HITM#	-127.436	198.454	-3236.88	5040.75
317	V_{SS}	-130.783	198.454	-3321.90	5040.75
318	V_{CC3}	-134.131	198.454	-3406.93	5040.75
319	ADS#	-137.478	198.454	-3491.95	5040.75
320	EADS#	-140.826	198.454	-3576.98	5040.75
321	D/C#	-144.173	198.454	-3662.00	5040.75
322	PWT	-147.520	198.454	-3747.02	5040.75
323	PCD	-150.868	198.454	-3832.05	5040.75

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   181 (TCK), 182 (TDO), 183 (TDI), 184 (TMS), 187 (TRST#)
5. FRCMC# - Can use an external pull-up for compatibility with other Pentium processors.

2.0 Intel Die Products Processing

2.1 Test Procedure

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

Next, full-speed functional testing is performed at the die level for SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

2.2 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts completely through the wafer.

2.3 Die Inspection

Upon completion of test, the die undergo visual inspection. This process is the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.4 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Assembly Process Order / Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

Note: GEL-PAKs require a Vacuum Release Station. Contact Vichem* Corporation for more information.

2.5 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.6 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.7 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 Specifications

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Table 2 defines Mobile Pentium® Processor with MMX™ Technology physical specifications.

Table 2. Mobile Pentium® Processor with MMX™ Technology Physical Specifications

Die Revision:	A-0 Step
Post-Saw Die Dimensions:	Mils: X = 356.8 ± 0.5, Y= 410.4 ± 0.5 See associated Die/Bond Pad Layout for X, Y orientation.
Die Thickness:	17 ± 1 mils
Minimum Pad Pitch:	85 microns (3.346 mils)
Pad Passivation Opening Size:	Mils: 2.594 x 5.552 (single pads) Microns: 65.89 x 141.02 (single pads)
Bond Pad Metallization: (outermost layer first)	17,850 Angstroms Aluminum (0.5% Copper), 1000 Angstroms Titanium
Pads per Die:	323
Die Backside Material: (outermost layer first)	1600 Angstroms Gold, 345 Angstroms Titanium
Passivation: (outermost layer first)	3.3 microns polyimide, 0.75 microns nitride
Intel Fabrication Process:	CMOS (min. feature size 0.25 microns)

NOTE: The die specifications provided are valid for A-step die only.

3.2 DC Specifications

Note: This product specification contains preliminary information on new products in production. These specifications are subject to change without notice.Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.2.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.

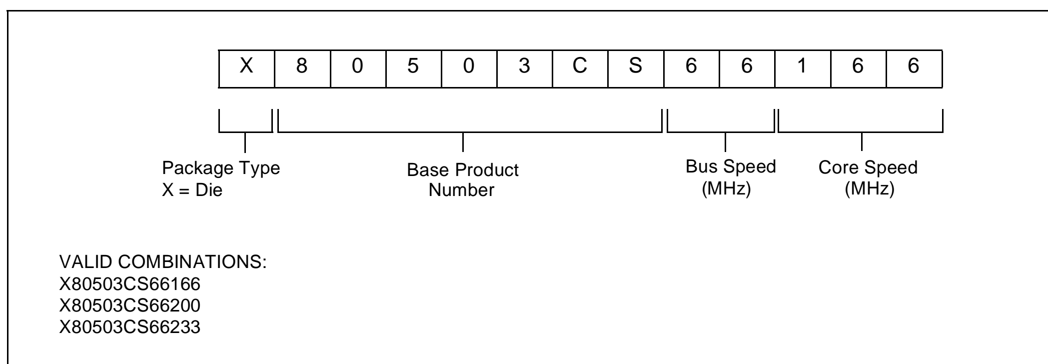
GEL-PAK Storage Temperature	0°C to +70°C
Junction Temperature Under Bias	-65°C to +110°C
3 V Supply Voltage wrt. V_{SS}	-0.5 V to +4.6 V
2.9 V Supply Voltage wrt. V_{SS}	-0.5 V to +3.7 V
3 V Only Buffer DC Input Voltage	-0.5 V to V_{CC3} + 0.5 V; not to exceed V_{CC3} max

3.2.2 Operating Conditions

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

V_{CC3} (I/O Supply Voltage)	2.5 V ± 0.125 V
V_{CC2} (Core Supply Voltage)	1.8 V ± 0.135 V at 166, 200, and 233 MHz
T_J (Junction Temperature Under Bias)	0°C to 105°C average die surface temperature
Substrate Bias	Float (Self Biasing to V_{SS}), Alternative is to drive V_{SS}
Core Operating Frequency	166 MHz, 200 MHz, 233 MHz (66 MHz Bus)

4.0 Device Nomenclature



5.0 Reference Information

Document Title	Order #
Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron datasheet	243468

6.0 Revision History

Revision	Date	Description
002	5/98	Revised Pad 31 definition in Table 1 and Post-Saw Die Dimensions in Table 2.
001	1/98	Initial release.