NEC

MOS INTEGRATED CIRCUIT

μPD705102

V832™
32-BIT MICROPROCESSOR

DESCRIPTION

The μPD705102 (V832) is a 32-bit RISC microprocessor for embedded control applications, with a high-performance 32-bit V830™ processor core and many peripheral functions such as a SDRAM/ROM controller, 4-channel DMA controller, real-time pulse unit, serial interface, interrupt controller, and power management.

In addition to high interrupt response speed and optimized pipeline structure, the V832 offers sum-of-products operation instructions, concatenated shift instructions, and high-speed branch instructions to realize multimedia functions, and therefore can provide high performance in multimedia systems such as Internet/intra-net systems, car navigation systems, digital still cameras, and color faxes.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V832 User's Manual — Hardware: U13577E
V830 Family™ User's Manual — Architecture: U12496E

FEATURES

- CPU function
  - V830-compatible instructions
  - Instruction cache: 4 Kbytes
  - Instruction RAM: 4 Kbytes
  - Data cache: 4 Kbytes
  - Data RAM: 4 Kbytes
  - Minimum number of instruction execution cycles: 1 cycle
  - Number of general purpose registers: 32 bits × 32
  - Memory space and I/O space: 4 Gbytes each
- Interrupt/exception processing function
  - Non-maskable: External input: 1
  - Maskable: External input: 8 (of which 4 are multiplexed with internal sources)
    Internal source: 11 types
- Bus control function
- Wait control function
- Memory access control function
- DMA controller: 4 channels
- Serial interface function
  - Asynchronous serial interface (UART): 1 channel
  - Clocked serial interface (CSI): 1 channel
  - Dedicated baud rate generator (BRG): 1 channel
- Timer/counter function
  - 16-bit timer/event counter: 1 channel
  - 16-bit interval timer: 1 channel
- Port function: 21 I/O ports
- Clock generation function: PLL clock synthesizer (6× or 8× multiplication)
- Standby function: HALT, STOP, and power management modes
- Debug function
  - Debug-dedicated synchronous serial interface: 1 channel
  - Trace-dedicated interface: 1 channel

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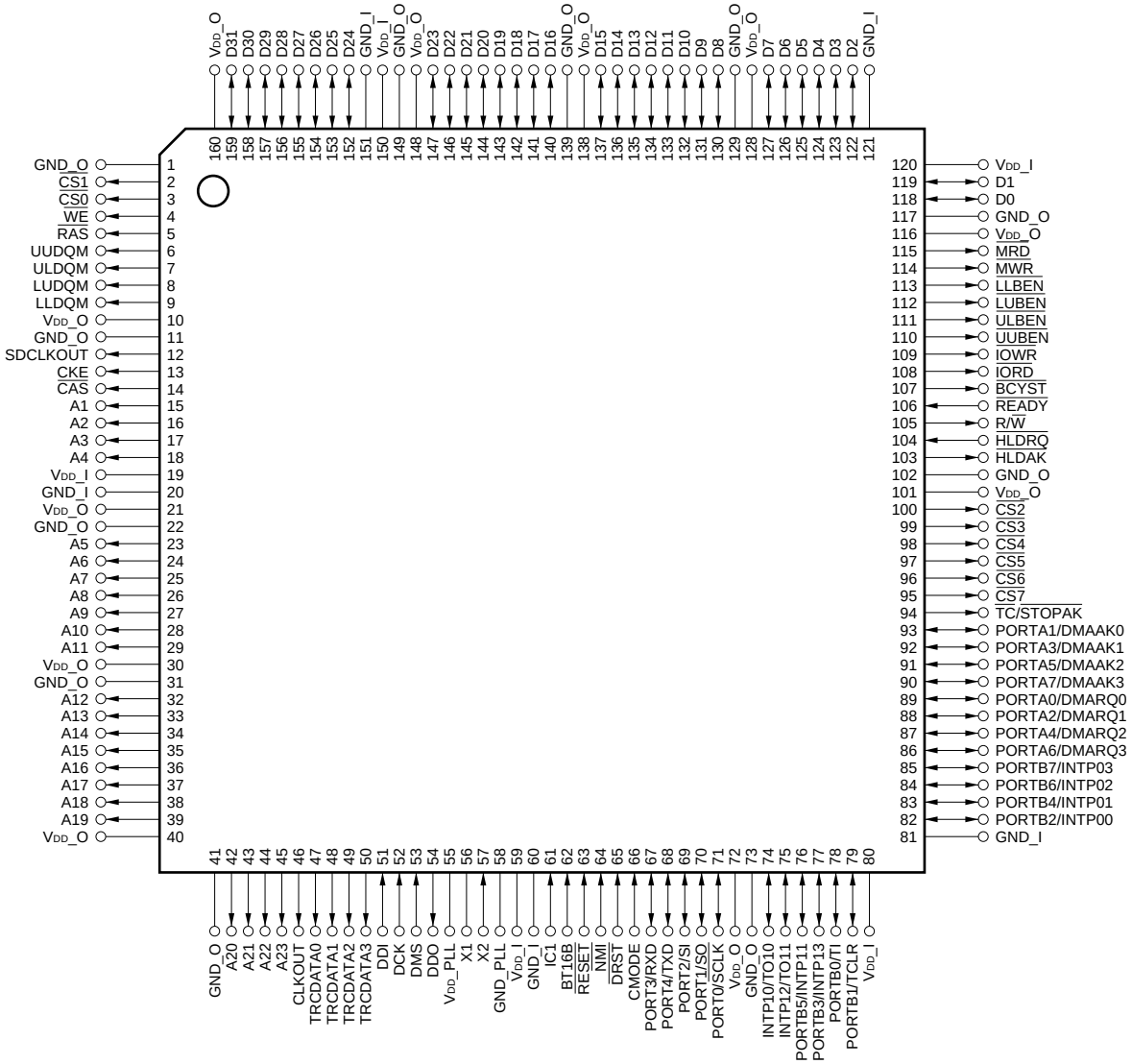
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD705102GM-143-8ED	160-pin plastic LQFP (fine pitch) (24 × 24 mm)
★ μPD705102GM-133-8ED	160-pin plastic LQFP (fine pitch) (24 × 24 mm)

PIN CONFIGURATION (TOP VIEW)

- **160-pin plastic LQFP (fine pitch) (24 × 24 mm)**
  μPD705102GM-143-8ED
- ★ **μPD705102GM-133-8ED**

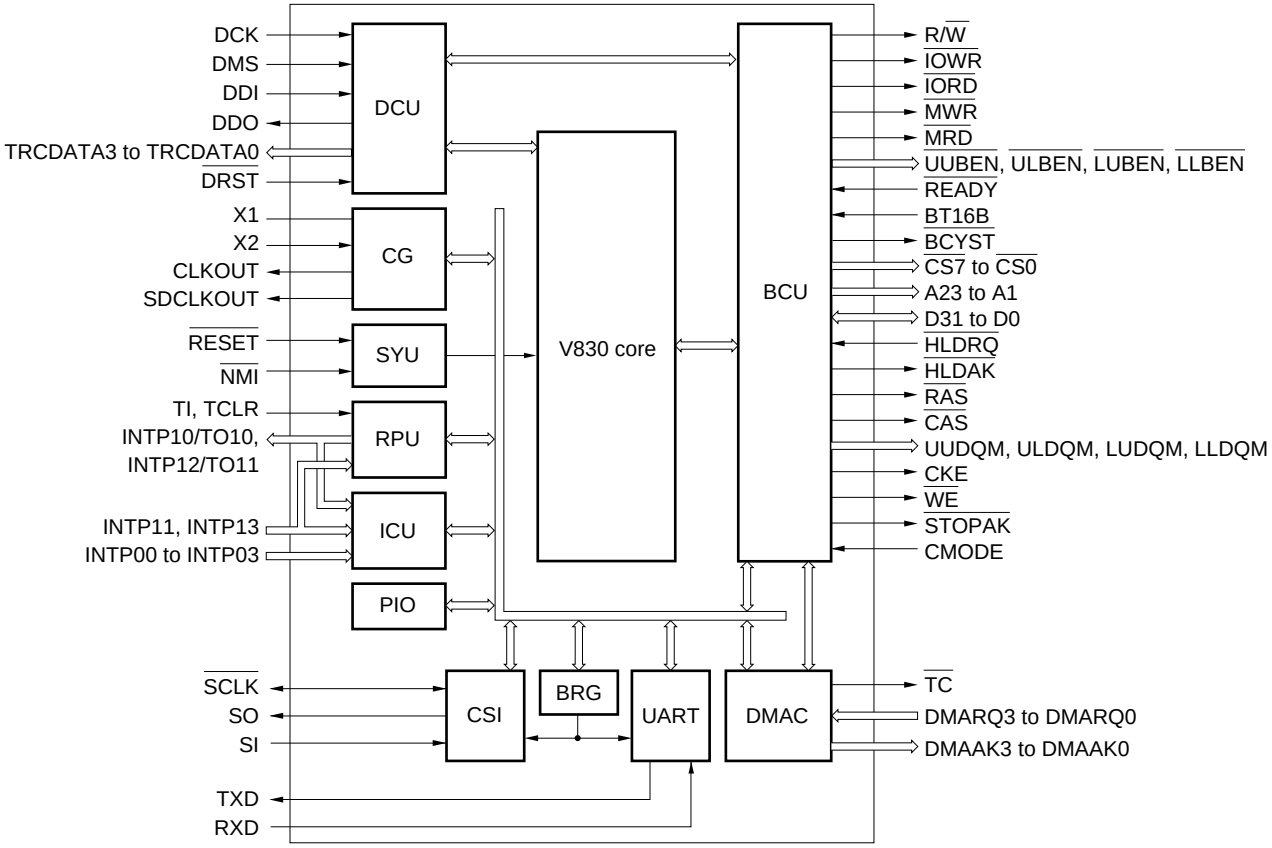


Caution Directly connect the IC1 (Internally connected 1) pin to GND_O.

PIN NAMES

A1 to A23: Address Bus
$\overline{BCYST}$: Bus Cycle Start
BT16B: Boot Bus Size 16-bit
$\overline{CAS}$: Column Address Strobe
CKE: Clock Enable
CLKOUT: Clock Out
CMODE: Clock Mode
$\overline{CS0}$ to $\overline{CS7}$: Chip Select
D0 to D31: Data Bus
DCK: Debug Clock
DDI: Debug Data Input
DDO: Debug Data Output
DMAAK0 to DMAAK3: DMA Acknowledge
DMARQ0 to DMARQ3: DMA Request
DMS: Debug Mode Select
$\overline{DRST}$: Debug Reset
GND_I: Ground
GND_O: Ground
GND_PLL: PLL Ground
$\overline{HLDAK}$: Hold Acknowledge
$\overline{HLDRQ}$: Hold Request
IC1: Internally Connected
INTP00 to INTP03, INTP10 to INTP13: Interrupt Request From Peripheral
$\overline{IORD}$: I/O Read
$\overline{IOWR}$: I/O Write
$\overline{LLBEN}$: Lower Lower Byte Enable
LLDQM: Lower Lower DQ Mask enable
$\overline{LUBEN}$: Lower Upper Byte Enable
LUDQM: Lower Upper DQ Mask enable
$\overline{MRD}$: Memory Read
$\overline{MWR}$: Memory Write
$\overline{NMI}$: Non-Maskable Interrupt Request
PORT0 to PORT4, PORTA0 to PORTA7, PORTB0 to PORTB7: Port
R/$\overline{W}$: Bus Read or Write Status
$\overline{RAS}$: Row Address Strobe
$\overline{READY}$: Ready
$\overline{RESET}$: Reset
RXD: Receive Data
$\overline{SCLK}$: Serial Clock
SDCLKOUT: SDRAM Clock Out
SI: Serial Input
SO: Serial Output
$\overline{STOPAK}$: Stop Acknowledge
$\overline{TC}$: Terminal Count
TCLR: Timer Clear
TI: Timer Input
TO10, TO11: Timer Output
TRCDATA0 to TRCDATA3: Trace Data
TXD: Transmit Data
$\overline{ULBEN}$: Upper Lower Byte Enable
ULDQM: Upper Lower DQ Mask enable
$\overline{UUBEN}$: Upper Upper Byte Enable
UUDQM: Upper Upper DQ Mask enable
V_{DD}_I: Power Supply (2.5 V)
V_{DD}_O: Power Supply (3.3 V)
V_{DD}_PLL: PLL Power Supply (2.5 V)
$\overline{WE}$: Write Enable
X1, X2: Crystal Oscillator

INTERNAL BLOCK DIAGRAM



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1. PIN FUNCTIONS

1.1 Port Pins

Pin Name	I/O	Function	Alternate Function
PORT0	Schmitt I/O	PORT 5-bit input/output port. Input/output can be specified in 1-bit units.	$\overline{\text{SCLK}}$
PORT1	I/O		SO
PORT2	Schmitt I/O		SI
PORT3			RXD
PORT4	I/O		TXD
PORTA0	I/O	PORTA 8-bit input/output port. Input/output can be specified in 1-bit units.	DMARQ0
PORTA1			DMAAK0
PORTA2			DMARQ1
PORTA3			DMAAK1
PORTA4			DMARQ2
PORTA5			DMAAK2
PORTA6			DMARQ3
PORTA7			DMAAK3
PORTB0	I/O	PORTB 8-bit input/output port. Input/output can be specified in 1-bit units.	TI
PORTB1			TCLR
PORTB2			INTP00
PORTB3			INTP13
PORTB4			INTP01
PORTB5			INTP11
PORTB6			INTP02
PORTB7			INTP03

1.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
D0 to D31	3-state I/O	Data bus	—
A1 to A23	3-state output	Address bus	—
$\overline{\text{READY}}$	Input	End of bus cycle enable	—
$\overline{\text{HLDRQ}}$	Input	Bus hold request	—
$\overline{\text{HLDAK}}$	Output	Bus hold enable	—
$\overline{\text{MRD}}$	3-state output	Memory read strobe	—
$\overline{\text{UUBEN}}$		Byte enable output (most significant byte: D31 to D24)	—
$\overline{\text{ULBEN}}$		Byte enable output (enables second byte: D23 to D16)	—
$\overline{\text{LUBEN}}$		Byte enable output (enables third byte: D15 to D8)	—
$\overline{\text{LLBEN}}$		Byte enable output (enables least significant byte: D7 to D0)	—
$\overline{\text{IORD}}$		I/O read strobe	—
$\overline{\text{IOWR}}$		I/O write strobe	—
$\overline{\text{MWR}}$		Memory write strobe	—
BT16B	Input	$\overline{\text{CS7}}$ space bus size setting	—
$\overline{\text{BCYST}}$	3-state output	Bus cycle start output	—
R/$\overline{\text{W}}$		R/W output	—
$\overline{\text{RESET}}$	Input	Reset input	—
X1	—	Crystal resonator connection (open when external clock input)	—
X2	Schmitt input	Crystal resonator connection/external clock input	—
CLKOUT	Output	Bus clock output	—
CMODE	Input	PLL multiplication factor setting (×6, ×8)	—
$\overline{\text{CS2}}$, $\overline{\text{CS7}}$	3-state output	Memory chip select output	—
$\overline{\text{CS3}}$ to $\overline{\text{CS6}}$		Memory I/O chip select output	—
$\overline{\text{STOPAK}}$	Output	STOP mode report output	$\overline{\text{TC}}$
INTP10	Input	Maskable interrupts	TO10
INTP11			PORTB5
INTP12			TO11
INTP13			PORTB3
INTP00			PORTB2
INTP01			PORTB4
INTP02			PORTB6
INTP03			PORTB7
$\overline{\text{NMI}}$		Non-maskable interrupt	—
$\overline{\text{RAS}}$	3-state output	SDRAM $\overline{\text{RAS}}$ strobe	—
UUDQM		DQ mask enable (most significant byte: D31 to D24)	—
ULDQM		DQ mask enable (second byte: D23 to D16)	—
LUDQM		DQ mask enable (third byte: D15 to D8)	—
LLDQM		DQ mask enable (least significant byte: D7 to D0)	—

(2/2)

Pin Name	I/O	Function	Alternate Function
$\overline{WE}$	3-state output	SDRAM write strobe	—
$\overline{CAS}$		SDRAM $\overline{CAS}$ strobe	—
$\overline{CS0}$		SDRAM chip select	—
$\overline{CS1}$		SDRAM/SRAM (ROM) chip select	—
CKE		SDRAM clock enable	—
SDCLKOUT	Output	SDRAM clock output	—
DMARQ0	Input	DMA requests (CH0 to CH3)	PORTA1
DMARQ1			PORTA3
DMARQ2			PORTA5
DMARQ3			PORTA7
DMAAK0	Output	DMA enable (CH0 to CH3)	PORTA0
DMAAK1			PORTA2
DMAAK2			PORTA4
DMAAK3			PORTA6
$\overline{TC}$		DMA transfer end output	$\overline{STOPAK}$
TO10		Timer 1 output	INTP10
TO11			INTP12
TCLR	Input	Timer 1 clear, start input	PORTB1
TI		Timer 1 count clock input	PORTB0
RXD	Schmitt input	UART data input	PORT3
TXD	Output	UART data output	PORT4
$\overline{SCLK}$	Schmitt I/O	CSI clock I/O	PORT0
SI	Schmitt input	CSI data input	PORT2
SO	Output	CSI data output	PORT1
DCK	Schmitt input	Debug clock input	—
DDI	Input	Debug data input	—
DDO	Output	Debug data output	—
DMS	Input	Debug mode select	—
$\overline{DRST}$		DCU reset input	—
TRCDATA0 to TRCDATA3	Output	Trace data output	—
V_{DD}_I	—	Positive power supply (2.5 V)	—
V_{DD}_O		Positive power supply (3.3 V)	—
GND_I		Ground (2.5 V)	—
GND_O		Ground (3.3 V)	—
V_{DD}_PLL		PLL (internal clock generator) positive power supply (2.5 V)	—
GND_PLL		PLL (internal clock generator) ground potential (2.5 V)	—

2. INTERNAL UNITS

(1) Bus control unit (BCU)

Controls the address bus, data bus, and control bus pins. The major functions of BCU are as follows:

(a) Bus arbitration

Arbitrates the bus mastership among bus masters (CPU, SDRAMC, DMAC, and external bus masters). The bus mastership can be changed after completion of the bus cycle under execution, and in an idle state.

(b) Wait control

Controls eight areas in the 16-Mbyte space corresponding to eight chip select signals ($\overline{CS0}$ through $\overline{CS7}$). Generates chip select signals, controls wait states, and selects the type of bus cycle.

(c) SDRAM controller

Generates commands and controls access to SDRAM. CAS latency is 2 only.

(d) ROM controller

Accessing ROM with page access function is supported. The bus cycle immediately before and addresses are compared, and wait states are controlled in the normal access (off-page) or page access (on-page) modes. A page width of 8 bytes to 16 bytes can be supported.

(2) Interrupt controller (ICU)

Services maskable interrupt requests (INTP00 through INTP03, and INTP10 through INTP13) from internal peripheral hardware and external sources. The priorities of these interrupt requests can be specified in units of four groups, and edge-triggered or level-triggered interrupts can be nested.

(3) DMA controller (DMAC)

Transfers data between memory and I/O in place of CPU. The transfer type is 2-cycle transfer. Two transfer modes, single transfer and demand transfer, are available.

(4) Serial interface (UART/CSI/BRG)

One asynchronous serial interface (UART) channel and one clocked serial interface (CSI) channel is provided. As the serial clock source, the output of the baud rate generator (BRG) and the bus clock can be selected.

(5) Real-time pulse unit (RPU)

Provides timer/counter functions. The on-chip 16-bit timer/event counter and 16-bit interval timer can be used to calculate pulse intervals and frequencies, and to output programmable pulses.

(6) Clock generator (CG)

A frequency six or eight times higher than that of the resonator connected to the X1 and X2 pins is supplied as the operating clock of the CPU. In addition, both a bus clock, which functions as the operating clock of the peripheral units, and SDCLKOUT, which functions as an operating clock, are supplied from the CLKOUT pin. An external clock can be also input instead of connecting a resonator.

For reducing the power consumption, the function switching the frequencies of the CPU clock and bus clock with power management control (PMC) is provided.

(7) Port (PIO)

Provides port functions. Twenty-one I/O ports are available. The pins of these ports can be used as port pins or other function pins.

(8) System control unit (SYU)

A circuit that eliminates noise on the $\overline{\text{RESET}}$ signal (input)/$\overline{\text{NMI}}$ signal (input) is provided.

(9) Debug control unit (DCU)

A circuit to realize mapping and trace functions is provided to implement basic debugging functions.

3. CPU FUNCTION

The features of the CPU function are as follows:

- High-performance 32-bit architecture for embedded control applications
  - Cache memory
    Instruction cache: 4 Kbytes
    Data cache: 4 Kbytes
  - Internal RAM
    Instruction RAM: 4 Kbytes
    Data RAM: 4 Kbytes
  - 1-clock pitch pipeline structure
  - 16-/32-bit length instruction format
  - Address/data separated type bus
  - 4-Gbyte linear address
  - Thirty-two 32-bit general registers
  - Register/flag hazard interlock is handled by hardware
  - 16 levels of interrupt response
- 16-bit bus fixed function
  - 16-bit bus system can be constructed
- Ideal instructions for any application field:
  - Sum-of-products operation
  - Saturation operation
  - Branch prediction
  - Concatenation shift
  - Block transfer instruction

4. INTERRUPT/EXCEPTION PROCESSING FUNCTION

The features of the interrupt/exception processing function are as follows:

- Interrupt
  - Non-maskable interrupt: 1 source
  - Maskable interrupt: 15 sources
  - Priority of the programmable interrupt can be specified in four levels
  - Nesting interrupt can be controlled according to the priority
  - Mask can be specified for each maskable interrupt request
  - Valid edge of an external interrupt request can be specified
  - Noise elimination circuit provided for the non-maskable interrupt pin ($\overline{NMI}$)
- Exception
  - Software exception: 32 sources
  - Exception trap: 4 sources

The interrupt/exception sources are shown in Tables 4-1 and 4-2.

Table 4-1. Reset/Non-maskable Interrupt/Exception Source List

Type	Classification	Source of Interrupt/Exception		Exception Code (ECR)	Handler Address	Restore PC[Note 2]
		Name[Note 1]	Cause			
Reset	Interrupt	RESET	Reset input	FFF0H	FFFFFFF0H	Undefined
Non-maskable	Interrupt	NMI	NMI input	FFD0H	FFFFFFD0H	next PC[Note 3]
Software exception	Exception	TRAP 1nH	TRAP instruction	FFBnH	FFFFFFB0H	next PC
		TRAP 0nH	TRAP instruction	FFAnH	FFFFFFA0H	
Exception trap	Exception	NMI	Dual exception	**Note 4**	FFFFFFD0H	current PC
		FAULT	Fatal exception	Not affected	FFFFFFE0H	
		I-OPC	Illegal instruction code	FF90H	FFFFFF90H	
		DIV0	Zero division	FF80H	FFFFFF80H	

Notes 1. Handler names used in development tools or software.

2. The PC value saved to EIPC/FEPC/DPC when interrupt/exception processing is started.

3. Execution of all instructions cannot be stopped by an interrupt.

4. The exception code of an exception causing a dual exception.

Remark n = 0H to FH

Table 4-2. Maskable Interrupt List

Type	Classification	Group	In-Group Priority	Interrupt Source			Exception Code	Handler Address[Note 3]		Restore PC[Note 1]
				Name	Cause	Unit		HCCW.IHA=0	HCCW.IHA=1	
Maskable	Interrupt	GR3	3	RESERVED	Reserved	—	FEF0H	FFFFFEF0H	FE0000F0H	next PC[Note 2]
			2	INTOV1	Timer 1 overflow	RPU	FEE0H	FFFFFEE0H	FE0000E0H	
			1	INTSER	UART receive error	UART	FED0H	FFFFFED0H	FE0000D0H	
			0	INTP03	INTP03 pin input	External	FEC0H	FFFFFEC0H	FE0000C0H	
		GR2	3	INTSR	UART receive end	UART	FEB0H	FFFFFEB0H	FE0000B0H	
			2	INTST	UART transmit end	UART	FEA0H	FFFFFEA0H	FE0000A0H	
			1	INTCSI	CSI transmit/receive end	CSI	FE90H	FFFFFE90H	FE000090H	
			0	INTP02	INTP02 pin input	External	FE80H	FFFFFE80H	FE000080H	
		GR1	3	INTDMA	DMA transfer end	DMAC	FE70H	FFFFFE70H	FE000070H	
			2	INTP10/ INTCC10	INTP10 pin input/ coincidence of CC10	External/ RPU	FE60H	FFFFFE60H	FE000060H	
			1	INTP11/ INTCC11	INTP11 pin input/ coincidence of CC11	External/ RPU	FE50H	FFFFFE50H	FE000050H	
			0	INTP01	INTP01 pin input	External	FE40H	FFFFFE40H	FE000040H	
		GR0	3	INTCM4	Coincidence of CM4	RPU	FE30H	FFFFFE30H	FE000030H	
			2	INTP12/ INTCC12	INTP12 pin input/ coincidence of CC12	External/ RPU	FE20H	FFFFFE20H	FE000020H	
			1	INTP13/ INTCC13	INTP13 pin input/ coincidence of CC13	External/ RPU	FE10H	FFFFFE10H	FE000010H	
			0	INTP00	INTP00 pin input	External	FE00H	FFFFFE00H	FE000000H	

Notes 1. The PC value saved to EIPC when interrupt processing is started.

2. Execution of all instructions cannot be stopped by an interrupt.

3. FFFFFEn0H can be selected as a handler address when HCCW.IHA = 0, and FE0000n0H can be selected when HCCW.IHA = 1 (n = 0H to FH).

Caution The exception codes and handler addresses of the maskable interrupts shown above are the values if the default priority (IGP = E4H) is used. The correspondence between the interrupt source and the handler address is changed from Table 4-2 if the priority of the group (GR0 to GR3) is changed according to the value of the interrupt group priority register (IGP).

5. BUS CONTROL FUNCTION

The features of the bus control function are as follows:

- SDRAM, Page-ROM, SRAM (ROM) or I/O can be directly connected
- SDRAM read/write access with 1 bus clock minimum
- SDRAM byte access control with four ××DQM signals
- Wait control with $\overline{\text{READY}}$ signal
- RAM, ROM or I/O byte access control with four ××$\overline{\text{BEN}}$ signals
- 32-/16-bit bus width can be set every CS space
  - When the 16-bit memory or I/O are accessed by data bus, the external data bus width can be set by the data bus width control register (DBC).

Remarks 1. ××$\overline{\text{BEN}}$: $\overline{\text{LLBEN}}$, $\overline{\text{LUBEN}}$, $\overline{\text{ULBEN}}$, $\overline{\text{UUBEN}}$

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

6. WAIT CONTROL FUNCTION

The features of the wait control function are as follows:

- Controls 8 blocks in accordance with I/O and memory spaces
- Linear address space of each block: 16 Mbytes
- Bus cycle select function

  Block 0: SDRAM
  Block 1: SDRAM, SRAM (ROM) selectable
  Block 2: SRAM (ROM)
  Blocks 3 through 6: I/O or SRAM (ROM) selectable
  Block 7: Page-ROM or SRAM (ROM) selectable
- Data bus width select function

  Data bus width selectable between 32 bits and 16 bits for each block
- Wait control function

  Blocks 0 and 1: SDRAM wait control function is not provided
  Blocks 1 through 4 and 7: 0 to 7 wait states
  Blocks 5 and 6: 0 to 15 wait states
- Idle state insertion function

  0 to 7 states for each block (bus clock)

7. MEMORY ACCESS CONTROL FUNCTION

The features of the memory access control function are as follows:

- SDRAM control function
  - Generates $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, LLDQM, LUDQM, ULDQM, and UUDQM signals
  - Address multiplex: 8 or 9 bits
  - Timing control of SDRAM access
    Command interval from REF to REF/ACT: 3 to 6 bus clocks selectable
    Command interval from ACT to PRE: 3 or 4 bus clocks selectable
    Command interval from PRE to ACT: 1 or 2 bus clocks selectable
    Command interval from ACT to READ/WRITE: 1 or 2 bus clocks selectable
    ★ $\overline{CAS}$ latency: 2 bus clocks fixed
  - Auto refresh and self-refresh functions
  - 8-bank control (4 banks × 2 blocks)
- Page-ROM control function
  - Page size: 8 or 16 bytes
  - Wait control during page access: 0 to 7 wait states

7.1 SDRAM Control Function

The BCU generates $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS0}$, $\overline{CS1}$, CKE, LLDQM, LUDQM, ULDQM, and UUDQM signals and controls access to the SDRAM. Addresses are output to the SDRAM from the address pins by multiplexing row and column addresses.

The connected SDRAM must be of ×8 bits or more.

The refresh mode is a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) mode, and the refresh cycle can be arbitrarily set.

Self refresh is performed in the STOP mode.

(1) Address multiplex function

An address is multiplexed as shown in Tables 7-1 and 7-2 when row and column addresses are output in the SDRAM cycle, depending on the values of the RAW and CAW bits of the SDRAM configuration register (SDC). In the tables, a1 through a23 indicate the address output by the CPU, and A1 through A15 indicate the address pins of the V832.

Table 7-1. Output of Row Address and Column Address (32-bit data width)

BAW	RAW	CAW	Output Timing	External Address Pin						
				A15	A14	A13	A12	A11	A10	A9 to A2
0	00	00	Column address	(a15)	(a14)	a21*	AP	(a11)	(a10)	a9 to a2
			Row address	a23	a22	a21*	a20	a19	a18	a17 to a10
0	00	01	Column address	(a15)	(a14)	a22*	AP	(a11)	a10	a9 to a2
			Row address	(a15)	a23	a22*	a21	a20	a19	a18 to a11
1	00	00	Column address	(a15)	a22*	a21*	AP	(a11)	(a10)	a9 to a2
			Row address	a23	a22*	a21*	a20	a19	a18	a17 to a10
1	00	01	Column address	(a15)	a23*	a22*	AP	(a11)	a10	a9 to a2
			Row address	(a15)	a23*	a22*	a21	a20	a19	a18 to a11
1	01	00	Column address	a23*	a22*	(a13)	AP	(a11)	(a10)	a9 to a2
			Row address	a23*	a22*	a21	a20	a19	a18	a17 to a10

Remarks 1. * indicates bank address specification.

2. AP is a bit used to specify a command and is fixed to low level.

3. Addresses in parentheses (a××) and A1 and A16 through A23 pins do not multiplex addresses and always output the original values.

Table 7-2. Output of Row Address and Column Address (16-bit data width)

BAW	RAW	CAW	Output Timing	External Address Pin							
				A15	A14	A13	A12	A11	A10	A9	A8 to A1
0	00	00	Column address	(a15)	(a14)	(a13)	a20*	AP	(a10)	(a9)	a8 to a1
			Row address	a23	a22	a21	a20*	a19	a18	a17	a16 to a9
0	00	01	Column address	(a15)	(a14)	(a13)	a21*	AP	(a10)	a9	a8 to a1
			Row address	(a15)	a23	a22	a21*	a20	a19	a18	a17 to a10
1	00	00	Column address	(a15)	(a14)	a21*	a20*	AP	(a10)	(a9)	a8 to a1
			Row address	a23	a22	a21*	a20*	a19	a18	a17	a16 to a9
1	00	01	Column address	(a15)	(a14)	a22*	a21*	AP	(a10)	a9	a8 to a1
			Row address	(a15)	a23	a22*	a21*	a20	a19	a18	a17 to a10
1	01	00	Column address	(a15)	a22*	a21*	(a12)	AP	(a10)	(a9)	a8 to a1
			Row address	a23	a22*	a21*	a20	a19	a18	a17	a16 to a9

Remarks 1. * indicates bank address specification.

2. AP is a bit used to specify a command and is fixed to low level.

3. Addresses in parentheses (a××) and A16 through A23 pins do not multiplex addresses and always output the original values.

(2) On-page/off-page decision

When the PAE bit of the SDRAM configuration register (SDC) is 1 (page access enabled), whether the SDRAM access to be started is in the same page as the previous SDRAM access is decided. When the PAE bit is 0, the off-page cycle is always started. Table 7-3 shows the relation between an address to be compared and address shift.

Table 7-3. Address Compared by on-page/off-page Decision

Address Shift	Data Bus Width	
	16 bits	32 bits
8	a23 to a9	a23 to a10
9	a23 to a10	a23 to a11

(3) Refresh function

The BCU can automatically generate the distributed auto refresh cycle necessary for refreshing the SDRAM. Whether refreshing is enabled or disabled and the refresh interval are set by the refresh control register (RFC). The BCU has a refresh request queue that can store refresh requests up to seven times.

7.2 Page-ROM Control Function

The BCU controls page access to the Page-ROM. Page access to the Page-ROM is valid during burst access. The page size (8 bytes/16 bytes) and the number of wait states (0 wait/1 wait) during page access can be set by using the Page-ROM configuration register (PRC).

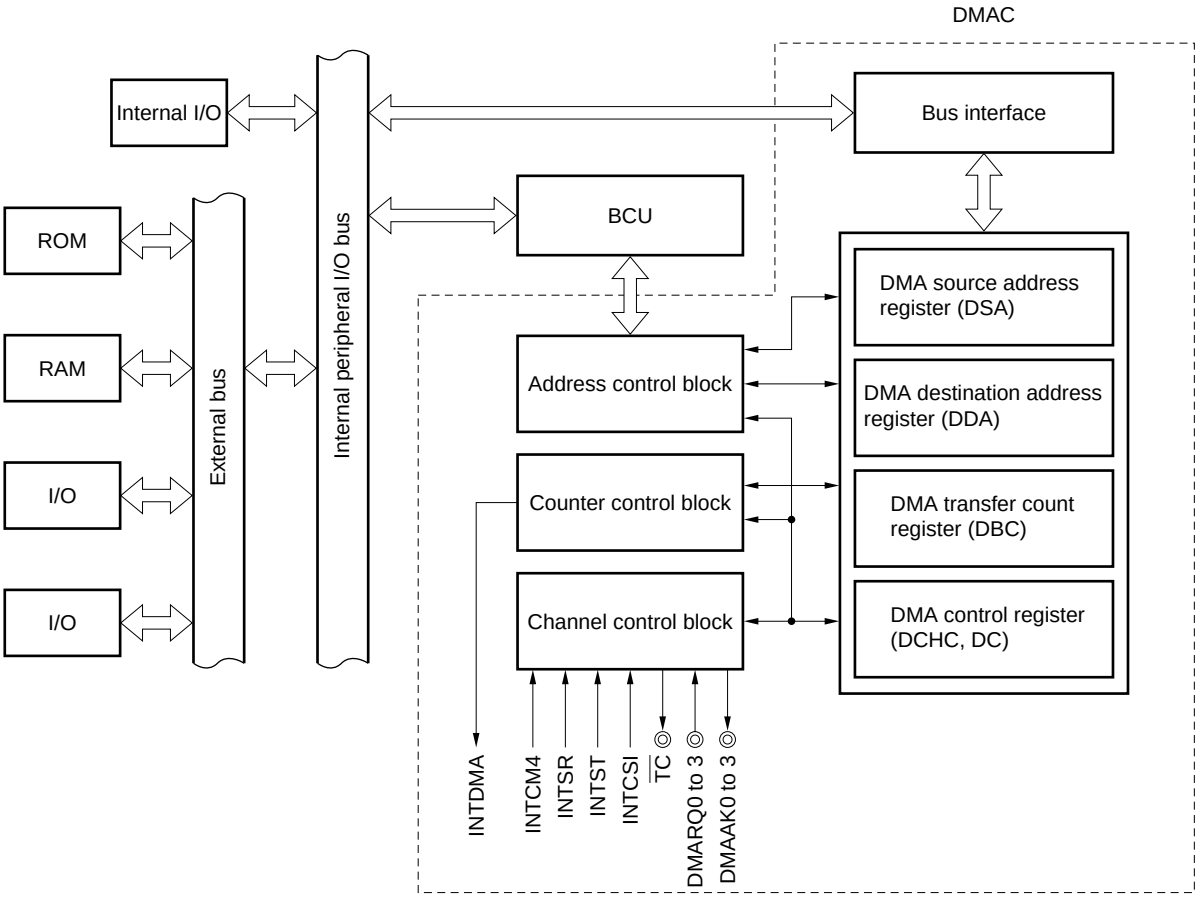
8. DMA FUNCTION

The features of the DMA function are as follows:

- Four independent DMA channels
- Transfer unit: bytes, half words (2 bytes), words (4 bytes)
- Maximum number of transfers: 16,777,216 (2^{24}) times
- Transfer type: 2-cycle transfer
- Two transfer modes
  - Single transfer mode
  - Demand transfer mode
- Transfer request
  - External DMARQ pin (×4)
  - Request from internal peripheral hardware (serial interface (×3 channels) and timer)
  - Request from software
- Transfer source and destination
  - Between memory and I/O
  - Between memory and memory
- Programmable wait function
- DMA transfer end signal output ($\overline{TC}$)

The configuration of the DMA controller (DMAC) is shown below.

Figure 8-1. Block Diagram of DMAC



9. SERIAL INTERFACE FUNCTION

The following channels are provided for the serial interface function.

- Asynchronous serial interface (UART): 1 channel
- Clocked serial interface (CSI): 1 channel
- Baud rate generator (BRG): 1 channel

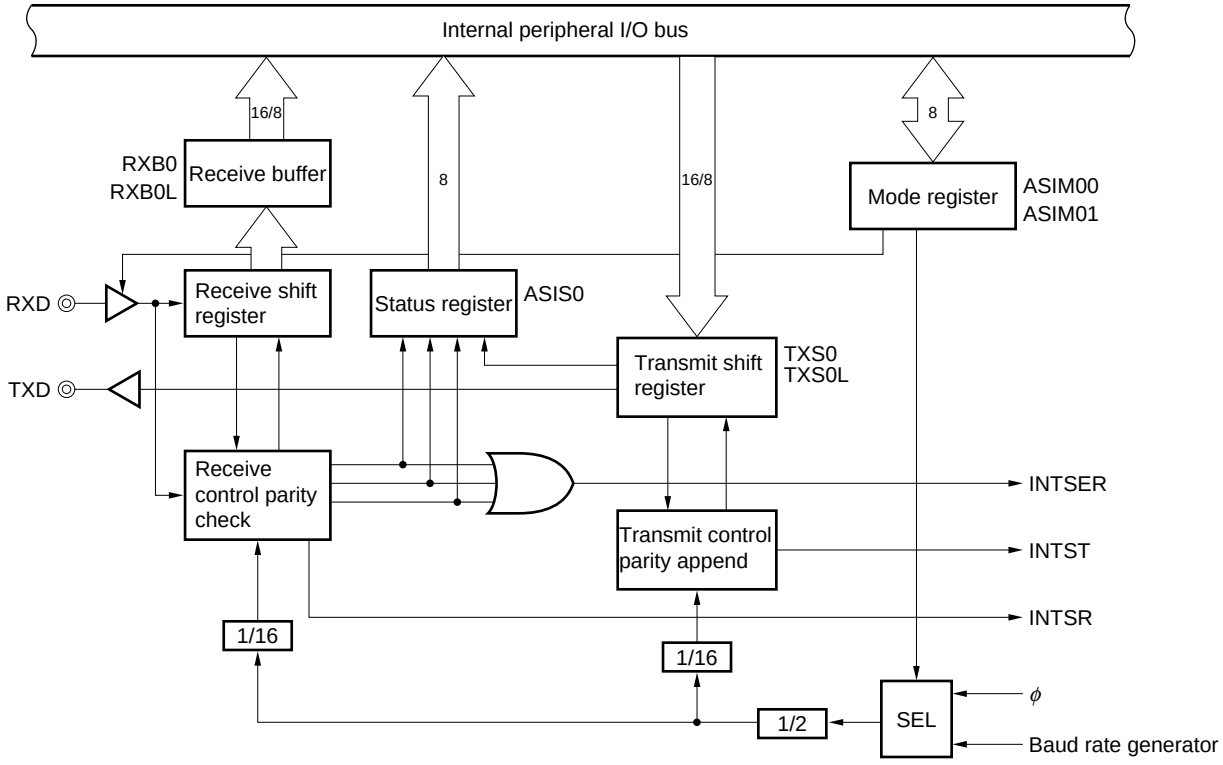
9.1 Asynchronous Serial Interface (UART)

The features of the asynchronous serial interface (UART) are as follows:

- Full duplex communication. Receive buffer (RXB) is provided (transmit buffer (TXB) is not provided).
- Two-pin configuration (The UART of the V832 does not have the SCLK and CTS pins.)
  - TXD: Transmit data output pin
  - RXD: Receive data input pin
- Transfer rate: 300 bps to 153600 bps (bus clock: 47.6 MHz, with BRG)
  : 150 bps to 76800 bps (bus clock: 35.7 MHz, with BRG)
- Baud rate generator
  Serial clock source can be selected from baud rate generator output or bus clock (ϕ)
- Receive error detection function
  - Parity error
  - Framing error
  - Overrun error
- Three interrupt sources
  - Receive error interrupt (INTSER)
    The interrupt request is generated by ORing three types of receive errors.
  - Receive end interrupt (INTSR)
    The receive end interrupt request is generated after completion of receive data transfer from the shift register to the receive buffer in the reception enabled status.
  - Transmit end interrupt (INTST)
    The transmit end interrupt request is generated after completion of serial transfer of transmit data (9, 8, or 7 bits) from the shift register. The character length of the transmit/receive data is specified by the ASIM00 and ASIM01 registers.
- Character length: 7 or 8 bits
  : 9 bits (with extension bit appended)
- Parity function: Odd, even, 0, or none
- Transmit stop bit: 1 or 2 bits

The configuration of the asynchronous serial interface (UART) is shown below.

Figure 9-1. Block Diagram of UART



★ **Remark** ϕ = bus clock : 48 M to 1.3 MHz: @input clock 6×
: 36 M to 0.73 MHz: @input clock 8×

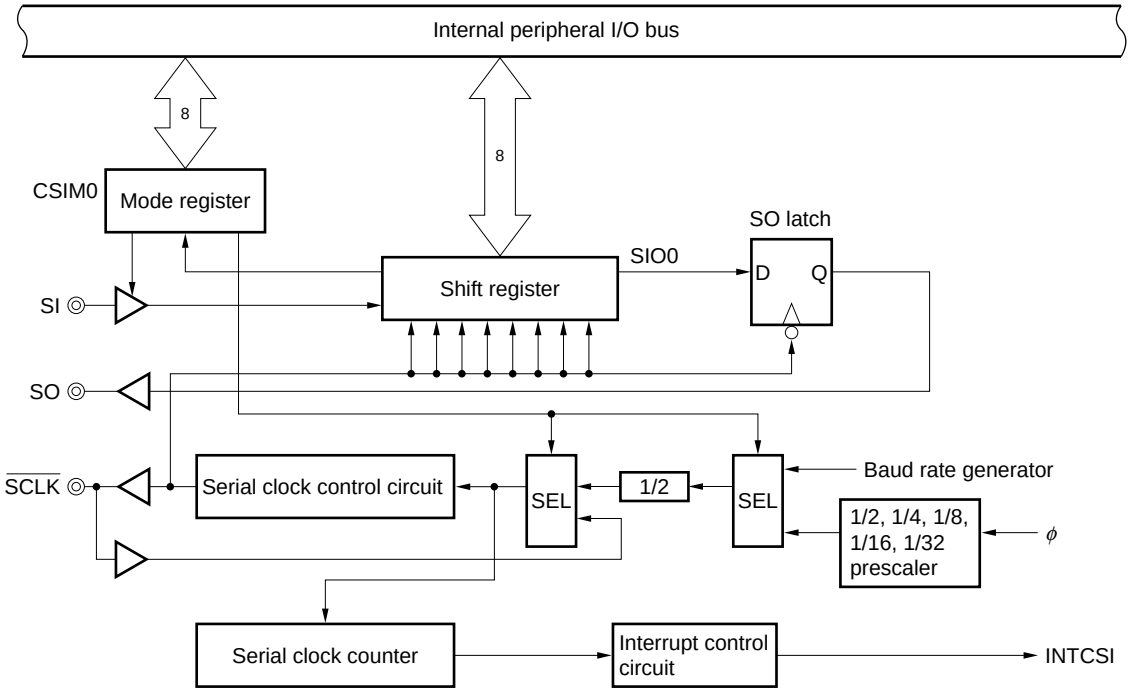
9.2 Clocked Serial Interface (CSI)

The features of the clocked serial interface (CSI) are as follows:

★
- High-speed transfer: 12.0 Mbps Max. (bus clock: 48.0 MHz)
- Half duplex communication for transmission/reception (buffer is not provided)
- Character length: 8 bits
- External or internal serial clock selectable

The configuration of the clocked serial interface (CSI) is shown below.

Figure 9-2. Block Diagram of CSI



★ **Remark** ϕ = bus clock : 48 M to 1.3 MHz: @input clock 6×
: 36 M to 0.73 MHz: @input clock 8×

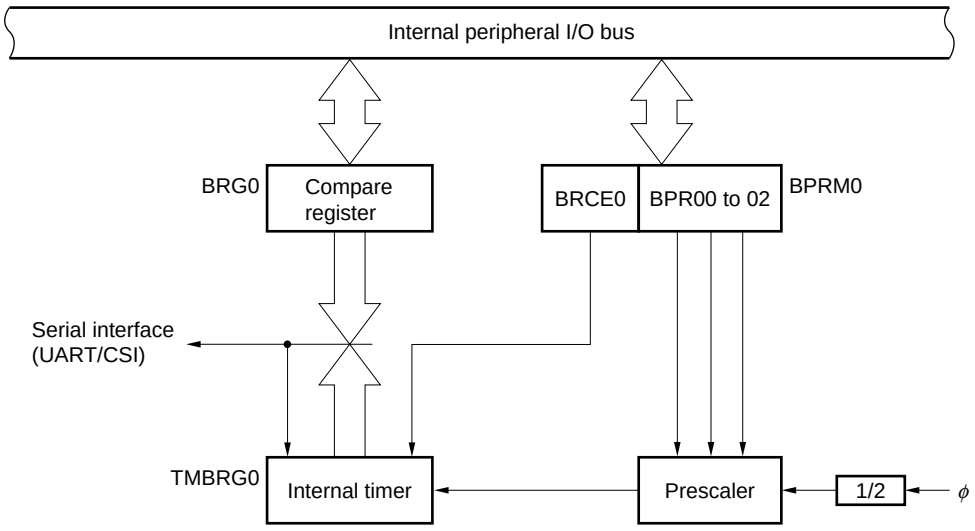
9.3 Baud Rate Generator (BRG)

The features of the baud rate generator (BRG) are as follows:

- The serial clock can be used as the baud rate generator output or the divided value of ϕ (bus clock) can be used as a baud rate.
- The serial clock source is specified by the following registers.
  - In the case of UART: Specified by the SCLS0 bit of the ASIM00 register.
  - In the case of CSI: Specified by the CLS02 through CLS00 bits of the CSIM0 register.
- The baud rate generator is shared by the UART and CSI.

The configuration of the baud rate generator (BRG) is shown below.

Figure 9-3. Block Configuration of Baud Rate Generator (BRG)



★ **Remark** ϕ = bus clock : 48 M to 1.3 MHz: @input clock 6×
: 36 M to 0.73 MHz: @input clock 8×

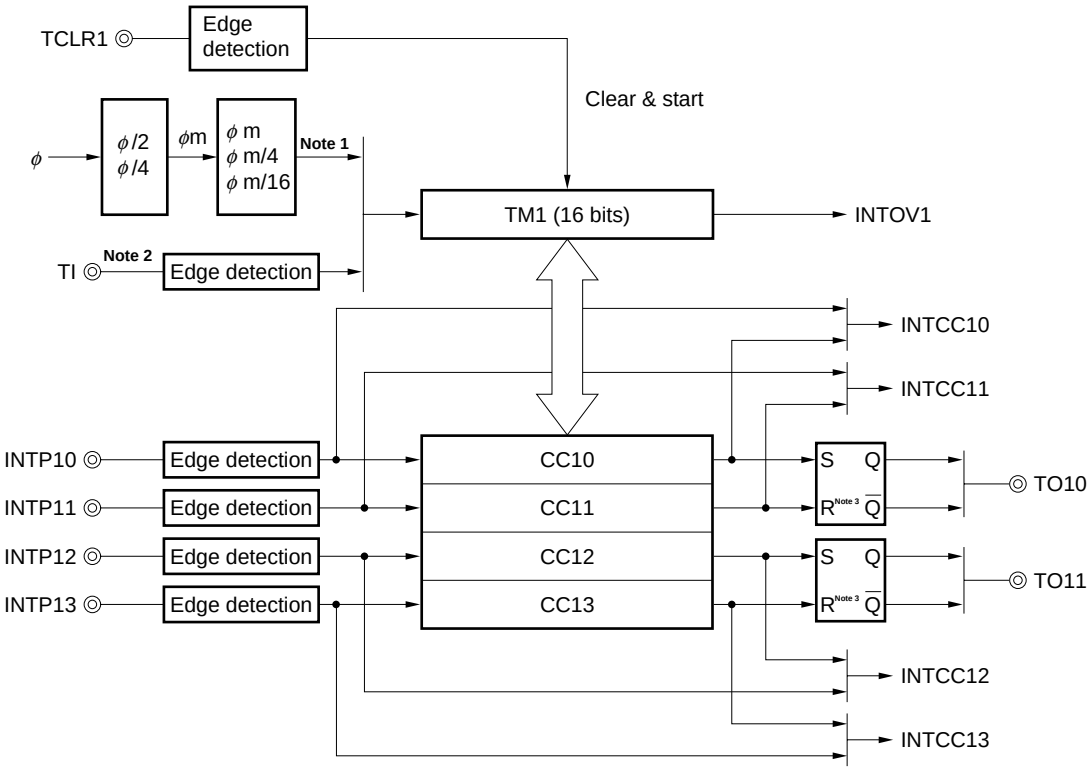
10. TIMER/COUNTER FUNCTION

The features of the timer/counter function are as follows:

- Measures pulse interval and frequency and outputs programmable pulse
  - 16-bit measurement
  - Can generate pulses of various shapes (interval pulse, one-shot pulse)
- Timer 1
  - 16-bit timer/event counter
  - Source of count clock: 2 types (selected by dividing system clock, external pulse input)
  - Capture/compare register: × 4
  - Count clear pin: TCLR
  - Interrupt source: 5 types
  - External pulse output: 2 pins
- Timer 4
  - 16-bit interval timer
  - Count clock selected by dividing system clock
  - Compare register: × 1
  - Interrupt source: 1 type

The configurations of timer 1 and timer 4 are shown below.

Figure 10-1. Block Configuration of Timer 1



★ **Notes 1.** Internal count clock

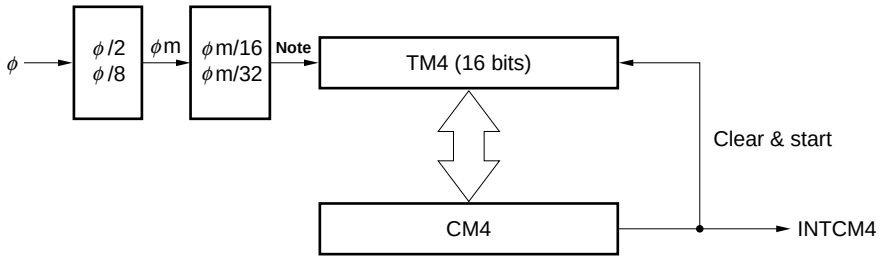
2. When the external count clock is TI: 6.0 MHz or lower: @input clock 6×
: 4.5 MHz or lower: @input clock 8×

3. Reset priority

★ **Remarks 1.** φ = bus clock: 48 M to 1.3 MHz: @input clock 6×
: 36 M to 0.73 MHz: @input clock 8×

2. φm = intermediate clock

Figure 10-2. Block Configuration of Timer 4



Note Internal count clock

★ **Remarks 1.** φ = bus clock: 48 M to 1.3 MHz: @input clock 6×
: 36 M to 0.73 MHz: @input clock 8×

2. φm = intermediate clock

11. PORT FUNCTION

The port function features are listed in Table 11-1.

Table 11-1. Port Functions

Port	Control Mode	Remark
PORT0	$\overline{SCLK}$	PORT 5-bit input/output port. Input/output can be specified in 1-bit units.
PORT1	SO	
PORT2	SI	
PORT3	RXD	
PORT4	TXD	
PORTA0	DMARQ0	PORTA 8-bit input/output port. Input/output can be specified in 1-bit units.
PORTA1	DMAAK0	
PORTA2	DMARQ1	
PORTA3	DMAAK1	
PORTA4	DMARQ2	
PORTA5	DMAAK2	
PORTA6	DMARQ3	
PORTA7	DMAAK3	
PORTB0	TI	PORTB 8-bit input/output port. Input/output can be specified in 1-bit units.
PORTB1	TCLR	
PORTB2	INTP00	
PORTB3	INTP13	
PORTB4	INTP01	
PORTB5	INTP11	
PORTB6	INTP02	
PORTB7	INTP03	

Port configurations are shown in Figures 11-1 to 11-6.

Figure 11-1. Block Diagram of PORT0

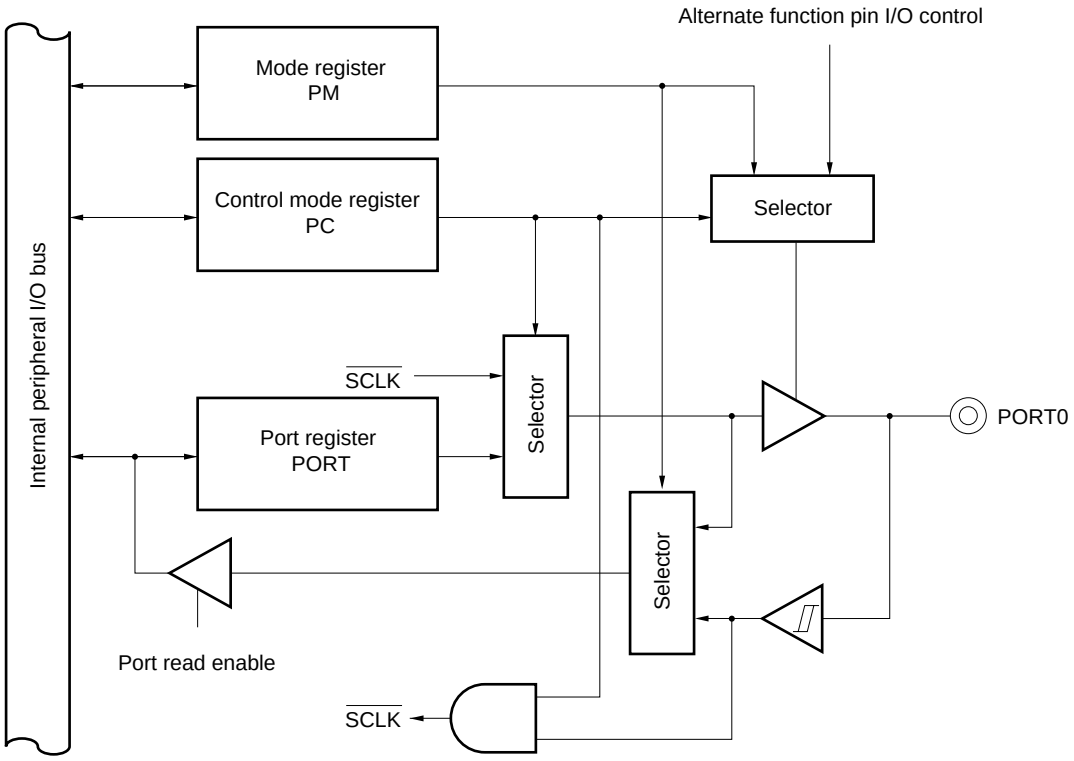


Figure 11-2. Block Diagram of PORT1 and PORT4

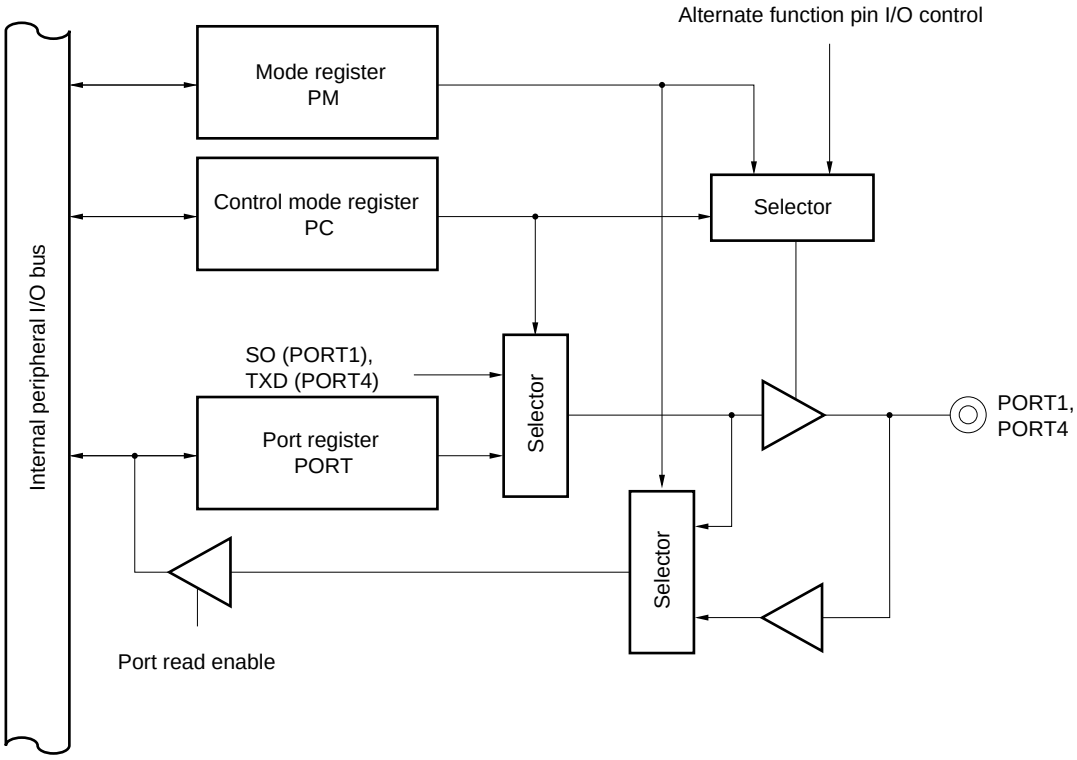


Figure 11-3. Block Diagram of PORT2 and PORT3

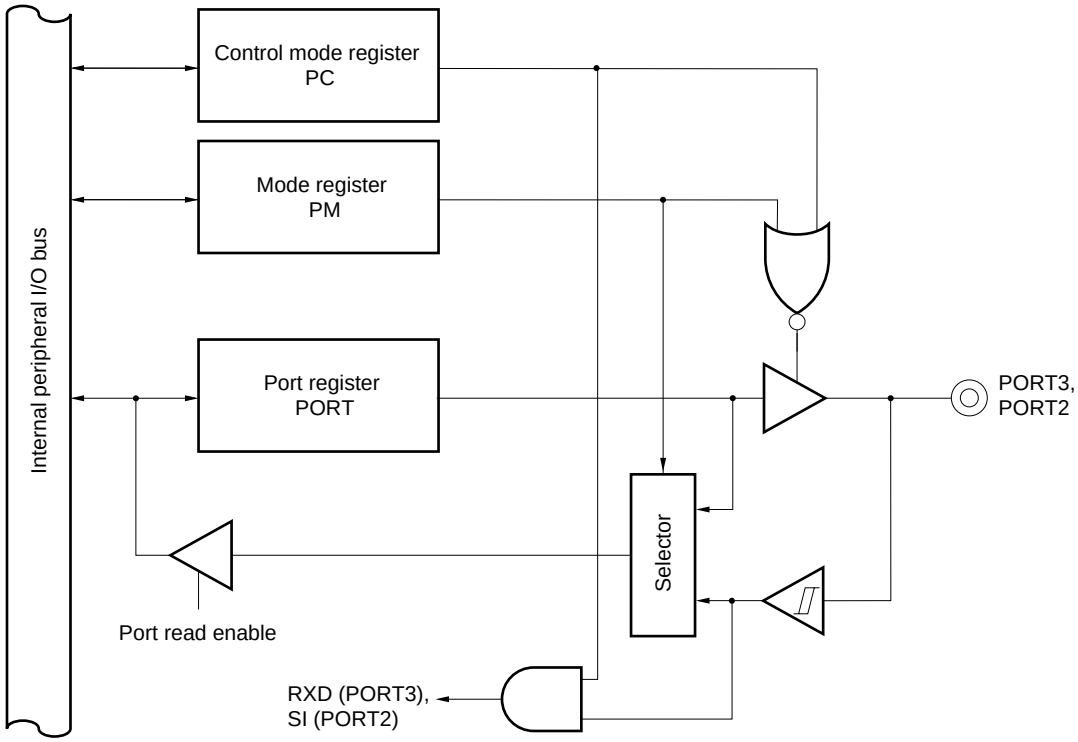


Figure 11-4. Block Diagram of PORTAn (n = 0, 2, 4, or 6)

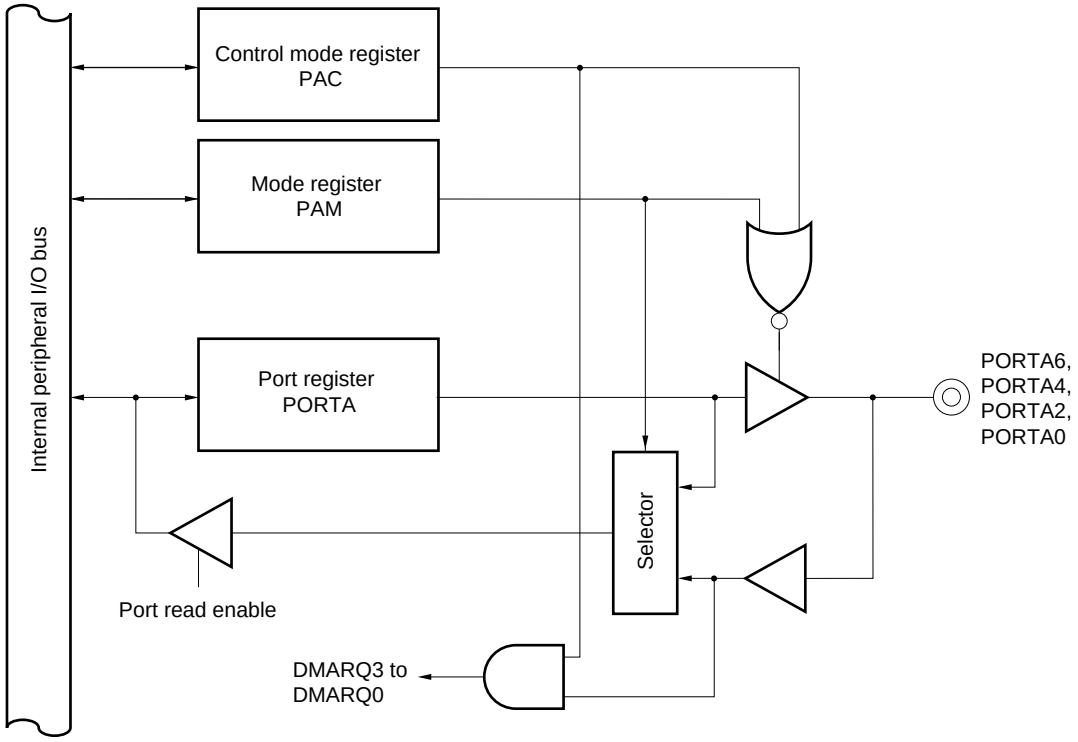


Figure 11-5. Block Diagram of PORTAn (n = 1, 3, 5, or 7)

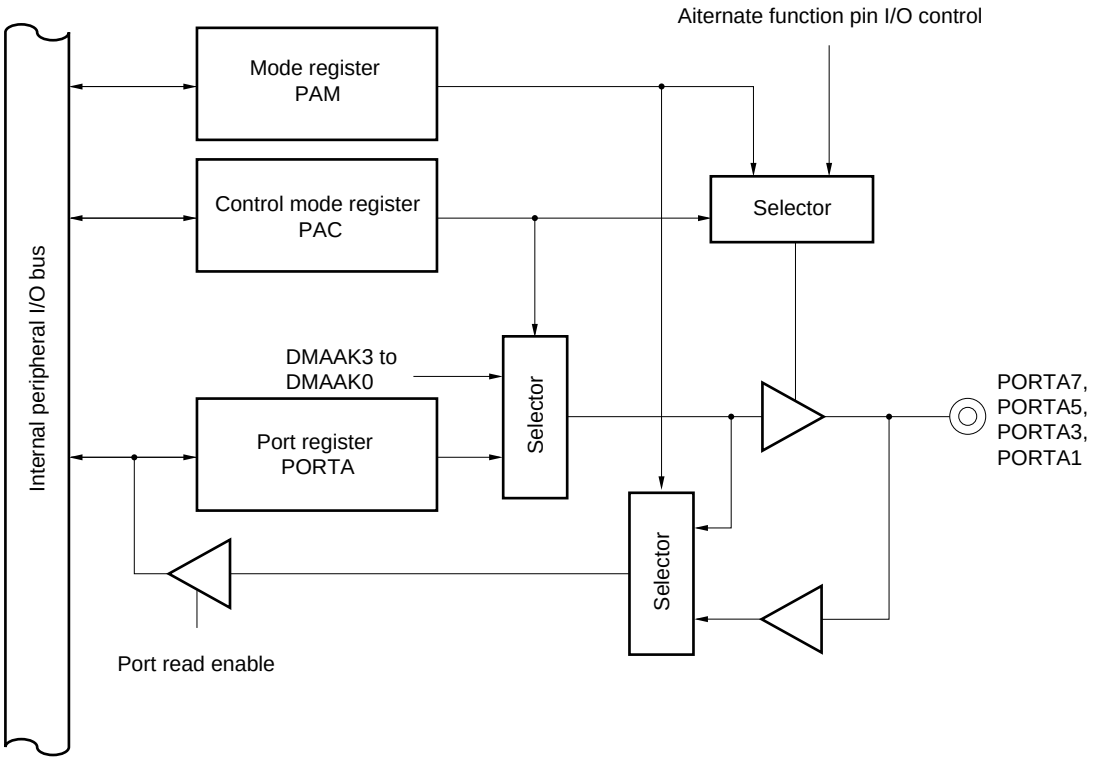
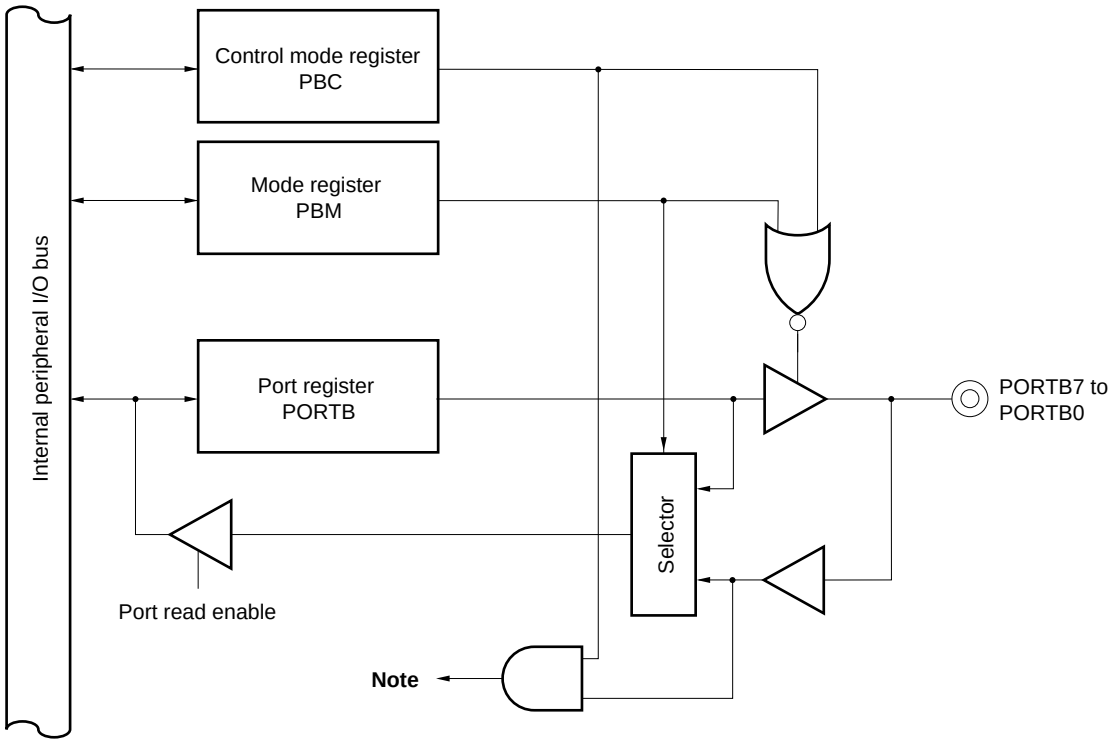


Figure 11-6. Block Diagram of PORTB0 through PORTB7



Note INTP03 (PORTB7), INTP02 (PORTB6), INTP11 (PORTB5), INTP01 (PORTB4), INTP13 (PORTB3), INTP00 (PORTB2), TCLR (PORTB1), TI (PORTB0)

Remark ( ) indicates the corresponding port.

12. CLOCK GENERATION FUNCTION

The clock generator generates and controls the CPU clock and bus clock that are supplied to the internal hardware units.

PMC and frequencies in PLL/direct modes are shown in Table 12-1 and Table 12-2.

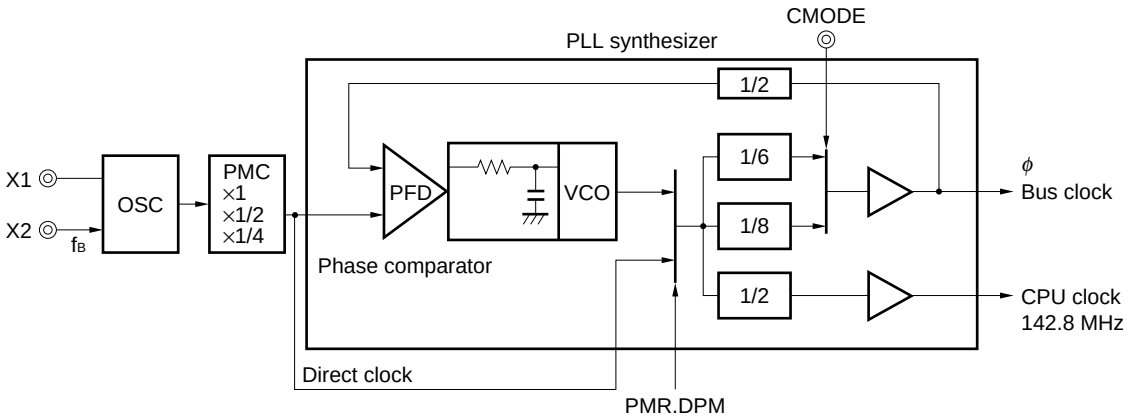
Table 12-1. PMC and Frequency in PLL/Direct Modes Example (μPD705102-143)

		PLL Mode		Direct Mode	
Input clock	PMC	CPU	Bus clock	CPU	Bus clock
23.8 MHz (6 times)	×1	142.8 MHz	47.6 MHz	11.9 MHz	3.96 MHz
	×1/2	71.4 MHz	23.8 MHz	5.95 MHz	1.98 MHz
	×1/4	35.7 MHz	11.9 MHz	—	—
17.85 MHz (8 times)	×1	142.8 MHz	35.7 MHz	8.925 MHz	2.231 MHz
	×1/2	71.4 MHz	17.85 MHz	4.463 MHz	1.116 MHz
	×1/4	35.7 MHz	8.925 MHz	—	—

★ **Table 12-2. PMC and Frequency in PLL/Direct Modes Example (μPD705102-133)**

		PLL Mode		Direct Mode	
Input clock	PMC	CPU	Bus clock	CPU	Bus clock
22.2 MHz (6 times)	×1	133.3 MHz	44.4 MHz	11.1 MHz	3.70 MHz
	×1/2	66.7 MHz	22.2 MHz	5.56 MHz	1.85 MHz
	×1/4	33.3 MHz	11.1 MHz	—	—
16.7 MHz (8 times)	×1	133.3 MHz	33.3 MHz	8.33 MHz	2.08 MHz
	×1/2	66.7 MHz	16.7 MHz	4.17 MHz	1.04 MHz
	×1/4	33.3 MHz	8.33 MHz	—	—

The configuration of the clock generator is shown below.



fB: Oscillation frequency or external clock frequency

ϕ: Bus clock

OSC: Oscillator

PFD: Phase Frequency Detector

VCO: Voltage Controlled Oscillator

PMC: Power Management Controller

13. STANDBY FUNCTION

The V832 has the following two modes as standby functions:

- Power management mode
- Standby mode

(1) Power management mode

The following two power management modes can be used. According to the combination of these modes, the operating frequency is actively changed.

- **PLL mode**

  This is the mode normally used. In this mode, the oscillation clock of the external input clock/OSC, which is expanded 6 or 8 times by the PLL synthesizer, is employed as the CPU clock.

- **Direct mode**

  In this mode, the oscillation clock of the external input clock/OSC is employed as the CPU clock without passing through the PLL synthesizer.

(2) Standby mode

The following two standby modes can be used.

- **HALT mode**

  In this mode, the clock generator (oscillator and PLL synthesizer) operates, but the operating clock of the CPU is stopped. The other internal peripheral functions are supplied with the clock and continue operation. By using this mode in combination with the normal mode, the power consumption of the entire system can be reduced.

- **STOP mode**

  This mode stops supply of the clock to the CPU and peripheral I/O.
  It can reduce the power consumption much more than the HALT mode.

  Clock output of PLL synthesizer

  - In PLL mode: Operation of the PLL can be started or stopped by the PLLSS bit of the power management register (PMR).
  - In direct mode: The PLL always stops.

Table 13-1 shows the operation of the clock generator in each mode.

Table 13-1. Operation of Clock Generator by Standby Control

Modes		Oscillator (OSC)	PLL Synthesizer	Clock Supply to Peripheral I/O	Clock Supply to CPU
Power Management Mode	Standby Mode				
PLL mode	Normal	○	○	○	○
	HALT	○	○	○	×
	STOP	○	Δ	×	×
Direct mode	Normal	○	×	○	○
	HALT	○	×	○	×
	STOP	○	×	×	×

Remark ○: Operates
×: Stops
Δ: Operates or stops depending on setting

Table 13-2. Operating Status in HALT/STOP Mode

Function	HALT Mode[Note 1]		STOP Mode
Oscillator	Operates		
PLL synthesizer	Operates[Note 2]		Stops[Note 3]
Bus clock	Operates		Stops
CPU	Stops		
Port output	Retained		
Peripheral function	Operates		Stops
Internal data	Internal data such as registers of CPU retain status before HALT mode is set.		
A1 to A23	Undefined	High impedance when $\overline{HLDAK}$ = 0	Undefined
D0 to D31	High impedance		
$\overline{BCYST}$	1	High impedance when $\overline{HLDAK}$ = 0	1
$\overline{CS0}$ to $\overline{CS7}$			
$\overline{IORD}$, $\overline{IOWR}$			
$\overline{MRD}$, $\overline{MWR}$, $\overline{LLBEN}$, $\overline{LUBEN}$, $\overline{ULBEN}$, $\overline{UUBEN}$			
★ LLDQM, LUDQM, ULDQM, UUDQM	0[Note 4]		Self refresh[Note 7]
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1[Note 5]		
CKE	1[Note 6]		
R/$\overline{W}$	Retained		Retained
$\overline{HLDRQ}$	Operates		Not accepted
CLKOUT, SDCLKOUT	Clock output (if clock output is not disabled)		0
$\overline{STOPAK}$	1		0

Notes 1. Each pin is in the operating status during DMA transfer.
2 Stops in the direct mode.
3. Occasionally operates in PLL mode.
4. After reset, 1 till first SDRAM access.
5. When auto refresh is not executed.
6. 0 in the power down mode.
7. When refresh is prohibited, self refresh cannot be performed. In that case, this pin retains the status before the STOP mode.

14. RESET/NMI CONTROL FUNCTION

The features of the reset/NMI control function are as follows:

- $\overline{\text{RESET}}$ and $\overline{\text{NMI}}$ pins have a noise rejection circuit that samples the clock.
- Performs forced reset, reset mask, and NMI mask processing from debug control unit

Table 14-1 shows the status of the output pins during the system reset period and immediately after reset. This status is retained during the reset period.

Table 14-1. Status of Output Pin Immediately after Reset

Function	Operating Status
A1 to A23	Undefined
D0 to D31	High impedance
$\overline{\text{CS0}}$ to $\overline{\text{CS7}}$	1
$\overline{\text{BCYST}}$	1
$\overline{\text{IORD}}$, $\overline{\text{IOWR}}$	1
$\overline{\text{WE}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, CKE	1
$\overline{\text{LLBEN}}$, $\overline{\text{LUBEN}}$, $\overline{\text{ULBEN}}$, $\overline{\text{UUBEN}}$	1
LLDQM, LUDQM, ULDQM, UUDQM	1
R/$\overline{\text{W}}$	1
$\overline{\text{MRD}}$, $\overline{\text{MWR}}$	1
CLKOUT, SDCLKOUT	Clock output
$\overline{\text{HLDAK}}$	1
PORT0 to PORT4[Note], PORTA0 to PORTA7[Note], PORTB0 to PORTB7[Note]	High impedance
DDO	Undefined
TRCDATA0 to TRCDATA3	Undefined
$\overline{\text{STOPAK}}$/$\overline{\text{TC}}$	1

Note Pins with alternate functions as ports serve as port pins immediately after reset.

15. INSTRUCTIONS

15.1 Instruction Format

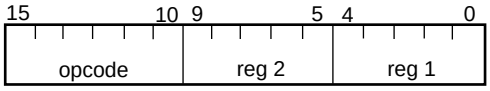
The V832 uses two instruction formats: 16-bit and 32-bit. The 16-bit instructions include binary operation, control, and conditional branch instructions, while the 32-bit instructions include load/store and I/O operation instructions, instructions for handling 16 bits of immediate data, and jump-and-link instructions.

Some instructions contain unused fields, which must be fixed to 0, which are provided for future use. When an instruction is actually loaded into memory, its configuration is as follows:

- Low-order part of each instruction format (including bit 0) → Low-order address
- High-order part of each instruction format (including bit 15 or 31) → High-order address

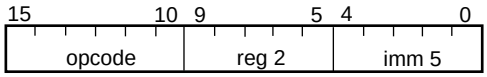
(1) reg-reg instruction format [FORMAT I]

This instruction format has a 6-bit operation code field and two general-purpose register designation fields for operand specification, giving a total length of 16 bits.



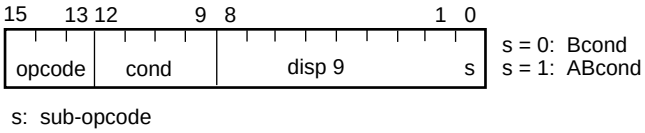
(2) imm-reg instruction format [FORMAT II]

This instruction format has a 6-bit operation code field, a 5-bit immediate data field, and a general-purpose register designation field, giving a total length of 16 bits.



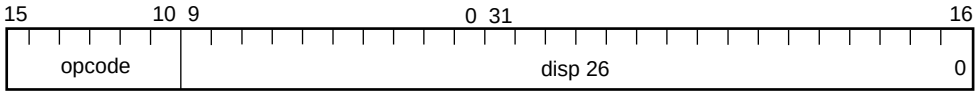
(3) Conditional branch instruction format [FORMAT III]

This instruction format has a 3-bit operation code field, a 4-bit condition code field, a 9-bit branch displacement field (bit 0 is handled as 0 and need not be specified), and a 1-bit sub-operation code, giving a total length of 16 bits.



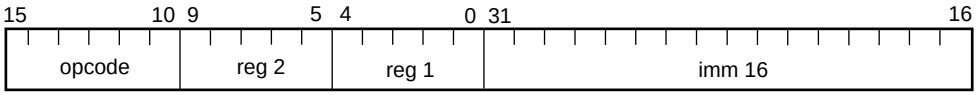
(4) Medium-distance jump instruction format [FORMAT IV]

This instruction format has a 6-bit operation code field and a 26-bit displacement field (the lowest-order bit must be 0), giving a total length of 32 bits.



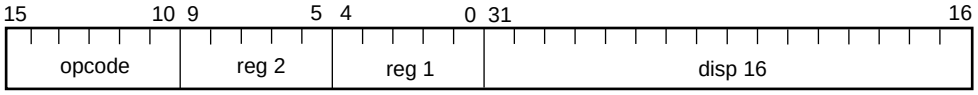
(5) Three-operand instruction format [FORMAT V]

This instruction format has a 6-bit operation code field, two general-purpose register designation fields, and a 16-bit immediate data field, giving a total length of 32 bits.



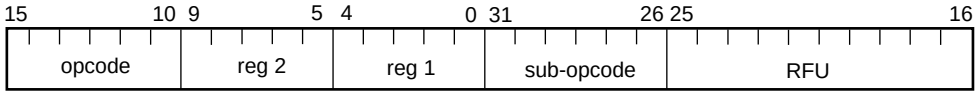
(6) Load/store instruction format [FORMAT VI]

This instruction format has a 6-bit operation code field, two general-purpose register designation fields, and a 16-bit displacement field, giving a total length of 32 bits.



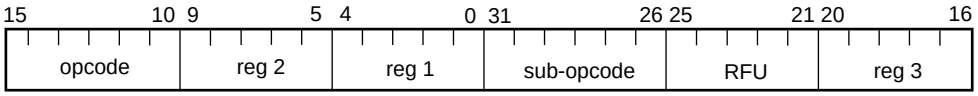
(7) Extended instruction format [FORMAT VII]

This instruction format has a 6-bit operation code field, two general-purpose register designation fields, and a 6-bit sub-operation code field, giving a total length of 32 bits.



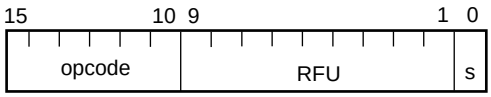
(8) Three-register operand instruction format [FORMAT VIII]

This instruction format has a 6-bit operation code field, three general-purpose register designation fields, and a 6-bit sub-operation code field, giving a total length of 32 bits.



(9) No-operand instruction format [FORMAT IX]

This instruction format has a 6-bit operation code field and a 1-bit sub-operation code field, giving a total length of 16 bits.



s: sub-opcode

15.2 Instructions (Listed Alphabetically)

The instructions are listed below in alphabetic order of their mnemonics.

Explanation of list format

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
ADD	reg1, reg2	I	*	*	*	*	

Instruction mnemonic

Instruction format (See **15.1 Instruction Format**)

Indicates how each flag changes.
—: Does not change.
*: Changes.
0: Becomes 0.
1: Becomes 1.

Abbreviations of operands

Abbreviation	Meaning
reg1	General-purpose register (used as a source register)
reg2	General-purpose register (used mainly as a destination register, but in some instructions, used as a source register)
reg3	General-purpose register (used mainly as a destination register, but in some instructions, used as a source register)
imm×	× bits of immediate data
disp×	×-bit displacement
regID	System register number
vector adr	Trap handler address corresponding to trap vector

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
ABC	disp9	III	—	—	—	—	High-speed conditional branch (if Carry) relative to PC.
ABE	disp9	III	—	—	—	—	High-speed conditional branch (if Equal) relative to PC.
ABGE	disp9	III	—	—	—	—	High-speed conditional branch (if Greater than or Equal) relative to PC.
ABGT	disp9	III	—	—	—	—	High-speed conditional branch (if Greater than) relative to PC.
ABH	disp9	III	—	—	—	—	High-speed conditional branch (if Higher) relative to PC.
ABL	disp9	III	—	—	—	—	High-speed conditional branch (if Lower) relative to PC.
ABLE	disp9	III	—	—	—	—	High-speed conditional branch (if Less than or Equal) relative to PC.
ABLT	disp9	III	—	—	—	—	High-speed conditional branch (if Less than) relative to PC.
ABN	disp9	III	—	—	—	—	High-speed conditional branch (if Negative) relative to PC.
ABNC	disp9	III	—	—	—	—	High-speed conditional branch (if Not Carry) relative to PC.
ABNE	disp9	III	—	—	—	—	High-speed conditional branch (if Not Equal) relative to PC.
ABNH	disp9	III	—	—	—	—	High-speed conditional branch (if Not Higher) relative to PC.
ABNL	disp9	III	—	—	—	—	High-speed conditional branch (if Not Lower) relative to PC.
ABNV	disp9	III	—	—	—	—	High-speed conditional branch (if Not Overflow) relative to PC.
ABNZ	disp9	III	—	—	—	—	High-speed conditional branch (if Not Zero) relative to PC.
ABP	disp9	III	—	—	—	—	High-speed conditional branch (if Positive) relative to PC.
ABR	disp9	III	—	—	—	—	High-speed unconditional branch (Always) relative to PC.
ABV	disp9	III	—	—	—	—	High-speed conditional branch (if Overflow) relative to PC.
ABZ	disp9	III	—	—	—	—	High-speed conditional branch (if Zero) relative to PC.
ADD	reg1, reg2	I	*	*	*	*	Addition. reg1 is added to reg2 and the sum is written into reg2.
	imm5, reg2	II	*	*	*	*	Addition. imm5, sign-extended to a word, is added to reg2 and the sum is written into reg2.
ADDI	imm16, reg1, reg2	V	*	*	*	*	Addition. imm16, sign-extended to a word, is added to reg1, and the sum is written into reg2.

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
AND	reg1, reg2	I	—	0	*	*	AND. reg2 and reg1 are ANDed and the result is written into reg2.
ANDI	imm16, reg1, reg2	V	—	0	0	*	AND. reg1 is ANDed with imm16, zero-extended to a word, and result is written into reg2.
BC	disp9	III	—	—	—	—	Conditional branch (if Carry) relative to PC.
BDLD	[reg1], [reg2]	VII	—	—	—	—	Block transfer. 4 words of data are transferred from external memory to on-chip data RAM.
BDST	[reg2], [reg1]	VII	—	—	—	—	Block transfer. 4 words of data are transferred from on-chip data RAM to external memory.
BE	disp9	III	—	—	—	—	Conditional branch (if Equal) relative to PC.
BGE	disp9	III	—	—	—	—	Conditional branch (if Greater than or Equal) relative to PC.
BGT	disp9	III	—	—	—	—	Conditional branch (if Greater than) relative to PC.
BH	disp9	III	—	—	—	—	Conditional branch (if Higher) relative to PC.
BILD	[reg1], [reg2]	VII	—	—	—	—	Block transfer. 4 words of data are transferred from external memory to on-chip instruction RAM.
BIST	[reg2], [reg1]	VII	—	—	—	—	Block transfer. 4 words of data are transferred from on-chip instruction RAM to external memory.
BL	disp9	III	—	—	—	—	Conditional branch (if Lower) relative to PC.
BLE	disp9	III	—	—	—	—	Conditional branch (if Less than or Equal) relative to PC.
BLT	disp9	III	—	—	—	—	Conditional branch (if Less than) relative to PC.
BN	disp9	III	—	—	—	—	Conditional branch (if Negative) relative to PC.
BNC	disp9	III	—	—	—	—	Conditional branch (if Not Carry) relative to PC.
BNE	disp9	III	—	—	—	—	Conditional branch (if Not Equal) relative to PC.
BNH	disp9	III	—	—	—	—	Conditional branch (if Not Higher) relative to PC.
BNL	disp9	III	—	—	—	—	Conditional branch (if Not Lower) relative to PC.
BNV	disp9	III	—	—	—	—	Conditional branch (if Not Overflow) relative to PC.
BNZ	disp9	III	—	—	—	—	Conditional branch (if Not Zero) relative to PC.
BP	disp9	III	—	—	—	—	Conditional branch (if Positive) relative to PC.
BR	disp9	III	—	—	—	—	Unconditional branch (Always) relative to PC.
BRKRET		IX	—	—	—	—	Return from fatal exception handling.
BV	disp9	III	—	—	—	—	Conditional branch (if Overflow) relative to PC.
BZ	disp9	III	—	—	—	—	Conditional branch (if Zero) relative to PC.
CAXI	disp16[reg1], reg2	VI	*	*	*	*	Inter-processor synchronization in multi-processor system.

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
CMP	reg1, reg2	I	*	*	*	*	Comparison. reg2 is compared with reg1 sign-extended to a word and the condition flag is set according to the result. The comparison involves subtracting reg1 from reg2.
	imm5, reg2	II	*	*	*	*	Comparison. reg2 is compared with imm5 sign-extended to a word and the condition flag is set according to the result. The comparison involves subtracting imm5, sign-extended to a word, from reg2.
DI		II	—	—	—	—	Disable interrupt. Maskable interrupts are disabled. DI instruction cannot disable non-maskable interrupts.
DIV	reg1, reg2	I	—	*	*	*	Division of signed operands. reg2 is divided by reg1 (signed operands). The quotient is stored in reg2 and the remainder in r30. The division is performed so that the sign of the remainder will match that of the dividend.
DIVU	reg1, reg2	I	—	0	*	*	Division of unsigned operands. reg2 is divided by reg1 (unsigned operands). The quotient is stored in reg2 and the remainder in r30. The division is performed so that the sign of the remainder will match that of the dividend.
EI		II	—	—	—	—	Enable interrupt. Maskable interrupts are enabled. EI instruction cannot enable non-maskable interrupts.
HALT		IX	—	—	—	—	Processor halt. The processor is placed in sleep mode.
IN.B	disp16[reg1], reg2	VI	—	—	—	—	Port input. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit port address. A byte of data is read from the resulting port address, zero-extended to a word, then stored in reg2.
IN.H	disp16[reg1], reg2	VI	—	—	—	—	Port input. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit port address. A halfword of data is read from the generated port address, zero-extended to a word, and stored in reg2. Bit 0 of the unsigned 32-bit port address is masked to 0.
IN.W	disp16[reg1], reg2	VI	—	—	—	—	Port input. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit port address. A word of data is read from the resulting port address, then written into reg2. Bits 0 and 1 of the unsigned 32-bit port address are masked to 0.

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
JAL	disp26	IV	—	—	—	—	Jump and link. The sum of the current PC and 4 is written into r31. disp26, sign-extended to a word, is added to the PC and the sum is set to the PC for control transfer. Bit 0 of disp26 is masked.
JMP	[reg1]	I	—	—	—	—	Indirect unconditional branch via register. Control is passed to the address designated by reg1. Bit 0 of the address is masked to 0.
JR	disp26	IV	—	—	—	—	Unconditional branch. disp26, sign-extended to a word, is added to the current PC and control is passed to the address specified by that sum. Bit 0 of disp26 is masked to 0.
LD.B	disp16[reg1], reg2	VI	—	—	—	—	Byte load. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit address. A byte of data is read from the generated address, sign-extended to a word, then written into reg2.
LD.H	disp16[reg1], reg2	VI	—	—	—	—	Halfword load. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit address. A halfword of data is read from the generated address, sign-extended to a word, then written into reg2. Bit 0 of the unsigned 32-bit address is masked to 0.
LD.W	disp16[reg1], reg2	VI	—	—	—	—	Word load. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit address. A word of data is read from the generated address, then written into reg2. Bits 0 and 1 of the unsigned 32-bit address are masked to 0.
LDSR	reg2, regID	II	*	*	*	*	Load into system register. The contents of reg2 are set in the system register identified by the system register number (regID).
MAC3	reg1, reg2, reg3	VIII	—	—	—	—	Saturation operation on signed 32-bit operands. reg1 and reg2 are multiplied together as signed integers and the product is added to reg3. [If no overflow has occurred:] The result is stored in reg3. [If an overflow has occurred:] The SAT bit is set. If the result is positive, the positive maximum is written into reg3; if the result is negative, the negative maximum is written into reg3.

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
MACI	imm16, reg1, reg2	V	—	—	—	—	Saturation operation on signed 32-bit operands. reg1 and imm16, sign-extended to 32 bits, are multiplied together as signed integers and the product is added to reg2 as a signed integer. [If no overflow has occurred:] The result is written into reg2. [If an overflow has occurred:] The SAT flag is set. If the result is positive, the positive maximum is written into reg2; if the result is negative, the negative maximum is written into reg2.
MACT3	reg1, reg2, reg3	VIII	—	—	—	—	Sum-of-products operation on signed 32-bit operands. reg1 and reg2 are multiplied together as signed integers and the high-order 32 bits of the product are added to reg3 as signed integers. [If no overflow has occurred:] The result is written into reg3. [If an overflow has occurred:] The SAT flag is set. If the result is positive, the positive maximum is written into reg3; if the result is negative, the negative maximum is written into reg3.
MAX3	reg1, reg2, reg3	VIII	—	—	—	—	Maximum. reg2 and reg1 are compared as signed integers. The larger value is written into reg3.
MIN3	reg1, reg2, reg3	VIII	—	—	—	—	Minimum. reg2 and reg1 are compared as signed integers. The smaller value is written into reg3.
MOV	reg1, reg2,	I	—	—	—	—	Data transfer. reg1 is copied to reg2 for data transfer.
	imm5, reg2	II	—	—	—	—	Data transfer. imm5, sign-extended to a word, is copied into reg2 for data transfer.
MOVEA	imm16, reg1, reg2	V	—	—	—	—	Addition. The high-order 16 bits (imm16), sign-extended to a word, are added to reg1 and the sum is written into reg2.
MOVHI	imm16, reg1, reg2	V	—	—	—	—	Addition. A word of data consisting of the high-order 16 bits (imm16) and low-order 16 bits (0) is added to reg1 and the sum is written into reg2.
MUL	reg1, reg2	I	—	*	*	*	Multiplication of signed operands. reg2 and reg1 are multiplied together as signed values. The high-order 32 bits of the product (double word) are written into r30 and low-order 32 bits are written into reg2.
MUL3	reg1, reg2, reg3	VIII	—	—	—	—	Multiplication of signed 32-bit operands. reg2 and reg1 are multiplied together as signed integers. The high-order 32 bits of the product are written into reg3.

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
MULI	imm16, reg1, reg2	V	—	—	—	—	Saturation multiplication of signed 32-bit operands. reg1 and imm16, sign-extended to 32 bits, are multiplied together as signed integers. [If no overflow has occurred:] The result is written into reg2. [If an overflow has occurred:] The SAT flag is set. If the result is positive, the positive maximum is written into reg2; if the result is negative, the negative maximum is written into reg2.
MULT3	reg1, reg2, reg3	VIII	—	—	—	—	Saturation multiplication of signed 32-bit operands. reg1 and reg2 are multiplied together as signed integers. The high-order 32 bits of the product are written into reg3.
MULU	reg1, reg2	I	—	*	*	*	Multiplication of unsigned operands. reg1 and reg2 are multiplied together as unsigned values. The high-order 32 bits of the product (double word) are written into r30 and the low-order 32 bits are written into reg2.
NOP		III	—	—	—	—	No operation.
NOT	reg1, reg2	I	—	0	*	*	NOT. The NOT (one's complement) of reg1 is taken and written into reg2.
OR	reg1, reg2	I	—	0	*	*	OR. The OR of reg2 and reg1 is taken and written into reg2.
ORI	imm16, reg1, reg2	V	—	0	*	*	OR. The OR of reg1 and imm16, zero-extended to a word, is taken and written into reg2.
OUT.B	reg2, disp16[reg1]	VI	—	—	—	—	Port output. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit port address. The low-order one byte of the data in reg2 is output to the resulting port address.
OUT.H	reg2, disp16[reg1]	VI	—	—	—	—	Port output. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit port address. The low-order two bytes of the data in reg2 are output to the resulting port address. Bit 0 of the unsigned 32-bit port address is masked to 0.
OUT.W	reg2, disp16[reg1]	VI	—	—	—	—	Port output. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit port address. The word of data in reg2 is output to the produced port address. Bits 0 and 1 of the unsigned 32-bit port address are masked to 0.
RETI		IX	*	*	*	*	Return from trap/interrupt handling routine. The return PC and PSW are read from the system registers so that program execution will return from the trap or interrupt handling routine.

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
SAR	reg1, reg2	I	*	0	*	*	Arithmetic right shift. reg2 is arithmetically shifted to the right by the displacement specified by the low-order five bits of reg1 (MSB value is copied to the MSB in sequence). The result is written into reg2.
	imm5, reg2	II	*	0	*	*	Arithmetic right shift. reg2 is arithmetically shifted to the right by the displacement specified by imm5, zero-extended to a word. The result is written into reg2.
SATADD3	reg1, reg2, reg3	VIII	*	*	*	*	Saturation addition. reg1 and reg2 are added together as signed integers. [If no overflow has occurred:] The result is written into reg3. [If an overflow has occurred:] The SAT flag is set. If the result is positive, the positive maximum is written into reg3; if the result is negative, the negative maximum is written into reg3.
SATSUB3	reg1, reg2, reg3	VIII	*	*	*	*	Saturation subtraction. reg1 is subtracted from reg2 as signed integers. [If no overflow has occurred:] The result is written into reg3. [If an overflow has occurred:] The SAT flag is set. If the result is positive, the positive maximum is written into reg3; if the result is negative, the negative maximum is written into reg3.
SETF	imm5, reg2	II	—	—	—	—	Set flag condition. reg2 is set to 1 if the condition specified by the low-order four bits of imm5 matches the condition flag; otherwise it is set to 0.
SHL	reg1, reg2	I	*	0	*	*	Logical left shift. reg2 is logically shifted to the left (0 is put on the LSB) by the displacement specified by the low-order five bits of reg1. The result is written into reg2.
	imm5, reg2	II	*	0	*	*	Logical left shift. reg2 is logically shifted to the left by the displacement specified by imm5, zero-extended to a word. The result is written into reg2.
SHLD3	reg1, reg2, reg3	VIII	—	—	—	—	Left shift of concatenation. The 64 bits consisting of reg3 (high order) and reg2 (low order) are logically shifted to the left by the displacement specified by the low-order five bits of reg1. The high-order 32 bits of the result are written into reg3.

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
SHR	reg1, reg2	I	*	0	*	*	Logical right shift. reg2 is logically shifted to the right by the displacement specified by the low-order five bits of reg1 (0 is put on the MSB). The result is written into reg2.
	imm5, reg2	II	*	0	*	*	Logical right shift. reg2 is logically shifted to the right by the displacement specified by imm5, zero-extended to a word. The result is written into reg2.
SHRD3	reg1, reg2, reg3	VIII	—	—	—	—	Right shift of concatenation. The 64 bits consisting of reg3 (high order) and reg2 (low order) are logically shifted to the right by the displacement specified by the low-order five bits of reg1. The low-order 32 bits of the result are written into reg3.
ST.B	reg2, disp16[reg1]	VI	—	—	—	—	Byte store. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit address. The low-order one byte of data in reg2 is stored at the resulting address.
ST.H	reg2, disp16[reg1]	VI	—	—	—	—	Halfword store. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit address. The low-order two bytes of the data in reg2 are stored at the resulting address. Bit 0 of the unsigned 32-bit address is masked to 0.
ST.W	reg2, disp16[reg1]	VI	—	—	—	—	Word store. disp16, sign-extended to a word, is added to reg1 to generate an unsigned 32-bit address. The word of data in reg2 is stored at the resulting address. Bits 0 and 1 of the unsigned 32-bit address are masked to 0.
STBY		IX	—	—	—	—	Processor stop. The processor is placed in stop mode.
STSR	regID, reg2	II	—	—	—	—	System register store. The contents of the system register identified by the system register number (regID) are set in reg2.
SUB	reg1, reg2	I	*	*	*	*	Subtraction. reg1 is subtracted from reg2. The difference is written into reg2.
TRAP	vector	II	—	—	—	—	Software trap. The return PC and PSW are saved in the system registers: PSW.EP = 1 → Save in FEPC, FEPSW PSW.EP = 0 → Save in EIPC, EIPSW The exception code is set in the ECR: PSW.EP = 1 → Set in FECC PSW.EP = 0 → Set in EICC PSW flags are set: PSW.EP = 1 → Set NP and ID PSW.EP = 0 → Set EP and ID Program execution jumps to the trap handler address corresponding to the trap vector (0-31) specified by vector and begins exception handling.

Instruction	Operand(s)	Format	CY	OV	S	Z	Function
XOR	reg1, reg2	I	—	0	*	*	Exclusive OR. The exclusive OR of reg2 and reg1 is taken and written into reg2.
XORI	imm16, reg1, reg2	V	—	0	*	*	Exclusive OR. The exclusive OR of reg1 and imm16, zero-extended to a word, is taken and written into reg2.

16. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
3.3-V operation supply voltage	V_{DDO}			–0.5 to +4.0	V
2.5-V operation supply voltage	V_{DDI}			–0.5 to +3.6	V
	V_{DDPLL}			–0.5 to +3.6	V
Input voltage[Note]	V_I	$V_{DDO} \geq 3.7$ V		–0.5 to +4.0	V
		$V_{DDO} < 3.7$ V		–0.5 to V_{DDO} + 0.3	
Clock input voltage	V_K			–0.5 to V_{DDO} + 0.3	V
Operating ambient temperature	T_A	μPD705102-143	CPU core frequency ≤ 143 MHz	–40 to +85	°C
★			CPU core frequency ≤ 144 MHz	–40 to +70	°C
★		μPD705102-133	CPU core frequency ≤ 133 MHz	–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note Includes output pins.

Cautions 1. Do not directly connect the output (or input/output) pins of an IC device to each other, and do not connect them directly to the V_{DD}, V_{CC} or GND. However, these restrictions do not apply to the high-impedance pins of an external circuit, whose timing has been specifically designed to avoid output collision.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. For IC products, normal operation and quality are guaranteed only when the ratings and conditions described under the DC and AC characteristics are satisfied.

Operating Conditions

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
3.3-V operation supply voltage	V_{DDO}			3.0	3.6	V
2.5-V operation supply voltage	V_{DDI}			2.3	2.7	V
Operating ambient temperature	T_A	μPD705102-143	CPU core frequency ≤ 143 MHz	–40	+85	°C
★			CPU core frequency ≤ 144 MHz	–40	+70	°C
★		μPD705102-133	CPU core frequency ≤ 133 MHz	–40	+85	°C

Caution V832 has two types of power supply, and there are no restrictions on the order that the voltage is to be applied. However, be sure not to keep a status whereby only one power supply is applied voltage for 1 second or more.

DC Characteristics (V_{DDO} = 3.0 to 3.6 V, V_{DDI} = 2.3 to 2.7 V)

(μPD705102-143 (CPU core frequency ≤ 143 MHz): T_A = –40 to +85°C
μPD705102-143 (CPU core frequency ≤ 144 MHz): T_A = –40 to +70°C
μPD705102-133: T_A = –40 to +85°C)

	Parameter		Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	Clock input voltage, low		V_{KL}	**Note 1**		–0.5		+0.2 V_{DDO}	V
	Clock input voltage, high		V_{KH}	**Note 1**		0.8 V_{DDO}		V_{DDO} + 0.3	V
	Input voltage, low		V_{IL}			–0.5		+0.6	V
	Input voltage, high		V_{IH}			2.0		V_{DDO} + 0.3	V
	Schmitt input voltage, low		V_{SL}	**Note 2**		–0.5		+0.2 V_{DDO}	V
	Schmitt input voltage, high		V_{SH}	**Note 2**		0.8 V_{DDO}		V_{DDO} + 0.3	V
	Output voltage, low		V_{OL}	I_{OL} = 3.2 mA				0.4	V
	Output voltage, high		V_{OH}	I_{OH} = –400 μA		0.85 V_{DDO}			V
	Input leakage current, low		I_{LIL}	V_{IN} = 0 V				–10	μA
	Input leakage current, high		I_{LIH}	V_{IN} = V_{DDO}				10	μA
	Output leakage current, low		I_{LOL}	V_O = 0 V				–10	μA
	Output leakage current, high		I_{LOH}	V_O = V_{DDO}				10	μA
★	Supply current**Note 3**	2.5 V	I_{DDI}	In normal operation (PLL mode)	Clock division ratio 1/1		115	160	mA
					Clock division ratio 1/2		60		mA
					Clock division ratio 1/4		33		mA
				In normal operation (Direct mode)	Clock division ratio 1/1		15		mA
					Clock division ratio 1/2		7.5		mA
				In HALT mode			20	29	mA
★				In STOP mode**Note 4**			25	450	μA
		3.3 V	I_{DDO}	In normal operation (PLL mode)	Clock division ratio 1/1		19	28	mA
					Clock division ratio 1/2		10		mA
					Clock division ratio 1/4		6		mA
				In normal operation (Direct mode)	Clock division ratio 1/1		4		mA
					Clock division ratio 1/2		3		mA
				In HALT mode			12	20	mA
				In STOP mode**Note 4**			5	10	μA

Notes 1. X2 pin, DCK pin, and $\overline{SCLK}$ pin at external clock input

2. PORT0/$\overline{SCLK}$, PORT2/SI, PORT3/RXD

3. Supply current at input clock: 17.85 MHz with output pins open, PLL 8×

4. External clock mode when clock input is stopped.

Capacitance

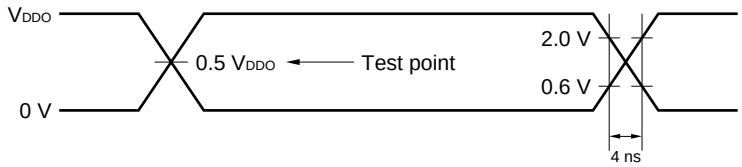
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		10	pF
I/O capacitance	C_{IO}			10	pF

Remark These parameters are sample values, not the value actually measured.

AC Characteristics (V_{DDO} = 3.0 to 3.6 V, V_{DDI} = 2.3 to 2.7 V, C_L = 50 pF)

μPD705102-143 (CPU core frequency ≤ 143 MHz): T_A = –40 to +85°C
μPD705102-143 (CPU core frequency ≤ 144 MHz): T_A = –40 to +70°C
μPD705102-133 : T_A = –40 to +85°C

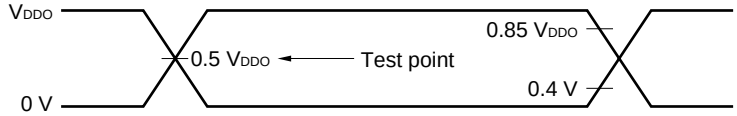
AC test input waveform



AC test output waveform

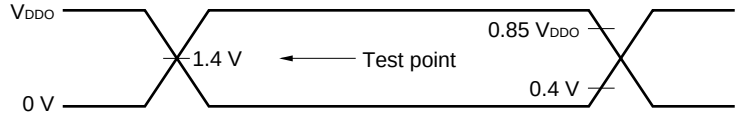
(a) $\overline{CS0}$, $\overline{CS1}$, $\overline{WE}$, $\overline{RAS}$, UUDQM, ULDQM, LUDQM, LLDQM, CKE, $\overline{CAS}$, SDCLKOUT, CLKOUT, A1 to A23, D0 to D31

★

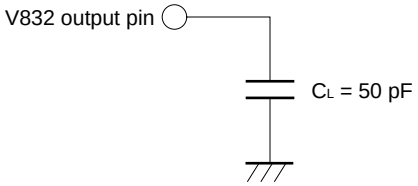


(b) Other than above (a)

★



Test load



★ **(1) Clock input (X2) timing (when external clock input used)**

- **μPD705102-143**

Parameter	Symbol		Conditions	PLL Magnification				Unit
				×6 mode		×8 mode		
				MIN.	MAX.	MIN.	MAX.	
External clock cycle	<1>	t_{CYX}	**Note 1**	42	60	56	80	ns
			Note 2		45		60	ns
			Note 3	41.6	60	55.5	80	ns
			Note 4		45		60	ns
External clock high-level time	<2>	t_{XXH}	**Note 1**	16		23		ns
			Note 3	15.8		22.75		ns
External clock low-level time	<3>	t_{XXL}	**Note 1**	16		23		ns
			Note 3	15.8		22.75		ns
External clock rise time	<4>	t_{XR}			5		5	ns
External clock fall time	<5>	t_{XF}			5		5	ns

Notes 1. T_A = –40 to +85°C, when other than 1/4 is selected as the division ratio of the input clock (CPU core frequency (when defaulted) = 100 to 143 MHz)

2. T_A = –40 to +85°C, when 1/4 is selected as the division ratio of the input clock (CPU core frequency = 33.3 to 35.8 MHz)

3. T_A = –40 to +70°C, when other than 1/4 is selected as the division ratio of the input clock (CPU core frequency (when defaulted) = 100 to 144 MHz)

4. T_A = –40 to +70°C, when 1/4 is selected as the division ratio of the input clock (CPU core frequency = 33.3 to 36 MHz)

Remark The stability of the input clock is 0.1% of t_{CYX} or lower.

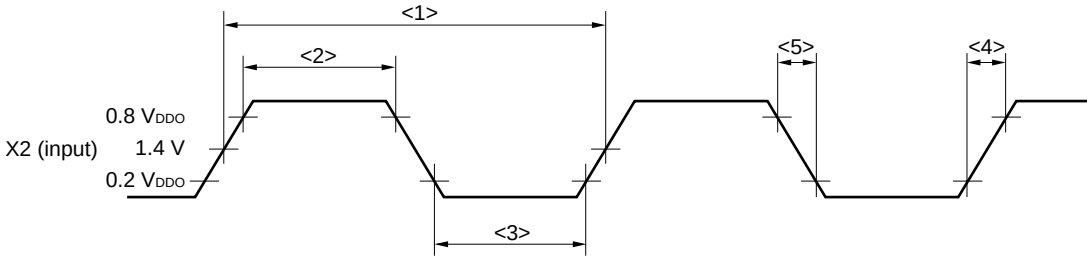
- **μPD705102-133**

Parameter	Symbol		Conditions	PLL Magnification				Unit
				×6 mode		×8 mode		
				MIN.	MAX.	MIN.	MAX.	
External clock cycle	<1>	t_{CYX}	**Note 1**	45	60	60	80	ns
			Note 2		45		60	ns
External clock high-level time	<2>	t_{XXH}		17.5		25		ns
External clock low-level time	<3>	t_{XXL}		17.5		25		ns
External clock rise time	<4>	t_{XR}			5		5	ns
External clock fall time	<5>	t_{XF}			5		5	ns

Notes 1. T_A = –40 to +85°C, when other than 1/4 is selected as the division ratio of the input clock (CPU core frequency (when defaulted) = 100 to 133 MHz)

2. T_A = –40 to +85°C, when 1/4 is selected as the division ratio of the input clock (CPU core frequency = 33.3 MHz)

Remark The stability of the input clock is 0.1% of t_{CYX} or lower.



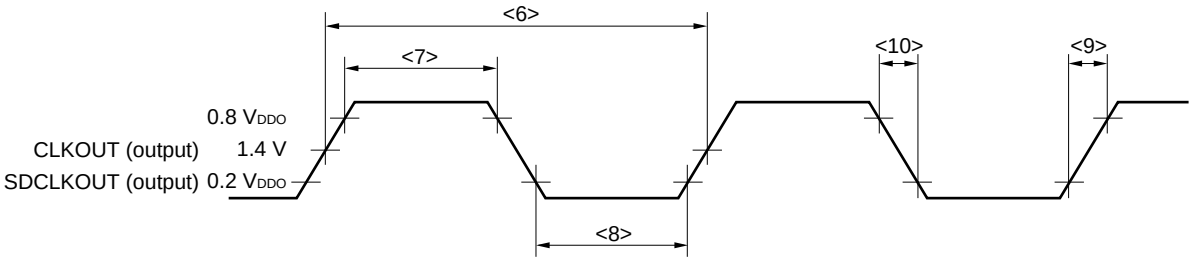
(2) Clock output timing (CLKOUT, SDCLKOUT)

	Parameter	Symbol		Conditions	PLL Magnification				Unit
					×6 mode		×8 mode		
					MIN.	MAX.	MIN.	MAX.	
	External clock cycle	<6>	t_{CYK}	**Note 1**	21		28		ns
★				**Note 2**	20.8		27.75		ns
★				**Note 3**	22.5		30		ns
	External clock high-level time	<7>	t_{KKH}		$t_{CYK}/2 - 5$		$t_{CYK}/2 - 5$		ns
	External clock low-level time	<8>	t_{KKL}		$t_{CYK}/2 - 5$		$t_{CYK}/2 - 5$		ns
	External clock rise time	<9>	t_{KR}			5		5	ns
	External clock fall time	<10>	t_{KF}			5		5	ns

Notes 1. μPD705102-143, T_A = –40 to +85°C

2. μPD705102-143, T_A = –40 to +70°C

3. μPD705102-133, T_A = –40 to +85°C



(3) Reset timing

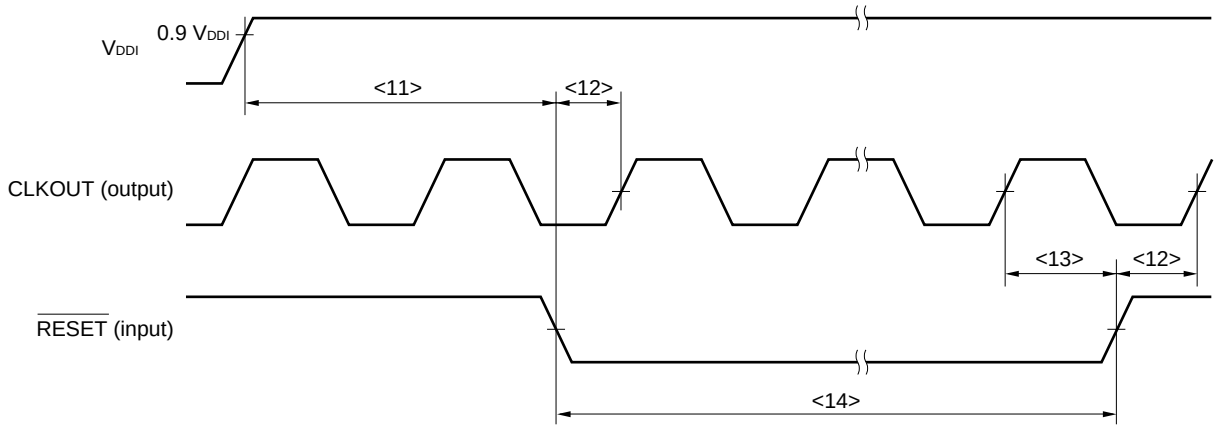
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ hold time (from V_{DDI} VALID)	<11>	t_{HVR}			2	μs
$\overline{\text{RESET}}$ setup time (to CLKOUT↑)	<12>	t_{SRK}		7		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↑)	<13>	t_{HKR}		7		ns
$\overline{\text{RESET}}$ pulse low-level width	<14>	t_{WRL}	**Note 1**	20		ms
			Note 2	10		ms
			Note 3	15 × t_{CYX}		ns

Notes 1. At power on or when returned from STOP mode, and the internal clock is generated.

2. At power on or when returned from STOP mode, and the external clock is generated, after clock has stabilized.

3. When clock has stabilized under conditions other than Notes 1 and 2.

Remark It is not necessary to satisfy t_{SRK} and t_{HKR} if reset during the period of t_{HVR}. In such a case, however, the reset acknowledge timing may be shifted.

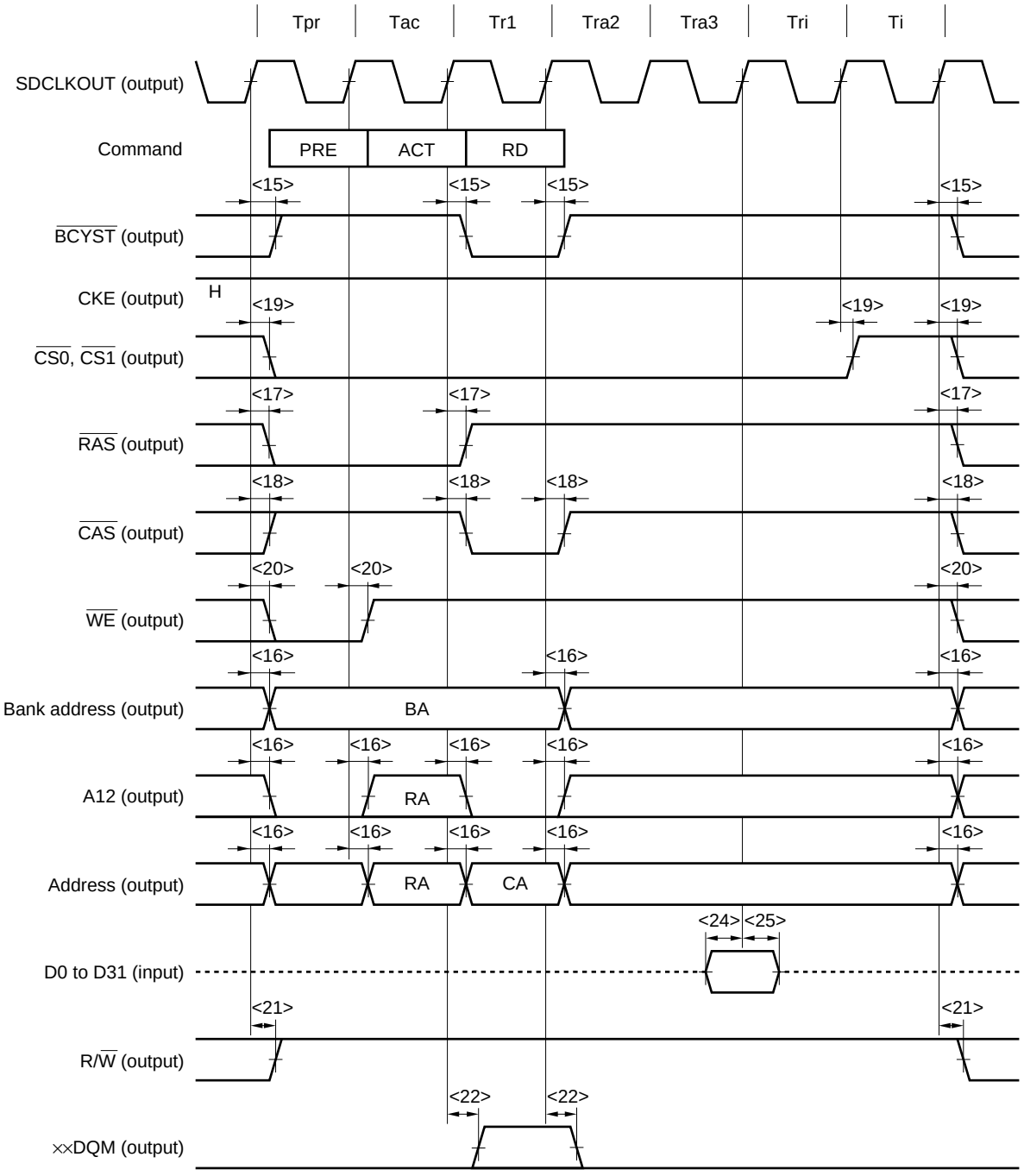


(4) SDRAM access timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{BCYST}$ delay time (from SDCLKOUT↑)	<15>	t_{DKBC}		2	12.5	ns
Address delay time (from SDCLKOUT↑)	<16>	t_{DKA}		2	12.5	ns
$\overline{RAS}$ delay time (from SDCLKOUT↑)	<17>	t_{DKRAS}		2	12.5	ns
$\overline{CAS}$ delay time (from SDCLKOUT↑)	<18>	t_{DKCAS}		2	12.5	ns
$\overline{CS0}$, $\overline{CS1}$ delay time (from SDCLKOUT↑)	<19>	t_{DKCS}		2	12.5	ns
$\overline{WE}$ delay time (from SDCLKOUT↑)	<20>	t_{DKWE}		2	12.5	ns
R/$\overline{W}$ delay time (from SDCLKOUT↑)	<21>	t_{DKRW}		2	12.5	ns
××DQM delay time (from SDCLKOUT↑)	<22>	t_{DKDQM}		2	12.5	ns
CKE delay time (from SDCLKOUT↑)	<23>	t_{DKCKE}		2	12.5	ns
Data input setup time (SDRAM read, to SDCLKOUT↑)	<24>	t_{SDRMK}		5		ns
Data input hold time (SDRAM read, from SDCLKOUT↑)	<25>	t_{HKDRM}		2		ns
Data output delay time (from active, from SDCLKOUT↑)	<26>	t_{DKDT}		2	12.5	ns
Data output delay time (from float, from SDCLKOUT↑)	<27>	t_{LZKDT}		2	12.5	ns
Data float delay time (from SDCLKOUT↑)	<28>	t_{HZKDT}		3	20	ns

Remark ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

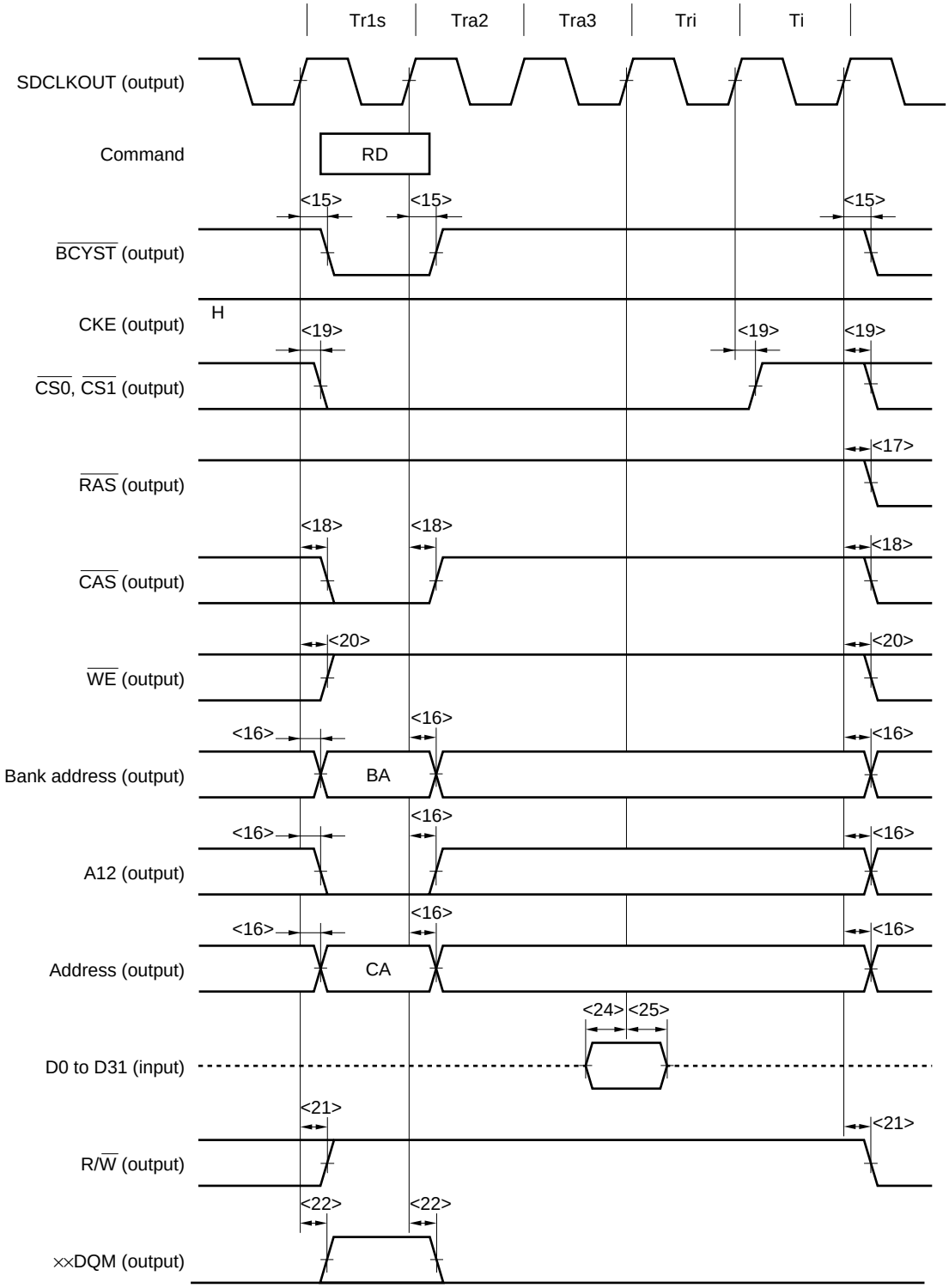
SDRAM single read cycle (off-page) (TRP = 0, TRCD = 0): with 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

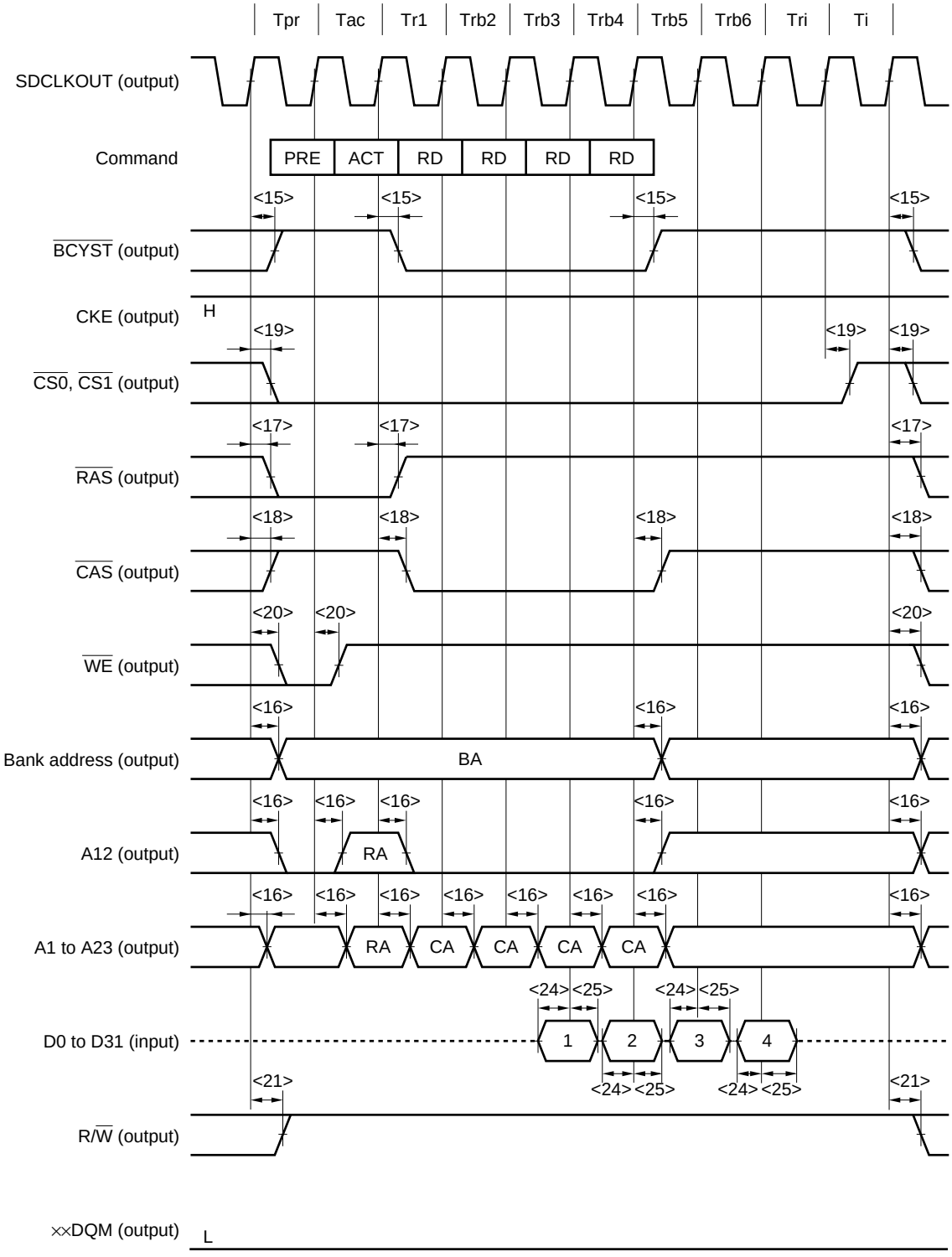
SDRAM single read cycle (on-page): with 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

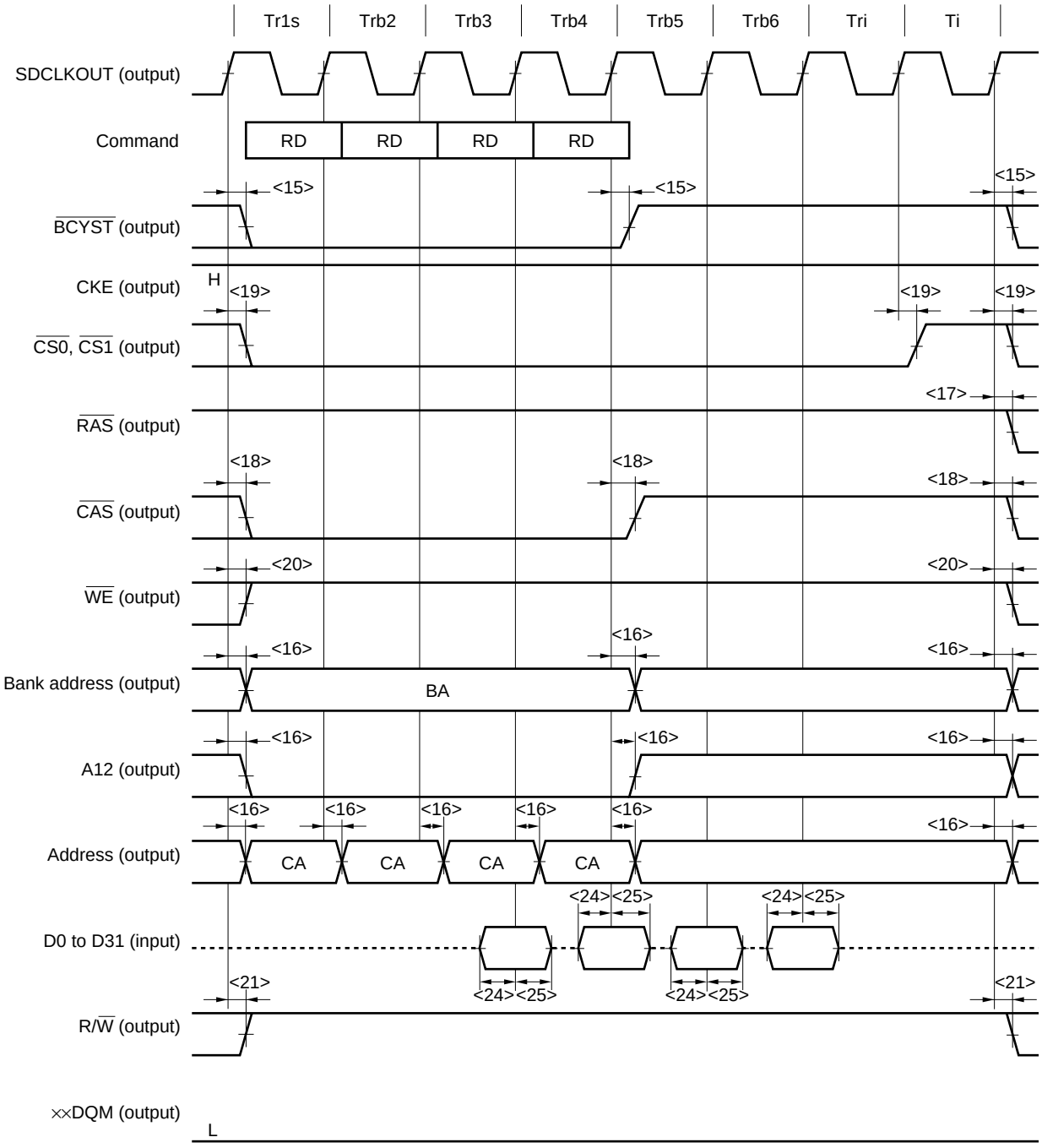
SDRAM burst read cycle (off-page) (TRP = 0, TRCD = 0): with 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

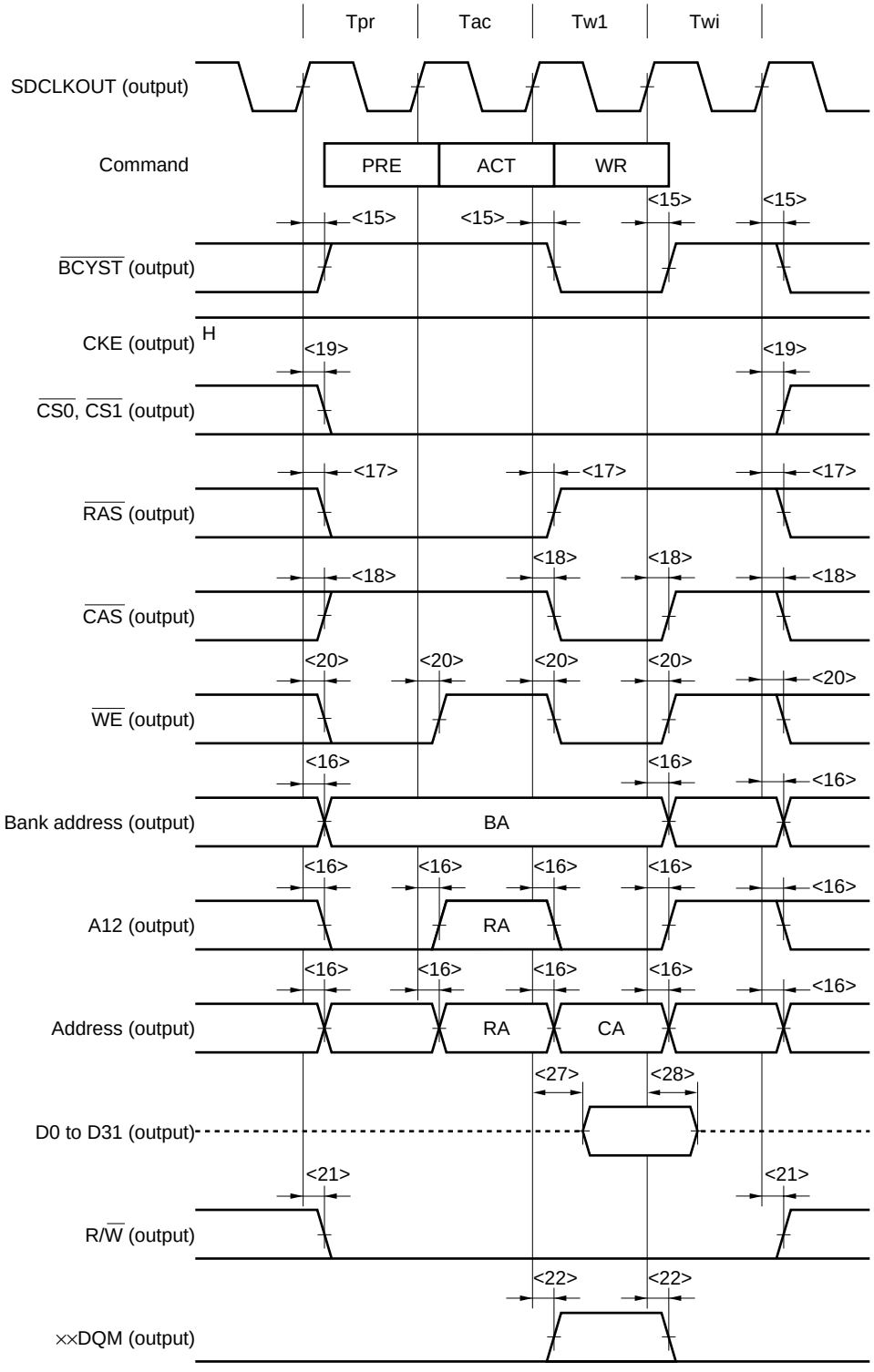
SDRAM burst read cycle (on-page): with 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

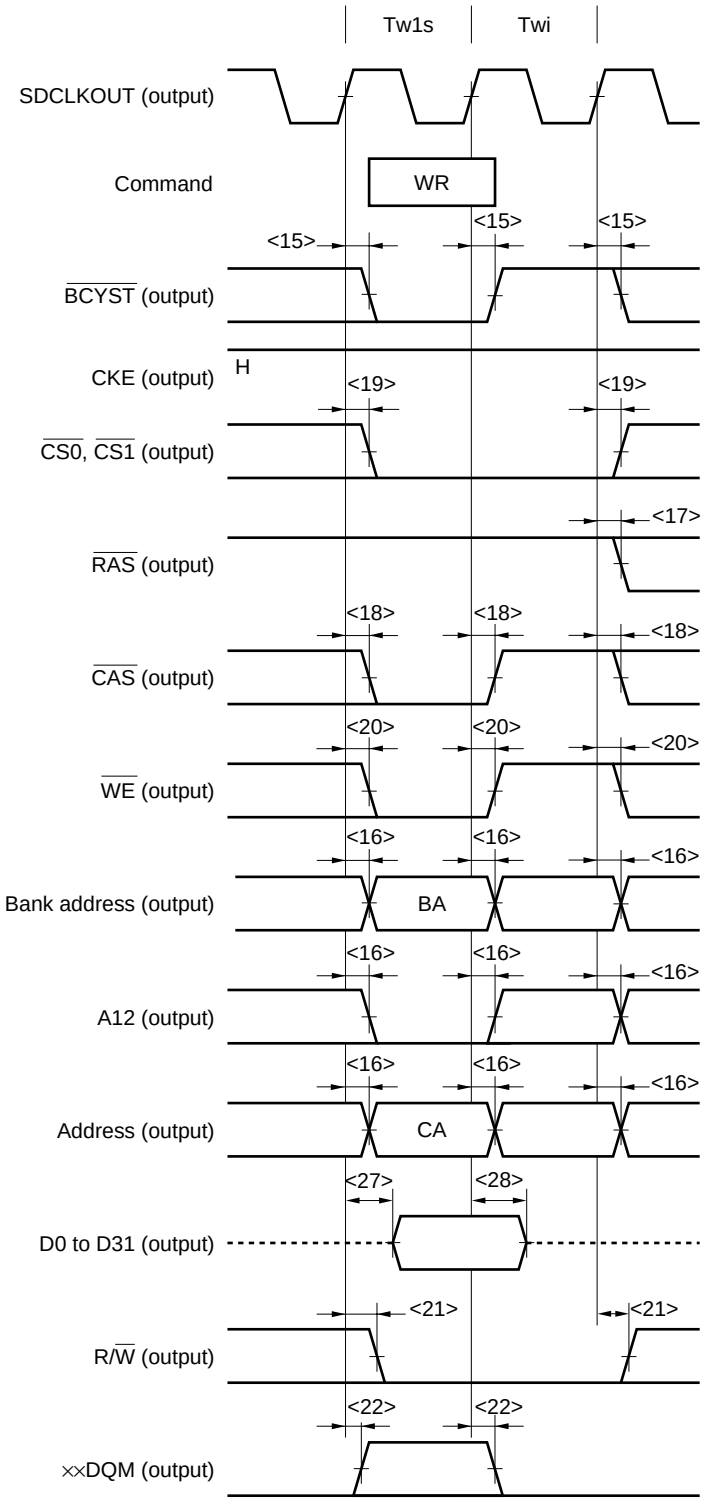
SDRAM single write cycle (off-page) (TRP = 0, TRCD = 0): with 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

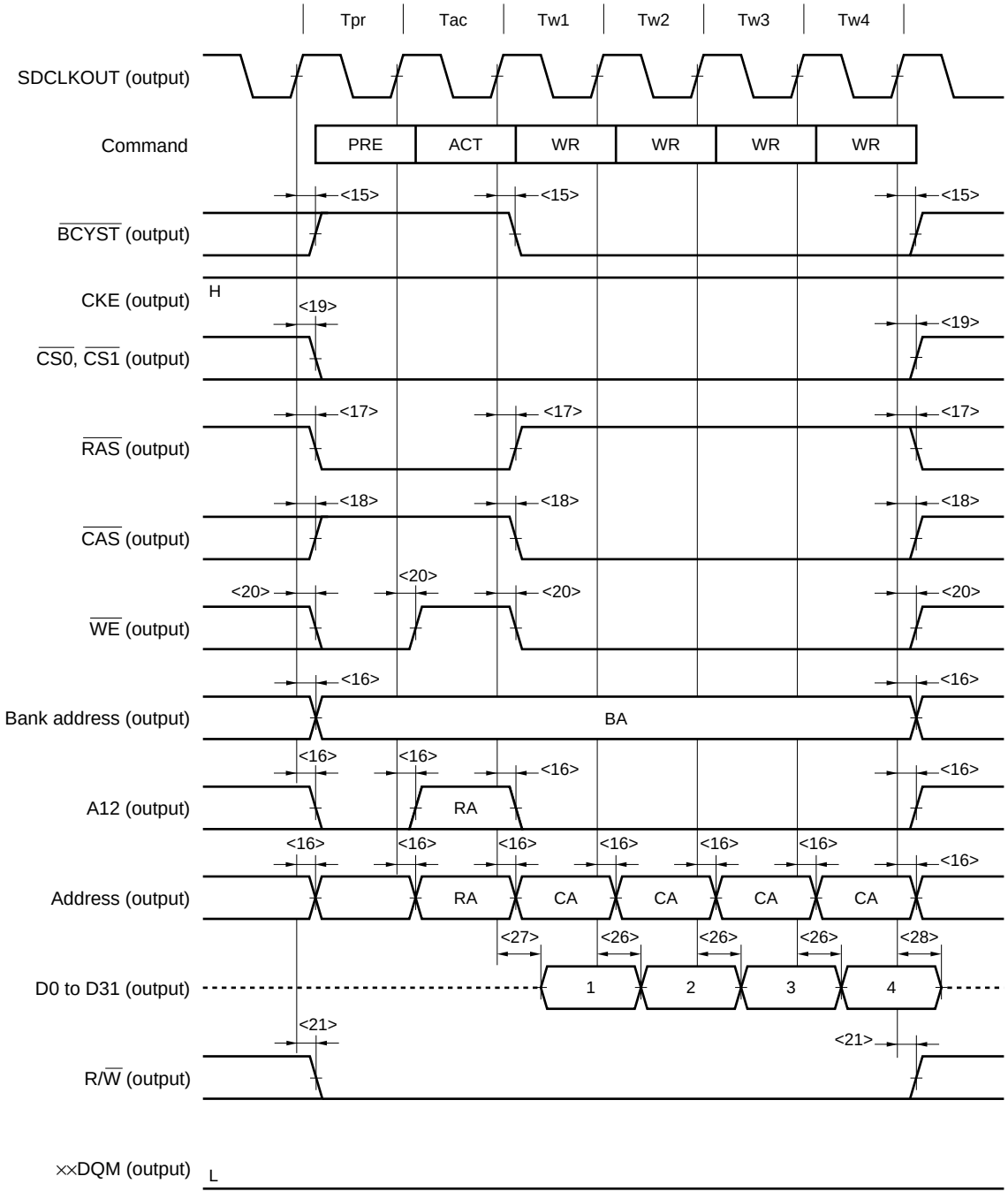
SDRAM single write cycle (on-page): with 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

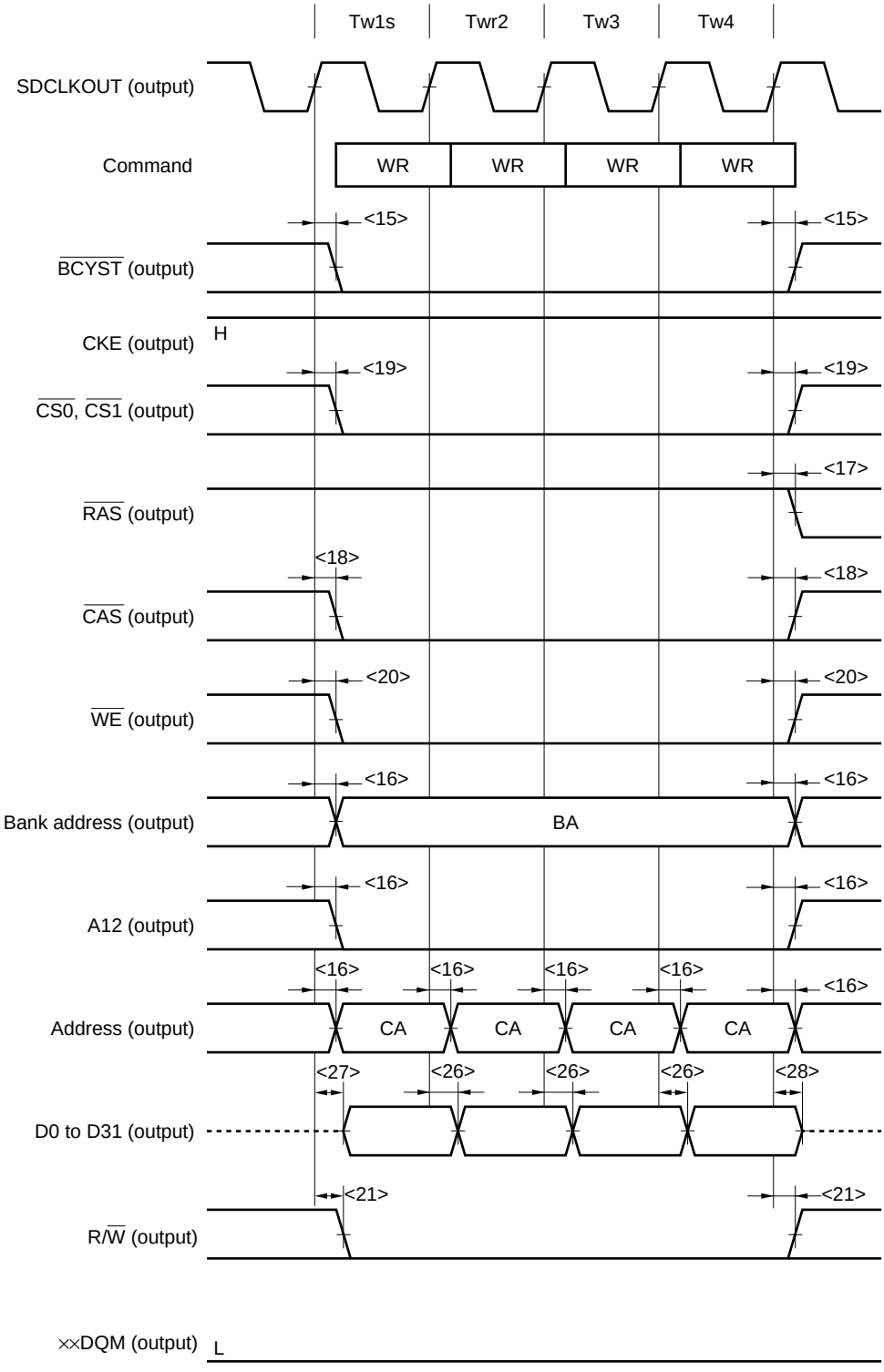
SDRAM burst write cycle (off-page) (TRP = 0, TRCD = 0): with 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

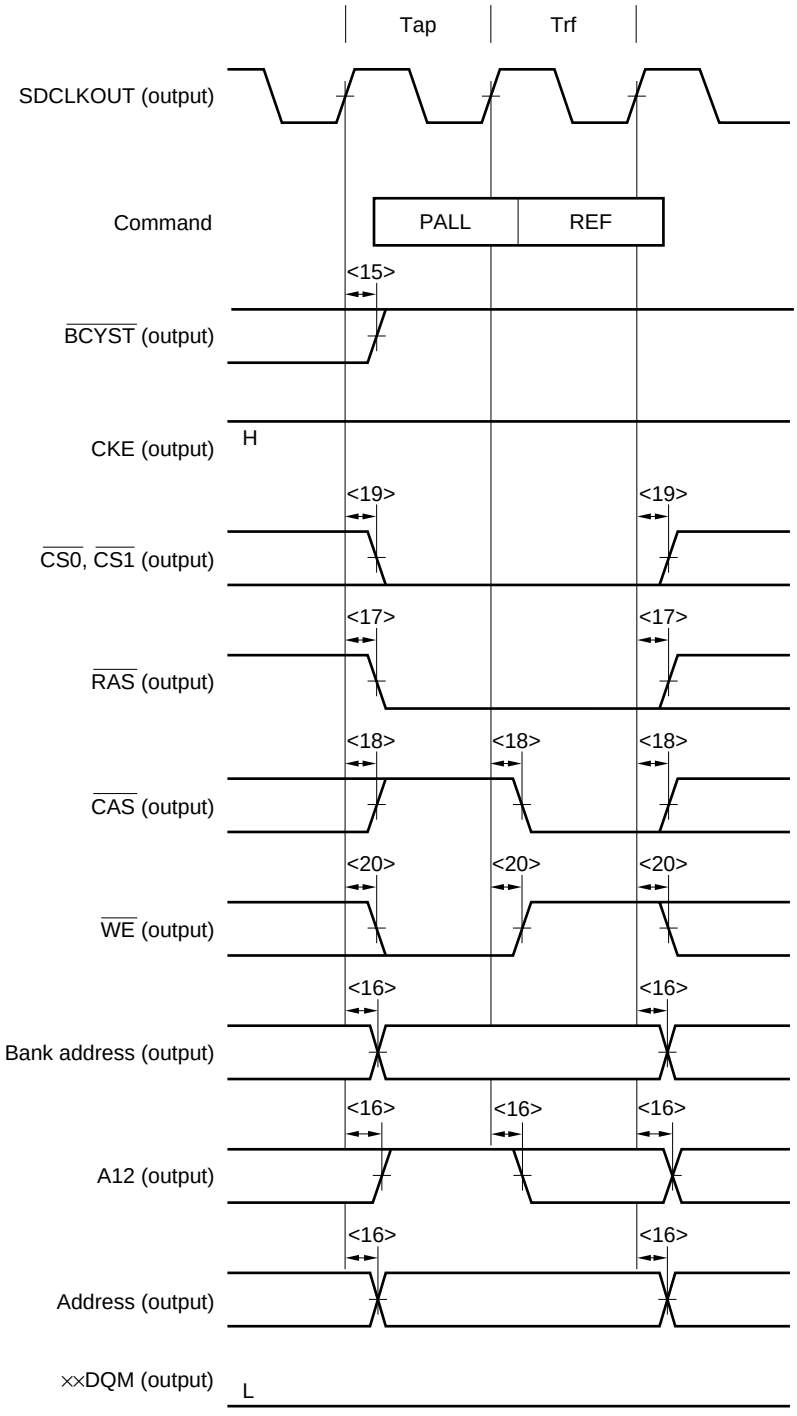
SDRAM burst write cycle (on-page): with 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

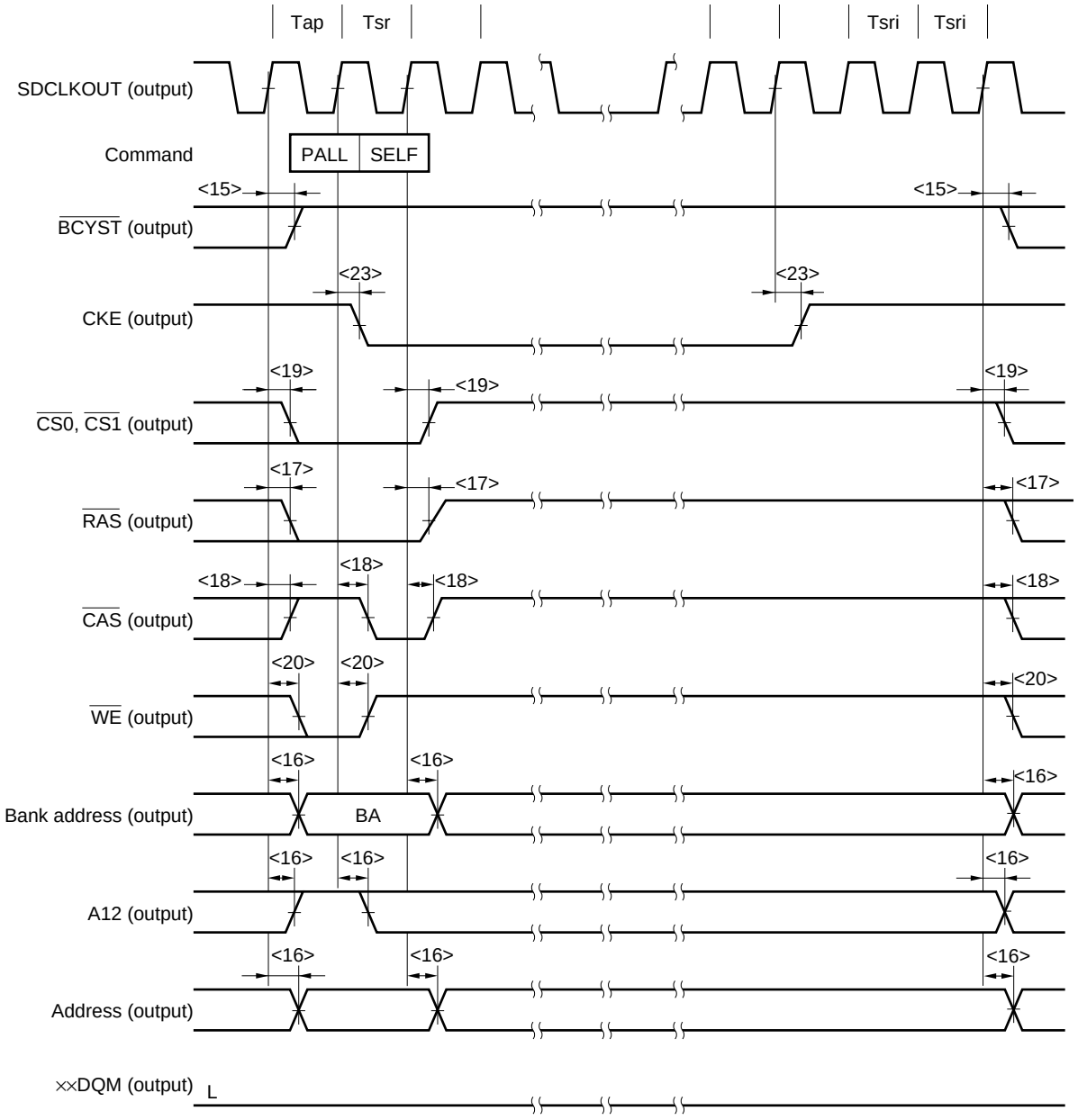
2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

Auto refresh cycle (TRP = 0): with 32-bit data bus



Remark ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

Self refresh cycle (TRP = 0): with 32-bit data bus



Remark ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

(5) Access timing of SRAM, Page-ROM and I/O

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{BCYST}}$ delay time (from CLKOUT↑)	<15>	t_{DKBC}		2	12.5	ns
Address delay time (from CLKOUT↑)	<16>	t_{DKA}		2	12.5	ns
$\overline{\text{CSn}}$**Note** delay time (from CLKOUT↑)	<19>	t_{DKCS}		2	12.5	ns
R/$\overline{\text{W}}$ delay time (from CLKOUT↑)	<21>	t_{DKRW}		2	12.5	ns
Data output delay time (from active, from CLKOUT↑)	<26>	t_{DKDT}		2	12.5	ns
Data output delay time (from float, from CLKOUT↑)	<27>	t_{LZKDT}		2	12.5	ns
Data float delay time (from CLKOUT↑)	<28>	t_{HZKDT}		3	20	ns
$\overline{\text{IORD}}$ output delay time (from CLKOUT↓)	<29>	t_{DKRD}		2	12.5	ns
$\overline{\text{MRD}}$ output delay time (from CLKOUT↓)	<30>	t_{DKMRD}		2	12.5	ns
$\overline{\text{IOWR}}$ output delay time (from CLKOUT↓)	<31>	t_{DKWR}		2	12.5	ns
$\overline{\text{MWR}}$ output delay time (from CLKOUT↓)	<32>	t_{DKMWR}		2	12.5	ns
$\overline{\times\times\text{BEN}}$ delay time (from CLKOUT↓)	<33>	t_{DKBEN}		2	12.5	ns
Data input setup time (to CLKOUT↓)	<34>	t_{SDTK}		5		ns
Data input hold time (from CLKOUT↓)	<35>	t_{HKDT}		2		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	<36>	t_{SRYK}		7		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	<37>	t_{HKRY}		3		ns

Note $\overline{\text{CSn}}$ indicates $\overline{\text{CS1}}$ through $\overline{\text{CS7}}$. Depending on the n value, a different area is used.

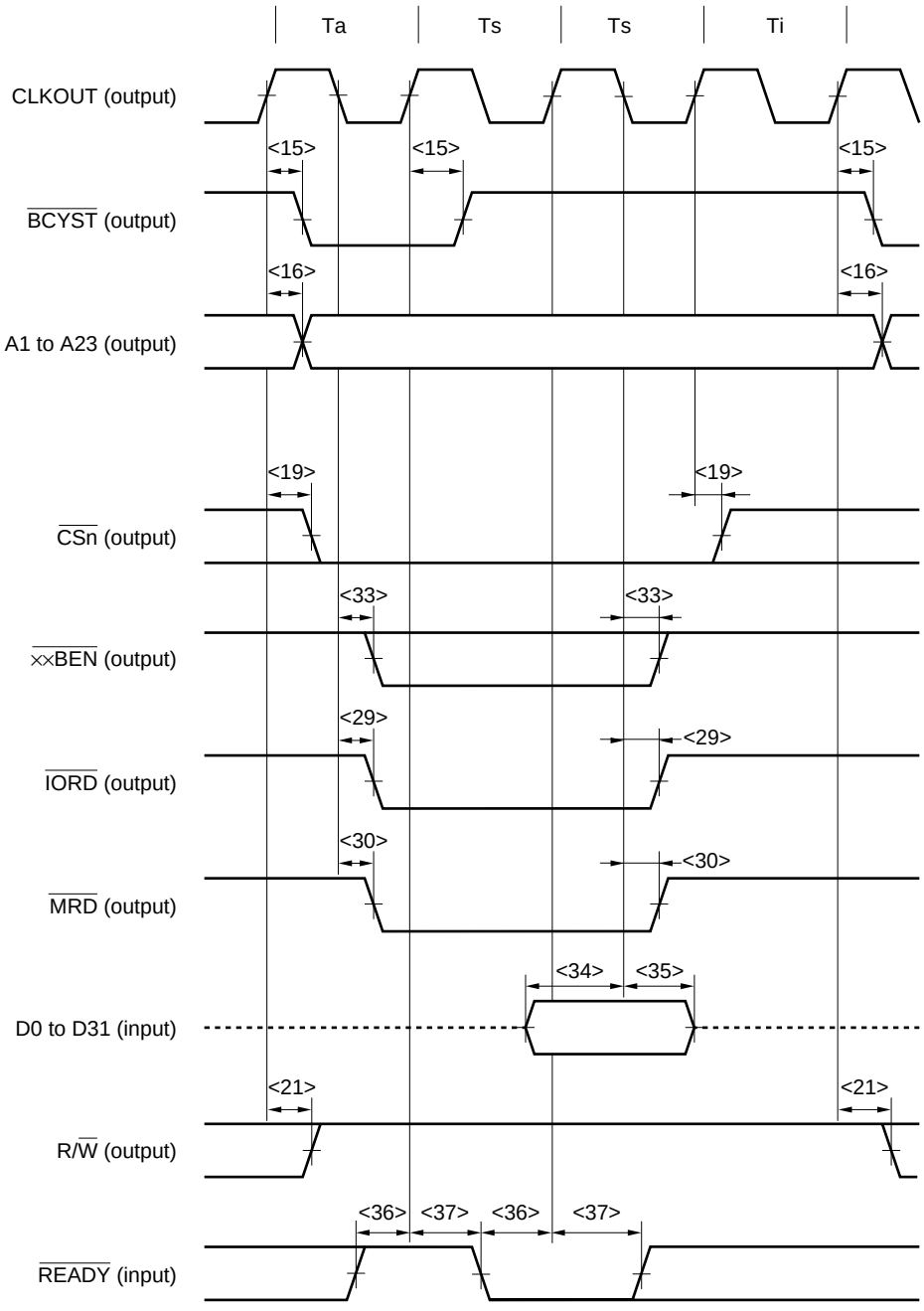
n = 1 to 7: When SRAM (ROM) is selected

n = 7: When Page-ROM is selected

n = 3 to 6: When I/O is selected

Remark $\overline{\times\times\text{BEN}}$: $\overline{\text{LLBEN}}$, $\overline{\text{LUBEN}}$, $\overline{\text{ULBEN}}$, $\overline{\text{UUBEN}}$

SRAM (ROM), Page-ROM single read cycle
I/O read timing



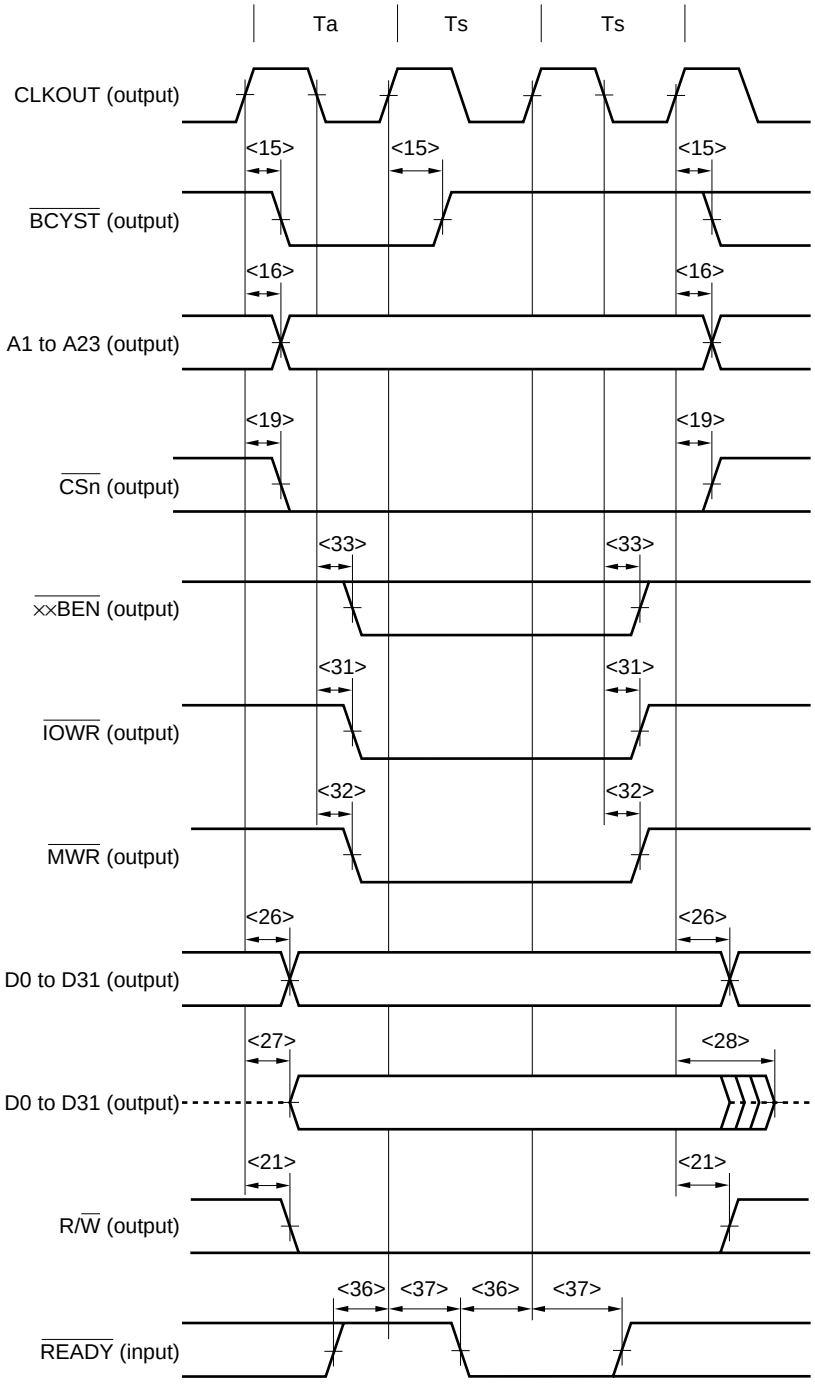
Remarks 1. The broken lines indicate high impedance.

2. n = 1 to 7

3. ××BEN: LLBEN, LUBEN, ULBEN, UUBEN

SRAM (ROM) single write cycle

I/O write timing

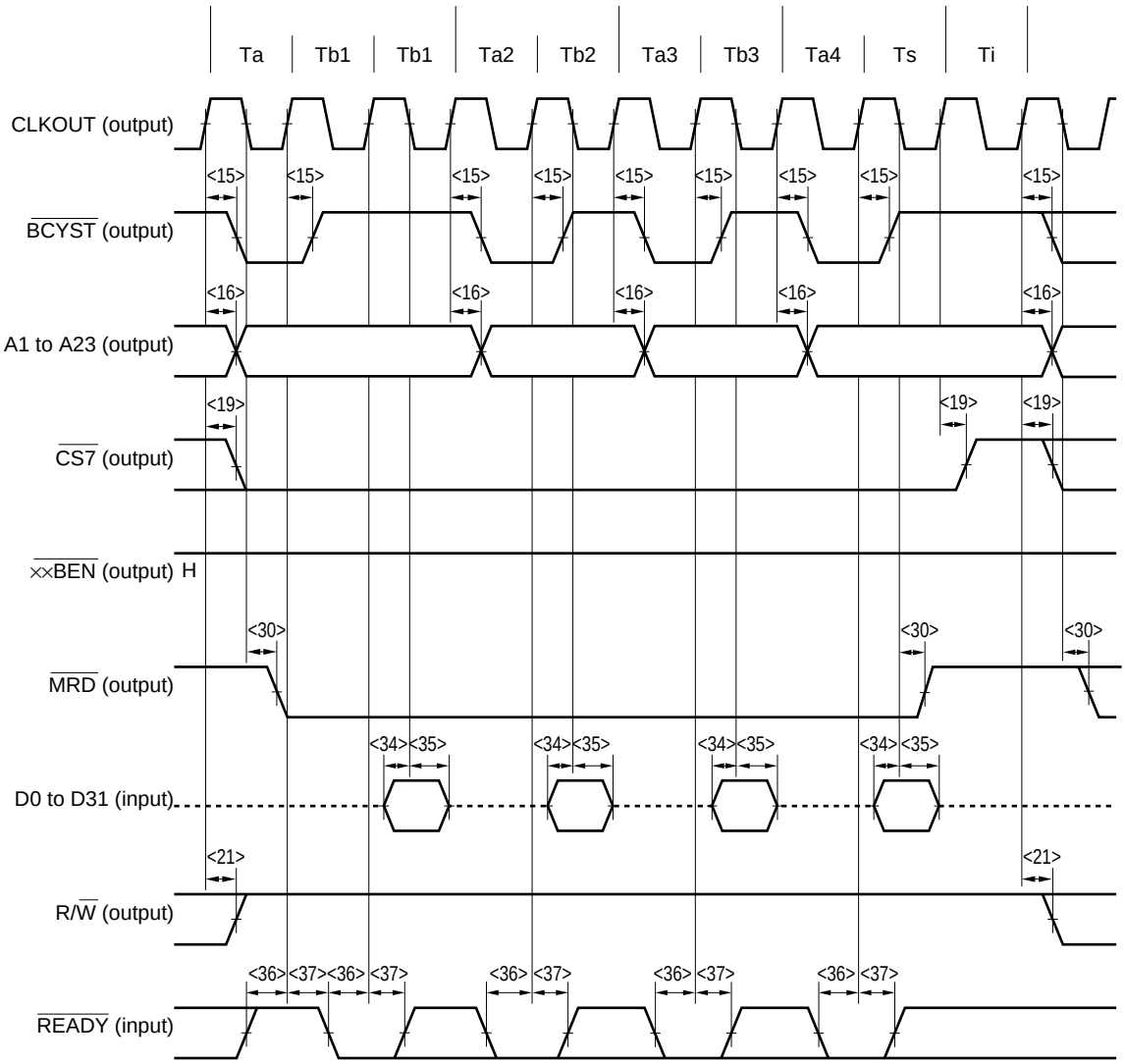


Remarks 1. The broken lines indicate high impedance.

2. n = 1 to 7

3. ××BEN: LLBEN, LUBEN, ULBEN, UUBEN

Page-ROM burst read cycle (with 32-bit data bus)



Remarks 1. The broken lines indicate high impedance.

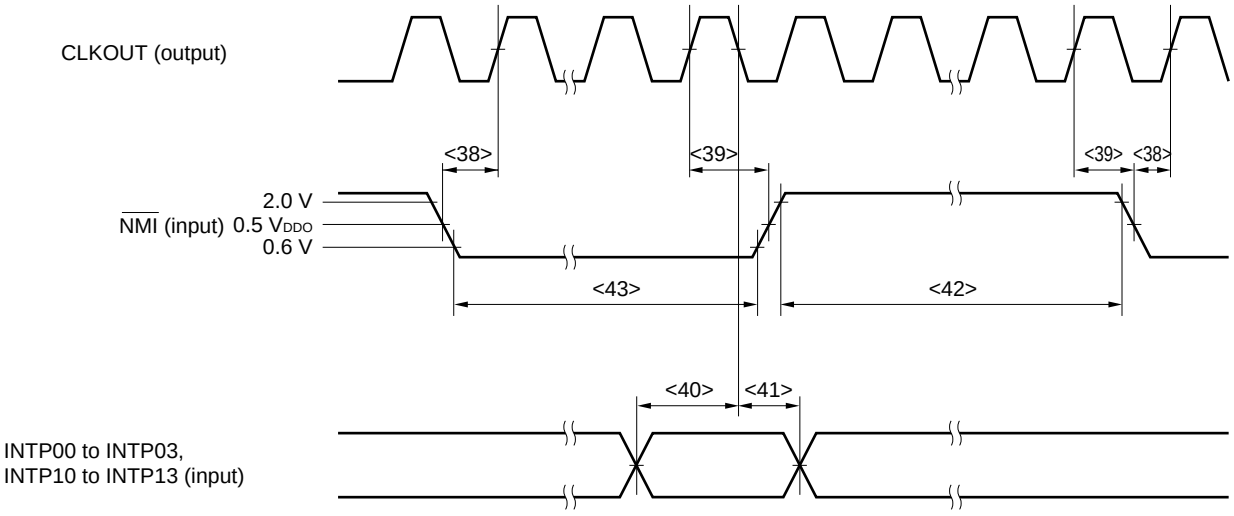
2. ××BEN: LLBEN, LUBEN, ULBEN, UUBEN

(6) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{NMI}$ setup time (to CLKOUT↑)	<38>	t_{SNK}		5		ns
$\overline{NMI}$ hold time (from CLKOUT↑)	<39>	t_{HKN}		7		ns
INTPxx setup time (to CLKOUT↓)	<40>	t_{SIK}		7		ns
INTPxx hold time (from CLKOUT↓)	<41>	t_{HKI}		3		ns
$\overline{NMI}$ high-level time	<42>	t_{NMH}		5T + 12		ns
$\overline{NMI}$ low-level time	<43>	t_{NML}		5T + 12		ns

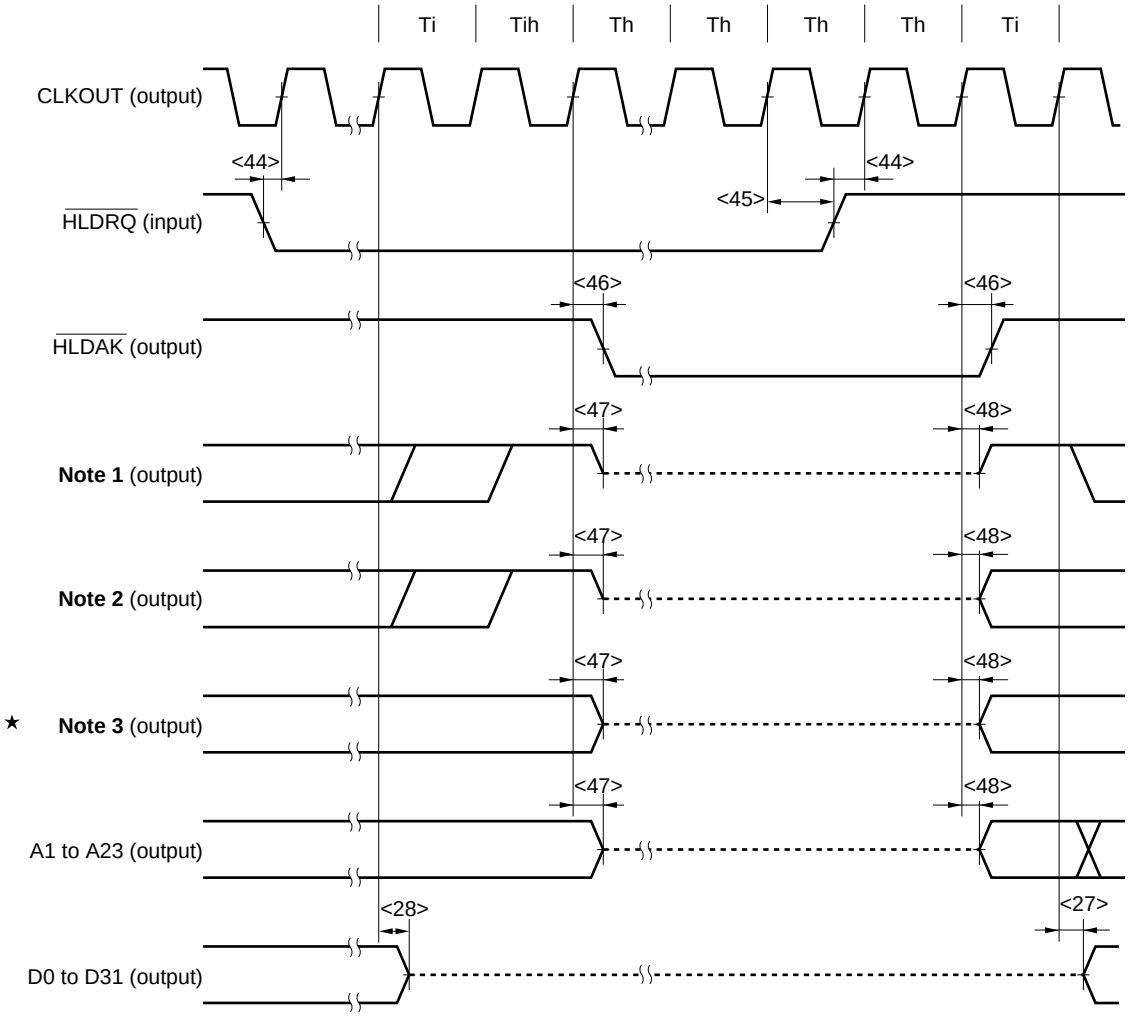
Remarks 1. T = t_{CYK} (external clock cycle)

2. Even if t_{SNK} and t_{HKN} are set to other than the above range, the NMI interrupt can be acknowledged, however, in this case NMI acknowledge timing may be delayed.



(7) Bus hold timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Data active delay time (from CLKOUT↑)	<27>	t_{LZKDT}		2	12.5	ns
Data float delay time (from CLKOUT↑)	<28>	t_{HZKDT}		3	20	ns
$\overline{\text{HLDRQ}}$ input setup time (to CLKOUT↑)	<44>	t_{SHQK}		7		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT↑)	<45>	t_{HKHQ}		3		ns
$\overline{\text{HLDAK}}$ output delay time (from CLKOUT↑)	<46>	t_{DKHA}		2	12.5	ns
Address float delay time (from CLKOUT↑)	<47>	t_{HZKA}		3	20	ns
Address active delay time (from CLKOUT↑)	<48>	t_{LZKA}		2	12.5	ns



Notes 1. $\overline{\text{BCYST}}$, $\overline{\text{WE}}$, $\overline{\text{CS0}}$ to $\overline{\text{CS7}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{MRD}}$, $\overline{\text{MWR}}$, CKE

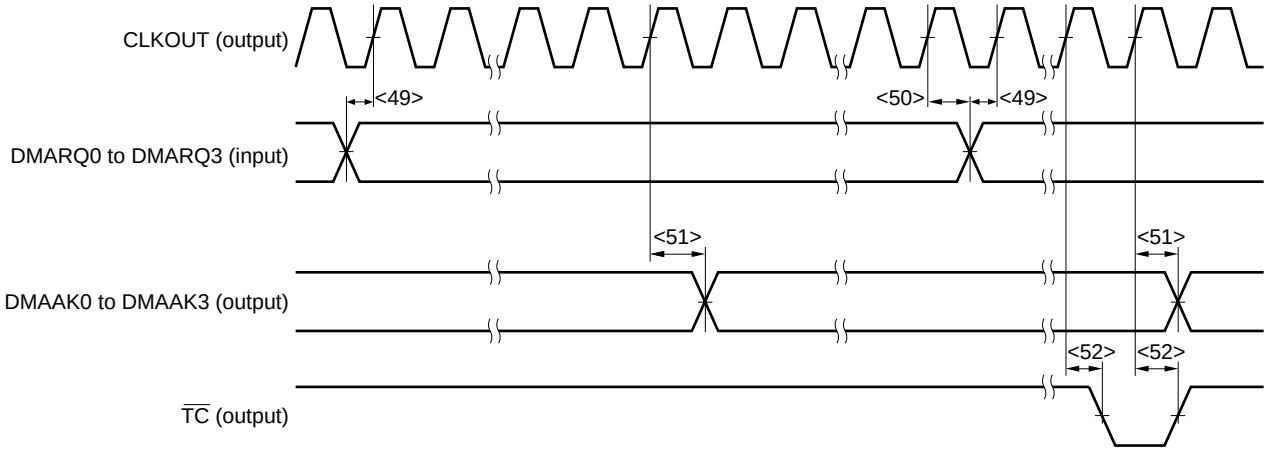
2. R/$\overline{\text{W}}$, $\overline{\text{LLBEN}}$, $\overline{\text{LUBEN}}$, $\overline{\text{ULBEN}}$, $\overline{\text{UUBEN}}$

3. LLDQM, LUDQM, ULDQM, UUDQM

Remark The broken lines indicate high impedance.

(8) DMA timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
DMARQ input setup time (to CLKOUT↑)	<49>	t_{SDQK}		7		ns
DMARQ hold time (from CLKOUT↑)	<50>	t_{HKDQ}		3		ns
DMAAK output delay time	<51>	t_{DKDAK}		2	12.5	ns
$\overline{TC}$ output delay time	<52>	t_{DKTC}		2	12.5	ns

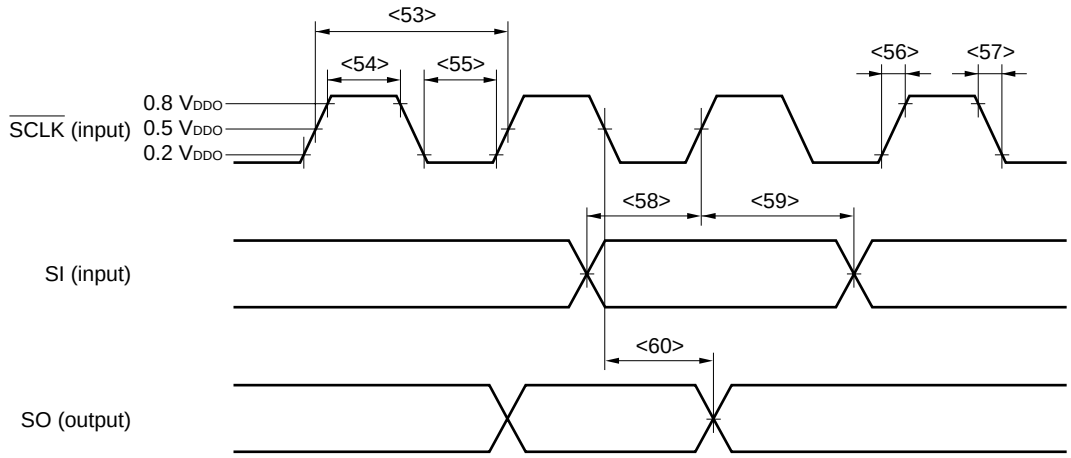


(9) CSI timing

(a) $\overline{\text{SCLK}}$ input mode

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
★	$\overline{\text{SCLK}}$ cycle	<53>	t_{CYSI}		4T		ns
	$\overline{\text{SCLK}}$ high-level time	<54>	t_{SIH}		t_{CYSI}/2 – 10		ns
	$\overline{\text{SCLK}}$ low-level time	<55>	t_{SIL}		t_{CYSI}/2 – 10		ns
	$\overline{\text{SCLK}}$ rise time	<56>	t_{SIR}			10	ns
	$\overline{\text{SCLK}}$ fall time	<57>	t_{SIF}			10	ns
	SI input setup time (to $\overline{\text{SCLK}}\uparrow$)	<58>	t_{SDTS}		21		ns
	SI input hold time (from $\overline{\text{SCLK}}\uparrow$)	<59>	t_{HSDT}		21		ns
	SO output delay time (from $\overline{\text{SCLK}}\downarrow$)	<60>	t_{DSDT}		2	21	ns

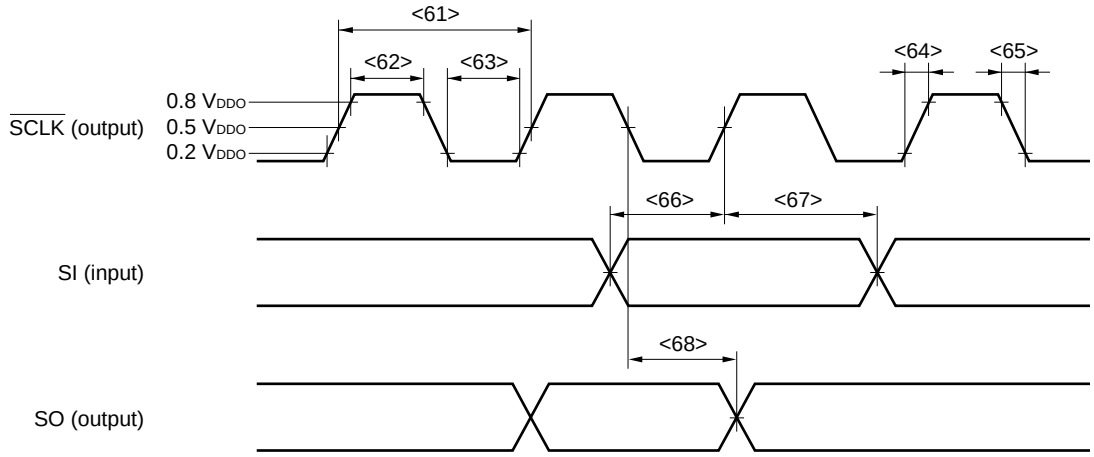
Remark T = t_{CYK} (external clock cycle)



(b) $\overline{\text{SCLK}}$ output mode

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
★	$\overline{\text{SCLK}}$ cycle	<61>	t_{CYSO}		4T		ns
	$\overline{\text{SCLK}}$ high-level time	<62>	t_{SOH}		$t_{CYSO}/2 - 10$		ns
	$\overline{\text{SCLK}}$ low-level time	<63>	t_{SOL}		$t_{CYSO}/2 - 10$		ns
	$\overline{\text{SCLK}}$ rise time	<64>	t_{SOR}			10	ns
	$\overline{\text{SCLK}}$ fall time	<65>	t_{SOF}			10	ns
	SI input setup time (to $\overline{\text{SCLK}}\uparrow$)	<66>	t_{SDTS}		21		ns
	SI input hold time (from $\overline{\text{SCLK}}\uparrow$)	<67>	t_{HSDT}		21		ns
	SO output delay time (from $\overline{\text{SCLK}}\downarrow$)	<68>	t_{DSDT}		2	21	ns

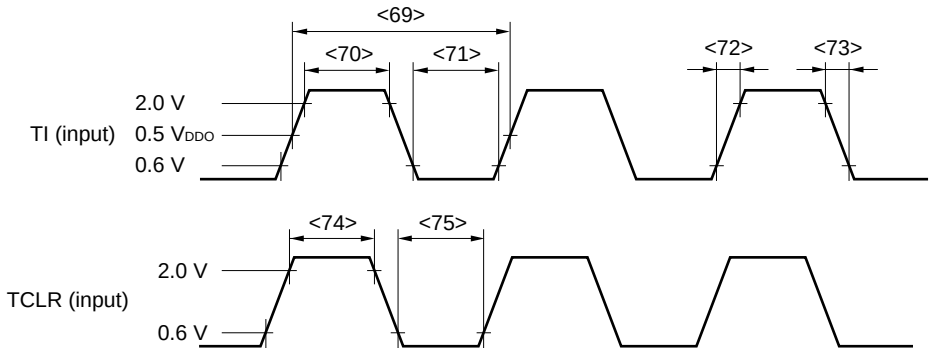
Remark T = t_{CYK} (external clock cycle)



(10) Timer timing

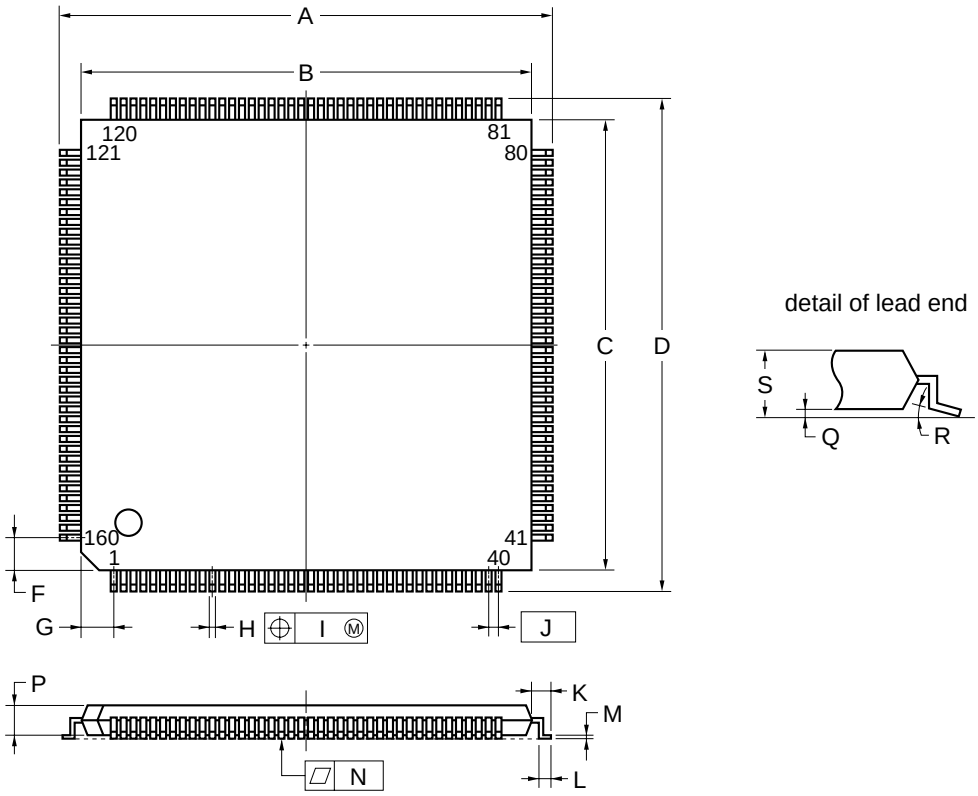
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TI clock cycle	<69>	t_{CYT}		8T		ns
TI clock high-level time	<70>	t_{TIH}		4T + 10		ns
TI clock low-level time	<71>	t_{TIL}		4T + 10		ns
TI clock rise time	<72>	t_{TR}			10	ns
TI clock fall time	<73>	t_{TF}			10	ns
TCLR clock high-level time	<74>	t_{CLH}		4T + 10		ns
TCLR clock low-level time	<75>	t_{CLL}		4T + 10		ns

Remark T = t_{CYK} (external clock cycle)



17. PACKAGE DRAWING

160 PIN PLASTIC LQFP (FINE PITCH) (□24)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	26.0±0.2	$1.024^{+0.008}_{-0.009}$
B	24.0±0.2	0.945±0.008
C	24.0±0.2	0.945±0.008
D	26.0±0.2	$1.024^{+0.008}_{-0.009}$
F	2.25	0.089
G	2.25	0.089
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.4±0.1	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.	0.067 MAX.

S160GM-50-8ED-2

★ 18. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 18-1. Surface Mounting Type Soldering Conditions

μPD705102GM-143-8ED: 160-pin plastic LQFP (fine pitch) (24 × 24 mm)
μPD705102GM-133-8ED: 160-pin plastic LQFP (fine pitch) (24 × 24 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less, Exposure limit: 3 days[Note] (after that, prebake 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times or less, Exposure limit: 3 days[Note] (after that, prebake 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	—

Note After opening dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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