



## Data Sheet

# **mP6™ MICROPROCESSOR FOR WINDOWS™ SYSTEMS**

The Rise™ mP6™ processor is a sixth generation processor optimized for low-power, high-performance multimedia Windows™ applications. The innovative Rise™ mP6™ processor is the first superscalar, superpipelined, Pentium® MMX\* compatible processor featuring 3 integer units, 3-way superscalar MMX technology, and a fully pipelined floating point unit. The innovative circuitry of the Rise™ mP6™ processor maximizes processing per clock cycle while requiring minimal power consumption – providing an ideal choice for cost-effective, power-efficient desktop and mobile Windows\* 95, Windows\* 98, and Windows NT\* systems.

<b>RATED PERFORMANCE †</b>	<b>266 MHz</b>	<b>233 MHz</b>	<b>166 MHz</b>
<b>HOST BUS FREQUENCY</b>	100 MHz	95 MHz	83 MHz
<b>CPU/HOST BUS RATIO</b>	2:1	2:1	2:1

- **x86 Instruction Set Enhanced with MMX™ Technology**
- **Pin Compatible with the Intel Pentium Processor (Socket 7)**
  - 296 Pin BPGA “Socket 7” Package
  - 387 Ball T<sup>2</sup>BGA® “Socket 7-like” Package
  - Split Voltage Planes
- **Advanced Power Management and Power Reduction Features**
  - SMM Compatible
  - Clock Control
  - ACPI Compliant
  - Facility Gating
  - Necessity Switching Only
  - Required Selection Only
- **Separate Code and Data Caches**
  - 8KB Code and 8KB Data
  - Split Line Access Mechanism
  - Filtered Tag Prefetching
- **High Performance FPU**
  - IEEE 854 and 754 Compliant
  - 80 Bit Results, 64 Bit Interface
- **Superscalar, Superpipelined Architecture**
  - Superscalar MMX Execution and Three Superpipelined Integer Units
  - Pipelined Floating Point Unit
- **Advanced Architectural Features**
  - Advanced Data Dependency Removal Techniques
  - Innovative Instruction Decode and Branch Prediction
  - Dynamic Allocation of Resources
- **IEEE 1149.1 Boundary Scan**
  - IEEE 854 and 754 Compliant
  - 80 Bit Results, 64 Bit Interface
- **ISO 9001 Wafer Fabrication, Assembly and Test**
- **Support for Bus Frequencies of 60, 66, 75, 83, 95, and 100 MHz**
- **CPU/Host Bus Ratio 2X, 2.5X, 3X, 3.5X**
- **3.3 V/2.8 V CMOS Technology**

† Rated performance levels for Rise™ mP6™ processors are based on the specified Host Bus Frequency and CPU/Host Bus Ratio. Use of different Host Bus Frequency and CPU/Host Bus Ratio to achieve the same core frequency may not provide the same level of performance.

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# 1 Processor Architecture Overview

The Rise<sup>™</sup> mP6<sup>™</sup> processor provides a unique combination of exceptional performance and low power. Designed with the entire personal computing system in mind, the Rise<sup>™</sup> mP6<sup>™</sup> processor is the ideal choice for x86 compatible notebook and desktop systems. The Rise<sup>™</sup> mP6<sup>™</sup> processor provides software compatibility with Microsoft\* Windows\*, Windows NT\*, MS-DOS\*, OS/2\* and UNIX\* along with the large installed base of x86 operating environments and applications. The Rise<sup>™</sup> mP6<sup>™</sup> processor is hardware compatible with existent Pentium® processor systems, and with Socket 7– or Super Socket 7–based systems.

## 1.1 Rise<sup>™</sup> mP6<sup>™</sup> processor Architecture

The 3-way superscalar architecture of the Rise<sup>™</sup> mP6<sup>™</sup> processor, utilizing three integer and MMX superpipelines, enables instruction tripling. With instruction tripling, three instructions can be issued and completed in a single clock cycle, greatly increasing system throughput. Aggressive instruction pairing and tripling rules combined with advanced branch prediction algorithms ensure that three pipelines of the processor are utilized to their fullest. Figure 1 shows a block diagram of the Rise<sup>™</sup> mP6<sup>™</sup> processor.

The Rise<sup>™</sup> mP6<sup>™</sup> processor has an eight-stage superpipelined architecture. Each integer pipeline contains six stages. Supporting the integer pipelines is a three-stage, non-interlocking instruction fetch pipeline and a two-stage non-interlocking data cache pipeline which is de-coupled from the decoder. The third stage of the instruction fetch is a buffer that is bypassed when the buffer is empty, resulting in a total of eight stage for the combined pipeline. These supporting pipelines and the eight-stage integer pipelines provide superpipelined efficiency that greatly reduces pipeline stalls, and increases the aggregate instruction completion rate.

To effectively manage its pipeline architecture, the Rise<sup>™</sup> mP6<sup>™</sup> processor uses innovative branch prediction and instruction decode techniques. A large 512 entry Branch Target Buffer (BTB), and an 8–entry call–return stack provide the base from which advanced branch prediction algorithms operate. By storing return addresses in its deep call–return stack, the Rise<sup>™</sup> mP6<sup>™</sup> processor is able to accurately predict return targets, even from nested subroutines.

Dual Instruction Stream Execution (DISE) is a unique feature that allows instructions to be decoded from three streams and issued from two different instruction streams simultaneously. Up to eight unresolved branches may simultaneously be operated upon by instruction fetch and integer pipelines. Pairing and tripling rules combined with the ability to decode from multiple streams tremendously increases the total instruction throughput.

To reduce pipeline stalls and to improve data movement efficiency, the Rise<sup>™</sup> mP6<sup>™</sup> processor resolves data dependency conflicts with the following features:

- Register Re–mapping
- Operand Forwarding
- Result Forwarding
- Zero Cycle Data Bypass
- Arithmetic Pairing

Each of these features reduces typical read after write, write after read, and write after write types of data dependencies. This allows the Rise<sup>™</sup> mP6<sup>™</sup> processor to simultaneously execute pairs of instructions that other processor cannot.

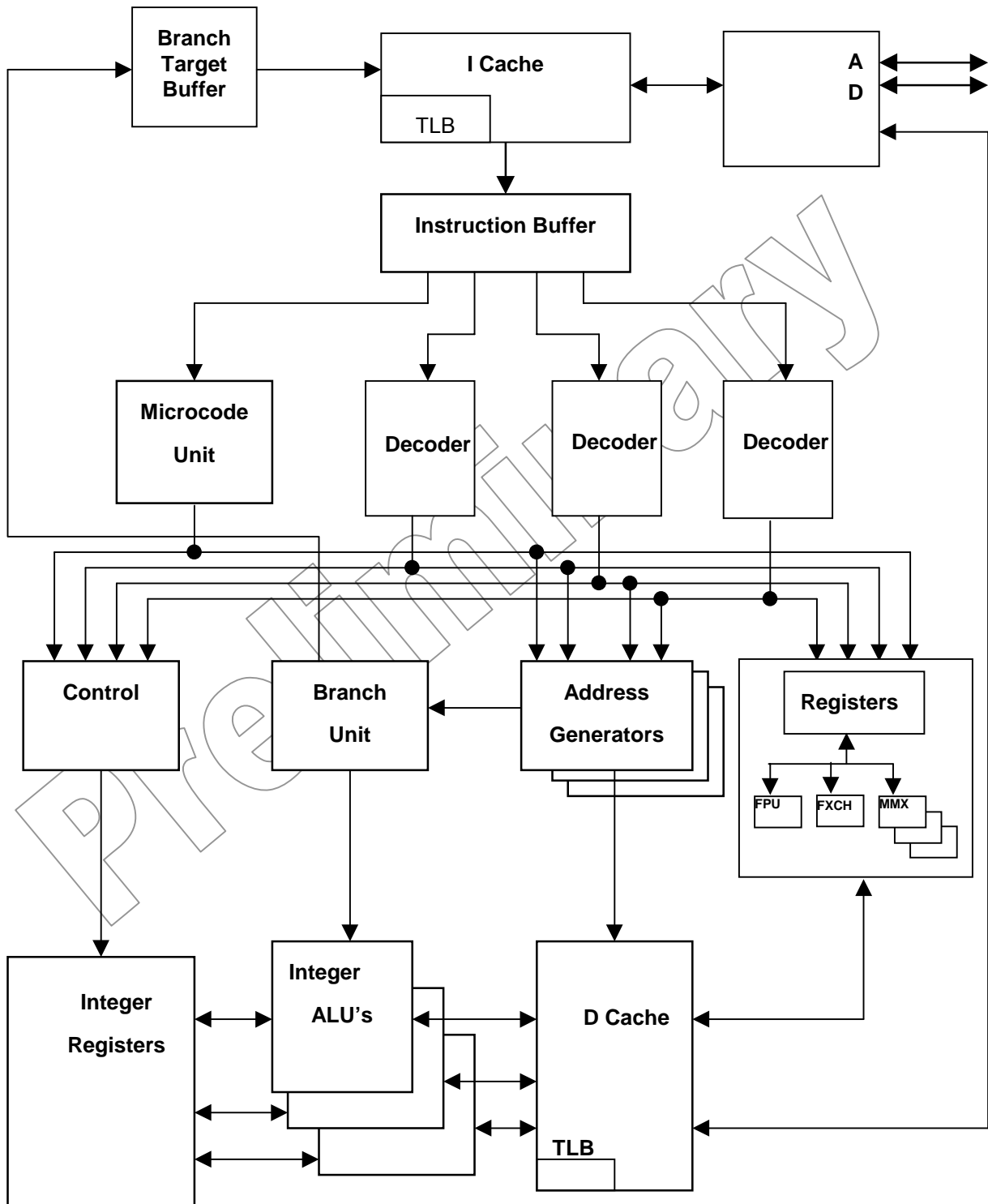


FIGURE 1. RISE™ mP6™ PROCESSOR BLOCK DIAGRAM

The integrated Floating Point Unit (FPU) of the processor has been designed as a four stage parallel operation pipeline. This high performance FPU produces 80 bit results and conforms to IEEE Standards

854 and 754. The Rise™ mP6™ processor can execute up to two floating point operations in the same cycle.

Three pipelines in the MMX\* Unit can execute up to three instructions per cycle in parallel and can resolve data dependency (twinning) to increase performance. The MMX Unit is geared for high performance multimedia such as image processing, video conferencing, and soft modem. Figure 2 depicts the multimedia features.

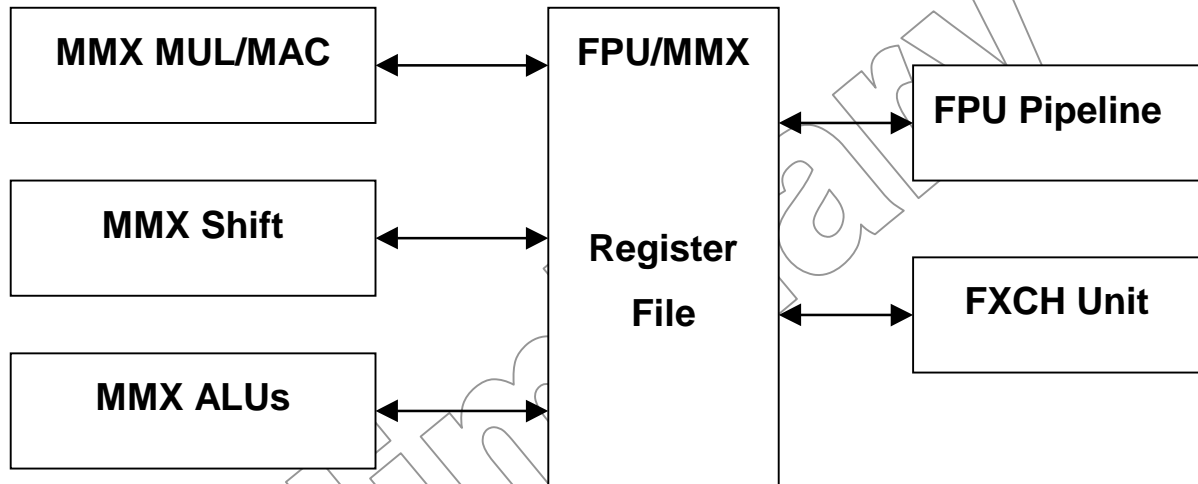


FIGURE 2. FPU/MMX UNIT

A 16 KByte L1 split cache design improves instruction and data handling, depending on the individual need. The instruction (“I”) cache, uses a split-line access mechanism to ensure that up to 16 bytes of data can be accessed with each cycle, even if the data spans multiple lines.

The data (“D”) cache utilizes eight interleaved banks to minimize conflicts between accesses. The “D” cache is dual ported (the tags are triple ported) to allow two read accesses, two write accesses, and a snoop access — all in the same cycle.

The “D” cache also contains a filtered tag prefetching mechanism to prefetch data while minimizing bus traffic and cache pollution. There is no misalignment penalty — an important factor for multimedia (e.g., MPEG playback).

The Integer Arithmetic Logic Units (ALUs) implement features that eliminate data dependency. The three major units in the ALU include the MUL/DIV/Shift Units, the 3-legged inputs, and the MOV/Jcc Units, which are illustrated in Figure 3.

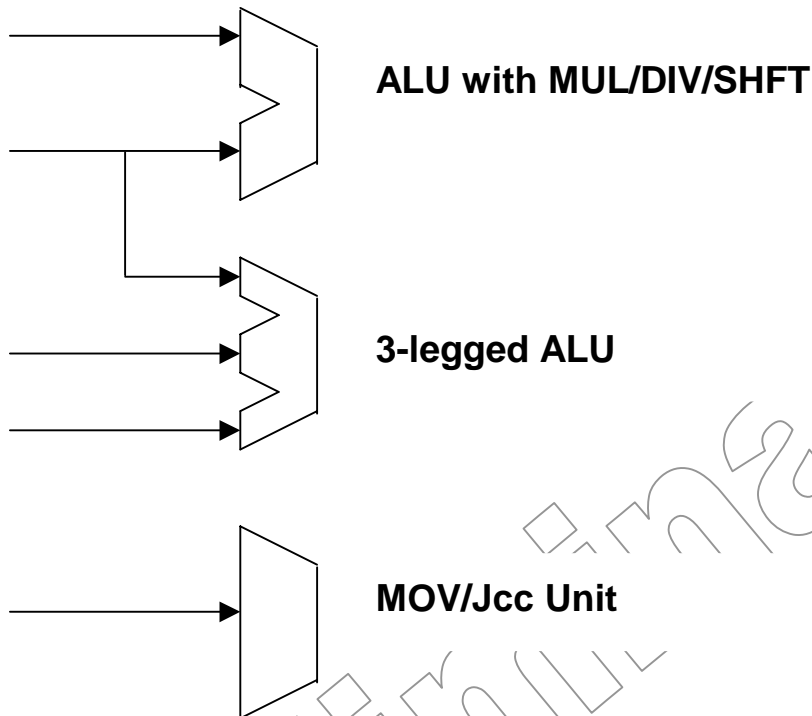
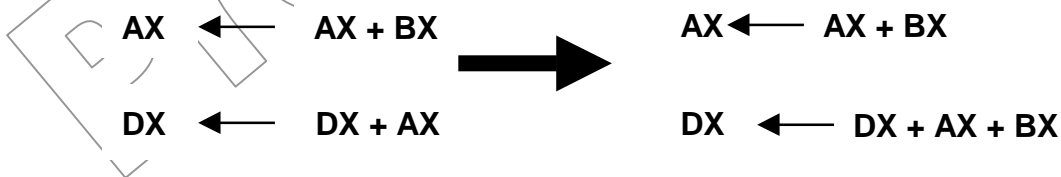


FIGURE 3. RISE™ MP6™ ARITHMETIC LOGIC UNITS

The following instruction stream can be accomplished in one cycle as the 3-legged ALU helps to collapse dependencies:



Dynamic Allocation of Resources (DAR) is a unique feature which provides an out-of-sequence-like execution technique utilized by the Rise™ mP6™ processor to improve instruction throughput. DAR breaks the typical resource-to-pipeline affinity found in most superscalar designs by allowing address generators, execution units, etc. of the processor to be allocated to various pipelines. Through DAR, resource utilization increases and instruction throughput is maximized.

## 1.2 Power Management

The Rise™ mP6™ processor is instruction and pin compatible with the Pentium processor implementation of the System Management Mode (SMM), Stop Grant State, Auto Halt Power Down State and Stop Clock State. The Rise™ mP6™ processor is also compliant with the Advanced Configuration and Power Interface (ACPI) Specification.

In addition to system level power saving facilities, the Rise™ mP6™ processor has the following internal architectural mechanisms that minimize power dissipation:

- Facility Gating Facility Gating turns off the clocks to portions of the processor that are not needed for the current operation.
- Necessity Switching Only (NSO) NSO reduces dynamic power dissipation by preventing unnecessary circuit switching.
- Required Selection Only (RSO) RSO allows the processor to address and access only the minimum required amount of data from its various cache and ROM structures. RSO minimizes dynamic power dissipation by limiting the number of sense amplifiers driven per access.

No action is required by the system designer or the end user to realize the power saving benefits of these architectural features.

### 1.3 Testability

To assist in board level testing, the Rise™ mP6™ processor implements IEEE Standard 1149.1 Boundary Scan (JTAG). Electrical specifications for the JTAG interface are defined in Table 29.

### 1.4 Compatibility

In general, the Rise™ mP6™ processor is instruction and pin compatible with other advanced Socket 7– or Super Socket 7–based x86 processor such as the Pentium® processor with MMX™ Technology. However, certain features of the Pentium processor that are not needed or used in desktop or mobile applications are not supported. Such features include multiprocessor and server capabilities as well as certain extended model–specific features as defined by the CPUID instruction.

#### 1.4.1 Omitted Multiprocessing and Server Capabilities

The Rise™ mP6™ processor is designed to specifically meet the needs of the mobile and desktop PC environments. The Rise™ mP6™ processor does not provide the Pentium compatible server environment features of multiprocessing, APIC, and Master/Checker functional redundancy.

#### 1.4.2 CPUID Instruction

The CPUID instruction is supported on the Rise™ mP6™ processor, and return values for the CPUID instruction are shown in Tables 1 through 3. For comparison, the Intel P55C processor return values are included in the tables.

**TABLE 1. CPUID RETURN VALUES WITH EAX == 0**

REGISTER	Rise™ mP6™	P55C
EAX	1	1
EBX:ECX:EDX	RiseRiseRise	GenuineIntel

**TABLE 2. CPUID EAX RETURN VALUES WITH EAX == 1**

PROCESSOR	[13:12] Type ID	[11:8] Family ID	[7:4] Model ID	[3:0] Stepping ID
Rise™ mP6™	0	5	0	Varies
P55C	0	5	4	Varies

**TABLE 3. CPUID EDX RETURN VALUES WITH EAX == 1**

EDX Bits – Meaning	RISE™ MP6™	P55C	Notes
0 – FP present	1	1	
1 – VM86 Extensions (VME)	0	1	
2 – Debugging Extensions	0	1	
3 – Page Size Extensions	0	0	
4 – Time Stamp Counter (TSC) supported	1	1	
5 – Model Specific Registers present	0	1	
6 – PAE supported	0	0	
7 – Machine Check Exception	0	1	
8 – CMPXCHG8B instruction	0	1	1
9 – APIC supported	0	1	
10:11 – RESERVED	-	-	
12 – Memory Range Registers	0	0	
13 – PTE global Bit supported	0	0	
14 – Machine Check Architecture supported	0	0	
15 – Conditional Move supported	0	0	
16:22 – RESERVED	-	-	
23 – MMX supported	1	1	
24:31 – RESERVED	-	-	

Notes:

1. The CMPXCHG8B instruction is supported and always enabled on the Rise™ mP6™ processor; however, the default CPUID function bit is set to 0 to circumvent a reported bug in Windows NT.

## 2 Pin References

The Rise™ mP6™ processor is available in a unique 296-pin package that is plug-in compatible with Socket 7- or Super Socket 7-based system designs. The package is consolidated with a ball grid array on top of a pin grid array (BPGA). An alternative turbo thermal ball grid array package (T<sup>2</sup>BGA®) is also available to provide reduced footprint, lower profile desktop positioning, and portable computing systems. The T<sup>2</sup>BGA package has 387 balls arranged as a “Socket 7-like” placement. With ball placement similar to the pin location of the Socket 7 processor, design and layout effort based on existing Socket 7 or Super Socket 7 motherboards is eased. BPGA package pinouts, T<sup>2</sup>BGA® ball placements, BPGA pin references, and T<sup>2</sup>BGA® ball references are depicted in the following figures and listed in the following tables.

## 2.1 BPGA Package Pinout

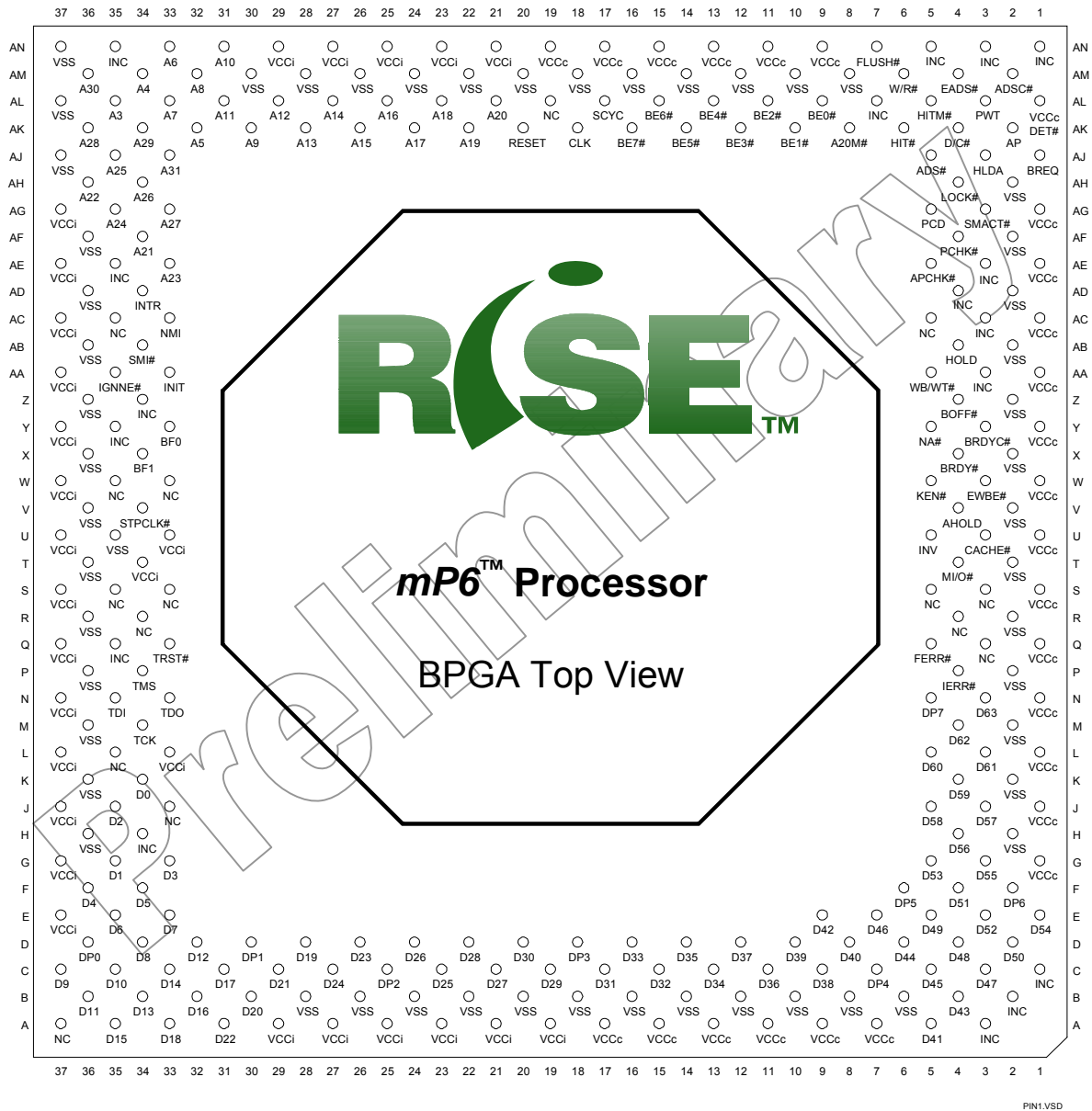


FIGURE 4. BPGA PACKAGE 'LOGICAL' TOP VIEW

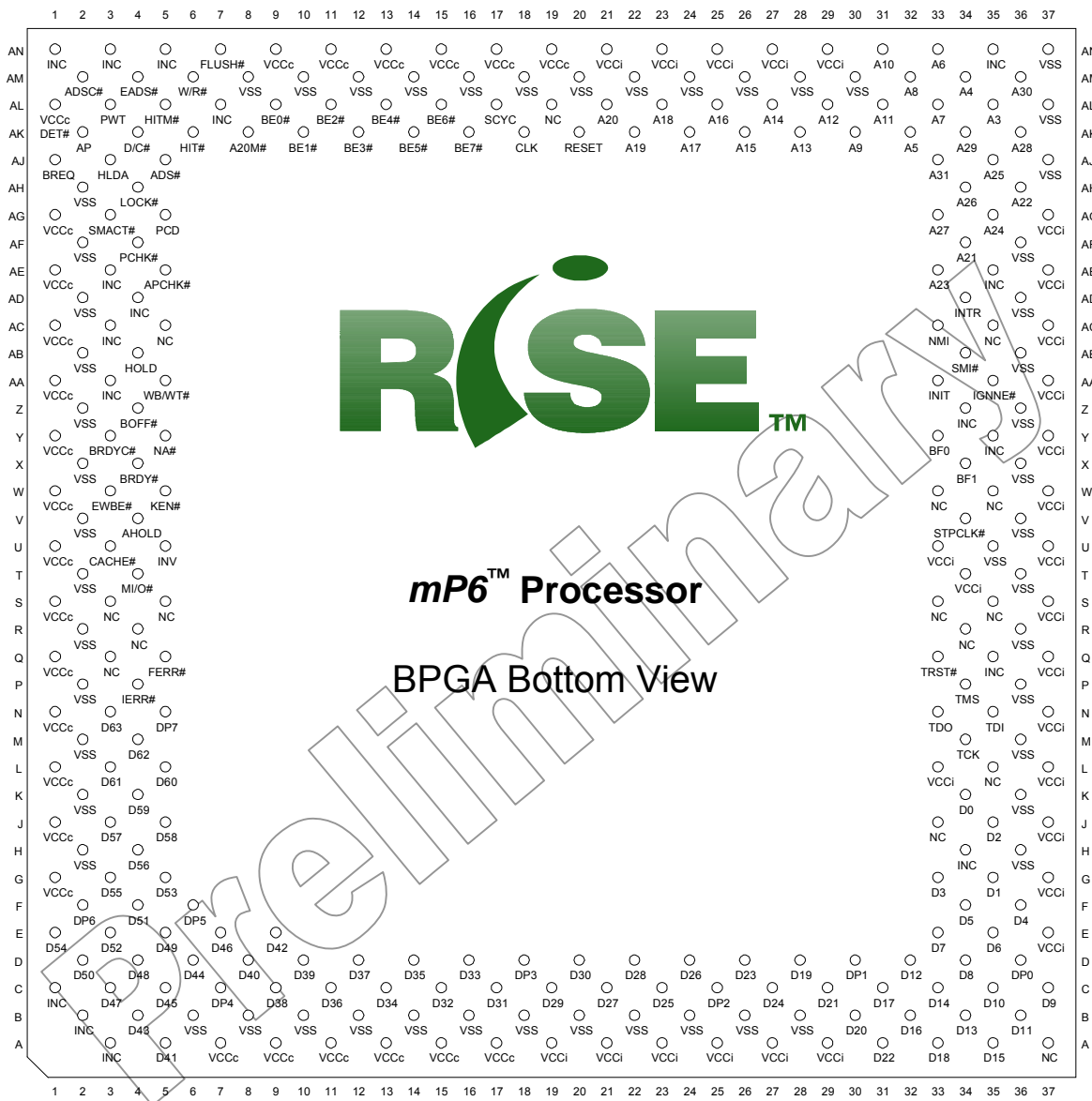


FIGURE 5. BPGA PACKAGE BOTTOM VIEW

## 2.2 BPGA Pin References by Type

**TABLE 4. BPGA ADDRESS PIN REFERENCE**

ADDRESS									
Addr	Loc	Addr	Loc	Addr	Loc	Addr	Loc	Addr	Loc
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		

**TABLE 5. BPGA DATA PIN REFERENCE**

DATA									
Data	Loc	Data	Loc	Data	Loc	Data	Loc	Data	Loc
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

TABLE 6. BPGA CONTROL PIN REFERENCE

CONTROL								
Signal	Loc	Type	Signal	Loc	Type	Signal	Loc	Type
A20M#	AK08	I	DP0	D36	I/O	INV	U05	I
ADS#	AJ05	O	DP1	D30	I/O	KEN#	W05	I
ADSC#	AM02	O	DP2	C25	I/O	LOCK#	AH04	O
AHOLD	V04	I	DP3	D18	I/O	M/IO#	T04	O
AP	AK02	I/O	DP4	C07	I/O	NA#	Y05	I
APCHK#	AE05	O	DP5	F06	I/O	NMI	AC33	I
BE0#	AL09	O	DP6	F02	I/O	PCD	AG05	O
BE1#	AK10	O	DP7	N05	I/O	PCHK#	AF04	O
BE2#	AL11	O	EADS#	AM04	I	PWT	AL03	O
BE3#	AK12	O	EWBE#	W03	I	RESET	AK20	I
BE4#	AL13	O	FERR#	Q05	O	SCYC	AL17	O
BE5#	AK14	O	FLUSH#	AN07	I	SMI#	AB34	I
BE6#	AL15	O	HIT#	AK06	O	SMIACT#	AG03	O
BE7#	AK16	O	HITM#	AL05	O	TCK	M34	I
BOFF#	Z04	I	HLDA	AJ03	O	TDI	N35	I
BRDY#	X04	I	HOLD	AB04	I	TDO	N33	O
BRDYC#	Y03	I	IERR#	P04	O	TMS	P34	I
BREQ	AJ01	O	IGNNE#	AA35	I	TRST#	Q33	I
CACHE#	U03	O	INIT	AA33	I	VCC2DET#	AL01	O
D/C#	AK04	O	INTR	AD34	I	WR#	AM06	O
						WB/WT#	AA05	I

TABLE 7. BPGA VCC<sub>IO</sub> PIN REFERENCE

VCC <sub>IO</sub>						
A19	A21	A23	A25	A27	A29	E37
G37	J37	L33	L37	N37	Q37	S37
T34	U33	U37	W37	Y37	AA37	AC37
AE37	AG37	AN21	AN23	AN25	AN27	AN29

**TABLE 8. BPGA VCC<sub>CORE</sub> PIN REFERENCE**

VCC <sub>CORE</sub>						
A07	A09	A11	A13	A15	A17	G01
J01	L01	N01	Q01	S01	U01	W01
Y01	AA01	AC01	AE01	AG01	AN09	AN11
AN13	AN15	AN17	AN19			

**TABLE 9. BPGA VSS PIN REFERENCE**

VSS								
B06	B08	B10	B12	B14	B16	B18	B20	B22
B24	B26	B28	H02	H36	K02	K36	M02	M36
P02	P36	R02	R36	T02	T36	U35	V02	V36
X02	X36	Z02	Z36	AB02	AB36	AD02	AD36	AF02
AF36	AH02	AJ37	AL37	AM08	AM10	AM12	AM14	AM16
AM18	AM20	AM22	AM24	AM26	AM28	AM30	AM37	

**TABLE 10. BPGA RESERVED PIN REFERENCE**

RESERVED (NC)					
A37	J33	L35	Q03	R04	R34
S03	S05	S33	S35	W33	W35
AC05	AC35	AL19			

**TABLE 11. BPGA INC PIN REFERENCE**

INC						
A03	B02	C01	H34	Q35	Y35	Z34
AA03	AC03	AD04	AE03	AE35	AL07	AN01
AN03	AN05	AN35				

**TABLE 12. BPGA CLOCK PIN REFERENCE**

CLOCK							
Signal	Loc	Signal	Loc	Signal	Loc	Signal	Loc
BF0	Y33	BF1	X34	CLK	AK18	STPCLK#	V34

## 2.3 T<sup>2</sup>BGA® Package Ball Assignment

TOP VIEW SEE THROUGH

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		
A		VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	D41	D39	D36	D33	D31	D28	D25	D23	D21	VCC <sub>c</sub>	D18	DP1	D13	D10	DP0	D5	D2	VCC <sub>c</sub>	VCC <sub>c</sub>	NC	VSS	VSS	A	
B	VSS	VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	D42	DP4	D37	D34	DP3	D29	D26	DP2	D22	VCC <sub>c</sub>	D17	D15	D12	D9	D7	D4	D1	VCC <sub>c</sub>	INC	NC	VSS	VSS	B	
C	VCC <sub>i</sub>	VCC <sub>i</sub>	VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	D40	D38	D35	D32	D30	D27	D24	D20	VCC <sub>c</sub>	D16	D14	D11	D8	D6	D3	D0	VCC <sub>c</sub>	NC	VSS	VCC <sub>c</sub>	VCC <sub>c</sub>	C	
D	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	VSS	VSS	VSS	VSS	VSS	VSS	D19	VCC <sub>c</sub>	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC <sub>c</sub>	VCC <sub>c</sub>	VSS	VCC <sub>c</sub>	VCC <sub>c</sub>	D	
E	D43	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>																			VCC <sub>c</sub>	VCC <sub>c</sub>	VCC <sub>c</sub>	INC	E	
F	D46	D45	D44	VCC <sub>i</sub>																			VCC <sub>c</sub>	VCC <sub>c</sub>	VCC <sub>c</sub>	INC	F	
G	D48	DP5	D47	VSS																			VCC <sub>c</sub>	NC	INC	INC	G	
H	D51	D50	D49	VSS																			VSS	NC	TCK	TD0	H	
J	D54	D53	D52	VSS																			VSS	TDI	TMS	TRST#	J	
K	D56	DP6	D55	VSS																			VSS	NC	STPCLK#	NC	K	
L	D58	D59	D57	VSS																			VSS	BF1	BF0	INC	L	
M	D60	D62	D61	VSS																			VSS	INIT	IGNNE#	SMI#	M	
N	VCC3	VCC3	VCC3	VCC3																			VSS	NMI	A21	INTR	NC	N
P	IERR#	FERR#	D63	DP7																			VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	P
R	NC	NC	NC	VSS	VSS	VSS	A22	A23	A24	R																		
T	NC	CACHE#	MIO#	VSS	VSS	VSS	VSS	A26	A25	A27	T																	
U	EWBE#	INV	KEN#	VSS	VSS	VSS	VSS	A29	A28	A30	U																	
V	AHOLD	BRDY#	NA#	VSS	VSS	VSS	VSS	A3	A31	A4	V																	
W	BOFF#	WBWT#	BRDY#	VSS	VSS	VSS	VSS	VSS	A6	A5	A7	W																
Y	HOLD	INC	INC	VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	A9	A8	A10	Y															
AA	VCC <sub>c</sub>	INC	INC	VCC <sub>c</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	A11	AA															
AB	VCC <sub>c</sub>	VCC <sub>c</sub>	VCC <sub>c</sub>	VCC <sub>c</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	AB															
AC	VCC <sub>c</sub>	VCC <sub>c</sub>	VCC <sub>c</sub>	VSS	VCC <sub>c</sub>	VCC <sub>c</sub>	VSS	VSS	VSS	VSS	VSS	VSS	VCC <sub>c</sub>	BE2#	VSS	PLL2	PLL3	VSS	VSS	VSS	VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	AC
AD	VCC <sub>c</sub>	VCC <sub>c</sub>	VSS	VCC <sub>c</sub>	VCC <sub>c</sub>	NC	BREQ	LOCK#	DC#	HITM#	INC	BE0#	VCC <sub>c</sub>	BE1#	BE7#	PLL2	PLL3	NC	A20	A18	A15	VCC <sub>i</sub>	VCC <sub>i</sub>	VSS	VCC <sub>i</sub>	VCC <sub>i</sub>	AD	
AE	VSS	VSS	VCC <sub>c</sub>	VCC <sub>c</sub>	VCC <sub>c</sub>	SMIACT#	APCHK#	AP	PWT	ADS#	WR#	A20M#	VCC <sub>c</sub>	BE4#	BE6#	PLL2	PLL3	CLK	RESET	A17	A14	A12	VCC <sub>i</sub>	VCC <sub>i</sub>	VSS	VSS	AE	
AF	VSS	VSS	VCC <sub>c</sub>	VCC <sub>c</sub>	VCC <sub>c</sub>	ADSC#	PCHK#	HLDA	PCD	EADS#	HIT#	FLUSH#	VCC <sub>c</sub>	BE3#	BE5#	PLL2	PLL3	SCYC	A19	A16	A13	VCC <sub>i</sub>	VCC <sub>i</sub>	VCC <sub>i</sub>	VSS	VSS	AF	

FIGURE 6. T<sup>2</sup>BGA® PACKAGE TOP VIEW

## 2.4 T<sup>2</sup>BGA<sup>®</sup> Ball References by Type

**TABLE 13. T<sup>2</sup>BGA<sup>®</sup> ADDRESS BALL REFERENCE**

ADDRESS									
Addr	Loc	Addr	Loc	Addr	Loc	Addr	Loc	Addr	Loc
A3	V24	A9	Y24	A15	AD21	A21	N24	A27	T26
A4	V26	A10	Y26	A16	AF20	A22	R24	A28	U25
A5	W25	A11	AA26	A17	AE20	A23	R25	A29	U24
A6	W24	A12	AE22	A18	AD20	A24	R26	A30	U26
A7	W26	A13	AF21	A19	AF19	A25	T25	A31	V25
A8	Y25	A14	AE21	A20	AD19	A26	T24		

**TABLE 14. T<sup>2</sup>BGA<sup>®</sup> DATA BALL REFERENCE**

DATA									
Data	Loc	Data	Loc	Data	Loc	Data	Loc	Data	Loc
D0	C21	D13	A17	D26	B11	D39	A6	D52	J3
D1	B21	D14	C16	D27	C11	D40	C6	D53	J2
D2	A21	D15	B16	D28	A10	D41	A5	D54	J1
D3	C20	D16	A16	D29	B10	D42	B5	D55	K3
D4	B20	D17	B15	D30	C10	D43	E1	D56	K1
D5	A20	D18	A15	D31	A9	D44	F3	D57	L3
D6	C19	D19	D13	D32	C9	D45	F2	D58	L1
D7	B19	D20	C13	D33	A8	D46	F1	D59	L2
D8	C18	D21	A13	D34	B8	D47	G3	D60	M1
D9	B18	D22	B13	D35	C8	D48	G1	D61	M3
D10	A18	D23	A12	D36	A7	D49	H3	D62	M2
D11	C17	D24	C12	D37	B7	D50	H2	D63	P3
D12	B17	D25	A11	D38	C7	D51	H1		

**TABLE 15. T<sup>2</sup>BGA® CONTROL BALL REFERENCE**

CONTROL								
Signal	Loc	Type	Signal	Loc	Type	Signal	Loc	Type
A20M#	AE12	I	DP0	A19	I/O	INV	U2	I
ADS#	AE10	O	DP1	A16	I/O	KEN#	U3	I
ADSC#	AF6	O	DP2	B12	I/O	LOCK#	AD8	O
AHOLD	V1	I	DP3	B9	I/O	M/IO#	T3	O
AP	AE8	I/O	DP4	B6	I/O	NA#	V3	I
APCHK#	AE7	O	DP5	G2	I/O	NMI	N23	I
BE0#	AD12	O	DP6	K2	I/O	PCD	AF9	O
BE1#	AD14	O	DP7	P4	I/O	PCHK#	AF7	O
BE2#	AC14	O	EADS#	AF10	I	PWT	AE9	O
BE3#	AF14	O	EWBE#	U1	I	RESET	AE19	I
BE4#	AE14	O	FERR#	P2	O	SCYC	AF18	O
BE5#	AF15	O	FLUSH#	AF12	I	SMI#	M26	I
BE6#	AE15	O	HIT#	AF11	O	SMIACT#	AE6	O
BE7#	AD15	O	HITM#	AD10	O	TCK	H25	I
BOFF#	W1	I	HLDA	AF8	O	TDI	J24	I
BRDY#	V2	I	HOLD	Y1	I	TDO	H26	O
BRDYC#	W3	I	IERR#	P1	O	TMS	J25	I
BREQ	AD7	O	IGNNE#	M25	I	TRST#	J26	I
CACHE#	T2	O	INIT	M24	I	WR#	AE11	O
D/C#	AD9	O	INTR	N25	I	WB/WT#	W2	I

**TABLE 16. T<sup>2</sup>BGA® VCC<sub>IO</sub> BALL REFERENCE**

VCC <sub>IO</sub>							
A3	A4	B3	B4	C1	C2	C4	C5
D1	D2	D3	D5	D6	E2	E3	E4
F4	N1	N2	N3	N4	P23	P24	P25
P26	Y23	AA23	AA24	AB23	AB24	AB25	AB26
AC21	AC22	AC24	AC25	AC26	AD22	AD23	AD25
AD26	AE23	AE24	AF22	AF23	AF24		

**TABLE 17. T<sup>2</sup>BGA® VCC<sub>CORE</sub> BALL REFERENCE**

VCC <sub>CORE</sub>							
A14	A22	A23	B14	B22	C14	C22	C25
C26	D14	D21	D22	D24	D25	D26	E23
E24	E25	F23	F24	F25	G23	AA1	AA4
AB1	AB2	AB3	AB4	AC1	AC2	AC3	AC5
AC6	AC13	AD1	AD2	AD4	AD5	AD13	AE3
AE4	AE5	AE13	AF3	AF4	AF5	AF13	

**TABLE 18. T<sup>2</sup>BGA® VSS BALL REFERENCE**

VSS								
A2	A25	A26	B1	B2	B25	B26	C3	C24
D4	D7	D8	D9	D10	D11	D12	D15	D16
D17	D18	D19	D20	D23	G4	H4	H23	J4
J23	K4	K23	L4	L11	L12	L13	L14	L15
L16	L23	M4	M11	M12	M13	M14	M15	M16
M23	N11	N12	N13	N14	N15	N16	P11	P12
P13	P14	P15	P16	R4	R11	R12	R13	R14
R15	R16	R23	T4	T11	T12	T13	T14	T15
T16	T23	U4	U23	V4	V23	W4	W23	Y4
AC4	AC7	AC8	AC9	AC10	AC11	AC12	AC15	AC18
AC19	AC20	AC23	AD3	AD24	AE1	AE2	AE25	AE26
AF1	AF2	AF25	AF26					

**TABLE 19. T<sup>2</sup>BGA® PLL BALL REFERENCE**

PLL3 - VCC <sub>IO</sub>			
AC17	AD17	AE17	AF17
PLL2 - VCC <sub>CORE</sub>			
AC16	AD16	AE16	AF16

**TABLE 20. T<sup>2</sup>BGA® RESERVED BALL REFERENCE**

RESERVED (NC)					
T1	R2	R3	R1	C23	A24
B24	G24	H24	K24	K26	N26
AD18	AD6				

**TABLE 21. T<sup>2</sup>BGA® INC BALL REFERENCE**

INC						
AD11	E26	G26	AA25	L26	G25	F26
AA3	AA2	Y2	Y3	B23		

**TABLE 22. T<sup>2</sup>BGA® CLOCK BALL REFERENCE**

CLOCK							
Signal	Loc	Signal	Loc	Signal	Loc	Signal	Loc
BF0	L25	BF1	L24	CLK	AE18	STPCLK#	K25

## 2.5 Signal Description

The following table lists all signals supported by the Rise™ mP6™ processor. Since multiprocessor and server-related features are not supported by the Rise™ mP6™ processor, signals are not listed for them.

**TABLE 23. RISE™ MP6™ CPU SIGNAL DESCRIPTION**

SIGNAL	I/O TYPE	DESCRIPTION
A20M#	I	The <b>address bit 20 mask</b> causes the Rise™ mP6™ processor to emulate the address wraparound at 1 Mbyte which occurs on the 8086 by masking physical address bit 20 (A20) before performing an internal cache access or driving a memory cycle. A20M# is asserted when the Rise™ mP6™ processor is in real mode and is undefined when it is in protected mode.
A31-A3	I/O	<b>Address lines and byte enables (BE#7–BE#0)</b> define memory or I/O access. The external system drives A31–A5 for cache inquiry cycles.
ADS#	O	The <b>address strobe</b> indicates that a new valid memory or I/O bus cycle is currently being driven by the Rise™ mP6™ processor.
ADSC#	O	The <b>address strobe copy</b> is functionally identical to ADS#.
AHOLD	I	The <b>address hold</b> input allows another bus master access to the address of the Rise™ mP6™ processor. The Rise™ mP6™ processor stops driving the address lines (A31–A3) and AP in the next clock, while the rest of the bus remains active so data can be returned or driven for previously issued bus cycles.

SIGNAL	I/O TYPE	DESCRIPTION
AP	I/O	<b>Address parity</b> is driven with even parity information on Rise™ mP6™ processor –generated cycles in the same clock that the address is driven. During cache inquire cycles, this pin is sampled in the same clock as EADS# to ensure that correct parity check status is indicated by <b>APCHK#</b> of the Rise™ mP6™ processor.
APCHK#	O	If the Rise™ mP6™ processor detects a parity error on the address bus during inquire cycles, the <b>address parity check</b> status pin is asserted two clocks after EADS# is sampled active and it remains active for one clock cycle.
BE7#-BE0#	O	<b>Byte enables</b> determine which data bytes are transferred for the current cycle. Byte enables and address lines A31–A3 are driven in the same clock.
BF[1:0]	I	The <b>bus frequency</b> inputs are sampled at <b>RESET</b> to determine the CPU-to-bus frequency ratio. See Table 24 for Host Bus Frequency Selections.
BOFF#	I	The <b>backoff</b> input forces the Rise™ mP6™ processor to abort all outstanding bus. The Rise™ mP6™ processor floats all pins to enter the bus hold state in the next clock. When BOFF# is negated, the Rise™ mP6™ processor restarts the aborted bus cycles.
BRDY#	I	<b>Burst ready</b> input indicates that the external system has presented valid data on the data pins in response to a read, or that the external system has accepted Rise™ mP6™ processor data in response to a write request. The processor samples BRDY# in the second and subsequent clocks of a bus cycle.
BRDYC#	I	The <b>burst ready (copy)</b> is functionally identical to BRDY#.
BREQ	O	The <b>bus request</b> output indicates to the external system that the Rise™ mP6™ processor has a bus cycle pending internally.
CACHE#	O	The <b>cache</b> pin indicates internal “cache–ability” of a read cycle or a burst write–back cycle. If this pin is driven inactive during a read cycle, the Rise™ mP6™ processor does not cache the returned data, regardless of the state of the KEN# pin. The <b>cache</b> pin is also used to determine the cycle length.
CLK	I	<b>Clock</b> input provides the fundamental timing for the Rise™ mP6™ processor. External timing parameters are specified with reference to the rising edge of CLK.
D63-D0	I/O	<b>Data lines</b> are three–state, bi-directional signals. Lines D7–D0 define the least significant byte of the data bus, and lines D63–D56 define the most significant. The data bus is driven only while a write cycle is active. During reads, the CPU samples the data bus when BRDY# is returned.
D/C#	O	The <b>data/code</b> is driven valid in the same clock that the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.

SIGNAL	I/O TYPE	DESCRIPTION
DP7-DP0	I/O	The <b>data parity</b> signals provide parity for the data bus — one for each byte of the data bus. These signals are driven by the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor with even parity information on writes in the same clock as the data. Even parity information must be driven back to the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor. DP7 applies to D63-D56.
EADS#	I	The <b>external address strobe</b> indicates a valid cache inquiry address is being driven onto the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor address bus in an inquire cycle.
EWBE#	I	The <b>external write buffer empty</b> indicates that there are no pending write cycles in the external system.
FEER#	O	The <b>floating-point error</b> pin is driven active when an unmasked floating point error occurs during the execution of the FPU instruction.
FLUSH#	I	The <b>flush</b> input forces the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor to flush the cache by writing back all modified lines in the data cache and invalidating its internal caches.
HIT#	O	<b>Hit</b> indicates that a current cache inquiry address has been found on a valid line in either the data or instruction cache. This pin is valid two clocks after EADS# is sampled as asserted, and remains valid until the next cache inquiry cycle.
HITM#	O	The <b>hit modified line</b> indicates that a current cache inquiry address has been found in the cache and dirty data exists in the cache line. It inhibits another bus master from accessing the data until the line is completely written back.
HLDA	O	The <b>bus hold acknowledge</b> indicates that a hold request being driven to the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor on the <b>HOLD</b> pin. When leaving bus hold, the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor resumes driving the bus and HLDA is driven inactive. If a bus cycle pending, the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor is driven one clock cycle after HLDA is de-asserted.
HOLD	I	The <b>bus hold request</b> indicates that another bus master has requested the control of the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor host bus. After completing all outstanding bus cycles, the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor enters a bus hold state until HOLD is de-asserted. The Rise <sup>TM</sup> mP6 <sup>TM</sup> processor recognizes HOLD during RESET but not in LOCK cycles.
IERR#	O	The <b>internal error</b> pin indicates internal parity errors.
IGNNE#	I	The <b>ignore numeric error</b> forces the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor to ignore any pending unmasked numeric exception and to continue executing floating-point instructions as long as this pin is asserted.
INIT	I	The <b>initialization</b> input forces the Rise <sup>TM</sup> mP6 <sup>TM</sup> processor to begin execution in a known state which is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain their values. If INIT is sampled high when RESET transitions from high to low, the processor performs the build-in self test prior to initiating program execution.

SIGNAL	I/O TYPE	DESCRIPTION
INTR	I	The <b>maskable interrupt</b> input indicates that an external interrupt has been generated. When the IF bit of the EFLAGS register is set, the Rise™ <i>mp6</i> ™ processor generates two locked interrupt acknowledge bus cycles and begins execution of an interrupt service routine after executing the current instruction.
INV	I	The <b>invalidation</b> input ascertains the final cache line state to be invalid or shared in a cache inquiry hit. It is sampled in the same clock with the cache inquiry address and the <b>EADS#</b> .
KEN#	I	The <b>cache enable</b> input allows the data being returned from the current cycle to be cacheable. When the Rise™ <i>mp6</i> ™ processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle is transformed into a 32-byte cache line fill cycle.
LOCK#	O	The <b>lock</b> pin indicates that the current bus cycle is locked. The Rise™ <i>mp6</i> ™ processor does not accept a bus hold request from another bus master while LOCK# is asserted.
M/IO#	O	The <b>memory/input-output</b> is driven valid in the same clock as the <b>ADS#</b> . M/IO# distinguishes between memory and I/O cycles.
NA#	I	The <b>next address</b> input indicates that the external memory system is ready to accept a new bus cycle, even though all data transfers for the current cycle are not yet complete. The Rise™ <i>mp6</i> ™ processor issues ADS# for a pending cycle two clocks after NA# is asserted.
NMI	I	The <b>non-maskable interrupt</b> request signal indicates that an external non-maskable interrupt has been generated. The Rise™ <i>mp6</i> ™ processor suspends execution of the current instruction stream and begins execution of a NMI interrupt service routine.
PCD	O	The <b>page cache disable</b> pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The PCD provides an external cache-ability indication on a page-by-page basis.
PCHK#	O	The <b>parity check</b> output indicates a data bus parity error in a data read cycle. It is driven with parity status two clocks after BRDY# is returned. Parity is checked only for the bytes on which valid data are returned.
PWT	O	The <b>page write through</b> pin reflects the state of the PWT bit in CR3, the page Directory Entry, or the Page Table Entry. The PWT pin is used to provide an external write back indication on a page-by-page basis. <b>PWT</b> has higher priority than <b>WB/WT#</b> .
RESET	I	<b>RESET</b> forces the Rise™ <i>mp6</i> ™ processor to begin execution at a known state. All data in the internal caches is invalidated.
SCYC	O	The <b>split cycle</b> is asserted during misaligned LOCKed transfers to indicate that more than two cycles are locked together. This signal is defined for locked cycles only.

SIGNAL	I/O TYPE	DESCRIPTION
SMI#	I	The <b>system management interrupt</b> causes the Rise™ mP6™ processor to System Management Mode. <b>SMI</b> has higher priority than <b>NMI</b> .
SMIACT#	O	The <b>system management interrupt active</b> indicates that the Rise™ mP6™ processor is in System Management Mode.
STPCLK#	I	The <b>stop clock</b> input is a request from the system to stop the internal clock of the Rise™ mP6™ processor. When the Rise™ mP6™ processor recognizes STPCLK#, it stops execution on the next instruction boundary and generates a stop grant acknowledge cycle. When STPCLK# is asserted, the Rise™ mP6™ processor still responds to external snoop requests.
TCK	I	The <b>testability clock (JTAG)</b> provides the clocking function for the Rise™ mP6™ processor boundary scan in accordance with the IEEE1149.1 Boundary Scan interface. It is used to clock state information and data into and out of the Rise™ mP6™ processor during boundary scan.
TDI	I	The <b>test data input (JTAG)</b> is a serial data input for the test logic. Data and instructions are shifted into the Rise™ mP6™ processor on this pin on the rising edge of TCK for testing.
TDO	O	The <b>test data output (JTAG)</b> is a serial data output of the test logic. Data and instructions are shifted out of the Rise™ mP6™ processor on this pin on the falling edge of TCK for testing.
TMS	I	The <b>test mode select (JTAG)</b> signal sampled on the rising edge of TCK controls the sequence of state changes of the boundary scan test logic.
TRST#	I	<b>Test reset (JTAG)</b> input asynchronously initializes boundary scan test logic.
VCC2DET#	O	<b>VCC2 detect</b> is always driven low by the Rise™ mP6™ processor. It is not available in the T <sup>2</sup> BGA® package.
W/R#	O	<b>Write/read</b> is driven valid in the same clock period that the ADS# signal is asserted. It distinguishes between write and read cycles for the current memory or I/O bus access.
WB/WT#	I	The <b>write back/write through</b> input defines the cache write policy to a data cache line as either write back or write through on a line-by-line basis.

## 2.6 Pin Connections

For reliable operation, any unused active high input must be tied to GND (VSS) and any unused active low input must be tied to VCC<sub>IO</sub>; however, if an unused input has an internal pull-up or pull-down resistor, then no external connection is required. Signals with internal pull-up or pull-down resistors are listed below (all internal pull-up and pull-down resistors are 33 kΩ ± 50%). If an external connection is made to an input with an internal resistor, it must be a direct connection (< 1 kΩ resistance). Unused inputs that do not have internal resistors should be connected to GND or VCC<sub>IO</sub> using a 20 kΩ resistor.

Signals with internal pull-up resistors include: BF0, CLK

Signals with internal pull-down resistors include: BF1, BRDY#, BRDYC#, SMI#, STPCLK#, TCK#, TDI#, TMS#, TRST#

**2.6.1 RESERVED Pins**

Pins labeled RESERVED must not be connected; if they are connected, they can cause the processor to produce unexpected results or to otherwise malfunction.

**2.6.2 INC Pins**

Pins labeled INC have no connection to the processor die and it is recommended (though not required) that these pins be left unconnected.

**2.6.3 CPU and Host Bus Frequency Control**

The Rise™ mP6™ processor operates at a multiple of the host bus frequency. Table 24 lists the relationship between BF1–BF0 values and the consequent CPU–to–host bus ratios. Both BF0 and BF1 are active high signals so the corresponding pins should be tied to VCC<sub>IO</sub> or VSS to obtain the desired CPU–to–host bus ratio. The processor uses internal pull-up/pull-down resistors to force a default CPU–to–host bus ratio of 2:1.

**TABLE 24. CPU AND HOST BUS FREQUENCY CONTROL**

BF1	BF0	CPU:HOST BUS RATIO	EXAMPLES	
			CPU FREQUENCY	HOST BUS FREQUENCY
1	0	2:1	166 MHz	83 MHz
1	0	2:1	190 MHz	95 MHz
1	0	2:1	200 MHz	100 MHz

### 3 Electrical Specifications

#### 3.1 Maximum Ratings

The values in Table 25 are worst-case stress ratings. CPU operation and reliability can be impaired and failure can occur if maximum ratings are exceeded. The CPU is not warranted, expressed or implied, to perform beyond these parameters. For best results, adhere to the operating conditions defined in the DC and AC specification tables listed below. The Rise™ mP6™ processor resists latch-up or circuit damage caused by electrostatic discharge (ESD). However, it is not possible to prevent all failures that can result from excessive ESD, and precautions to avoid E/M fields and static shocks should always be taken when handling, storing, or operating the Rise™ mP6™ processor.

**TABLE 25. MIN/MAX RATINGS**

SYMBOL	PARAMETER	MIN	MAX	UNITS
T <sub>s</sub>	Storage temperature	-65	150	°C
T <sub>CASE</sub>	Case temperature under bias or voltage applied	-65	110	°C
VCC <sub>IO</sub>	3.3 V supply voltage relative to VSS	-0.5	3.6	V
VCC <sub>CORE</sub>	2.8 V supply voltage relative to VSS	-0.05	2.9 <sup>1</sup>	V
VIN <sub>IO</sub> <sup>1</sup>	DC input voltage at any pin	-0.5	VCC <sub>IO</sub> + 0.5	V

Notes:

1. To avoid CPU damage, do not exceed the MAX voltage under any circumstances.

### 3.2 DC Specifications

TABLE 26. DC SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T <sub>CASE</sub>	Operating case temperature	0		70	°C	
VCC <sub>CORE</sub>	Core voltage	2.75	2.8	2.85	V	
VCC <sub>IO</sub>	I/O voltage	3.135	3.3	3.465	V	3.3V ± 5% <sup>1</sup>
ICC <sub>CORE</sub>	Power supply current			4	A	200 MHz <sup>2</sup>
ICC <sub>IO</sub>	Power supply current			1	A	190 MHz <sup>2</sup> 166 MHz <sup>2</sup>
V <sub>IL,IO</sub>	Input low voltage	-0.3		0.8	V	3
V <sub>IH,IO</sub>	Input high voltage	2.0		VCC <sub>IO</sub> + 0.3	V	3
V <sub>OL,IO</sub>	Output low voltage			0.4	V	3,4
V <sub>OH,IO</sub>	Output high voltage	2.4	–	–	V	3, 5
I <sub>LI</sub>	Input leakage current	–	–	± 15	µA	0 ≤ V <sub>IN</sub> ≤ VCC <sub>IO</sub> <sup>6</sup>
I <sub>LO</sub>	Output leakage current	–	–	± 15	µA	0 ≤ V <sub>IN</sub> ≤ VCC <sub>IO</sub> <sup>7</sup>
I <sub>IH</sub>	Input Leakage Current	–	–	200	µA	V <sub>IN</sub> = 2.4 V <sup>8</sup>
I <sub>IL</sub>	Input leakage current	–	–	- 400	µA	9
C <sub>IN</sub>	Input Capacitance	–	–	15	pF	10
C <sub>OUT</sub>	Output Capacitance	–	–	20	pF	10
C <sub>I/Output</sub>	I/Output Capacitance	–	–	25	pF	10
C <sub>CLK</sub>	CLK Input Capacitance	–	–	15	pF	10
C <sub>TIN</sub>	Test Input Capacitance	–	–	15	pF	10
C <sub>TOUT</sub>	Test Output Capacitance	–	–	20	pF	10
C <sub>TCK</sub>	Test Clock Capacitance	–	–	15	pF	8

Notes:

- Unit not guaranteed to work beyond the MAX operating voltage in the MAX temperature.
- These values should be used for power supply design.
- All signals are 3.3 V TTL levels.
- Measured with a 4 mA load.
- Measured with a –3 mA load.
- For signals without an internal pull up or pull down resistor.
- For signals with an internal pull up or pull down resistor.
- For inputs with an internal pull down resistor.
- For inputs with an internal pull up resistor.
- Not 100% tested, guaranteed by design.

**TABLE 27. POWER DISSIPATION SPECIFICATIONS**

PARAMETER	TYP <sup>1</sup>	MAX	UNITS	FREQUENCY
Active power dissipation	6.28	8.54	W	200 MHz
	5.96	8.11	W	190 MHz
	5.28	7.28	W	166 MHz
Stop Grant and Auto Halt Power Down power dissipation	–	–	W	200 MHz
			W	190 MHz
			W	166 MHz
Stop Clock power dissipation	–	–	W	All

Notes

1. Typical system power dissipation running a typical sequence of instructions. Power dissipation varies across applications. System thermal solutions should be designed to dissipate the maximum power dissipation.

Preliminary

### 3.3 AC Specifications

The AC specifications are listed in two tables (28A and 28B). Table 28A lists the AC specifications of processors for host buses that run at 60 MHz, 66MHz, and 75MHz, while Table 28B lists the AC specifications of processors for host buses that run at 83 MHz, 95MHz, and 100MHz. The two tables are divided into several parts, each of which is followed by a related timing diagram in the following pages.

**TABLE 28A. AC SPECIFICATIONS**

See Table 26 for recommended operating range,  $C_L = 50 \text{ pF}$

SYMBOL	PARAMETER	60 MHz		66 MHz		75 MHz		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
f	CLK Frequency	30.0	60.0	33.3	66.7	37.5	75	MHz	
$t_1$	CLK Period	16.7	33.3	15.0	30.0	13.33	26.7	nS	
$t_2$	CLK Period Stability	-	±250	-	±250	-	±250	pS	
$t_3$	CLK High Time	4.0	-	4.0	-	4.0	-	nS	
$t_4$	CLK Low Time	4.0	-	4.0	-	4.0	-	nS	
$t_5$	CLK Fall Time	0.15	1.5	0.15	1.5	0.15	1.5	nS	
$t_6$	CLK Rise Time	0.15	1.5	0.15	1.5	0.15	1.5	nS	

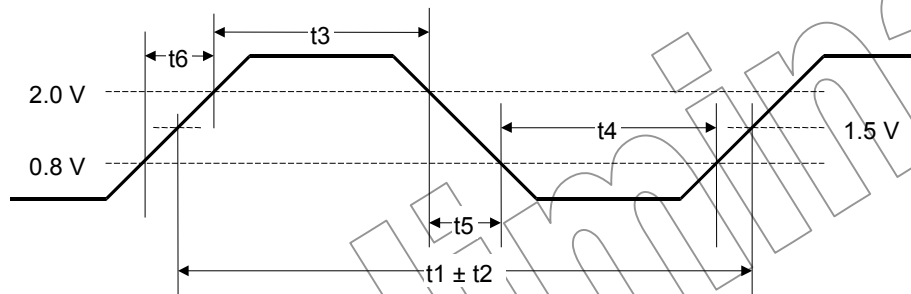


FIGURE 7A. CLOCK INPUT WAVEFORM

**TABLE 28B. AC SPECIFICATIONS**

See Table 26 for recommended operating range,  $C_L = 0 \text{ pF}$

Symbol	Parameter	83 MHz		95 MHz		100 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
f	CLK Frequency	41.5	83	47.5	95	50	100	MHz	
$t_1$	CLK Period	12.1	24.1	10.5	21.1	10	20	ns	
$t_2$	CLK Period Stability	–	±250	–	±250	–	±250	ps	
$t_3$	CLK High Time	3.0	–	3.0	–	3.0	–	ns	
$t_4$	CLK Low Time	3.0	–	3.0	–	3.0	–	ns	
$t_5$	CLK Fall Time	0.15	1.5	0.15	1.5	0.15	1.5	ns	
$t_6$	CLK Rise Time	0.15	1.5	0.15	1.5	0.15	1.5	ns	

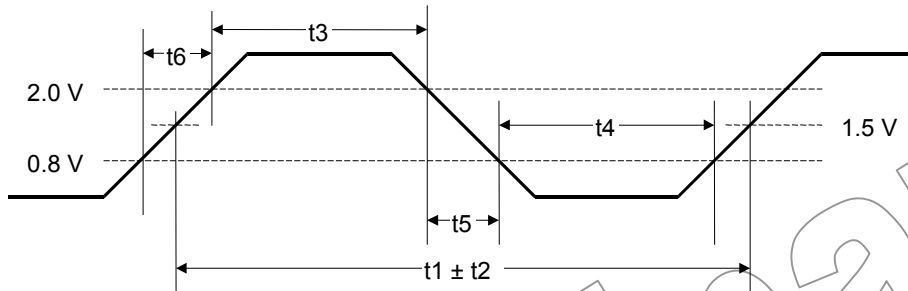
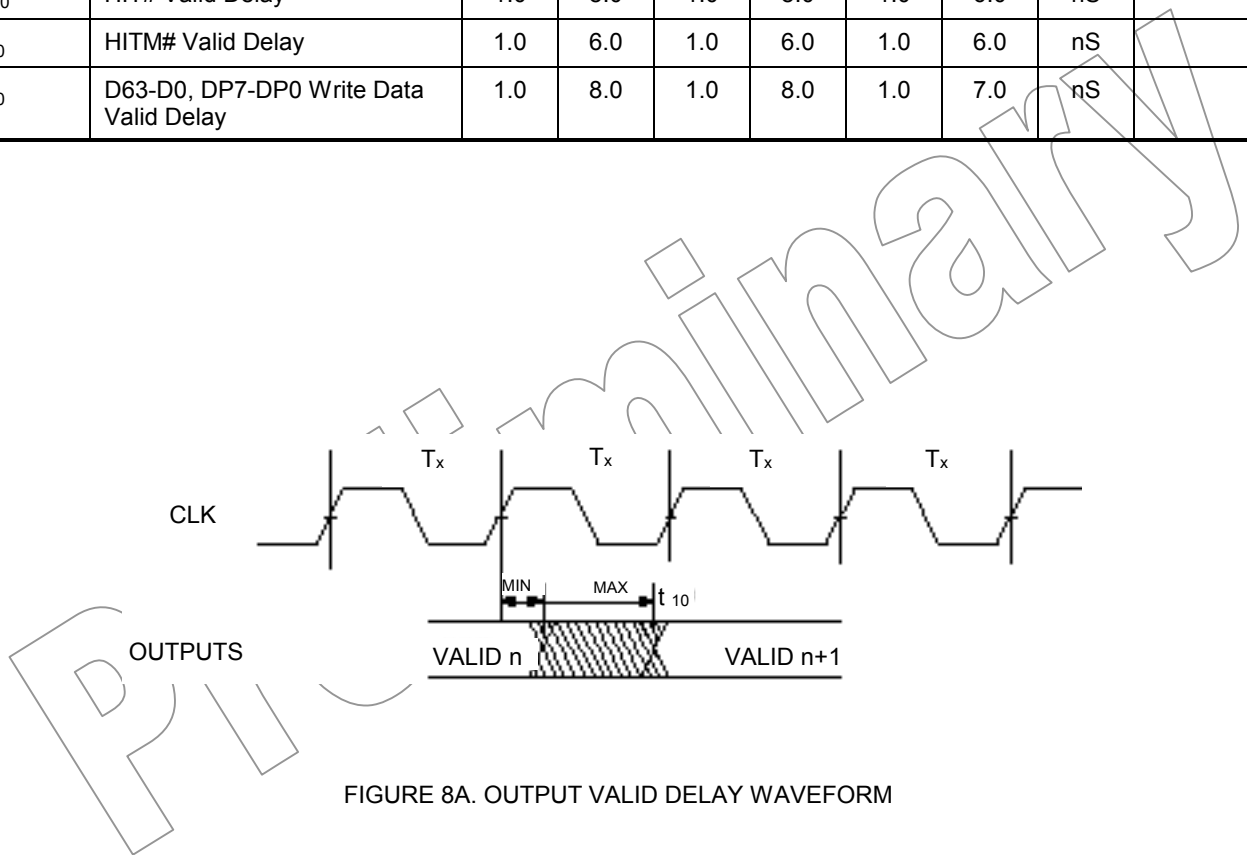


FIGURE 7B. CLOCK INPUT WAVEFORM

**TABLE 28A. AC SPECIFICATIONS (CONTINUED)**

See Table 26 for recommended operating range,  $C_L = 50$  pF

Symbol	Parameter	60 MHz		66 MHz		75 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
$t_{10}$	A31-3, ADSC#, BE7-BE0#, CACHE#, D/C#, LOCK3, PCD, PWT, SCYC, W/R# Valid Delay	1.0	7.0	1.0	7.0	1.0	6.0	nS	
$t_{10}$	AP Valid Delay	1.0	8.5	1.0	8.5	1.0	7.5	nS	
$t_{10}$	ADS#, M/IO# Valid Delay	1.0	7.0	1.0	6.0	1.0	6.0		
$t_{10}$	APCHK#, FERR#, IERR# Valid Delay	1.0	8.0	1.0	8.0	1.0	7.0	nS	
$t_{10}$	PCHK# Valid Delay	1.0	7.0	1.0	7.0	1.0	6.0	nS	
$t_{10}$	BREQ, HLDA, SMIACK# Valid Delay	1.0	8.0	1.0	8.0	1.0	6.0	nS	
$t_{10}$	HIT# Valid Delay	1.0	8.0	1.0	8.0	1.0	6.0	nS	
$t_{10}$	HITM# Valid Delay	1.0	6.0	1.0	6.0	1.0	6.0	nS	
$t_{10}$	D63-D0, DP7-DP0 Write Data Valid Delay	1.0	8.0	1.0	8.0	1.0	7.0	nS	



**FIGURE 8A. OUTPUT VALID DELAY WAVEFORM**

**TABLE 28B. AC SPECIFICATIONS (CONTINUED)**

See Table 26 for recommended operating range,  $C_L = 0$  pF

Symbol	Parameter	83 MHz		95 MHz		100 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
$t_{10}$	A31-A3 Valid Delay	1.1	4.0	1.1	4.0	1.1	4.0	ns	
$t_{10}$	AP Valid Delay	1.0	5.5	1.0	5.5	1.0	5.5	ns	
$t_{10}$	ADS#, ADSC#, D/C#, M/IO#, W/R# Valid Delay	1.0	4.0	1.0	4.0	1.0	4.0	ns	
$t_{10}$	APCHK#, FERR#, IERR# Valid Delay	1.0	4.5	1.0	4.5	1.0	4.5	ns	
$t_{10}$	PCHK# Valid Delay	1.0	4.5	1.0	4.5	1.0	4.5	ns	
$t_{10}$	BREQ, HLDA, SMIACK# Valid Delay	1.0	4.0	1.0	4.0	1.0	4.0	ns	
$t_{10}$	HIT# Valid Delay	1.0	4.0	1.0	4.0	1.0	4.0	ns	
$t_{10}$	BE7-BE0#, CACHE#, PCD, PWT, SCYC Valid Delay	1.0	4.0	1.0	4.0	1.0	4.0	ns	
$t_{10}$	D63-D0, DP7-DP0 Write Data Valid Delay	1.3	4.5	1.3	4.5	1.3	4.5	ns	
$t_{10}$	HITM# Valid Delay	1.0	5.5	1.1	4.0	1.1	4.0	ns	
$t_{10}$	LOCK# Valid Delay	1.0	6.0	1.1	4.0	1.1	4.0	ns	

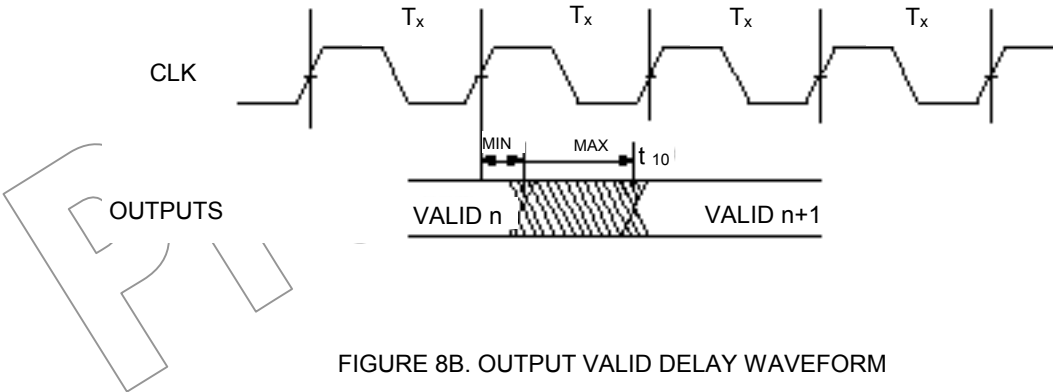


FIGURE 8B. OUTPUT VALID DELAY WAVEFORM

**TABLE 28A. AC SPECIFICATIONS (CONTINUED)** SEE TABLE 26 FOR RECOMMENDED OPERATING RANGE,  $C_L = 50$  PF

Symbol	Parameter	60 MHZ		66 MHZ		75 MHZ		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
$t_{20}$	A31-A3, ADS#, ADSC#, AP, BE7-BE0#, CACHE#, D/C#, LOCK#, M/IO#, PCD, PWT, SCYC, W/R# D63-D0, DP7-DP0 Write Data Float Delay		7.0		7.0		7.0	ns	1

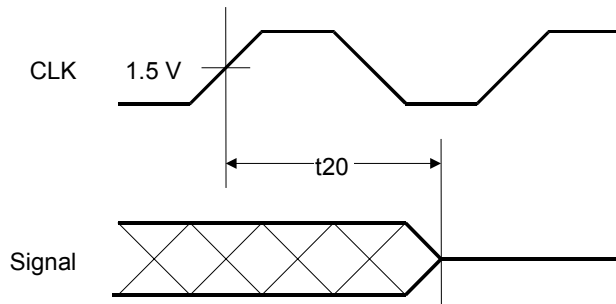


FIGURE 9A. OUTPUT FLOAT DELAY WAVEFORM

**TABLE 28B. AC SPECIFICATIONS (CONTINUED)** SEE TABLE 26 FOR RECOMMENDED OPERATING RANGE,  $C_L = 50$  PF

Symbol	Parameter	83 MHZ		95 MHZ		100 MHZ		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
$t_{20}$	A31-A3, ADS#, ADSC#, AP, BE7-BE0#, CACHE#, D/C#, LOCK#, M/IO#, PCD, PWT, SCYC, W/R# D63-D0, DP7-DP0 Write Data Float Delay		7.0		7.0		7.0	ns	1

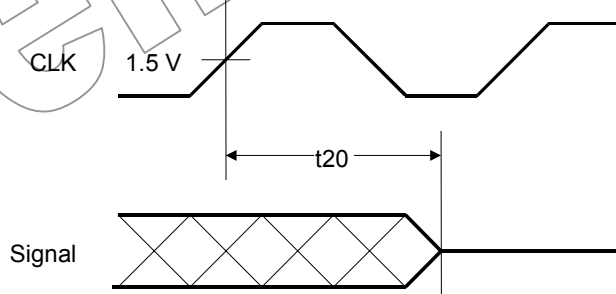
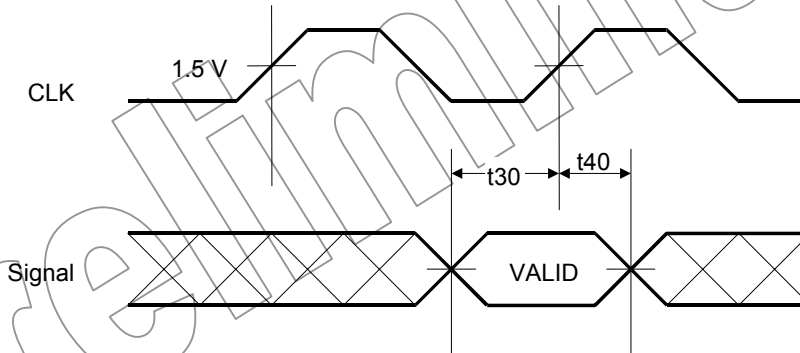


FIGURE 9B. OUTPUT FLOAT DELAY WAVEFORM

**TABLE 28A. AC SPECIFICATIONS (CONTINUED)**

See Table 26 for recommended operating range,  $C_L = 50$  pF

Symbol	Parameter	60 MHZ		66 MHZ		75 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t <sub>30</sub>	D63-D0, DP7-DP0 Read Data Setup Time	3.0		3.0		3.0		nS	
t <sub>30</sub>	NA#, WB/WT# Setup Time	4.5		4.5		3.3		nS	
t <sub>30</sub>	A31-A5, A20M#, AHOLD, AP, BOFF#, BRDY#, BRDYC#, EWBE#, HOLD, INTR, INV, KEN#, STPCLK# Setup Time	5.0		5.0		3.3		nS	
t <sub>30</sub>	FLUSH#, IGNNE#, INIT, NMI, SMI# Setup Time	5.0		5.0		3.3		nS	2
t <sub>30</sub>	EADS# Setup Time	5.0		5.0		4.0		nS	
t <sub>40</sub>	A20M#, AHOLD, AP, BOFF#, BRDY#, BRDYC#, EADS#, EWBE#, FLUSH#, HOL, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, SMI#, STPCL, WB/WT#, D63-D0, DP7-DP0, Read Data Hold Time	1.0		1.0		1.0		ns	
t <sub>45</sub>	FLUSH#, INIT, NMI, SMI#, IGNNE# Pulse Width, Async.	2		2		2		CLKs	2



**FIGURE 10A. INPUT SETUP AND HOLD WAVEFORM**

TABLE 28B. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range,  $C_L = 0$  pF

Symbol	Parameter	83 MHZ		95 MHZ		100 MHZ		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
$t_{30}$	STPCLK# Setup Time, and D63-D0, DP7-DP0 Read Data Setup Time	1.7		1.7		1.7		ns	
$t_{30}$	NMI, SMI# Setup Time	1.7		1.7		1.7		ns	2
$t_{30}$	A31-A5, A20M#, AP, BRDY#, BRDYC#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, WB/WT# Setup Time	3.0		3.0		3.0		ns	
$t_{30}$	AHOLD, BOFF# Setup Time	3.5		3.5		3.5		ns	
$t_{40}$	A31-A5, A20M#, AHOLD, AP, BOFF#, BRDY#, BRDYC#, EADS#, EWBE#, FLUSH#, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, SMI#, STPCLK#, WB/WT#, D63-D0, DP7-DP0, HOLD Read Data Hold Time	1.0		1.0		1.0		ns	
$t_{45}$	FLUSH#, INIT, NMI, SMI#, IGNNE# Pulse Width, Async.	2		2		2		CLKs	2

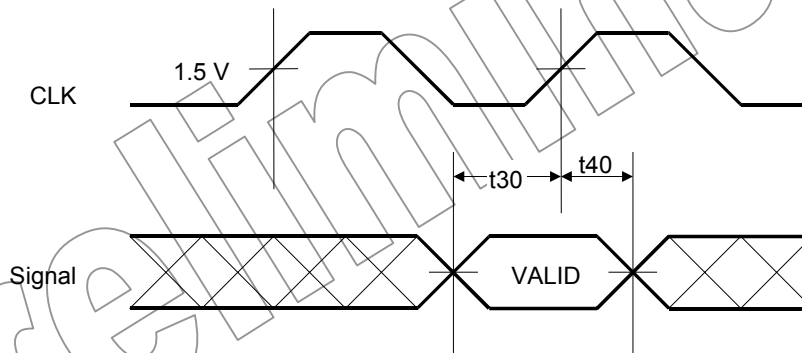


FIGURE 10B. INPUT SETUP AND HOLD WAVEFORM

TABLE 28A. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range,  $C_L = 50$  pF

Symbol	Parameter	60 MHZ		66 MHZ		75 MHZ		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t <sub>50</sub>	RESET Setup Time	5.0		5.0		5.0		ns	
t <sub>51</sub>	RESET Hold Time	1.0		1.0		1.0		ns	
t <sub>52</sub>	RESET Pulse Width, VCC & CLK Stable	15		15		15		CLKs	2
t <sub>52</sub>	RESET Active After VCC & CLK Stable	1.0		1.0		1.0		ms	7
t <sub>53</sub>	RESET Configuration Signals (BRDY#, BRDYC#, FLUSH#, INIT) Setup Time	2.0		2.0		2.0		CLKs	3, 4
t <sub>54</sub>	RESET Configuration Signals (BRDY#, BRDYC#, FLUSH#, INIT) Hold Time	2.0		2.0		2.0		CLKs	3, 4
t <sub>53</sub>	BF0, BF1 Setup Time	1.0		1.0		1.0		ms	5, 6
t <sub>54</sub>	BF0, BF1 Hold Time	2		2		2		CLKs	5, 6

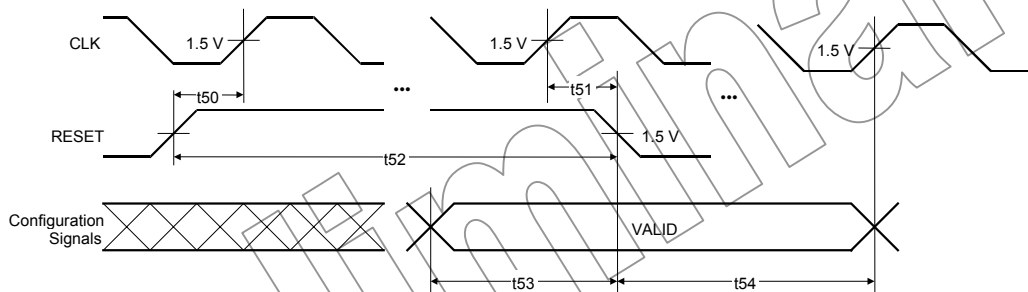


FIGURE 11A. RESET-CONFIGURATION WAVEFORMS

Notes:

1. Not 100% tested, guaranteed by design.
2. To provide proper asynchronous operation, RESET, NMI, FLUSH#, INIT and SMI# must be inactive for a minimum of 2 clocks before returning to the active state.
3. If FLUSH# is sampled active (low) at the falling edge of RESET, the output drivers will be put into tristate mode.
4. If INIT is sampled active (high) at the falling edge of RESET, the processor will execute its BIST algorithm.
5. Timing is relative to the falling edge of RESET.
6. BF1 and BF0 should be tied to VCC<sub>IO</sub> or VSS. Also see Table 24. Defaults via internal pull up / pull down resistors are BF1=1, BF0=0.
7. Active period at system power up.

TABLE 28B. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range,  $C_L = 0 \text{ pF}$

Symbol	Parameter	83 MHZ		95 MHZ		100 MHZ		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t <sub>50</sub>	RESET Setup Time	1.7		1.7		1.7		ns	
t <sub>51</sub>	RESET Hold Time	1.0		1.0		1.0		ns	
t <sub>52</sub>	RESET Pulse Width, VCC & CLK Stable	15		15		15		CLKs	2
t <sub>52</sub>	RESET Active After VCC & CLK Stable	1.0		1.0		1.0		ms	7
t <sub>53</sub>	RESET Configuration Signals (BRDY#, BRDYC#, FLUSH#, INIT) Setup Time	2		2		2		CLKs	3, 4
t <sub>54</sub>	RESET Configuration Signals (BRDY#, BRDYC#, FLUSH#, INIT) Hold Time	2		2		2		CLKs	3, 4
t <sub>53</sub>	BF0, BF1 Setup Time	1.0		1.0		1.0		ms	5, 6
t <sub>54</sub>	BF0, BF1 Hold Time	2		2		2		CLKs	5, 6

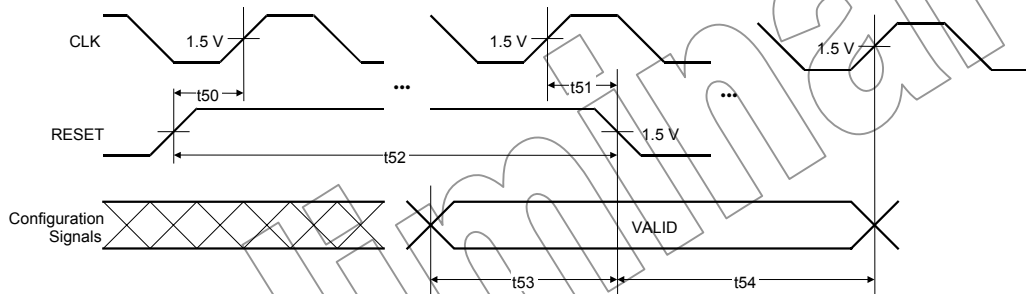


FIGURE 11B. RESET-CONFIGURATION WAVEFORMS

Notes:

1. Not 100% tested, guaranteed by design.
2. To provide proper asynchronous operation, RESET, NMI, FLUSH#, INIT and SMI# must be inactive for a minimum of 2 clocks before returning to the active state.
3. If FLUSH# is sampled active (low) at the falling edge of RESET, the output drivers will be put into tristate mode.
4. If INIT is sampled active (high) at the falling edge of RESET, the processor will execute its BIST algorithm.
5. Timing is relative to the falling edge of RESET.
6. BF1 and BF0 should be tied to VCC<sub>IO</sub> or VSS. Also see Table 24. Defaults via internal pull up / pull down resistors are BF1=1, BF0=0.
7. Active period at system power up.

**TABLE 29. JTAG AC SPECIFICATIONS**

See Table 16 for recommended operating range,  $C_L = 50$  pF

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
$f_{TCK}$	TCK Frequency		16.0	MHz		
$t_{61}$	TCK Period	62.5		ns		
$t_{63}$	TCK High Time	25.0		ns		
$t_{64}$	TCK Low Time	25.0		ns		
$t_{65}$	TCK Fall Time		5.0	ns		
$t_{66}$	TCK Rise Time		5.0	ns		
$t_{69}$	TRST# Pulse Width – Asynchronous	40.0		ns		1
$t_{71}$	TDI, TMS Setup Time	10.0		ns		2
$t_{72}$	TDI, TMS Hold Time	13.0		ns		2
$t_{73}$	TDO Valid Delay	3.0	20.0	ns		3
$t_{74}$	TDO Float Delay		25.0	ns		3
$t_{75}$	All outputs (excluding test) Valid Delay	3.0	20.0	ns		3,4
$t_{76}$	All outputs (excluding test) Float Delay		25.0	ns		3,4
$t_{77}$	All inputs (excluding test) Setup Time	10.0		ns		2,4
$t_{78}$	All inputs (excluding test) Hold Time	13.0		ns		2,4

Notes:

1. Not 100% tested, guaranteed by design.
2. Referenced to rising edge of TCK.
3. Referenced to falling edge of TCK.
4. Test input and outputs are TCK, TRST#, TDI, TDO, and TMS. Timing for the normal inputs and outputs are in response to JTAG boundary scan operations.

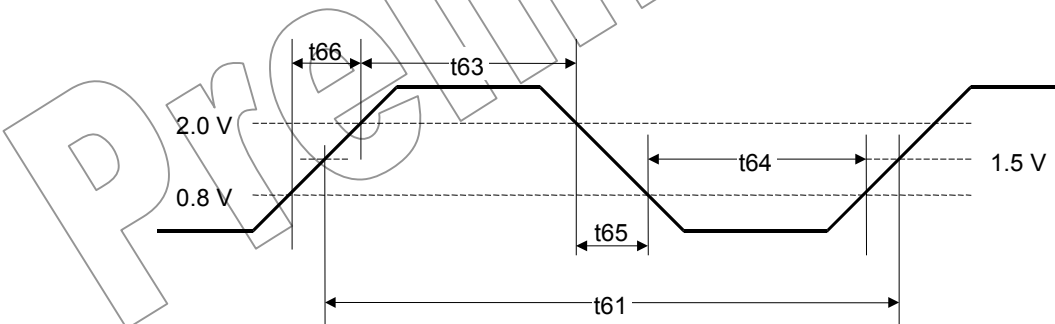


FIGURE 12. TEST CLOCK INPUT WAVEFORM

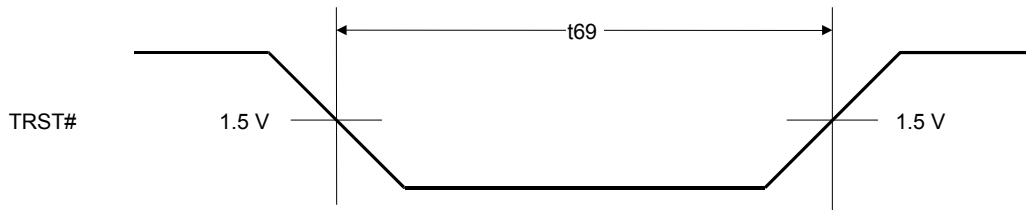


FIGURE 13. TEST RESET WAVEFORM

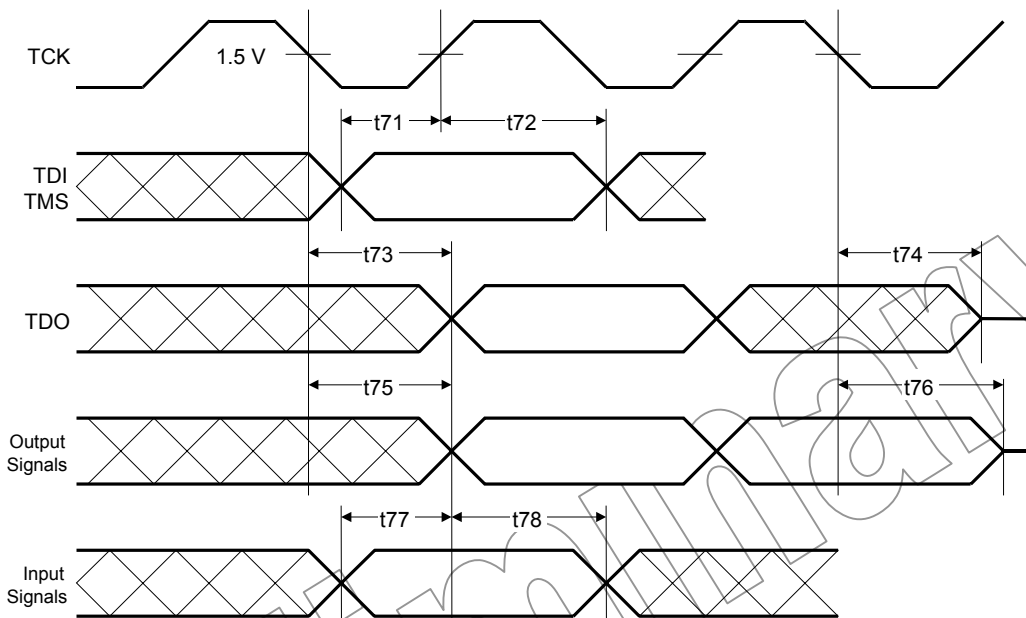


FIGURE 14. JTAG TEST WAVEFORMS



## 4.2 387 Ball T<sup>2</sup>BGA® Mechanical Drawing

### Top View

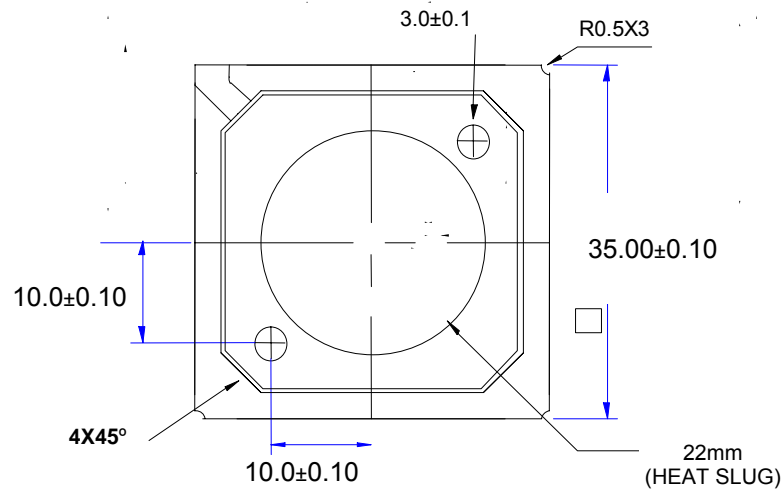
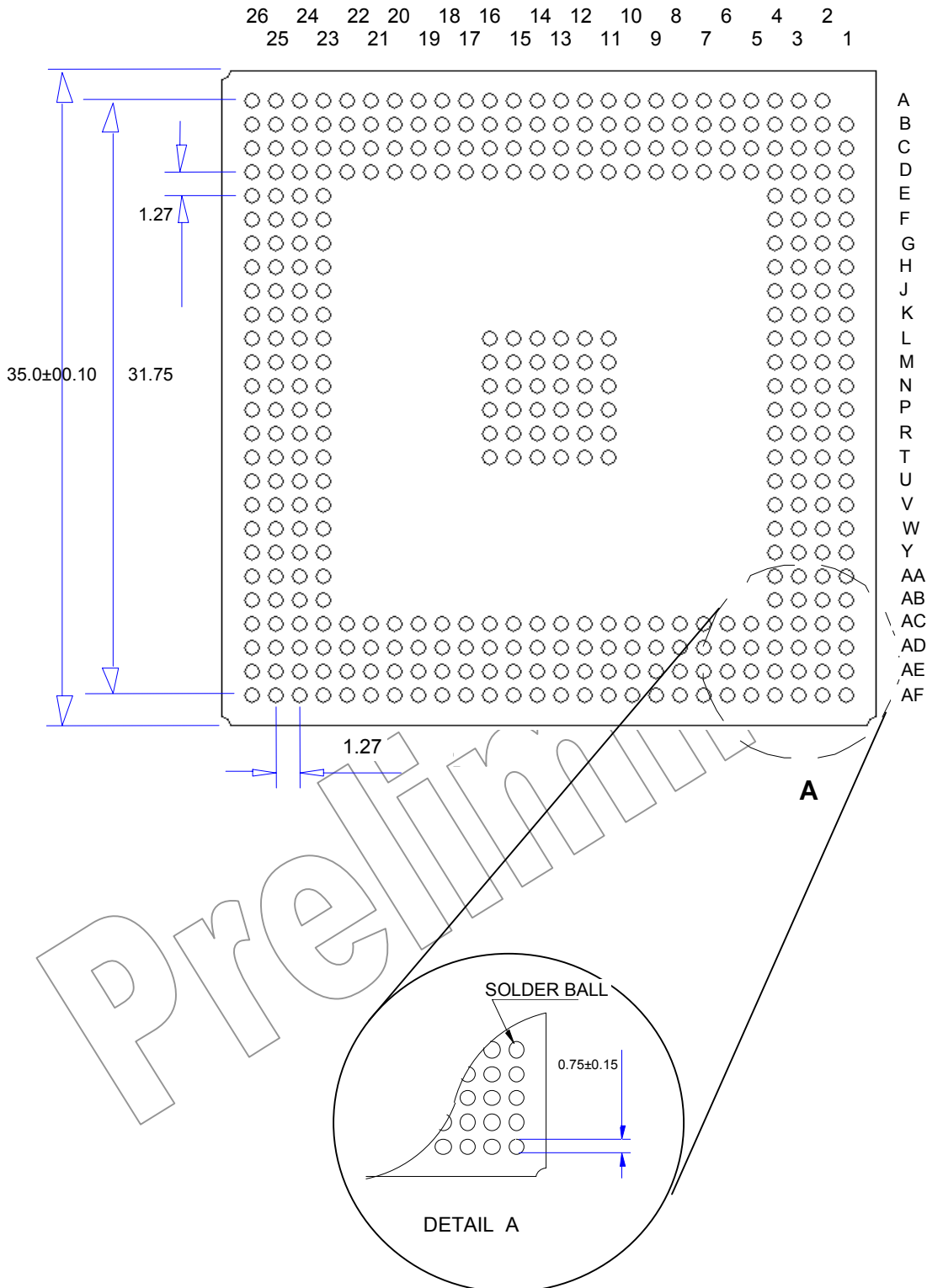


FIGURE 16. T<sup>2</sup>BGA® OUTLINE DRAWING

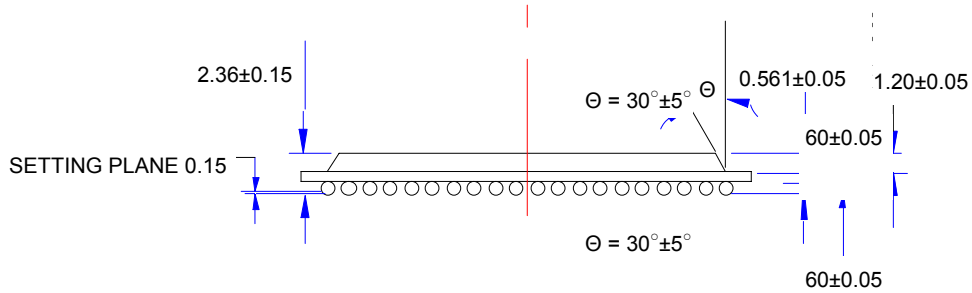
Bottom View

Figure 16. T<sup>2</sup>BGA® Outline Drawing (continued)



Side View

Figure 16. T<sup>2</sup>BGA® Outline Drawing (continued)



Note:

1. A1 Corner is identified by the metalized marking on substrate.
2. Ball Pitch is 1.27mm, Solder ball depopulation is allowed.  
(Depopulation is the omission of balls from a full matrix.)
3. Substrate thickness is optional: 0.56mm.

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Preliminary