


LC868016/12/08A
**8-Bit Single Chip Microcontroller with
16/12/08K-Byte ROM and 640-Byte RAM On Chip**
Preliminary
Overview

The LC868016A/12A/08A microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5 μ s (microseconds)
- On-chip ROM maximum capacity : 16K bytes
- On-chip RAM capacity : 640 bytes
- Dot-matrix liquid crystal display (LCD) automatic display controller / driver
- External memory
- 16-bit timer / counter (or two 8-bit timers)
- 16-bit timer / PWM (or two 8-bit timers)
- Two 8-bit synchronous serial-interface circuits
- 13-source 9-vectored interrupt system

All of the above functions are fabricated on a single chip.

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SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Features

(1) Read Only Memory (ROM) : LC868016A 16384 × 8 bits
 : LC868012A 12288 × 8 bits
 : LC868008A 8192 × 8 bits

(2) Random Access Memory (RAM) : 512 × 8 bits (calculation area)
 128 × 8 bits (display area)

(3) Bus Cycle Time / Instruction Cycle Time

| Bus cycle time | Instruction cycle time | System clock oscillation | Oscillation frequency | Voltage | Note |
|----------------|------------------------|--------------------------|-----------------------|----------|--------|
| 0.5μs | 1μs | Ceramic (CF) | 12MHz | 4.5-6.0V | OCR7=0 |
| | | | 6MHz | | OCR7=1 |
| 2.0μs | 4μs | Ceramic (CF) | 3MHz | 2.5-6.0V | OCR7=0 |
| | | | 1.5MHz | | OCR7=1 |
| 7.5μs | 15μs | Internal RC | 800kHz | 2.5-6.0V | OCR7=0 |
| 3.8μs | 7.5μs | | | | OCR7=1 |
| 183μs | 366μs | Crystal (XTAL) | 32.768kHz | 2.5-6.0V | OCR7=0 |
| 91.5 | 183μs | | | | OCR7=1 |

* Bus cycle time means ROM-read period.
 OCR7 : Bit-7 of the oscillation control register.

(4) Ports

- Input / output ports : 6 ports (47 terminals)
 Input/output port programmable in a nibble : 1 port (8 terminals)
 Input/output port programmable every function unit : 1 port (7 terminals)
 Input/output port programmable in a bit : 4 ports (32 terminals)
- Input port : 1 port (4 terminals)
- Ports at external memory mode
 1. External Latch
 - Port 0 : Address output of lower 8-bit, input/output of data
 - Port 2 : Address output of upper 8-bit
 - Port 5 : Bank address output
 2. No External Latch
 - Port 0 : Input/output of data
 - Port 3 : Address output of lower 8-bit
 - Port 2 : Address output of upper 8-bit
 - Port 5 : Bank address output
 (Set whether the external latch is used or not by program.)
- LCD segment driver output ports : 48 terminals
 (Function change available : segment/common)
- LCD common driver output ports : 16 terminals
 (1/64 duty maximum : at using segment output ports as common output by mask option)

(5) External memory access

- External program memory access function
 External program memory capacity : 64K bytes
 Programmable switch internal program/external program
 (At initial Internal program)
 Enable/disable control of external program --> internal program memory switch

Ports

Port 2 : Address output of upper 8-bit

Uses $\overline{\text{EROE}}$ terminal ($\overline{\text{OE}}$ signal of the external ROM)

1. Using the external latch

Port 0 : Address output of lower 8-bit, data input port

Uses the ADLC terminal (latch clock of the lower 8-bit address signal)

2. Not use the external latch

Port 0 : Input port of data

Port 3 : Address output of lower 8-bit

- External data memory access function

Using the LDC instruction

External memory capacity : 16M bytes

1. Internal program memory

Switch the reference of internal ROM data/external ROM data by program.

2. External program memory

Reference external ROM data only.

Ports

Port 2 : Address output of upper 8-bit

Port 5 : Bank address output

Uses $\overline{\text{EROE}}$ terminal ($\overline{\text{OE}}$ signal of the external ROM)

1. Using external latch

Port 0 : Address output of lower 8-bit, input port of data

Uses the ADLC terminal (latch clock of the lower 8-bit address signal)

2. Not use external latch

Port 0 : Input port of data

Port 3 : Address output of lower 8-bit

- External RAM memory access function

Using the LDX, STX instruction

External memory capacity : 16M bytes

Ports

Port 2 : Address output of upper 8-bit

Port 5 : Bank address output

Uses the P46 terminal ($\overline{\text{OE}}$ signal of external RAM) : the LDX instruction execution

Uses the P47 terminal ($\overline{\text{WE}}$ signal of external RAM) : the STX instruction execution

1. Using the external latch circuit

Port 0 : Address output of lower 8-bit, input/output port of data

Uses the ADLC terminal (latch clock of the lower 8-bit address signal)

2. Not use the external latch circuit

Port 0 : Input/output port of data

Port 3 : Address output of lower 8-bit

(6) LCD automatic display controller

- Display duty : 1/1 - 1/64 duty
- Display bias : 1/4, 1/5, 1/7, 1/9 bias
- Programmable character display / graphic display
- Character display

1. On-chip character generator ROM

ROM capacity : 8960 bits

Character font : 5 × 7 dots

Number of Characters : 256

2. LCD instruction

Display : ON/OFF

Cursor : ON/OFF/BLINK

Character blink : ON/OFF

Character scroll : Control by specified starting address

- Graphic display
 - LC868000 series : 1024 dots Maximum
 - External segment driver : Enable to extend of LCD drive
- LCD contrast
 - LCD display contrast programmable
- LCD display power supply
 - Doubler/Tripler circuit programmable
 - Doubler voltage in the tripler mode must not be used for LCD display power supply
 - If doubler voltage is used for LCD display power supply, the doubler mode must be selected by user program.

- LCD driver

Following three kinds of combination can be selected by mask option

| No. | Segment output port | Common output port |
|-----|---------------------|--------------------|
| 1 | 48 | 16 |
| 2 | 32 | 32 |
| 3 | 0 | 64 |

(7) Serial-interface

- Two 8-bit serial-interface circuits
 - LSB first / MSB first function available
- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(8) Timers

- Timer0 (T0L, T0H)
 - 16-bit timer / counter
 - 2-bit prescaler + 8-bit programmable prescaler
 - Mode 0 : Two 8-bit timers with programmable prescaler
 - Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
 - Mode 2 : 16-bit timer with a programmable prescaler
 - Mode 3 : 16-bit counter
- Timer1 (T1L, T1H)
 - 16-bit timer / PWM
 - Mode 0 : Two 8-bit timers
 - Mode 1 : 8-bit timer + 8-bit PWM
 - Mode 2 : 16-bit timer
 - Mode 3 : Variable-bit PWM (9-16 bits)
- Base timer
 - Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)
 - The Base timer clock selectable : 32.768kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(9) Buzzer output

- The Buzzer sound frequency selectable ; 4KHz, 2KHz

(10) Remote control receiver circuit (using P73/INT3/T0IN terminal)

- Noise rejection available
- The interrupt polarity selectable

(11) Watchdog timer

- The watchdog timer is taken on RC outside. (using P70/INT0 terminal)
- Watchdog timer operation selectable : interrupt system, system reset

(12) Interrupts system

- 13-source 9-vector interrupts :

1. External interrupt INT0 (includes watchdog timer)
2. External interrupt INT1
3. External interrupt INT2, timer / counter T0L (timer 0 lower 8 bits)
4. External interrupt INT3, base timer
5. Timer / counter T0H (timer 0 upper 8-bit)
6. Timer T1L (timer 1 lower 8-bit), Timer T1H (timer 1 upper 8-bit)
7. Serial interface SIO0
8. Serial interface SIO1
9. Port 0 or Port 3

- Interrupt priority control available

Microcomputer allows 3 levels of interrupt; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 0 or port 3 (the above interrupt number from three through nine). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(13) Sub-routine stack levels

- 128 levels (Max.) : stack area included in RAM area

(14) Multiplication and division

- 16 bits \times 8-bit (7 instruction cycle times)
- 16 bits / 8-bit (7 instruction cycle times)

(15) Three oscillation circuits

- On-chip RC oscillation circuit using for the system clock, for the LCD display and for the step-up circuit.
- On-chip CF oscillation circuit using for the system clock and for the LCD display.
- On-chip crystal oscillation circuit using for the system clock, for time-base clock and for the LCD display.

(16) Standby function

- HALT mode function

The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This operation mode can be released by the interrupt request signals or setting to low level for the reset terminal ($\overline{\text{RES}}$).

- HOLD mode function

The HOLD mode is used to freeze all the oscillations, RC (internal), CF and Crystal oscillations. This mode can be released by the following operations:

- Reset terminal ($\overline{\text{RES}}$) set to low level.
- Set to assigned level to INT0/1 terminals.
- Set to assigned level to Port 0/3.

(17) Factory shipment

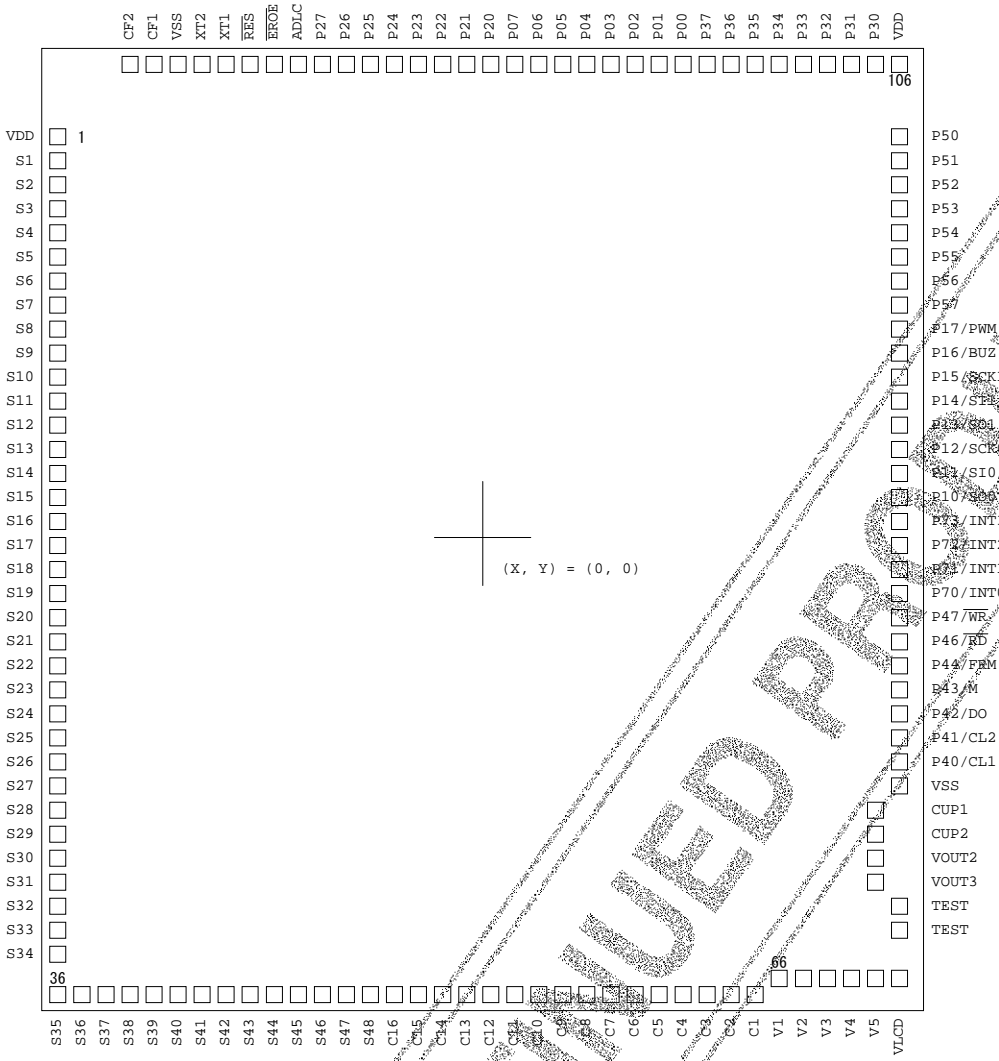
- Chip

QIC160 package shipping available for sample evaluation.

(18) Development support tools

- Evaluation (EVA) chip : LC868099
- Emulator : EVA86000 + ECB868000 (Evaluation chip board)

Pin Assignment



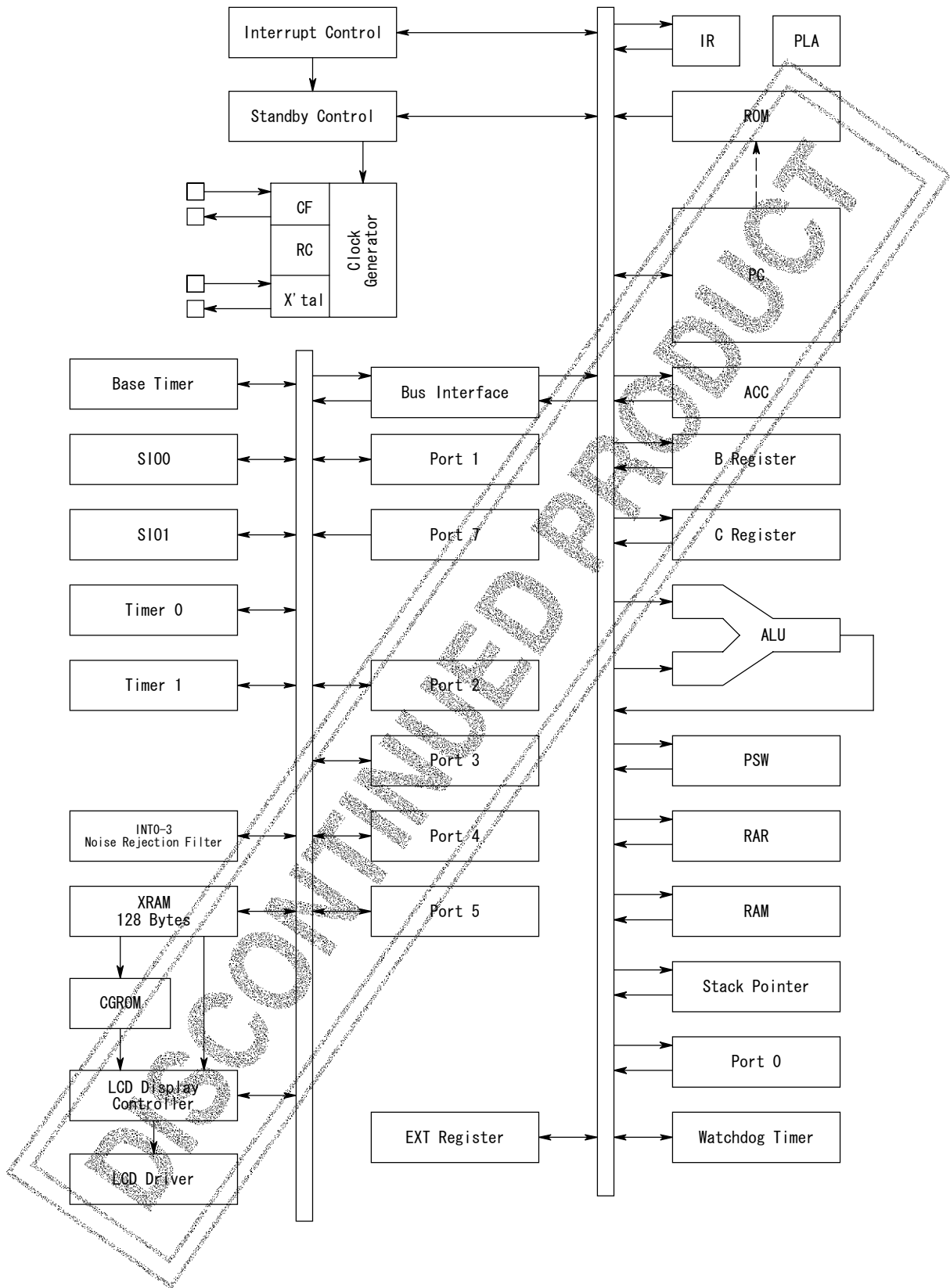
DISCONTINUED PRODUCT

Pad Name and coordinates table

| Pad No. | Name | Coordinates | | Pad No. | Name | Coordinates | | Pad No. | Name | Coordinates | |
|---------|------|-------------|-----------|---------|-------|-------------|-----------|---------|------|-------------|-----------|
| | | X μ m | Y μ m | | | X μ m | Y μ m | | | X μ m | Y μ m |
| 1 | VDD | -2960 | 2695 | 47 | S46 | -1075 | -3630 | 93 | P13 | 2845 | 500 |
| 2 | S1 | -2960 | 2505 | 48 | S47 | -915 | -3630 | 94 | P14 | 2845 | 675 |
| 3 | S2 | -2960 | 2345 | 49 | S48 | -750 | -3630 | 95 | P15 | 2845 | 855 |
| 4 | S3 | -2960 | 2180 | 50 | C16 | -590 | -3630 | 96 | P16 | 2845 | 1035 |
| 5 | S4 | -2960 | 2020 | 51 | C15 | -425 | -3630 | 97 | P17 | 2845 | 1215 |
| 6 | S5 | -2960 | 1855 | 52 | C14 | -265 | -3630 | 98 | P57 | 2845 | 1400 |
| 7 | S6 | -2960 | 1695 | 53 | C13 | -100 | -3630 | 99 | P56 | 2845 | 1580 |
| 8 | S7 | -2960 | 1530 | 54 | C12 | 60 | -3630 | 100 | P55 | 2845 | 1760 |
| 9 | S8 | -2960 | 1370 | 55 | C11 | 225 | -3630 | 101 | P54 | 2845 | 1935 |
| 10 | S9 | -2960 | 1205 | 56 | C10 | 385 | -3630 | 102 | P53 | 2845 | 2115 |
| 11 | S10 | -2960 | 1045 | 57 | C9 | 550 | -3630 | 103 | P52 | 2845 | 2295 |
| 12 | S11 | -2960 | 880 | 58 | C8 | 710 | -3630 | 104 | P51 | 2845 | 2475 |
| 13 | S12 | -2960 | 720 | 59 | C7 | 875 | -3630 | 105 | P50 | 2845 | 2650 |
| 14 | S13 | -2960 | 555 | 60 | C6 | 1035 | -3630 | 106 | VDD | 2965 | 3530 |
| 15 | S14 | -2960 | 395 | 61 | C5 | 1200 | -3630 | 107 | P30 | 2800 | 3530 |
| 16 | S15 | -2960 | 230 | 62 | C4 | 1360 | -3630 | 108 | P31 | 2620 | 3530 |
| 17 | S16 | -2960 | 70 | 63 | C3 | 1525 | -3630 | 109 | P32 | 2445 | 3530 |
| 18 | S17 | -2960 | -95 | 64 | C2 | 1685 | -3630 | 110 | P33 | 2265 | 3530 |
| 19 | S18 | -2960 | -255 | 65 | C1 | 1850 | -3630 | 111 | P34 | 2085 | 3530 |
| 20 | S19 | -2960 | -420 | 66 | V1 | 2055 | -3445 | 112 | P35 | 1905 | 3530 |
| 21 | S20 | -2960 | -580 | 67 | V2 | 2220 | -3445 | 113 | P36 | 1730 | 3530 |
| 22 | S21 | -2960 | -745 | 68 | V3 | 2380 | -3445 | 114 | P37 | 1550 | 3530 |
| 23 | S22 | -2960 | -905 | 69 | V4 | 2545 | -3445 | 115 | P00 | 1370 | 3530 |
| 24 | S23 | -2960 | -1070 | 70 | V5 | 2705 | -3445 | 116 | P01 | 1190 | 3530 |
| 25 | S24 | -2960 | -1230 | 71 | VLCD | 2870 | -3445 | 117 | P02 | 1015 | 3530 |
| 26 | S25 | -2960 | -1395 | 72 | TEST | 2915 | -3180 | 118 | P03 | 835 | 3530 |
| 27 | S26 | -2960 | -1555 | 73 | TEST | 2915 | -2995 | 119 | P04 | 655 | 3530 |
| 28 | S27 | -2960 | -1720 | 74 | VOUT3 | 2820 | -2810 | 120 | P05 | 475 | 3530 |
| 29 | S28 | -2960 | -1880 | 75 | VOUT2 | 2820 | -2650 | 121 | P06 | 300 | 3530 |
| 30 | S29 | -2960 | -2045 | 76 | CUP2 | 2820 | -2485 | 122 | P07 | 120 | 3530 |
| 31 | S30 | -2960 | -2205 | 77 | CUP1 | 2820 | -2325 | 123 | P20 | -60 | 3530 |
| 32 | S31 | -2960 | -2370 | 78 | VSS | 2845 | -2120 | 124 | P21 | -240 | 3530 |
| 33 | S32 | -2960 | -2530 | 79 | P40 | 2845 | -1945 | 125 | P22 | -415 | 3530 |
| 34 | S33 | -2960 | -2695 | 80 | P41 | 2845 | -1765 | 126 | P23 | -595 | 3530 |
| 35 | S34 | -2960 | -2855 | 81 | P42 | 2845 | -1585 | 127 | P24 | -775 | 3530 |
| 36 | S35 | -2865 | -3630 | 82 | P43 | 2845 | -1410 | 128 | P25 | -955 | 3530 |
| 37 | S36 | -2700 | -3630 | 83 | P44 | 2845 | -1230 | 129 | P26 | -1130 | 3530 |
| 38 | S37 | -2540 | -3630 | 84 | P46 | 2845 | -1050 | 130 | P27 | -1310 | 3530 |
| 39 | S38 | -2375 | -3630 | 85 | P47 | 2845 | -870 | 131 | ADLC | -1490 | 3530 |
| 40 | S39 | -2215 | -3630 | 86 | P70 | 2845 | -690 | 132 | EROE | -1670 | 3530 |
| 41 | S40 | -2050 | -3630 | 87 | P71 | 2845 | -525 | 133 | RES | -1845 | 3530 |
| 42 | S41 | -1890 | -3630 | 88 | P72 | 2845 | -365 | 134 | XT1 | -2025 | 3530 |
| 43 | S42 | -1725 | -3630 | 89 | P73 | 2845 | -200 | 135 | XT2 | -2205 | 3530 |
| 44 | S43 | -1565 | -3630 | 90 | P10 | 2845 | -40 | 136 | VSS | -2385 | 3530 |
| 45 | S44 | -1400 | -3630 | 91 | P11 | 2845 | 140 | 137 | CF1 | -2560 | 3530 |
| 46 | S45 | -1240 | -3630 | 92 | P12 | 2845 | 320 | 138 | CF2 | -2740 | 3530 |

Note ; Connect the substrate of chip to VDD (or open).

System Block Diagram

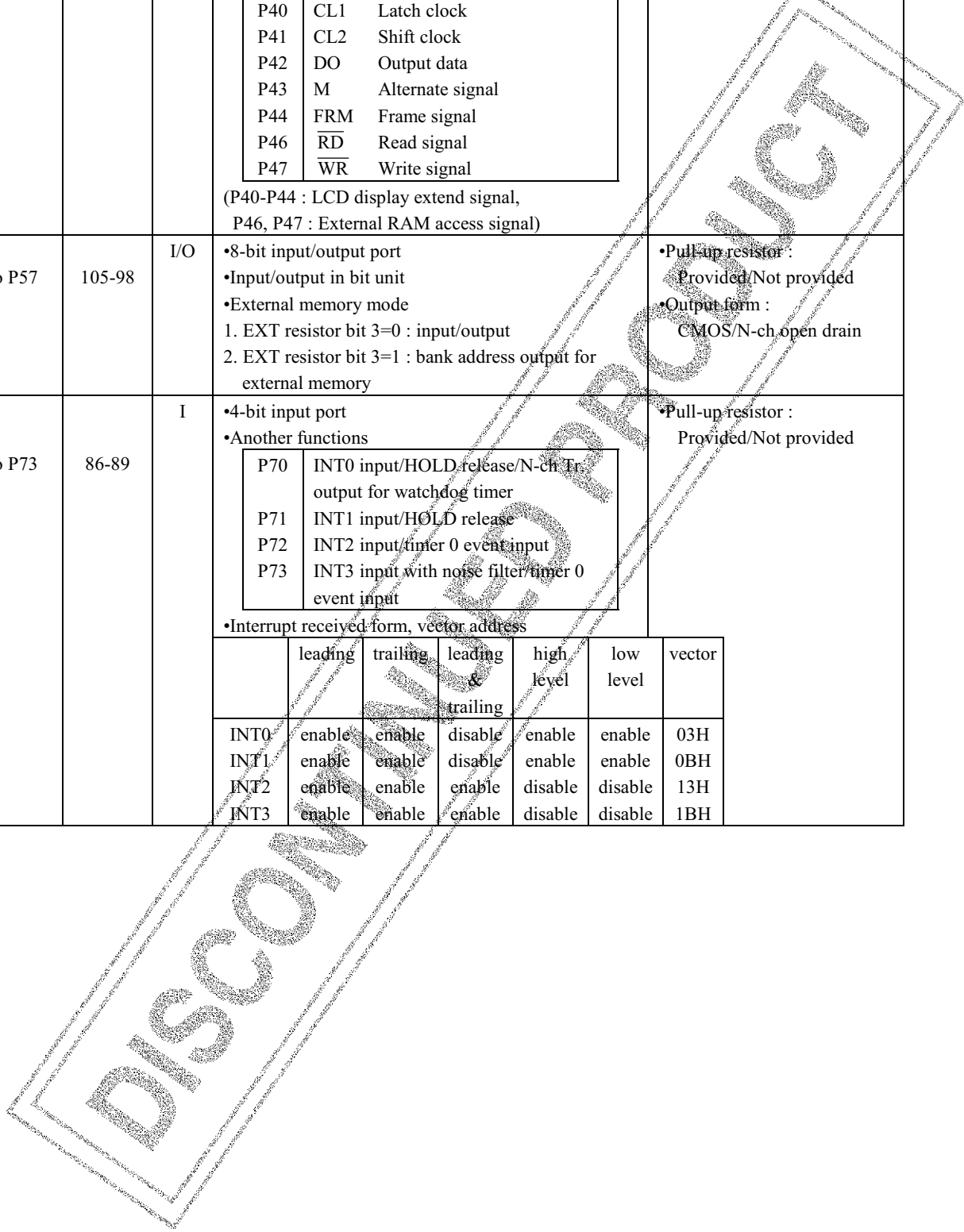


Pin Description

| Name | No. | I/O | Function description | Option | | | | | | | | | | | | | | | | |
|---------------------|-----------------------------------|-----|---|--|------------------|-----|-----------------------------------|-----|-------------------------|-----|------------------|-----|-----------------------------------|-----|-------------------------|-----|---------------|-----|-----------------------------|---|
| VSS | 78,136 | - | Power terminal (-) | - | | | | | | | | | | | | | | | | |
| VDD | 1,106 | - | Power terminal (+) | - | | | | | | | | | | | | | | | | |
| VLCD | 71 | - | Power terminal (-) for LCD driver | - | | | | | | | | | | | | | | | | |
| V1 to 5 | 66-70 | - | Voltage supply terminals to LCD drivers | - | | | | | | | | | | | | | | | | |
| VOU2,3 | 75,74 | - | Output terminals for doubler, tripler | - | | | | | | | | | | | | | | | | |
| CUP1,2 | 77,76 | - | Capacitor connecting terminals for doubler, tripler | - | | | | | | | | | | | | | | | | |
| Port0 P00 to P07 | 115-122 | I/O | <ul style="list-style-type: none"> •8-bit input/output port •Input/output can be specified in 4-bit •External memory mode <ol style="list-style-type: none"> 1. EXT resistor bit 2=0 Address output of lower 8-bit, input/output of data 2. EXT resistor bit 2=1 •Input/output of data •Input for key interrupt (P30INT=0)* | <ul style="list-style-type: none"> •Pull-up resistor Provided/Not provided •Output form CMOS/N-ch open drain | | | | | | | | | | | | | | | | |
| Port1 P10 to P17 | 90-97 | I/O | <ul style="list-style-type: none"> •8-bit input/output port •Input/output can be specified in a bit •Another functions <table border="1" style="margin-left: 20px; width: 100%;"> <tbody> <tr><td>P10</td><td>SIO0 data output</td></tr> <tr><td>P11</td><td>SIO0 data input, bus input/output</td></tr> <tr><td>P12</td><td>SIO0 clock input/output</td></tr> <tr><td>P13</td><td>SIO1 data output</td></tr> <tr><td>P14</td><td>SIO1 data input, bus input/output</td></tr> <tr><td>P15</td><td>SIO1 clock input/output</td></tr> <tr><td>P16</td><td>Buzzer output</td></tr> <tr><td>P17</td><td>Timer 1 output (PWM output)</td></tr> </tbody> </table> | P10 | SIO0 data output | P11 | SIO0 data input, bus input/output | P12 | SIO0 clock input/output | P13 | SIO1 data output | P14 | SIO1 data input, bus input/output | P15 | SIO1 clock input/output | P16 | Buzzer output | P17 | Timer 1 output (PWM output) | <ul style="list-style-type: none"> •Output form : CMOS/N-ch open drain |
| P10 | SIO0 data output | | | | | | | | | | | | | | | | | | | |
| P11 | SIO0 data input, bus input/output | | | | | | | | | | | | | | | | | | | |
| P12 | SIO0 clock input/output | | | | | | | | | | | | | | | | | | | |
| P13 | SIO1 data output | | | | | | | | | | | | | | | | | | | |
| P14 | SIO1 data input, bus input/output | | | | | | | | | | | | | | | | | | | |
| P15 | SIO1 clock input/output | | | | | | | | | | | | | | | | | | | |
| P16 | Buzzer output | | | | | | | | | | | | | | | | | | | |
| P17 | Timer 1 output (PWM output) | | | | | | | | | | | | | | | | | | | |
| Port2 P20 to P27 | 123-130 | I/O | <ul style="list-style-type: none"> •8-bit input/output port •Input/output can be specified in a bit •External memory mode Address output of upper 8-bit | <ul style="list-style-type: none"> •Output form : CMOS/N-ch open drain | | | | | | | | | | | | | | | | |
| Port3 P30 to P37 | 107-114 | I/O | <ul style="list-style-type: none"> •8-bit input/output port •Input/output in a bit •External memory mode <ol style="list-style-type: none"> 1. EXT resistor bit 2=0 : input/output port 2. EXT resistor bit 2=1 : address output of lower 8-bit for external memory •Input for key interrupt (P30INT=L)* | <ul style="list-style-type: none"> •Pull-up resistor : Provided/Not provided •Output form : CMOS/N-ch open drain | | | | | | | | | | | | | | | | |

*P30INT : Bit 0 of Port 3 interrupt control register.

| Name | No. | I/O | Function description | Option | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------------|---|------------------|--|--|---|-------------|-------------------------|-----|--------------------------------|-----|--|-------------|---------|----------|--------------------|------------|-----------|--------------|------|-----------------|-------------|---------|-----------------|--------------|--|------|--------|--------|---------|--------|--------|-----|------|--------|--------|--------|---------|---------|-----|------|--------|--------|--------|---------|---------|-----|---|
| Port4 P40 to P44 P46, P47 | 79-83 84,85 | I/O | <ul style="list-style-type: none"> •7-bit input/output port •Input/output can be specified each upper 2 bits and lower 5 bits •Another functions <table border="1" style="margin-left: 20px;"> <tr><td>P40</td><td>CL1</td><td>Latch clock</td></tr> <tr><td>P41</td><td>CL2</td><td>Shift clock</td></tr> <tr><td>P42</td><td>DO</td><td>Output data</td></tr> <tr><td>P43</td><td>M</td><td>Alternate signal</td></tr> <tr><td>P44</td><td>FRM</td><td>Frame signal</td></tr> <tr><td>P46</td><td>\overline{RD}</td><td>Read signal</td></tr> <tr><td>P47</td><td>\overline{WR}</td><td>Write signal</td></tr> </table> <p>(P40-P44 : LCD display extend signal, P46, P47 : External RAM access signal)</p> | P40 | CL1 | Latch clock | P41 | CL2 | Shift clock | P42 | DO | Output data | P43 | M | Alternate signal | P44 | FRM | Frame signal | P46 | \overline{RD} | Read signal | P47 | \overline{WR} | Write signal | <ul style="list-style-type: none"> •Pull-up resistor : Provided/Not provided •Output form : CMOS/N-ch open drain | | | | | | | | | | | | | | | | | | | | | | |
| P40 | CL1 | Latch clock | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P41 | CL2 | Shift clock | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P42 | DO | Output data | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P43 | M | Alternate signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P44 | FRM | Frame signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P46 | \overline{RD} | Read signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P47 | \overline{WR} | Write signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port5 P50 to P57 | 105-98 | I/O | <ul style="list-style-type: none"> •8-bit input/output port •Input/output in bit unit •External memory mode <ol style="list-style-type: none"> 1. EXT resistor bit 3=0 : input/output 2. EXT resistor bit 3=1 : bank address output for external memory | <ul style="list-style-type: none"> •Pull-up resistor : Provided/Not provided •Output form : CMOS/N-ch open drain | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port7 P70 to P73 | 86-89 | I | <ul style="list-style-type: none"> •4-bit input port •Another functions <table border="1" style="margin-left: 20px;"> <tr><td>P70</td><td>INT0 input/HOLD release/N-ch Tr output for watchdog timer</td></tr> <tr><td>P71</td><td>INT1 input/HOLD release</td></tr> <tr><td>P72</td><td>INT2 input/timer 0 event input</td></tr> <tr><td>P73</td><td>INT3 input with noise filter/timer 0 event input</td></tr> </table> •Interrupt received form, vector address <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>leading</th> <th>trailing</th> <th>leading & trailing</th> <th>high level</th> <th>low level</th> <th>vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table> | P70 | INT0 input/HOLD release/N-ch Tr output for watchdog timer | P71 | INT1 input/HOLD release | P72 | INT2 input/timer 0 event input | P73 | INT3 input with noise filter/timer 0 event input | | leading | trailing | leading & trailing | high level | low level | vector | INT0 | enable | enable | disable | enable | enable | 03H | INT1 | enable | enable | disable | enable | enable | 0BH | INT2 | enable | enable | enable | disable | disable | 13H | INT3 | enable | enable | enable | disable | disable | 1BH | <ul style="list-style-type: none"> •Pull-up resistor : Provided/Not provided |
| P70 | INT0 input/HOLD release/N-ch Tr output for watchdog timer | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P71 | INT1 input/HOLD release | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P72 | INT2 input/timer 0 event input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P73 | INT3 input with noise filter/timer 0 event input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | leading | trailing | leading & trailing | high level | low level | vector | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT0 | enable | enable | disable | enable | enable | 03H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT1 | enable | enable | disable | enable | enable | 0BH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT2 | enable | enable | enable | disable | disable | 13H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT3 | enable | enable | enable | disable | disable | 1BH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |



| Name | No. | I/O | Function description | Option |
|-----------|-------|-----|--|--|
| C1 to C16 | 65-50 | O | LCD output terminals for common | - |
| S1 to S48 | 2-49 | O | LCD output terminals for segment | LCD output terminals : segment/common |
| RES | 133 | I | Reset | - |
| ADLC | 131 | O | Address control signal for external memory | - |
| EROE | 132 | O | Enable signal of external ROM output | - |
| XT1 | 134 | I | Input for 32.768kHz crystal oscillation In case of non use, connect to VDD | - |
| XT2 | 135 | O | Output for 32.768kHz crystal oscillation In case of non use, should be left unconnected | - |
| CF1 | 137 | I | Input for ceramic resonator oscillation In case of non use, connect to VDD | - |
| CF2 | 138 | O | Output for ceramic resonator oscillation In case of non use, should be left unconnected | - |

* Port options can be specified in a bit.

* A state of port at initial

| Pin name | Input/output mode | A state of pull-up resistor specified at pull-up option |
|--------------------------|-------------------|---|
| Port 0, 7 | Input | Fixed pull-up resistor exist |
| Ports 1, 2 Ports 3, 5 | Input | Programmable pull-up resistor OFF |
| Port 4 | Input | Programmable pull-up resistor ON |

| Name | Output level |
|-----------|-------------------|
| C1 to C16 | VDD (Display OFF) |
| S1 to S48 | VDD (Display OFF) |

DISCONTINUED PRODUCT

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | | |
|-----------------------------|----------------------|--------------------------------|---|------------------------------|----------|------|---------|------|--|
| | | | | VDD[V] | min. | typ. | | max. | |
| Supply voltage | VDDMAX | VDD | | | -0.3 | | +7.0 | V | |
| Input voltage | VI(1) | •Ports 71,72,73 •RES | | | -0.3 | | VDD+0.3 | | |
| | VI(2) | VLCD | | | VDD-21 | | VDD+0.3 | | |
| Output voltage | VO(1) | •C1 to C16 •S1 to S48 | | | VLCD-0.3 | | VDD+0.3 | | |
| | VO(2) | •VOUT2,VOUT3 •CUP1,CUP2 | | | VDD-21 | | VDD+0.3 | | |
| | VO(3) | ADLC, $\overline{\text{EROE}}$ | | | -0.3 | | VDD+0.3 | | |
| Input/output voltage | VIO(1) | •Ports 0,1,2,3,4,5 •Port 70 | | | -0.3 | | VDD+0.3 | | |
| High level output current | Peak output current | IOPH(1) | •Ports 0,1,2,3,4,5 •ADLC, $\overline{\text{EROE}}$ | •CMOS output •At each pin | -4 | | | mA | |
| | Total output current | Σ IOAH(1) | •Ports 0,2,3 •C1-C16,S1-S48 •ADLC, $\overline{\text{EROE}}$ | Total all pins | -25 | | | | |
| | | Σ IOAH(2) | Ports 1, 4, 5 | Total all pins | -25 | | | | |
| Low level output current | Peak output current | IOPL(1) | •Ports 0,1,2,3,4,5 •ADLC, $\overline{\text{EROE}}$ | At each pin | | | 20 | | |
| | | IOPL(2) | Port 70 | At each pin | | | 15 | | |
| | Total output current | Σ IOAL(1) | Port 0 | Total all pins | | | | 40 | |
| | | Σ IOAL(2) | •Port 2 •ADLC, $\overline{\text{EROE}}$ | Total all pins | | | | 40 | |
| | | Σ IOAL(3) | Port 3 | Total all pins | | | | 40 | |
| | | Σ IOAL(4) | Ports 1, 5 | Total all pins | | | | 40 | |
| | | Σ IOAL(5) | Port 4 | Total all pins | | | | 40 | |
| | | Σ IOAL(6) | Port 70 | Total all pins | | | | 15 | |
| Σ IOAL(7) | C1-C16,S1-S48 | Total all pins | | | | 30 | | | |
| Operating temperature range | Topr | | | | -30 | | +70 | °C | |
| Storage temperature range | Tstg | | | | -55 | | +125 | | |

Notes :

The specifications above are for a die mounted in a QIC160 type package.
 However, we ship this product as a die only, not a package chip.
 Therefore, the operational characteristics may vary depending on the user's packaging techniques.

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | | |
|---|----------|---|--|--|------------|--------|------------|------|-----|
| | | | | VDD[V] | min. | typ. | | max. | |
| Operating supply voltage range | VDD(1) | VDD | 0.98μs ≤ tCYC ≤ 400μs | | 4.5 | | 6.0 | V | |
| | VDD(2) | | 1.9μs ≤ tCYC ≤ 400μs | | 4.5 | | 6.0 | | |
| | VDD(3) | | 3.9μs ≤ tCYC ≤ 400μs | | 2.5 | | 6.0 | | |
| Hold voltage | VHD | VDD | RAMs and the registers hold voltage at HOLD mode. | | 2.0 | | 6.0 | | |
| LCD display voltage | VLCD | VLCD | | 4.5-6.0 | -2VDD | | VDD-4.5 | | |
| | | | | 2.5-4.5 | -VDD | | VDD-4.5 | | |
| Input high voltage | VIH(1) | Port 0 (Schmitt) | Output disable | 2.5-6.0 | 0.4VDD+0.9 | | VDD | | |
| | VIH(2) | •Ports 1,2,4,5 •Ports 72,73 (Schmitt) | Output disable | 2.5-6.0 | 0.75VDD | | VDD | | |
| | VIH(3) | •Port 70 for Port input/interrupt •Port 71 •RES (Schmitt) | Output N-channel Tr. OFF | 2.5-6.0 | 0.75VDD | | VDD | | |
| | VIH(4) | Port 70 for watchdog timer | Output N-channel Tr. OFF | 2.5-6.0 | 0.9VDD | | VDD | | |
| | VIH(5) | Port 3 | Output disable | 2.5-6.0 | 0.75VDD | | VDD | | |
| Input low voltage | VIL(1) | Port 0 (Schmitt) | Output disable | 2.5-6.0 | VSS | | 0.2VDD | | |
| | VIL(2) | •Ports 1,2,4,5 •Ports 72,73 (Schmitt) | Output disable | 2.5-6.0 | VSS | | 0.25VDD | | |
| | VIL(3) | •Port 70 Port input/interrupt •Port 71 •RES | Output N-channel Tr. OFF | 2.5-6.0 | VSS | | 0.25VDD | | |
| | VIL(4) | Port 70 for watchdog timer | Output N-channel Tr. OFF | 2.5-6.0 | VSS | | 0.8VDD-1.0 | | |
| | VIL(5) | Port 3 | Output disable | 2.5-6.0 | VSS | | 0.25VDD | | |
| Operation cycle time | tCYC | | | 4.5-6.0 | 0.98 | | 400 | μs | |
| | | | | 2.5-6.0 | 3.9 | | 400 | | |
| Oscillation frequency range (Note 1) | FmCF(1) | CF1, CF2 | •12MHz (ceramic resonator oscillation) •Refer to figure 1 | 4.5-6.0 | 11.76 | 12 | 12.24 | MHz | |
| | FmCF(2) | CF1, CF2 | •6MHz (ceramic resonator oscillation) •Refer to figure 1 | 4.5-6.0 | 5.88 | 6 | 6.12 | | |
| | FmCF(3) | CF1, CF2 | •3MHz (ceramic resonator oscillation) •Refer to figure 1 | 2.5-6.0 | 2.94 | 3 | 3.06 | | |
| | FmRC | | | •Internal RC oscillation Mask option is 'High' | 2.5-4.5 | 1.0 | 1.4 | | 2.0 |
| | | | | | 4.5-6.0 | 0.8 | 1.3 | | 1.8 |
| | FmRC | | | •Internal RC oscillation Mask option is 'Low' | 2.5-4.5 | 0.5 | 0.9 | | 1.2 |
| 4.5-6.0 | | | | | 0.4 | 0.75 | 1.0 | | |
| FsXtal | XT1, XT2 | | •32.768kHz (crystal oscillation) •Refer to figure 2 | 2.5-6.0 | | 32.768 | | kHz | |

Continue.

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|---|----------|----------|---|--------------------|------|------------|----------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Oscillation stabilizing time period (Note 1) | tmsCF(1) | CF1, CF2 | •12MHz (ceramic resonator oscillation) •Refer to figure 3 | 4.5-6.0 | | 0.02 | 0.3 | ms |
| | tmsCF(2) | CF1, CF2 | •6MHz (ceramic resonator oscillation) •Refer to figure 3 | 4.5-6.0 | | 0.02 | 0.3 | |
| | tmsCF(3) | CF1, CF2 | •3MHz (ceramic resonator oscillation) •Refer to figure 3 | 4.5-6.0 2.5-6.0 | | 0.1 0.1 | 1 3 | |
| | tssXtal | XT1, XT2 | •32.768kHz (crystal oscillation) •Refer to figure 3 | 4.5-6.0 2.5-6.0 | | 1 1 | 1.5 3 | s |

(Note 1) The oscillation constant is shown on table 1 and table 2.

DISCONTINUED PRODUCT

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|--------------------------|--------|---|---|---------|---------|--------|------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Input high current | IIH(1) | •Ports 1,2,3,4,5 •Port 0 without pull-up MOS Tr. | •Output disable •Pull-up MOS Tr. OFF •VIN=VDD (including the off-leak current of the output Tr.) | 2.5-6.0 | | | 1 | μA |
| | IIH(2) | Port 7 without pull-up MOS Tr. | •Output Nch Tr. OFF •VIN=VDD (including the off-leak current of the output Tr.) | 2.5-6.0 | | | 1 | |
| | IIH(3) | $\overline{\text{RES}}$ | VIN=VDD | 2.5-6.0 | | | 1 | |
| Input low current | IIL(1) | •Ports 1,2,3,4,5 •Port 0 without pull-up MOS Tr. | •Output disable •Pull-up MOS Tr. OFF •VIN=VSS (including the off-leak current of the output Tr.) | 2.5-6.0 | -1 | | | |
| | IIL(2) | Port 7 without pull-up MOS Tr. | •Output Nch Tr. OFF •VIN=VSS (including the off-leak current of the output Tr.) | 2.5-6.0 | -1 | | | |
| | IIL(3) | $\overline{\text{RES}}$ | VIN=VSS | 2.5-6.0 | -1 | | | |
| Output high voltage | VOH(1) | Port 0 of | IOH=-10mA | 4.5-6.0 | VDD-1.5 | | | V |
| | VOH(2) | CMOS output | IOH=-1mA | 2.5-6.0 | VDD-0.4 | | | |
| | VOH(3) | •Ports 1,2,3,4,5 of | IOH=-1.0mA | 4.5-6.0 | VDD-1 | | | |
| | VOH(4) | CMOS output •ADLC, EROE | IOH=-0.1mA | 2.5-6.0 | VDD-0.5 | | | |
| Output low voltage | VOL(1) | •Ports 0,1,2,3,4,5 | IOL=10mA | 4.5-6.0 | | | 1.5 | |
| | VOL(2) | •ADLC, EROE | IOL=1.6mA | 4.5-6.0 | | | 0.4 | |
| | VOL(3) | | •IOL=1.0mA •The current of any measurement pin is not over 1mA. | 2.5-6.0 | | | 0.4 | |
| | VOL(4) | Port 7 | IOL=1mA | 4.5-6.0 | | | 0.4 | |
| | VOL(5) | | IOL=0.5mA | 2.5-6.0 | | | 0.4 | |
| Pull-up MOS Tr. resistor | Rpu | •Ports 0,1,2,3,4,5 •Port 7 | VOH=0.9VDD | 4.5-6.0 | 15 | 40 | 70 | kΩ |
| | | | | 2.5-4.5 | 25 | 60 | 120 | |
| Hysteresis voltage | VHIS | •Ports 0,1,2,3,4,5 •Port 7 •RES | Output disable | 2.5-6.0 | | 0.1VDD | | V |
| Pin capacitance | CP | All pins | •f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C | 2.5-6.0 | | 10 | | pF |

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | | |
|---------------|--|------------------------|----------------------|--|--|---------|------|--------------|------|
| | | | | VDD[V] | min. | typ. | | max. | |
| Serial clock | Input clock | Cycle | tCKCY(1) | SCK0, SCK1 | Refer to figure 5. | 2.5-6.0 | 2 | | tCYC |
| | | Low Level pulse width | tCKL(1) | | | | 1 | | |
| | | High Level pulse width | tCKH(1) | | | | 1 | | |
| | Output clock | Cycle | tCKCY(2) | SCK0, SCK1 | •Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 5. | 2.5-6.0 | 2 | | |
| | | Low Level pulse width | tCKL(2) | | | | | 1/2 tCKCY | |
| | | High Level pulse width | tCKH(2) | | | | | 1/2 tCKCY | |
| Serial input | Data set up time | tICK | •SI0,SI1 •SB0,SB1 | •Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5. | 4.5-6.0 | 0.1 | | μs | |
| | Data hold time | tCKI | | | 2.5-6.0 | 0.4 | | | |
| | | | | | 4.5-6.0 | 0.1 | | | |
| Serial output | Output delay time (Serial clock is external clock) | tCKO(1) | •SO0,SO1 •SB0,SB1 | •Data set-up to SCK0,1 •Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 5. | 4.5-6.0 | | | 7/12 tCYC | |
| | | | | | 2.5-6.0 | | | +0.2 | |
| | | | | | 2.5-6.0 | | | 7/12 tCYC +1 | |
| | Output delay time (Serial clock is internal clock) | tCKO(2) | •SO0,SO1 •SB0,SB1 | •Data hold from SCK0,1 •Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 5. | 4.5-6.0 | | | 1/3 tCYC | |
| | | | | | 2.5-6.0 | | | +0.2 | |
| | | | | | 2.5-6.0 | | | 1/3 tCYC +1 | |

DISCONTINUED PRODUCT

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit |
|----------------------------|--------------------|--|--|---------|------|------|------|
| | | | | VDD[V] | min. | typ. | |
| High/low level pulse width | tPIH(1) tPIL(1) | •INT0, INT1 •INT2/T0IN •Refer to figure 6 | •Interrupt acceptable •Timer0-countable | 2.5-6.0 | 1 | | tCYC |
| | tPIH(2) tPIL(2) | •INT3/T0IN (The noise rejection clock is selected to 1/1.) •Refer to figure 6 | •Interrupt acceptable •Timer0-countable | 2.5-6.0 | 2 | | |
| | tPIH(3) tPIL(3) | •INT3/T0IN (The noise rejection clock is selected to 1/16.) •Refer to figure 6 | •Interrupt acceptable •Timer0-countable | 2.5-6.0 | 32 | | |
| | tPIH(4) tPIL(4) | •INT3/T0IN (The noise rejection clock is selected to 1/64.) •Refer to figure 6 | •Interrupt acceptable •Timer0-countable | 2.5-6.0 | 128 | | |
| | tPIL(5) | •RES •Refer to figure 6 | Reset acceptable | 2.5-6.0 | 200 | | μs |

DISCONTINUED PRODUCT

6. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | | | | |
|---|-----------|------|---|-----------------------|---------|---------|---------|------|------|-----|-----|
| | | | | OCR7 | VDD[V] | min. | | typ. | max. | | |
| Current dissipation during basic operation (Note 2) | IDDOP(1) | VDD | <ul style="list-style-type: none"> •FmCF=12MHz •Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 12MHz •Internal RC oscillation stops | 0 | 4.5-6.0 | | 10 | 25 | mA | | |
| | IDDOP(2) | | <ul style="list-style-type: none"> •FmCF=6MHz •Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 6MHz •Internal RC oscillation stops | 1 | 4.5-6.0 | | 10 | 25 | | | |
| | IDDOP(3) | | <ul style="list-style-type: none"> •FmCF=3MHz •Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 3MHz •Internal RC oscillation stops | 0 | 4.5-6.0 | | 3 | 9 | | | |
| | IDDOP(4) | | | 1 | | | 6 | 15 | | | |
| | IDDOP(5) | | | 0 | | 2.5-4.5 | | 1.5 | | 5 | |
| | IDDOP(6) | | <ul style="list-style-type: none"> •FmCF=0Hz •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation | Mask option is "High" | 0 | 4.5-6.0 | | 1.2 | | 5.8 | |
| | IDDOP(7) | | | | 1 | | | 2.0 | | 7.8 | |
| | IDDOP(8) | | | Mask option is "Low" | 0 | 2.5-4.5 | | 0.7 | | 4.8 | |
| | IDDOP(9) | | | | 1 | | | 1.4 | | 6.2 | |
| | IDDOP(10) | | | | 0 | | 4.5-6.0 | | | 0.7 | 3.4 |
| | IDDOP(11) | | | 1 | | 1.2 | | 4.5 | | | |
| | IDDOP(12) | | | 0 | 2.5-4.5 | | | 0.4 | | 2.8 | |
| | IDDOP(13) | | 1 | | | 0.8 | 3.6 | | | | |
| | IDDOP(14) | | <ul style="list-style-type: none"> •FmCF=0Hz •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops | 0 | 4.5-6.0 | | 38 | 150 | | μA | |
| | IDDOP(15) | | | 1 | | | 60 | 300 | | | |
| | IDDOP(16) | | | 0 | | 2.5-4.5 | | 15 | | | 70 |
| | IDDOP(17) | | | 1 | | | | 25 | | | 120 |

*OSCR : Bit 7 of the oscillation control register.

Continue.

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | | | |
|---|-------------|------|--|---------|---------|------|------|------|------|----|
| | | | | OCR7 | VDD[V] | min. | | typ. | max. | |
| Current dissipation in HALT mode (Note 2) | IDDHALT(1) | VDD | <ul style="list-style-type: none"> •HALT mode •FmCF=12MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 12MHz •Internal RC oscillation stops | 0 | 4.5-6.0 | | 5.0 | 14 | mA | |
| | IDDHALT(2) | | <ul style="list-style-type: none"> •HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 6MHz •Internal RC oscillation stops | 1 | 4.5-6.0 | | 5.0 | 14 | | |
| | IDDHALT(3) | | <ul style="list-style-type: none"> •HALT mode | 0 | 4.5-6.0 | | 2.3 | 7 | | |
| | IDDHALT(4) | | <ul style="list-style-type: none"> •FmCF=3MHz | 1 | | | 4.5 | 15 | | |
| | IDDHALT(5) | | <ul style="list-style-type: none"> Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 3MHz •Internal RC oscillation stops | 0 | 2.5-4.5 | | 0.8 | 4 | | |
| | IDDHALT(6) | | <ul style="list-style-type: none"> •HALT mode | 0 | 4.5-6.0 | | 650 | 2700 | | |
| | IDDHALT(7) | | <ul style="list-style-type: none"> •FmCF=0Hz | 1 | | | 1000 | 4200 | | |
| | IDDHALT(8) | | <ul style="list-style-type: none"> (when oscillation stops) | 0 | 2.5-4.5 | | 340 | 2200 | | |
| | IDDHALT(9) | | | 1 | | | 600 | 2500 | | |
| | IDDHALT(10) | | <ul style="list-style-type: none"> •FsXtal=32.768kHz crystal oscillation | 0 | 4.5-6.0 | | 400 | 1600 | | |
| | IDDHALT(11) | | <ul style="list-style-type: none"> •System clock : | 1 | | | 600 | 2400 | | |
| | IDDHALT(12) | | <ul style="list-style-type: none"> RC oscillation | 0 | 2.5-4.5 | | 200 | 1300 | | |
| | IDDHALT(13) | | | 1 | | | 350 | 1500 | | |
| | IDDHALT(14) | | <ul style="list-style-type: none"> •HALT mode | 0 | 4.5-6.0 | | 25 | 100 | | μA |
| | IDDHALT(15) | | <ul style="list-style-type: none"> •FmCF=0Hz | 1 | | | 36 | 140 | | |
| | IDDHALT(16) | | <ul style="list-style-type: none"> (when oscillation stops) | 0 | 2.5-4.5 | | 8 | 55 | | |
| | IDDHALT(17) | | <ul style="list-style-type: none"> •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops | 1 | | | 12 | 85 | | |
| Current dissipation in HOLD mode (Note 2) | IDDHOLD(1) | VDD | HOLD mode | | 4.5-6.0 | | 0.05 | 30 | | |
| | IDDHOLD(2) | | | | 2.5-4.5 | | 0.02 | 20 | | |

(Note 2) The currents of the output transistors, pull-up transistors and the LCD bleeder resistors are ignored. Refer to figure 7.

7. LCD Voltage and LCD Driver Characteristics at Ta=-30°C to +70°C, VSS=0V

| Parameter | Symbol | Pins, Conditions | Ratings | | | | unit | |
|--|--------|---|-----------|----------|---------|---------|------|----|
| | | | VDD[V] | min. | typ. | max. | | |
| VDD-Ci drop voltage (i : 1 to 16) | VD1 | •Only a Ci terminal for -15μA •LCD display ON | 2.9 | | | 120 | mV | |
| | | | 5.0 | | | 200 | | |
| VX-Ci drop voltage (X : 1 to 4) (i : 1 to 16) | VD2 | •1/5 bias •V5=0V | 2.9 | | | 120 | | |
| | | | 5.0 | | | 200 | | |
| VX-Ci drop voltage (X : 1 to 5) (i : 1 to 16) | VD3 | •Only a Ci terminal for +15μA •LCD display ON •1/5 bias •V5=0V | 2.9 | -120 | | | | |
| | | | 5.0 | -200 | | | | |
| VDD-Si drop voltage (i : 1 to 48) | VD4 | •Only a Si terminal for -15μA •LCD display ON | 2.9 | | | 120 | | |
| | | | 5.0 | | | 200 | | |
| VX-Si drop voltage (X : 1 to 4) (i : 1 to 48) | VD5 | •1/5 bias •V5=0V | 2.9 | | | 120 | | |
| | | | 5.0 | | | 200 | | |
| VX-Si drop voltage (i : 1 to 5) (i : 1 to 48) | VD6 | •Only a Ci terminal for +15μA •LCD display ON •1/5 bias •V5=0V | 2.9 | -120 | | | | |
| | | | 5.0 | -200 | | | | |
| V1 output voltage | VV1 | •LCD clock frequency=0Hz •LCD display ON | 2.9 | 0.75VDD | 0.80VDD | 0.85VDD | V | |
| | | | 5.0 | | | | | |
| V2 output voltage | VV2 | •1/5 bias •V5=0V | 2.9 | 0.55VDD | 0.60VDD | 0.65VDD | | |
| | | | 5.0 | | | | | |
| V3 output voltage | VV3 | •Refer to figure 9 | 2.9 | 0.35VDD | 0.40VDD | 0.45VDD | | |
| | | | 5.0 | | | | | |
| V4 output voltage | VV4 | | 2.9 | 0.15VDD | 0.20VDD | 0.25VDD | | |
| | | | 5.0 | | | | | |
| LCD display current | LCD1 | •LCD display ON •1/5 bias | 20kΩ mode | 5 | 25 | 50 | 100 | μA |
| | | | 4kΩ mode | 2.9 | 15 | 29 | 60 | |
| | LCD2 | •VLCD=0V •V1-V5 are opened •Refer to figure 8 | 4kΩ mode | 5 | 125 | 250 | 500 | |
| | | | | 2.9 | 75 | 150 | 300 | |
| Step up voltage | VOUT2 | •V1-V5 resistor=20kΩ •LCD display ON •LVCR0=1 (doubler) •VOUT2 •C5=C6=0.1μF •Internal RC oscillation start •Refer to figure 10 | IL=100μA | 2.7 | -2.7 | -1.9 | -1.7 | V |
| | | | | 3 | -3 | -2.8 | -2.6 | |
| | | | 5 | -5 | -4.8 | -4.5 | | |
| | | | IL=500μA | 2.7 | -2.7 | -1.8 | -1.5 | |
| | 3 | -3 | -2.6 | -2.2 | | | | |
| | 5 | -5 | -4.6 | 4.2 | | | | |
| | VOUT3 | •V1-V5 resistor=20kΩ •LCD display ON •LVCR0=0 (trippler) •VOUT3 •C5=C6=0.1μF •Internal RC oscillation start •Refer to figure 11 | IL=100μA | 5 | -10 | -9.4 | -9.0 | |
| | | | | IL=500μA | 5 | -10 | -8.5 | |
| Contrast current (VLCD terminal) | LC1 | •LCD display ON | VCCR=1 | 5 | 5 | 10 | 20 | mA |
| | | | VCCR=2 | 5 | 2.5 | 5 | 10 | |
| | LC3 | •VLCD=-3V | VCCR=4 | 5 | 1.25 | 2.5 | 5 | μA |
| | | | VCCR=8 | 5 | 0.6 | 1.25 | 2.5 | |
| | LC5 | •Refer to figure 12 | VCCR=10H | 5 | 0.3 | 0.6 | 1.25 | |

VCCR : The LCD contrast control register

LVCR0 : Bit 0 of the LCD bias control register

Table 1. Ceramic resonator oscillation recommended constant (main clock)

| Oscillation type | Maker | Oscillator | C1 | C2 |
|-------------------------------------|---------|-------------|---------|------|
| 12MHz ceramic resonator oscillation | Murata | CSA12.0MT | 33pF | 33pF |
| | | CST12.00MTW | on chip | |
| 6MHz ceramic resonator oscillation | Kyocera | KBR-12.0M | 33pF | 33pF |
| | Murata | CSA6.00MG | 33pF | 33pF |
| | | CST6.00MGW | on chip | |
| | Kyocera | KBR-6.0MSA | 33pF | 33pF |
| KBR-6.0MKS | | on chip | | |
| 3MHz ceramic resonator oscillation | Murata | CSA3.0MG | 33pF | 33pF |
| | | CST3.0MGW | on chip | |
| | Kyocera | KBR-3.0MS | 47pF | 47pF |

* Both C1 and C2 must use K rank ($\pm 10\%$) and SL characteristics.

Table 2. Crystal oscillation recommended constant (sub clock)

| Oscillation type | Maker | Oscillator | C3 | C4 |
|-------------------------------|---------|------------|------|------|
| 32.768kHz crystal oscillation | CITIZEN | CFS-308 | 18pF | 18pF |
| | SII | DT-VT-200 | 18pF | 18pF |

* Both C3 and C4 must use J rank ($\pm 5\%$) and CH characteristics.

(It is about the application which is not in need of high precision. Use K rank ($\pm 10\%$) and SL characteristics.)

- (Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
 - For other oscillators, please request an evaluation of microcomputer and oscillator matching to the oscillator manufacturer.

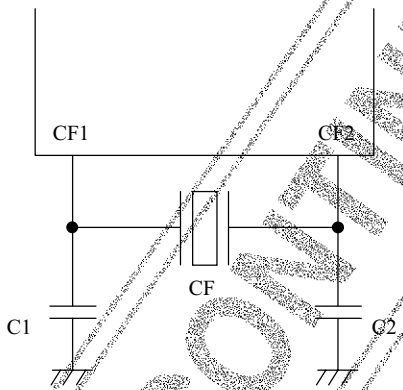


Figure 1 Ceramic oscillation circuit

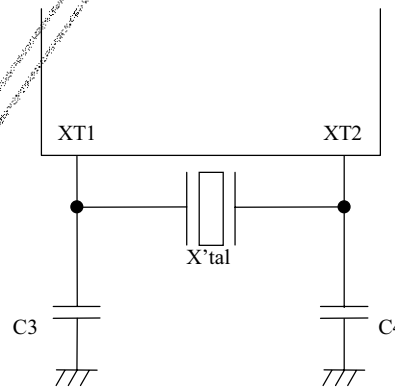


Figure 2 Crystal oscillation circuit

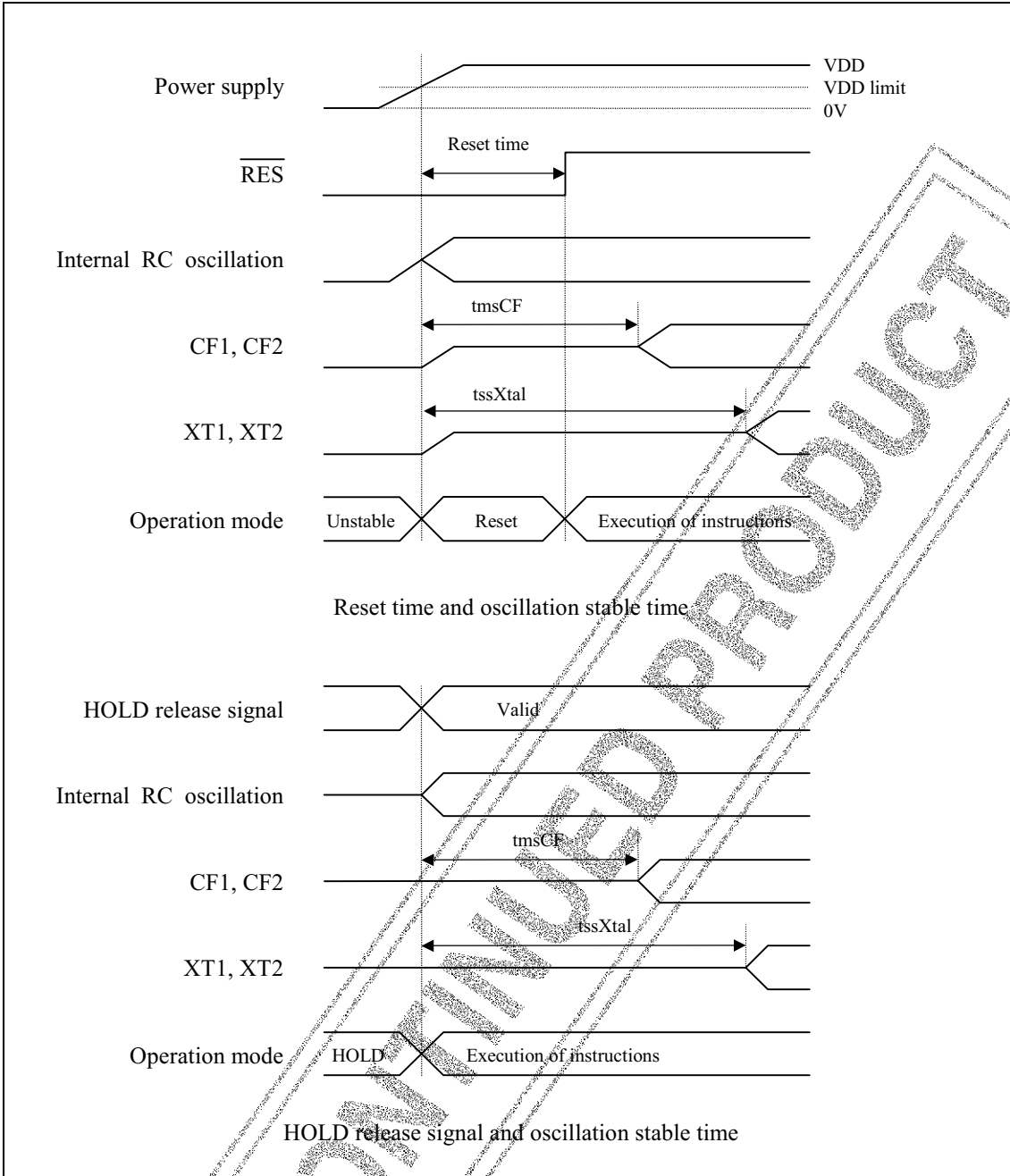
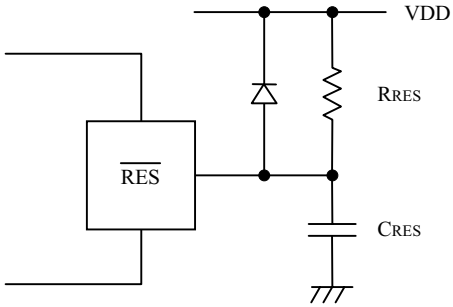


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200 μ s, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

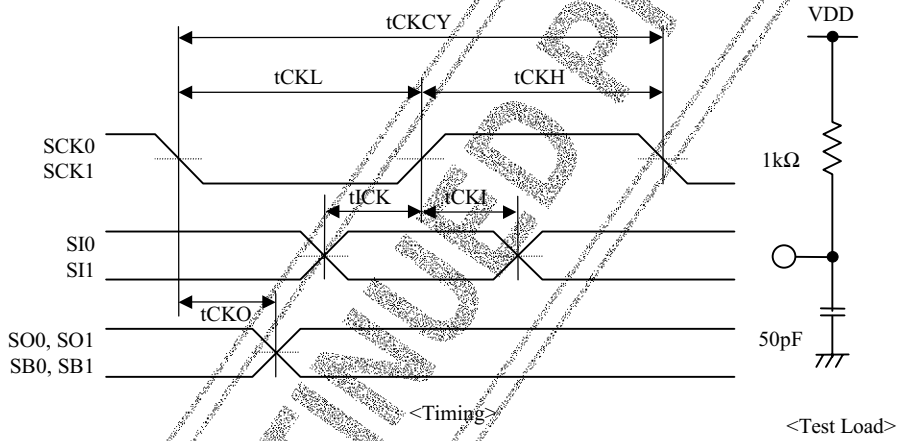


Figure 5 Serial input / output test condition

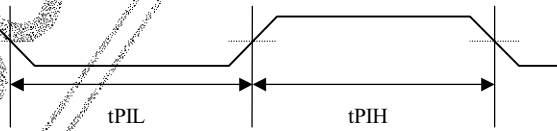


Figure 6 Pulse input timing condition

DISCONTINUED PRODUCT

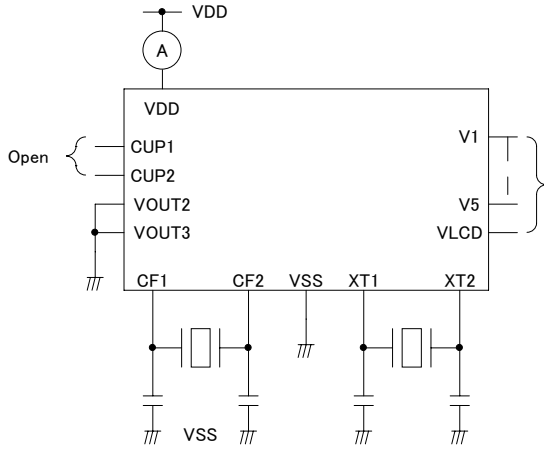


Figure 7 Current dissipation measurement

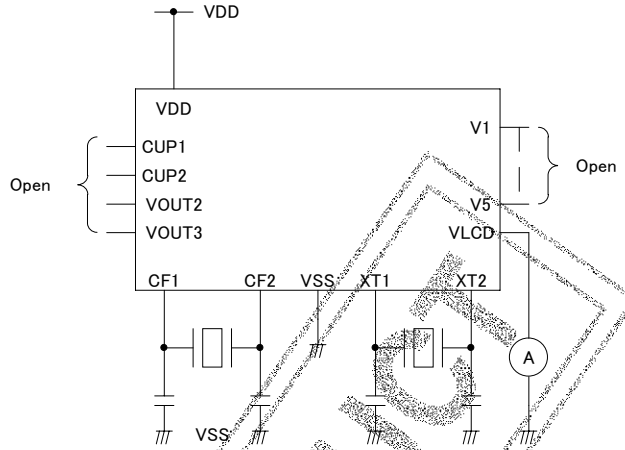


Figure 8 LCD display current measurement

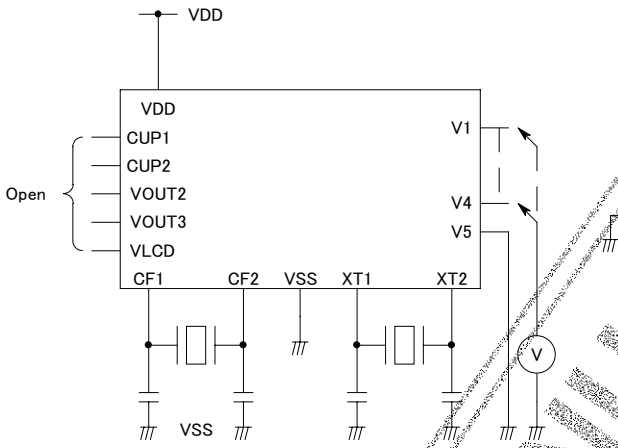


Figure 9 Output voltage of V1-V4 measurement

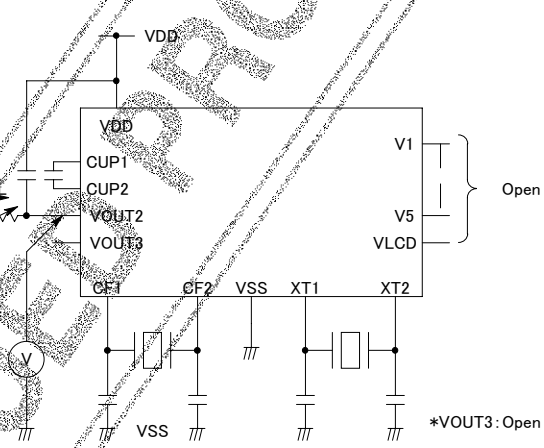


Figure 10 Step up output voltage measurement (1)

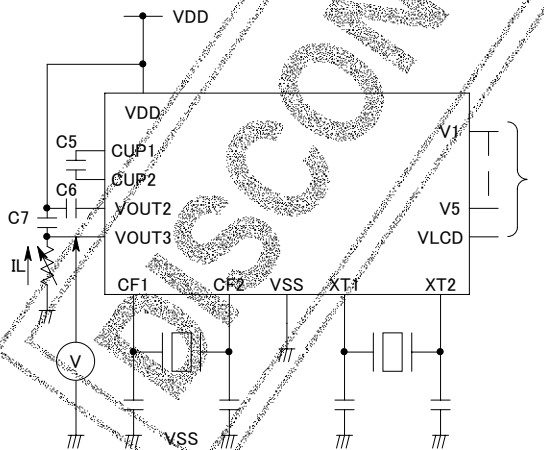


Figure 11 Step up output voltage measurement (2)

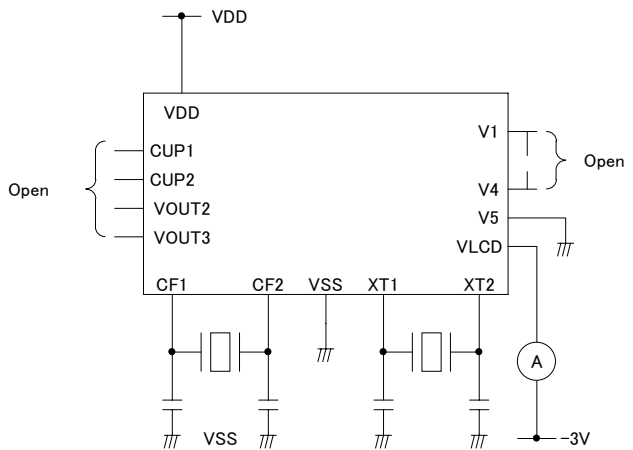


Figure 8 Contrast current measurement

8. AC Characteristics at Ta=-30°C to +70°C, VSS=0V

Load capacity : 100pF (Port 0, ADLC, $\overline{\text{EROE}}$)
 Load capacity : 80pF (Output terminals except above)
 *tCLCL=1/12 tCYC

External program memory timing

| Parameter | Symbol | Pads and Conditions | Ratings | | unit |
|---------------------------------------|--------|-------------------------------|-----------|-------------|------|
| | | | VDD[V] | min. / max. | |
| ADLC pulse width | tLHLL | | 4.5 - 6.0 | 2tCLCL-40 | ns |
| | | | 2.5 - 6.0 | 2tCLCL-160 | |
| Address settling time | tAVLL | For ADLC | 4.5 - 6.0 | tCLCL-40 | |
| | | | 2.5 - 6.0 | tCLCL-160 | |
| Address hold time | tLLAX | For ADLC | 4.5 - 6.0 | tCLCL-35 | |
| | | | 2.5 - 6.0 | tCLCL-140 | |
| ADLC → control signal | tLLEL | For $\overline{\text{EROE}}$ | 4.5 - 6.0 | tCLCL-25 | |
| | | | 2.5 - 6.0 | tCLCL-100 | |
| $\overline{\text{EROE}}$ pulse width | tELEH | | 4.5 - 6.0 | 3tCLCL-35 | |
| | | | 2.5 - 6.0 | 3tCLCL-140 | |
| Data delay time | tELIV | From $\overline{\text{EROE}}$ | 4.5 - 6.0 | 3tCLCL-125 | |
| | | | 2.5 - 6.0 | 3tCLCL-400 | |
| Data hold time | tEHIX | For $\overline{\text{EROE}}$ | 4.5 - 6.0 | 0 | |
| | | | 2.5 - 6.0 | 0 | |
| $\overline{\text{EROE}}$ → address in | tEHAV | | 4.5 - 6.0 | tCLCL-8 | |
| | | | 2.5 - 6.0 | tCLCL-32 | |

Refer to figure 13.

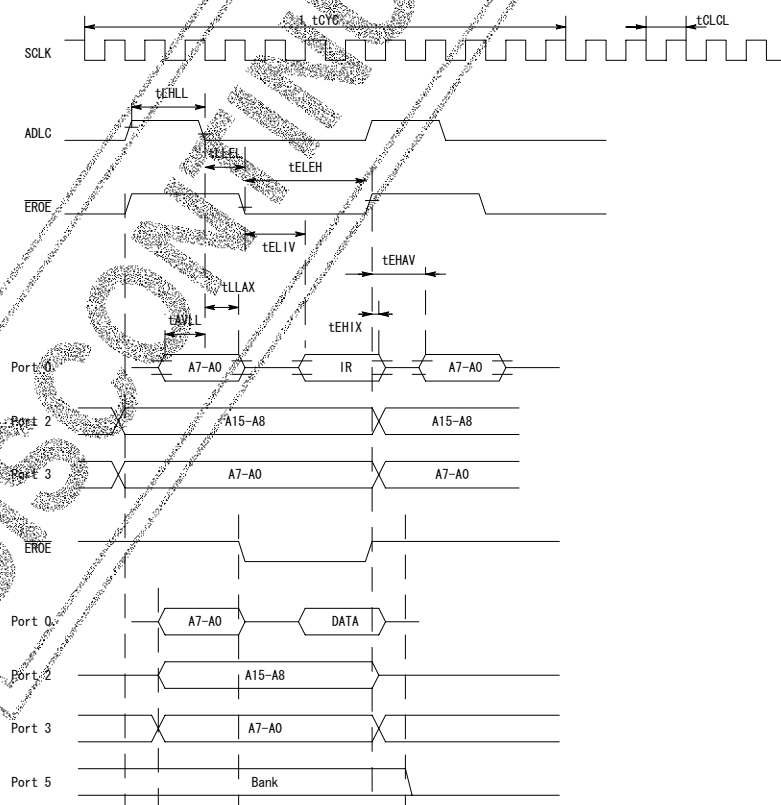


Figure 13 Timing of the external Program Memory/Data Memory

External data memory timing

| Parameter | Symbol | Pads and Conditions | Ratings | | unit |
|---------------------------|--------|---------------------|-----------|-------------|-----------|
| | | | VDD[V] | min. / max. | |
| RD pulse width | tRLRH | | 4.5 - 6.0 | 6tCLCL-80 | ns |
| | | | 2.5 - 6.0 | 6tCLCL-320 | |
| WR pulse width | tWLWH | | 4.5 - 6.0 | 6tCLCL-80 | |
| | | | 2.5 - 6.0 | 6tCLCL-320 | |
| Data address hold time | tLLAX | For ADLC (at LDX) | 4.5 - 6.0 | 2tCLCL-35 | |
| | | | 2.5 - 6.0 | 2tCLCL-140 | |
| | | For ADLC (at STX) | 4.5 - 6.0 | 2tCLCL-35 | |
| | | | 2.5 - 6.0 | 2tCLCL-140 | |
| Data delay time | tRLDV | From RD | 4.5 - 6.0 | 5tCLCL-125 | |
| | | | 2.5 - 6.0 | 5tCLCL-400 | |
| Data hold time | tRHDX | From RD | 4.5 - 6.0 | 0 | |
| | | | 2.5 - 6.0 | 0 | |
| Data floating time | tRHDZ | From RD | 4.5 - 6.0 | 2tCLCL-70 | 2tCLCL+70 |
| | | | 2.5 - 6.0 | 2tCLCL-280 | |
| Data address setting time | tAVLL | For ADLC | 4.5 - 6.0 | tCLCL-40 | |
| | | | 2.5 - 6.0 | tCLCL-160 | |
| ADLC → control signal | tLLRL | For RD | 4.5 - 6.0 | 3tCLCL-50 | 3tCLCL+50 |
| | | | 2.5 - 6.0 | 3tCLCL-200 | |
| | tLLWL | For WR | 4.5 - 6.0 | 3tCLCL-50 | 3tCLCL+50 |
| | | | 2.5 - 6.0 | 3tCLCL-200 | |
| Data settling time | tQVWL | For WR | 4.5 - 6.0 | tCLCL-60 | |
| | | | 2.5 - 6.0 | tCLCL-240 | |
| Data in WR=1 | tQVWH | | 4.5 - 6.0 | 7tCLCL-140 | |
| | | | 2.5 - 6.0 | 7tCLCL-560 | |
| Data hold time | tWHQX | From WR | 4.5 - 6.0 | tCLCL-50 | |
| | | | 2.5 - 6.0 | tCLCL-200 | |
| Control signal → ADLC | tRHLH | For RD | 4.5 - 6.0 | tCLCL-50 | tCLCL+50 |
| | | | 2.5 - 6.0 | tCLCL-200 | |
| | tWHLH | For WR | 4.5 - 6.0 | tCLCL-50 | tCLCL+50 |
| | | | 2.5 - 6.0 | tCLCL-200 | |

Refer to figure 14.

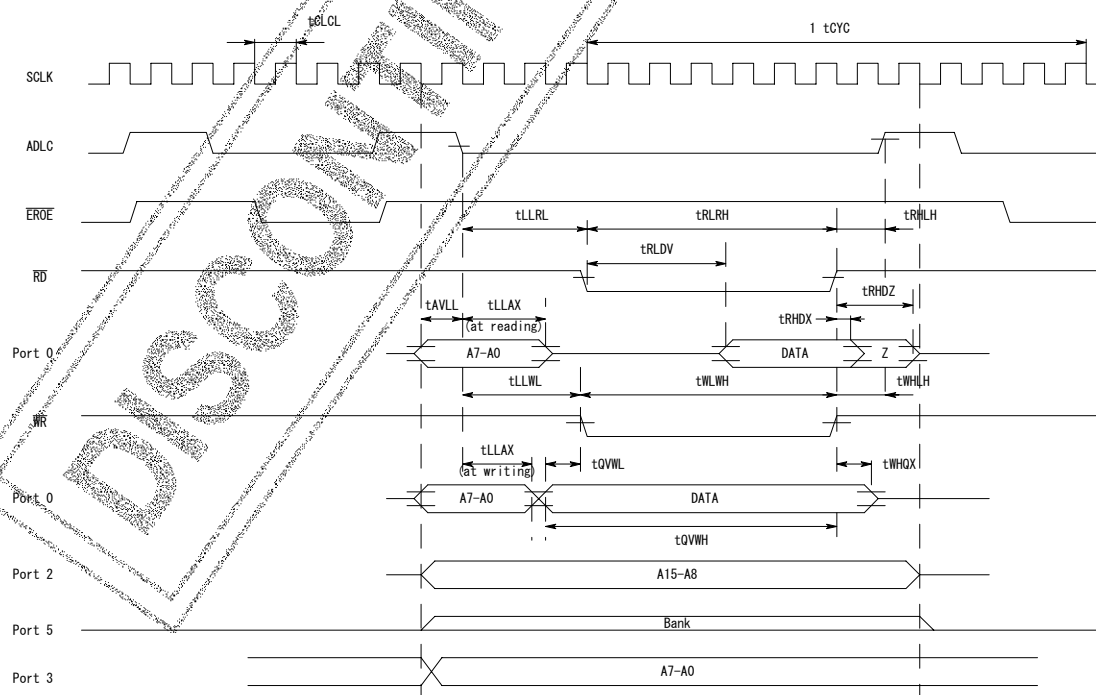


Figure 14 Timing of the external RAM

• Evaluation Sample (ES)

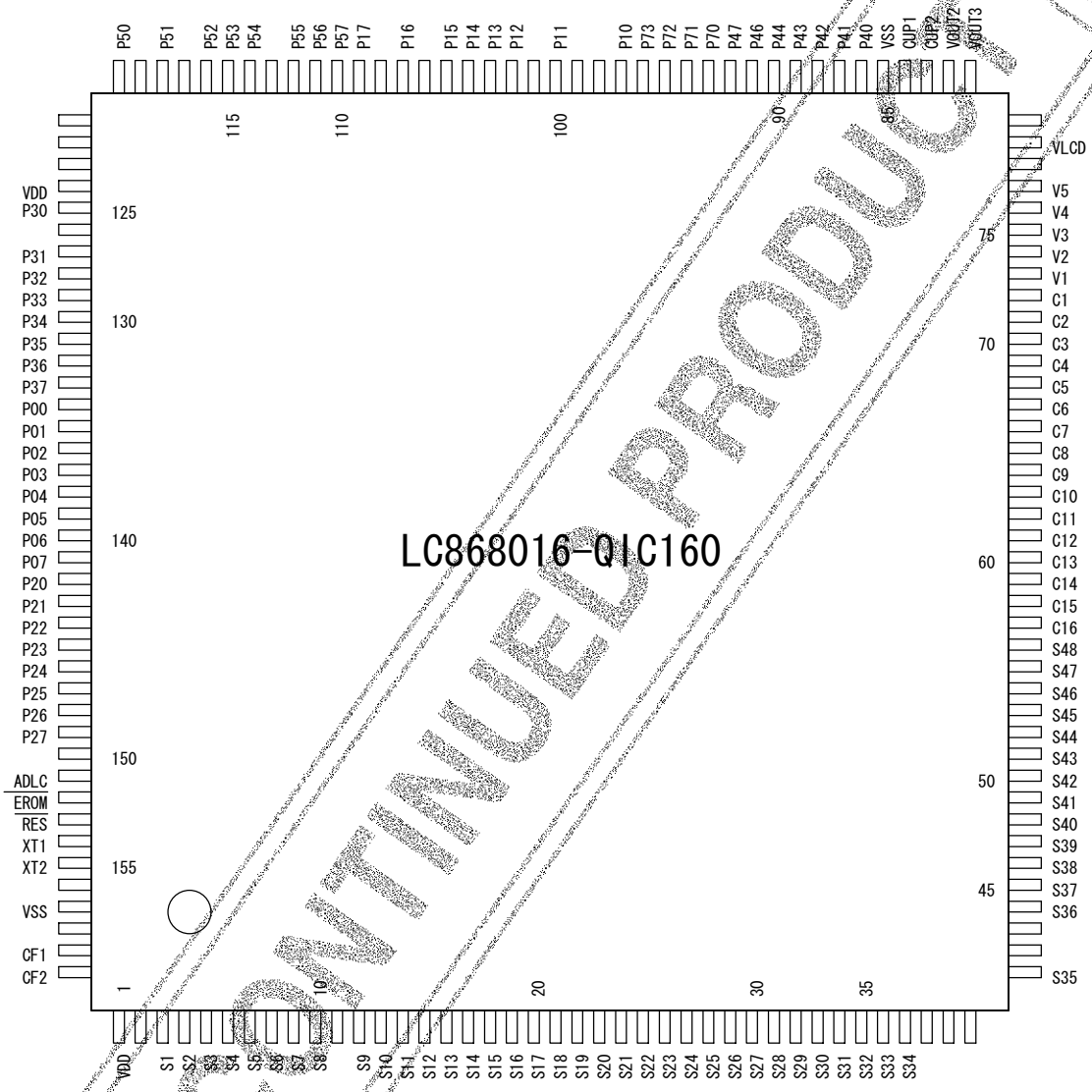
The factory shipment of this microcomputer is chip.

But there are two types of shipment of evaluation sample.

One type is chip and the other is package (QIC160).

If you selected package type, please refer to the following pin assignment and layout, and make the user target board.

• Pin Assignment of evaluation sample (Package type)



- Layout of evaluation sample (Package type) : QIC160

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