SiS550Family Detail Feature List

Integrated x86 Compatible CPU

x86 Instruction Set Compatible Processor

High Performance with Advanced Architectures

Superscalar Execution

Three Superpipelined Integer Units

Pipelined Floating Point Unit

Innovative Instruction Decode and Branch Prediction

Separate Code and Data Caches

Support for Bus Frequency up to 100MHz

Low Power Consumption Design

Software Compatibility with Microsoft Windows, Windows CE, MS-DOS, QNX and
    LINUX

Supports Host Bus Direct Access GUI Engine for Integrated A.G.P. VGA Controller

Integrated DRAM Controller

Supports up to 2 Double Sided DIMMs (4 Rows Memory)

Supports PC100/PC133 SDRAM Technology

Supports NEC Virtual Channel Memory (VC-SDRAM) Technology

System Memory Size up to 1 GB

Supports 16Mb, 64Mb, 128Mb, 256Mb, 512Mb SDRAM Technology

Supports Suspend-To-RAM (STR)

Relocatable System Management Memory Region

Programmable Buffer Strength for CS#, DQM[7:0], WE#, RAS#, CAS#, CKE,
    MA[14:0] and MD[63:0]

Shadow RAM Size from 640KB to 1MB In 16KB Increments

Two Programmable PCI Hole Areas

Integrated A.G.P. Compliant Target Host-To-PCI Bridge

AGP V2.0 Compliant

Supports Graphic Window Size from 4Mbytes To 256Mbytes

Supports Pipelined Process in CPU-To-Integrated A.G.P. VGA Access

Supports 8 Way, 16 Entries Page Table Cache for GART to Enhance Integrated

A.G.P. VGA Controller Read/Write Performance

Supports PCI-To-PCI Bridge Function for Memory Write from 33Mhz PCI Bus to
    Integrated A.G.P. VGA

Meets PC99a Requirements

PCI 2.2 Specification Compliant

High Performance PCI Arbiter

Supports up to 3 external PCI Masters

Rotating Priority Arbitration Scheme

Advanced Arbitration Scheme Minimizing Arbitration Overhead

Guaranteed Minimum Access Time for CPU And PCI Masters

Integrated Host-To-PCI Bridge

Zero Wait State Burst Cycles

CPU-To-PCI Pipeline Access

256B to 4KB PCI Burst Length for PCI Masters

PCI Master Initiated Graphical Texture Write Cycles Re-Mapping

Reassembles PCI Burst Data Size into Optimized Block Size

Fast PCI IDE Master/Slave Controller

Supports PCI Bus Mastering

Supports Native Mode and Compatibility Mode

Supports PIO Mode 0, 1, 2, 3, 4

Supports Multiword DMA Mode 0, 1, 2

Supports Ultra DMA 33/66/100

Virtual PCI-To-PCI Bridge

Integrated Ultra-AGPᴛᴍ VGA for Hardware 2D/Video/Graphics Accelerators

Supports Tightly Coupled 64 Bits 100Mhz Host Interface to VGA to Speed Up GUI

Performance and the Video Playback Frame Rate

AGP Rev. 2.0 Compliant

Zero-Wait-State Post-Write Buffer with Write Combine Capability

Zero-Wait-State Read Ahead Cache Capability

Re-Locatable Memory-Mapped and I/O Address Decoding

Flexible Design Shared Frame Buffer Architecture for Display Memory

Shared System Memory Area up to 128 MB

128-Bit 2D Engine with a Full Instruction Set

Built-In 64x64x2 Bit-Mapped Hardware Cursor

Built-In 32x32x16, 32x32x32 Bit-Mapped Hardware Color Cursor and Alpha Cursor

MPEG-2 ISO/IEC 13818-2 MP@ML and MPEG-1 ISO/IEC 11172-2 Standards
  Compliant

Supports Advanced H/W DVD Accelerator

Built-in Video Processor to Support De-interlace Function and High Quality Multi-tap
  Video Scaling

Direct DVD to TV Playback

Supports Two Independent Video Windows with Overlay Function and Scaling
  Factors

Supports YUV-To-RGB Color Space Conversion

Supports Bi-Linear Video Interpolation with Integer Increments of Pixel Accuracy

Supports Graphic and Video Overlay Function

Supports VCD/DVD to TV Playback Mode

Simultaneous Graphic and TV Video Playback Overlay

Supports Current Scan Line Of Refresh Red-Back and Interrupt

Supports Tearing Free Double/Triple Buffer Flipping

Supports Input Video Vertical Blank or Line Interrupt

Supports RGB555, RGB565, YUV422 and YUV420 Video Playback Format

Supports Filtered Horizontal up and down Scaling Playback

Supports DVD Sub-Picture Playback Overlay

Supports DVD Playback Auto-Flipping

Built-In Two Video Playback Line Buffers

Supports DCI Drivers

Supports Direct Draw Drivers

Built-In Programmable 24-Bit True-Color RAMDAC up to 300 MHz Pixel Clock
  RAMDAC

with Snoop Function

Built-In Reference Voltage Generator and Monitor Sense Circuit

Supports Down-Loadable RAMDAC for Gamma Correction In High Color and True
  Color Modes

Built-In Dual-Clock Generator

Supports Multiple Adapters and Multiple Monitors

Built-In Digital Interface for Digital TV-Out Encoder, PanellinkTM (TMDS), LVDS and
  DSTN

Supports Digital Flat Panel Port for Digital Monitor (LCD Panel)

Built-In Secondary CRT Controller for Independent Secondary CRT, LCD or TV
  Digital Output

Supports VESA Standard Super High Resolution Graphic Modes

640x480 16/256/32K/64K/16M Colors 160 Hz NI

800x600 16/256/32K/64K/16M Colors 120 Hz NI

1024x768 256/32K/64K/16M Colors 120 Hz NI

1280x1024 256/32K/64K/16M Colors 85 Hz NI

1600x1200 256/32K/64K/16M Colors 85 Hz NI

1920x1440 256/32K/64K Colors 60 Hz NI

1920x1440 256 Colors 75 Hz NI

Low Resolution Modes

Supports Virtual Screen up to 4096x4096

Fully DirectX 8.0 Compliant

Efficient and Flexible Power Management with ACPI Compliance

Supports DDC1, DDC2B and DDC 3.0 Specifications

Cooperate with "SiS301 Video Bridge" to Support

   NTSC/PAL Video Output

   Digital LCD Monitor

   Secondary CRT Monitor

Low Pin Count Interface

Forwards PCI I/O and Memory Cycles into LPC Bus

Translates 8-/16-Bit DMA Cycles into PCI Bus Cycles

Advanced PCI H/W Audio & S/W Modem

Hardware DirectSound™ accelerator

   64-Channel DirectSound™ acceleration with High Quality sampling rate converter.

   64-Voice DirectSound™ 3D Channels.

   16 On-Chip High-Precision re-routable Sub-Mixers.

   Full-duplex supports of Stereo/Mono, 8-/16-bits, and Signed/Unsigned Samples.

   Per Channel Control of Volume and Pan.

Advanced DLS-2 compliant Wavetable Synthesizer

   64-Voices Polyphony Wavetable Synthesizer fully compliant with DLS-2.

   Per Channel control of Volume, Envelope, Pitch, Pan, Tremolo, and Vibrato etc.

   Per Channel Resonance and Cut-Off Frequency control of Low-Pass Filter.

Fully Compliant with AC97 V2.1

   Support for up to 3 AC97 CODEC's.

   Support for AC3 2-4-6-channels Output over AC-link.

   Support for DRC and VRC over AC-link.

   Support ever slot defined in AC97 V2.1.

   Power Management Control of AC97 Codec.

Telephony & Modem

   Full-Duplex Support for Line1 and Line2 over AC-link.

   Full-Duplex Support for Handset over AC-link.

Consumer Digital Audio Interface

   Support PCM/AC-3 digital audio output.

   Support AC97 CODEC̓s digital audio output.

Advanced Power Management

Meets ACPI 1.0 Requirements

Meets APM 1.2 Requirements

ACPI Sleep States Include S1, S2, S3, S4, S5

CPU Power States Include C0, C1, C2, C3

Power Button with Override

RTC Day-Of -Month, Mont h-Of -Year Alarm

24-Bit Power Management Timer

LED Blinking In S0, S1, S2 and S3 States

System Power-Up Events Include: Power Button, Hot-Key, Keyboard Password/ Hot-Key,
   RTC Alarm, Modem Ring-In, SMBALT#, LAN, PME#, AC̓97 Wake-Up and USB
   Wake-Up

Software Watchdog Timer

PCI Bus Power Management Interface Spec. 1.0

Integrated DMA Controller

Two 8237A Compatible DMA Controllers

8/16- Bit DMA Data Transfer

Distributed DMA Support

Integrated Interrupt Controller

Two 8259A Compatible Interrupt Controllers

Level- Or Edge-Triggered Programmable Serial IRQ

Interrupt Sources Re-Routable to Any IRQ Channel

Three 8254 Compatible Programmable 16-Bit Counters

System Timer Interrupt

Generate Refresh Request

Speaker Tone Output

Integrated Keyboard Controller

Hardwired Logic Provides Instant Response

Supports PS/2 Mouse Interface

Password Security and Password Power-Up

System Sleep and Power-Up By Hot-Key

KBC and PS/2 Mouse Can Be Individually Disabled

Integrated Real Time Clock (RTC) with 256B CMOS SRAM

Supports ACPI Day-Of-Month and Month-Of-Year Alarm

256 Bytes Of CMOS SRAM

Provides RTC H/W Year 2000 Solution

Integrated Universal Serial Bus Host Controller

OpenHCI Host Controller with Root Hub

Three USB Ports

Supports Legacy Devices

Over Current Detection

Integrated Parallel Port Controller

Supports Parallel Port SPP mode

Integrated CIR Controller

Supports programmable Amplitude Shift Keyed (ASK) serial communication protocol

Supports various popular protocols including RC-5, NEC and RECS-80

Supports 7 kinds of decoders

   Forward-Coded Decoder

   Space-Coded Decoder

   Pulse-Coded Decoder

   Silitek-Coded Decoder

   Chicony1/2-Coded Decoder

   BTC-Coded Decoder

   Software Decoder

Supports Sample rates up to 3MHz

Supports Hardware power on/off key decode ability

Supports interrupt and software reset

32-bytes FIFO length for data reception and supports FIFO clear

Integrated Smart Card Controller

Compliant with Personal Computer Smart Card (PC/SC) Working Group standard

\# Compliant with smart card (ISO 7816) protocols

\# Supports card present detect

\# Supports smart card insertion power on feature

Integrated Memory Stick Controller

\# Compliant with SONY memory stick protocol 1.2

\# Supports memory stick present detect

\# Supports power switch for memory stick

NAND Tree for Ball Connectivity Testing

672-Balls BGA Package

1.9V Core with Mixed 3.3V and 5V I/O CMOS Technology