

SIEMENS

Microcomputer Components

16-Bit CMOS Single-Chip Microcontroller

SAB 80C166/83C166

C16x-Family of High-Performance CMOS 16-Bit Microcontrollers

SAB 80C166/83C166

Preliminary

SAB 80C166/83C166 16-Bit Microcontroller

- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU Clock
- 500 ns Multiplication (16 × 16 bit), 1 μs Division (32 / 16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Up to 256 KBytes Linear Address Space for Code and Data
- 1 KByte On-Chip RAM
- 32 KBytes On-Chip ROM (SAB 83C166 only)
- Programmable External Bus Characteristics for Different Address Ranges
- 8-Bit or 16-Bit External Data Bus
- Multiplexed or Demultiplexed External Address/Data Buses
- Hold and Hold-Acknowledge Bus Arbitration Support
- 512 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System
- 10-Channel 10-bit A/D Converter with 9.7 μs Conversion Time
- 16-Channel Capture/Compare Unit
- Two Multi-Functional General Purpose Timer Units with 5 Timers
- Two Serial Channels (USARTs)
- Programmable Watchdog Timer
- Up to 76 General Purpose I/O Lines
- Supported by a Wealth of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 100-Pin Plastic MQFP Package (EIAJ)

Introduction

The SAB 80C166 is the first representative of the Siemens SAB 80C166 family of full featured single-chip CMOS microcontrollers. It combines high CPU performance (up to 10 million instructions per second) with high peripheral functionality and enhanced IO-capabilities.

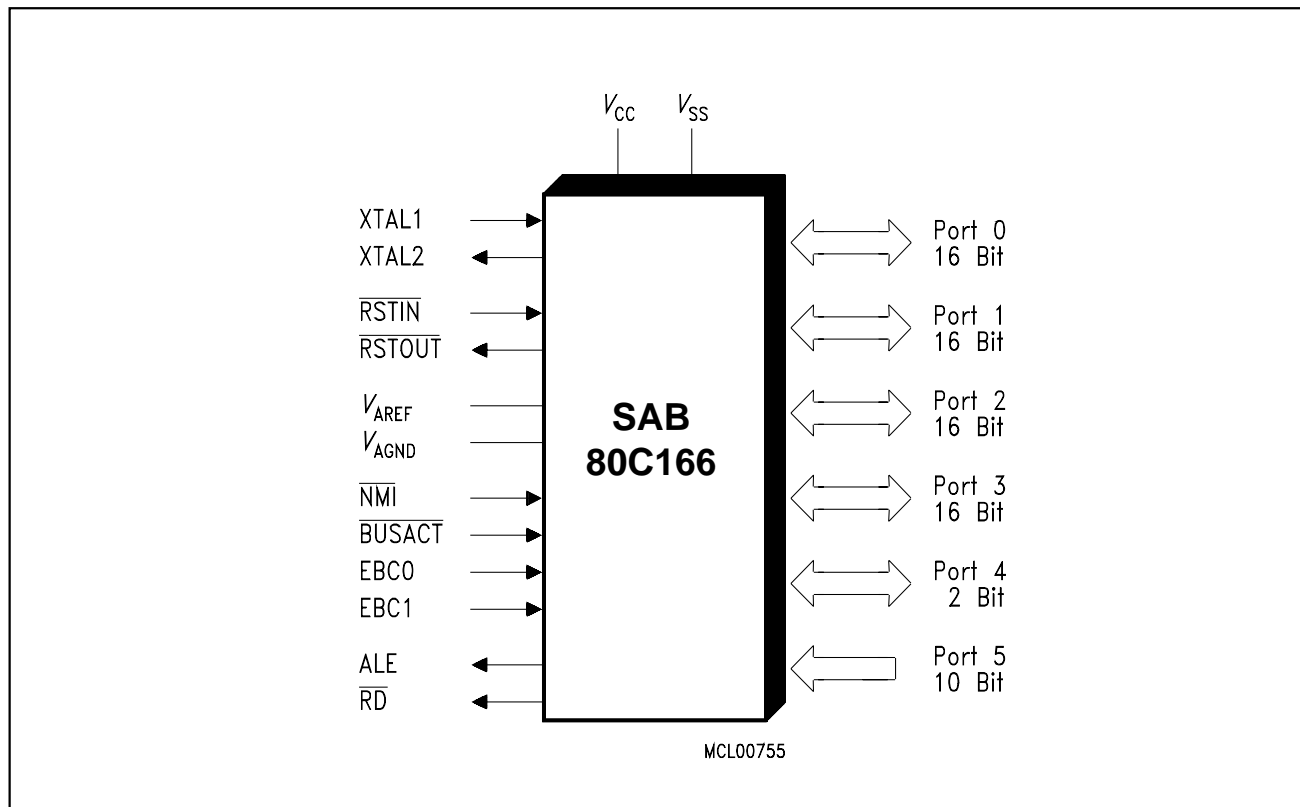


Figure 1
Logic Symbol

Ordering Information

| Type | Ordering Code | Package | Function |
|------------------|---------------|--------------|--|
| SAB 83C166-5M | Q67121-D... | P-MQFP-100-2 | 16-bit microcontroller, 0 °C to +70 °C, 1 KByte RAM and 32 KByte ROM |
| SAB 83C166-5M-T3 | Q67121-D... | P-MQFP-100-2 | 16-bit microcontroller, -40 °C to +85 °C, 1 KByte RAM and 32 KByte ROM |
| SAB 80C166-M | Q67121-C848 | P-MQFP-100-2 | 16-bit microcontroller, 0 °C to +70 °C 1 KByte RAM |
| SAB 80C166-M-T3 | Q67121-C900 | P-MQFP-100-2 | 16-bit microcontroller, -40 °C to +85 °C 1 KByte RAM |

Note: The ordering codes (Q67120-D...) for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

Pin Configuration Rectangular P-MQFP-100-2 (top view)

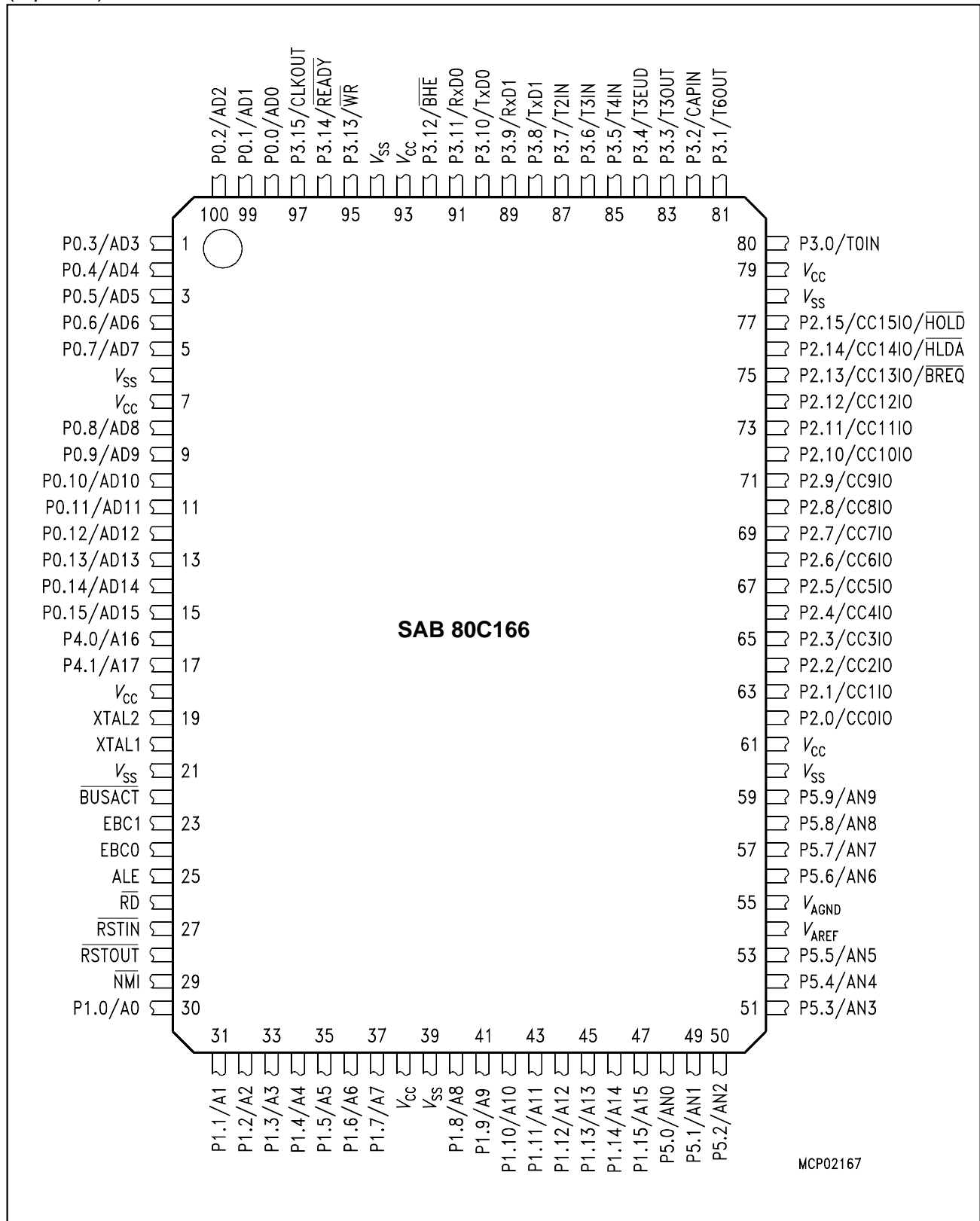


Figure 2

Pin Definitions and Functions

| Symbol | Pin Number | Input Output | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|----------------|--------------------------------------|--|----------------------------|------|--------------------------------------|------------------------|-----|-------------------------------------|---|-------------------------|---|---|---|-----------------------|---|---|---|------------------------|---|---|---|--------------------------|---|---|---|------------------|---|---|---|-----------|---|---|---|-----------|---|---|---|-----------|
| P4.0 – P4.1 | 16-17 | I/O | <p>Port 4 is a 2-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.</p> <p>In case of an external bus configuration, Port 4 can be used to output the segment address lines:</p> <table border="0"> <tr> <td>P4.0</td> <td>A16</td> <td>Least Significant Segment Addr. Line</td> </tr> <tr> <td>P4.1</td> <td>A17</td> <td>Most Significant Segment Addr. Line</td> </tr> </table> | P4.0 | A16 | Least Significant Segment Addr. Line | P4.1 | A17 | Most Significant Segment Addr. Line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P4.0 | A16 | Least Significant Segment Addr. Line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P4.1 | A17 | Most Significant Segment Addr. Line | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| XTAL1 | 20 | I | XTAL1: Input to the oscillator amplifier and input to the internal clock generator | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| XTAL2 | 19 | O | XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{BUSACT}}$, EBC1, EBC0 | 22 23 24 | I I I | <p>External Bus Configuration selection inputs. These pins are sampled during reset and select either the single chip mode or one of the four external bus configurations:</p> <table border="0"> <thead> <tr> <th>$\overline{\text{BUSACT}}$</th> <th>EBC1</th> <th>EBC0</th> <th>Mode/Bus Configuration</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>8-bit demultiplexed bus</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>8-bit multiplexed bus</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>16-bit multiplexed bus</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>16-bit demultiplexed bus</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Single chip mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Reserved.</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Reserved.</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Reserved.</td> </tr> </tbody> </table> <p>ROMless versions must have pin $\overline{\text{BUSACT}}$ tied to '0'.</p> | $\overline{\text{BUSACT}}$ | EBC1 | EBC0 | Mode/Bus Configuration | 0 | 0 | 0 | 8-bit demultiplexed bus | 0 | 0 | 1 | 8-bit multiplexed bus | 0 | 1 | 0 | 16-bit multiplexed bus | 0 | 1 | 1 | 16-bit demultiplexed bus | 1 | 0 | 0 | Single chip mode | 1 | 0 | 1 | Reserved. | 1 | 1 | 0 | Reserved. | 1 | 1 | 1 | Reserved. |
| $\overline{\text{BUSACT}}$ | EBC1 | EBC0 | Mode/Bus Configuration | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 8-bit demultiplexed bus | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 8-bit multiplexed bus | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 16-bit multiplexed bus | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 16-bit demultiplexed bus | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | Single chip mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | Reserved. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | Reserved. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | Reserved. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{RSTIN}}$ | 27 | I | Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the SAB 80C166. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS} . | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{RSTOUT}}$ | 28 | O | Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | Input Output | Function |
|-------------------------|----------------|--------------|--|
| $\overline{\text{NMI}}$ | 29 | I | Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, pin $\overline{\text{NMI}}$ must be low in order to force the SAB 80C166 to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pull $\overline{\text{NMI}}$ high externally. |
| ALE | 25 | O | Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes. |
| $\overline{\text{RD}}$ | 26 | O | External Memory Read Strobe. $\overline{\text{RD}}$ is activated for every external instruction or data read access. |
| P1.0 – P1.15 | 30-37 40-47 | I/O | Port 1 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. |
| P5.0 – P5.9 | 48-53 56-59 | I I | Port 5 is a 10-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as the (up to 10) analog input channels for the A/D converter, where P5.x equals ANx (Analog input channel x). |
| P2.0 – P2.15 | 62-77 | I/O | Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following Port 2 pins also serve for alternate functions: |
| | 62 | I/O | P2.0 CC0IO CAPCOM: CC0 Cap.-In/Comp.Out |
| | 75 | I/O | P2.13 CC13IO CAPCOM: CC13 Cap.-In/Comp.Out, $\overline{\text{BREQ}}$ External Bus Request Output |
| | 76 | I/O | P2.14 CC14IO CAPCOM: CC14 Cap.-In/Comp.Out, $\overline{\text{HLDA}}$ External Bus Hold Acknowl. Output |
| | 77 | O | P2.15 CC15IO CAPCOM: CC15 Cap.-In/Comp.Out, $\overline{\text{HOLD}}$ External Bus Hold Request Input |
| | | I | |

Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | Input Output | Function | | | | | | | | | | | | | | | | | | |
|-------------------|------------------|--------------|--|------------------|-------|--------|--------------|---------|---------|---------------|---------|----------|------------------|-------|--------|--------------|-----------|-----------|---------------|----------|------------|
| P3.0 – P3.15 | 80-92, 95-97 | I/O I/O | <p>Port 3 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.</p> <p>The following Port 3 pins also serve for alternate functions:</p> <p>P3.0 T0IN CAPCOM Timer T0 Count Input</p> <p>P3.1 T6OUT GPT2 Timer T6 Toggle Latch Output</p> <p>P3.2 CAPIN GPT2 Register CAPREL Capture Input</p> <p>P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output</p> <p>P3.4 T3EUD GPT1 Timer T3 Ext.Up/Down Ctrl.Input</p> <p>P3.5 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture</p> <p>P3.6 T3IN GPT1 Timer T3 Count/Gate Input</p> <p>P3.7 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture</p> <p>P3.8 TxD1 ASC1 Clock/Data Output (Asyn./Syn.)</p> <p>P3.9 RxD1 ASC1 Data Input (Asyn.) or I/O (Syn.)</p> <p>P3.10 TxD0 ASC0 Clock/Data Output (Asyn./Syn.)</p> <p>P3.11 RxD0 ASC0 Data Input (Asyn.) or I/O (Syn.)</p> <p>P3.12 $\overline{\text{BHE}}$ Ext. Memory High Byte Enable Signal</p> <p>P3.13 $\overline{\text{WR}}$ External Memory Write Strobe</p> <p>P3.14 $\overline{\text{READY}}$ Ready Signal Input</p> <p>P3.15 CLKOUT System Clock Output (=CPU Clock)</p> | | | | | | | | | | | | | | | | | | |
| P0.0 – P0.15 | 98 – 5 8 – 15 | I/O | <p>Port 0 is a 16-bit bidirectional IO port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.</p> <p>In case of an external bus configuration, Port 0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.</p> <p>Demultiplexed bus modes:</p> <table> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0.0 – P0.7:</td> <td>D0 – D7</td> <td>D0 - D7</td> </tr> <tr> <td>P0.8 – P0.15:</td> <td>output!</td> <td>D8 - D15</td> </tr> </table> <p>Multiplexed bus modes:</p> <table> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0.0 – P0.7:</td> <td>AD0 – AD7</td> <td>AD0 - AD7</td> </tr> <tr> <td>P0.8 – P0.15:</td> <td>A8 - A15</td> <td>AD8 - AD15</td> </tr> </table> | Data Path Width: | 8-bit | 16-bit | P0.0 – P0.7: | D0 – D7 | D0 - D7 | P0.8 – P0.15: | output! | D8 - D15 | Data Path Width: | 8-bit | 16-bit | P0.0 – P0.7: | AD0 – AD7 | AD0 - AD7 | P0.8 – P0.15: | A8 - A15 | AD8 - AD15 |
| Data Path Width: | 8-bit | 16-bit | | | | | | | | | | | | | | | | | | | |
| P0.0 – P0.7: | D0 – D7 | D0 - D7 | | | | | | | | | | | | | | | | | | | |
| P0.8 – P0.15: | output! | D8 - D15 | | | | | | | | | | | | | | | | | | | |
| Data Path Width: | 8-bit | 16-bit | | | | | | | | | | | | | | | | | | | |
| P0.0 – P0.7: | AD0 – AD7 | AD0 - AD7 | | | | | | | | | | | | | | | | | | | |
| P0.8 – P0.15: | A8 - A15 | AD8 - AD15 | | | | | | | | | | | | | | | | | | | |
| V_{AREF} | 54 | - | Reference voltage for the A/D converter. | | | | | | | | | | | | | | | | | | |
| V_{AGND} | 55 | - | Reference ground for the A/D converter. | | | | | | | | | | | | | | | | | | |

Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | Input Output | Function |
|---------------|-----------------------------|---------------------|---|
| V_{CC} | 7, 18, 38, 61, 79, 93 | - | Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode |
| V_{SS} | 6, 21, 39, 60, 78, 94 | - | Digital Ground. |

Functional Description

The architecture of the SAB 80C166 combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the SAB 80C166.

Note: All time specifications refer to a CPU clock of 20 MHz
(see definition in the AC Characteristics section).

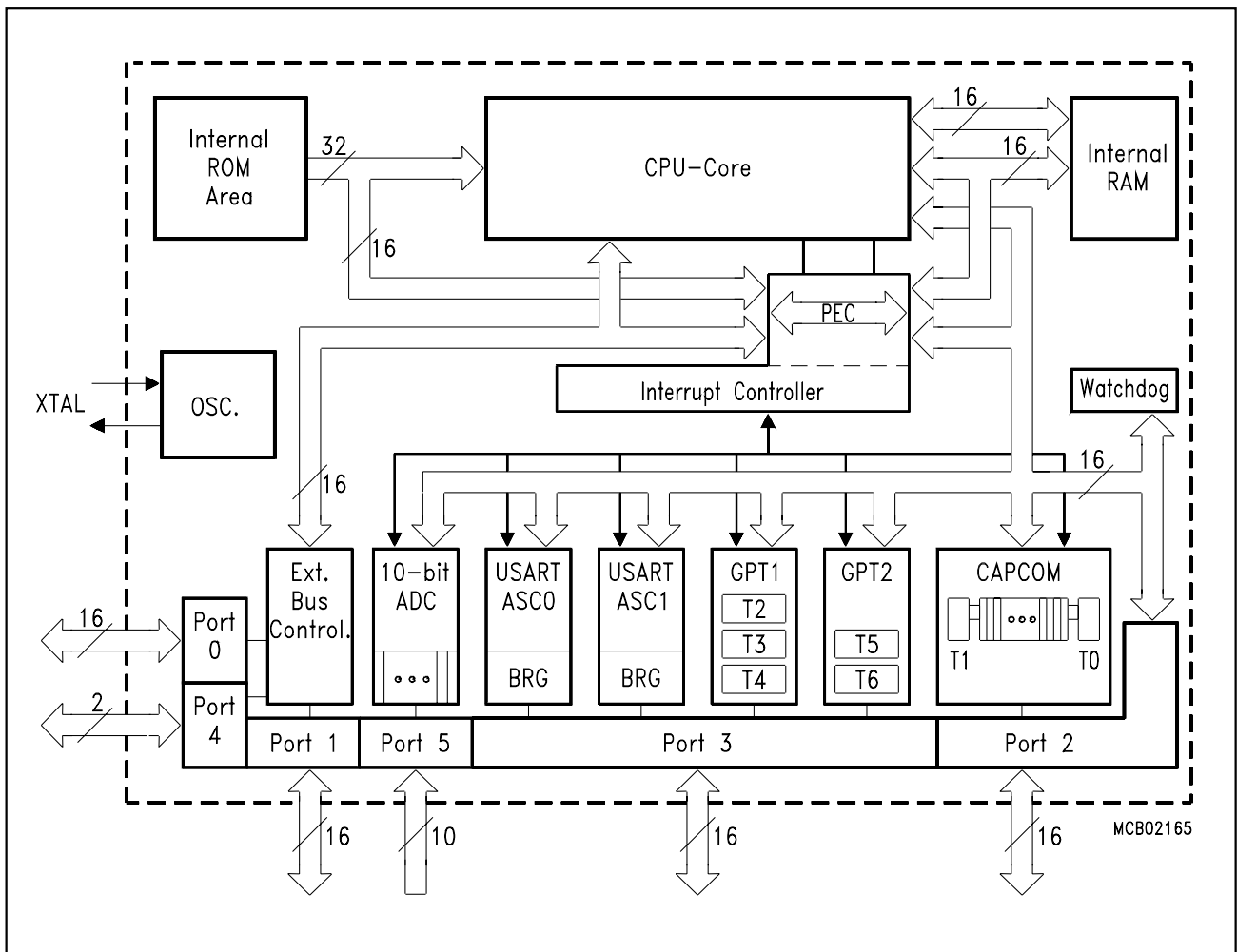


Figure 3
Block Diagram

Memory Organization

The memory space of the SAB 80C166 is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 256 KBytes. Address space expansion to 16 MBytes is provided for future versions. The entire memory space can be accessed byte-wise or word-wise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

The SAB 83C166 contains 32 KBytes of on-chip mask-programmable ROM for code or constant data. The ROM can be mapped to either segment 0 or segment 1.

1 KByte of on-chip RAM is provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

512 bytes of the address space are reserved for the Special Function Register area. SFRs are word-wide registers which are used for controlling and monitoring functions of the different on-chip units. 98 SFRs are currently implemented. Unused SFR addresses are reserved for future members of the SAB 80C166 family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 256 KBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on Port 1 and data is input/output on Port 0. In the multiplexed bus modes both addresses and data use Port 0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Read/Write Delay and Length of ALE, i.e. address setup/hold time with respect to ALE) have been made programmable to allow the user the adaption of a wide range of different types of memories. In addition, different address ranges may be accessed with different bus characteristics. Access to very slow memories is supported via a particular 'Ready' function. A $\overline{\text{HOLD}}/\overline{\text{HLDA}}$ protocol is available for bus arbitration.

For applications which require less than 64 KBytes of external memory space, a non-segmented memory model can be selected. In this case all memory locations can be addressed by 16 bits and Port 4 is not required to output the additional segment address lines.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the SAB 80C166's instructions can be executed in just one machine cycle which requires 100 ns at 20-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

The CPU disposes of an actual register context consisting of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at a time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

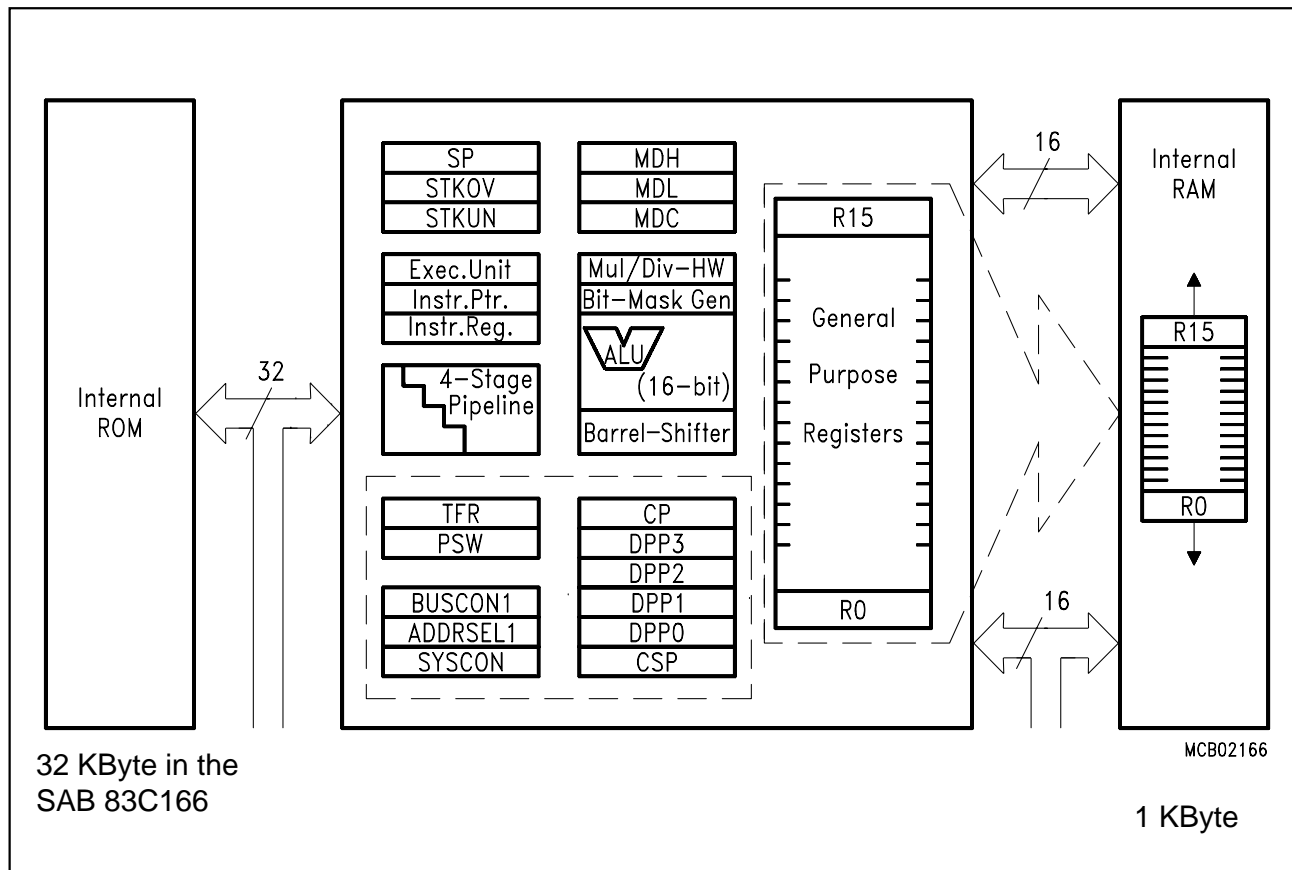


Figure 4
CPU Block Diagram

A system stack of up to 512 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient SAB 80C166 instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 250 ns to 600 ns (in case of internal program execution), the SAB 80C166 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the SAB 80C166 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data, or for transferring A/D converted results to a memory table. The SAB 80C166 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible SAB 80C166 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

| Source of Interrupt or PEC Service Request | Request Flag | Enable Flag | Interrupt Vector | Vector Location | Trap Number |
|--|--------------|-------------|------------------|-----------------|-----------------|
| CAPCOM Register 0 | CC0IR | CC0IE | CC0INT | 40 _H | 10 _H |
| CAPCOM Register 1 | CC1IR | CC1IE | CC1INT | 44 _H | 11 _H |
| CAPCOM Register 2 | CC2IR | CC2IE | CC2INT | 48 _H | 12 _H |
| CAPCOM Register 3 | CC3IR | CC3IE | CC3INT | 4C _H | 13 _H |
| CAPCOM Register 4 | CC4IR | CC4IE | CC4INT | 50 _H | 14 _H |
| CAPCOM Register 5 | CC5IR | CC5IE | CC5INT | 54 _H | 15 _H |
| CAPCOM Register 6 | CC6IR | CC6IE | CC6INT | 58 _H | 16 _H |
| CAPCOM Register 7 | CC7IR | CC7IE | CC7INT | 5C _H | 17 _H |
| CAPCOM Register 8 | CC8IR | CC8IE | CC8INT | 60 _H | 18 _H |
| CAPCOM Register 9 | CC9IR | CC9IE | CC9INT | 64 _H | 19 _H |
| CAPCOM Register 10 | CC10IR | CC10IE | CC10INT | 68 _H | 1A _H |
| CAPCOM Register 11 | CC11IR | CC11IE | CC11INT | 6C _H | 1B _H |
| CAPCOM Register 12 | CC12IR | CC12IE | CC12INT | 70 _H | 1C _H |
| CAPCOM Register 13 | CC13IR | CC13IE | CC13INT | 74 _H | 1D _H |
| CAPCOM Register 14 | CC14IR | CC14IE | CC14INT | 78 _H | 1E _H |
| CAPCOM Register 15 | CC15IR | CC15IE | CC15INT | 7C _H | 1F _H |
| CAPCOM Timer 0 | T0IR | T0IE | T0INT | 80 _H | 20 _H |
| CAPCOM Timer 1 | T1IR | T1IE | T1INT | 84 _H | 21 _H |
| GPT1 Timer 2 | T2IR | T2IE | T2INT | 88 _H | 22 _H |
| GPT1 Timer 3 | T3IR | T3IE | T3INT | 8C _H | 23 _H |
| GPT1 Timer 4 | T4IR | T4IE | T4INT | 90 _H | 24 _H |
| GPT2 Timer 5 | T5IR | T5IE | T5INT | 94 _H | 25 _H |
| GPT2 Timer 6 | T6IR | T6IE | T6INT | 98 _H | 26 _H |
| GPT2 CAPREL Register | CRIR | CRIE | CRINT | 9C _H | 27 _H |
| A/D Conversion Complete | ADCIR | ADCIE | ADCINT | A0 _H | 28 _H |
| A/D Overrun Error | ADEIR | ADEIE | ADEINT | A4 _H | 29 _H |
| ASC0 Transmit | S0TIR | S0TIE | S0TINT | A8 _H | 2A _H |
| ASC0 Receive | S0RIR | S0RIE | S0RINT | AC _H | 2B _H |
| ASC0 Error | S0EIR | S0EIE | S0EINT | B0 _H | 2C _H |
| ASC1 Transmit | S1TIR | S1TIE | S1TINT | B4 _H | 2D _H |
| ASC1 Receive | S1RIR | S1RIE | S1RINT | B8 _H | 2E _H |
| ASC1 Error | S1EIR | S1EIE | S1EINT | BC _H | 2F _H |

The SAB 80C166 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

| Exception Condition | Trap Flag | Trap Vector | Vector Location | Trap Number | Trap Priority |
|-----------------------------|-----------|-------------|---|--------------------------------------|----------------------|
| Reset Functions: | | | | | |
| Hardware Reset | | RESET | 0000 _H | 00 _H | III |
| Software Reset | | RESET | 0000 _H | 00 _H | III |
| Watchdog Timer Overflow | | RESET | 0000 _H | 00 _H | III |
| Class A Hardware Traps: | | | | | |
| Non-Maskable Interrupt | NMI | NMITRAP | 0008 _H | 02 _H | II |
| Stack Overflow | STKOF | STOTRAP | 0010 _H | 04 _H | II |
| Stack Underflow | STKUF | STUTRAP | 0018 _H | 06 _H | II |
| Class B Hardware Traps: | | | | | |
| Undefined Opcode | UNDOPC | BTRAP | 0028 _H | 0A _H | I |
| Protected Instruction Fault | PRTFLT | BTRAP | 0028 _H | 0A _H | I |
| Illegal Word Operand Access | ILLOPA | BTRAP | 0028 _H | 0A _H | I |
| Illegal Instruction Access | ILLINA | BTRAP | 0028 _H | 0A _H | I |
| Illegal External Bus Access | ILLBUS | BTRAP | 0028 _H | 0A _H | I |
| Reserved | | | [002C _H – 003C _H] | [0B _H – 0F _H] | |
| Software Traps | | | Any | Any | Current CPU Priority |
| TRAP Instruction | | | [0000 _H – 01FC _H] in steps of 04 _H | [00 _H – 7F _H] | |

Capture/Compare (CAPCOM) Unit

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of 400 ns (@ 20 MHz CPU clock). The CAPCOM unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T0/T1) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the CPU clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, an external count input for CAPCOM timer T0 allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1, and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (captured) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

| Compare Modes | Function |
|----------------------|---|
| Mode 0 | Interrupt-only compare mode; several compare interrupts per timer period are possible |
| Mode 1 | Pin toggles on each compare match; several compare events per timer period are possible |
| Mode 2 | Interrupt-only compare mode; only one compare interrupt per timer period is generated |
| Mode 3 | Pin set '1' on match; pin reset '0' on compare time overflow; only one compare event per timer period is generated |
| Double Register Mode | Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible. |

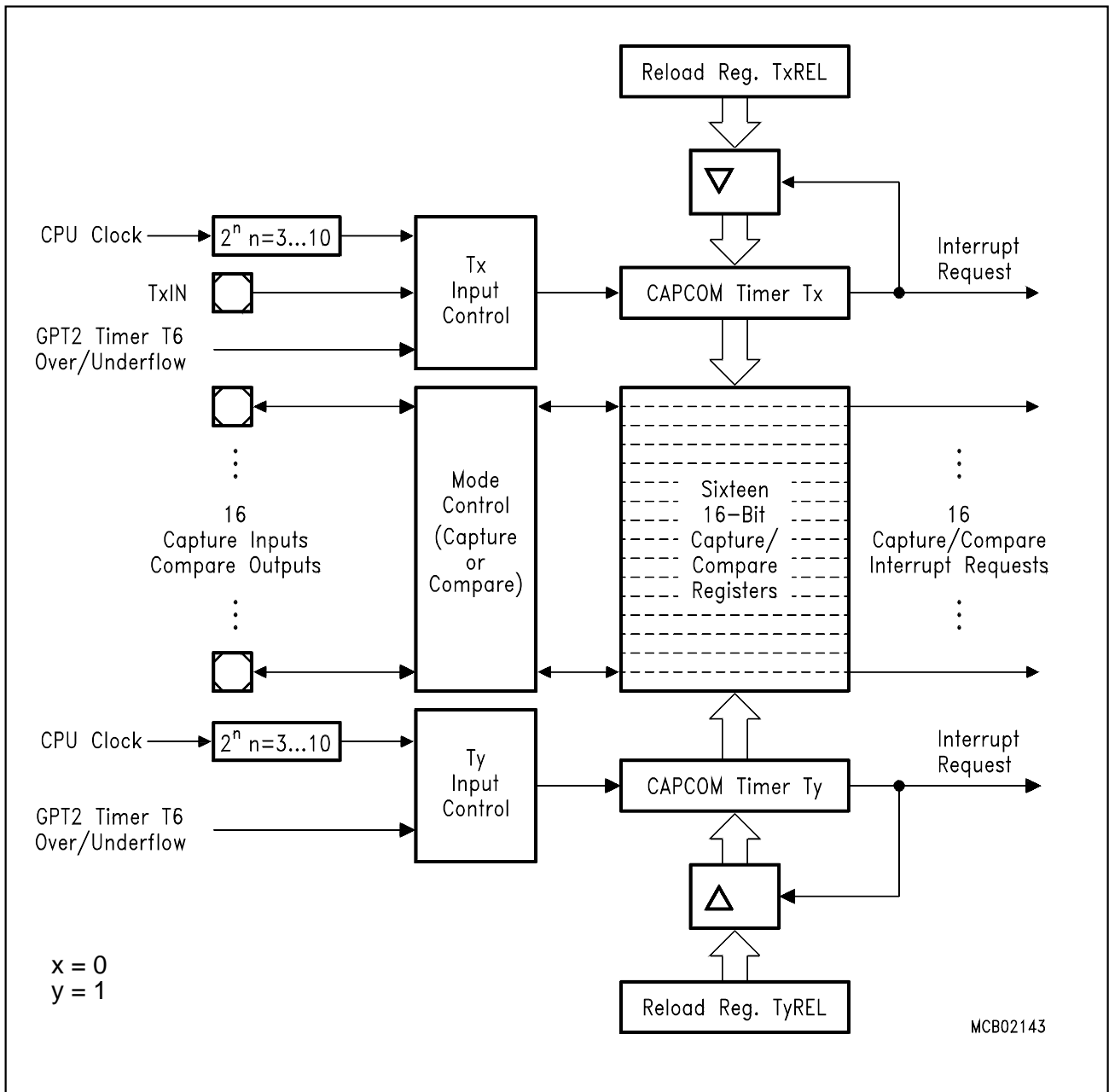


Figure 5
CAPCOM Unit Block Diagram

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of module GPT1 can be configured individually for one of three basic modes of operation, which are Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 400 ns (@ 20 MHz CPU clock).

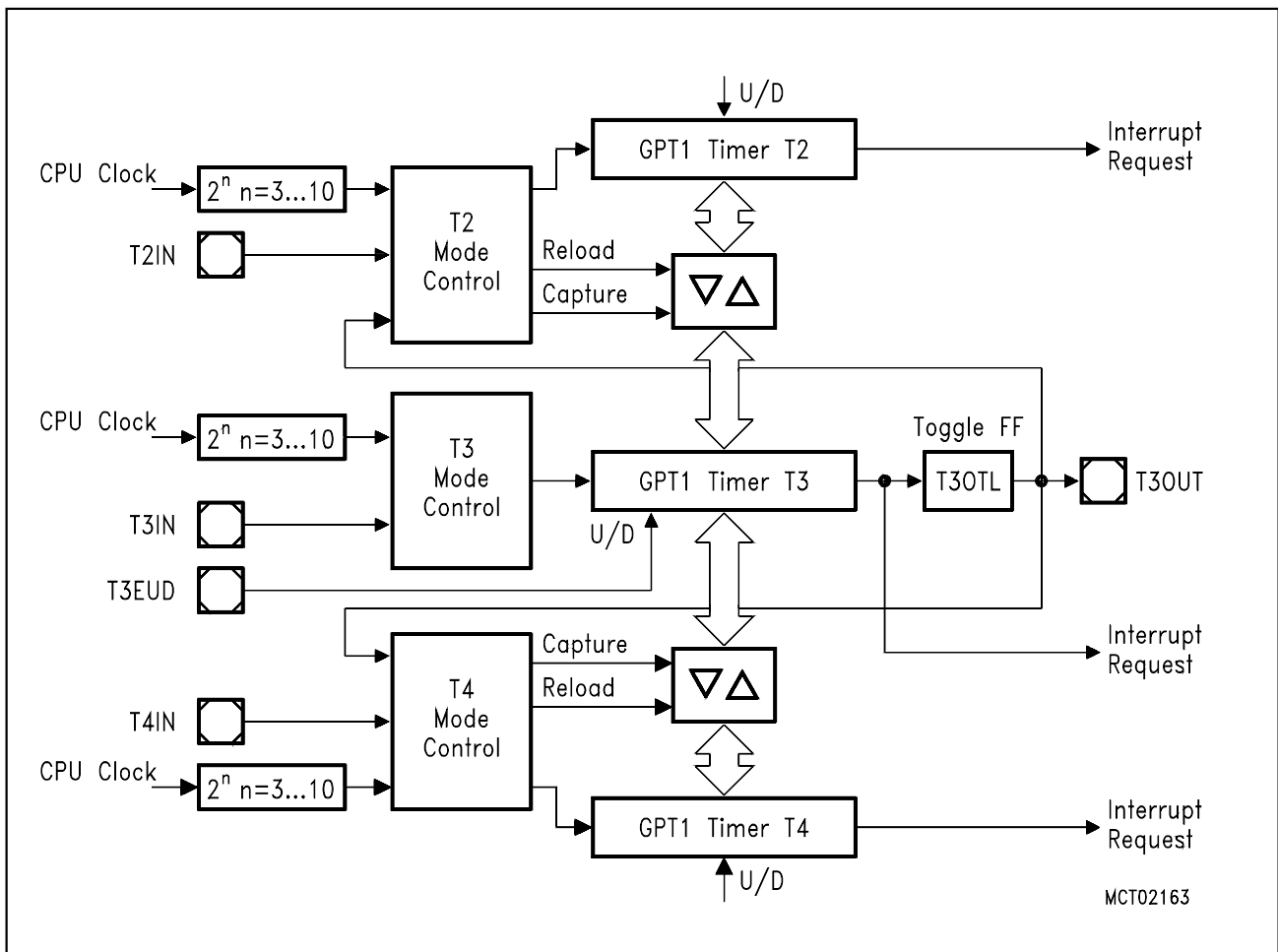


Figure 6
Block Diagram of GPT1

The count direction (up/down) for each timer is programmable by software. For timer T3 the count direction may additionally be altered dynamically by an external signal on a port pin (T3EUD) to facilitate e. g. position tracking.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on a port pin (T3OUT) e. g. for timeout monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

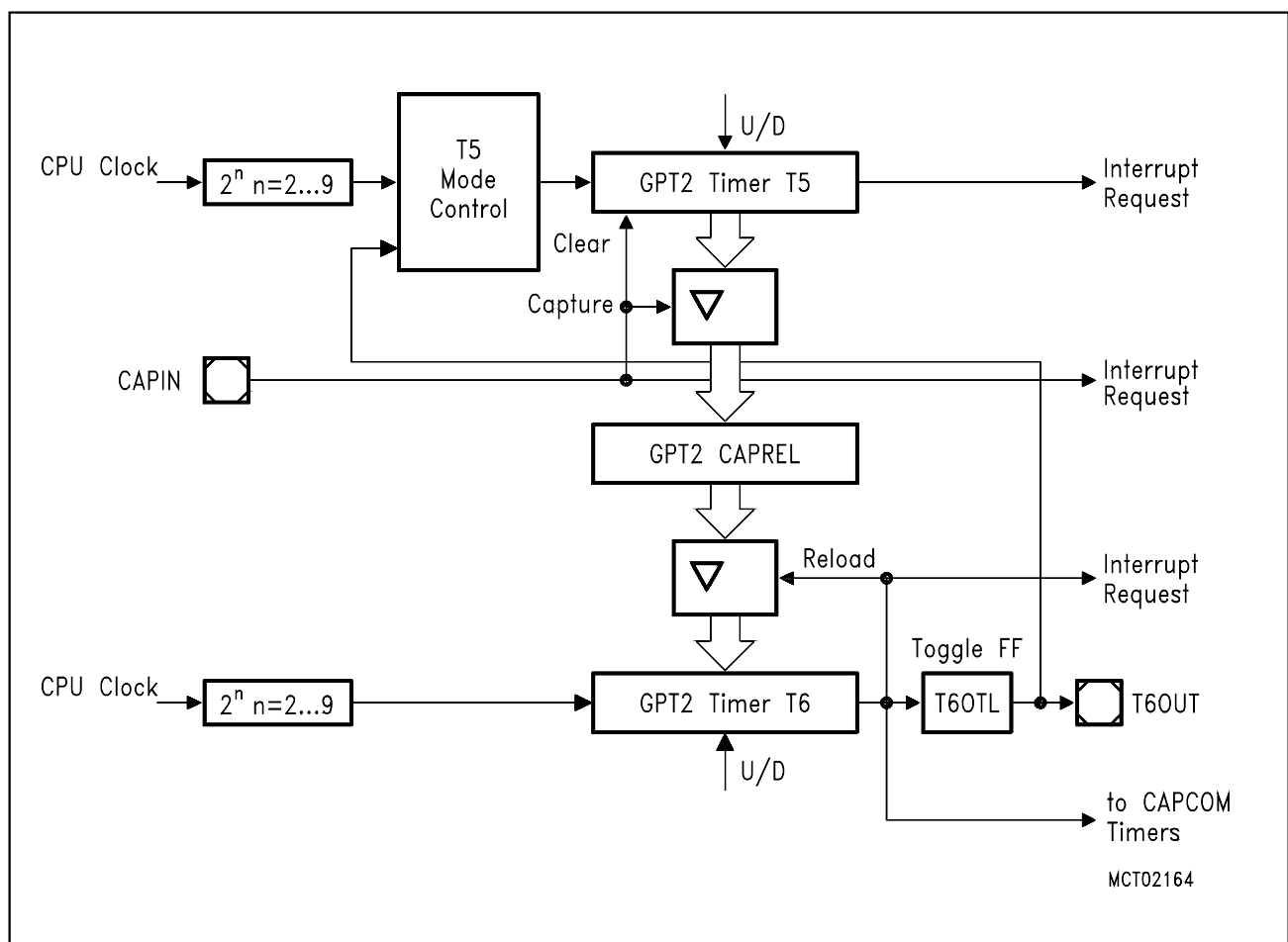


Figure 7
Block Diagram of GPT2

With its maximum resolution of 200 ns (@ 20 MHz), the GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler. The count direction (up/down) for each timer is programmable by software. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

A/D Converter

For analog signal measurement, a 10-bit A/D converter with 10 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time adds up to 9.7 us @ 20 MHz CPU clock.

Overrun error detection/protection is provided for the conversion result register (ADDAT): an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete.

For applications which require less than 10 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the SAB 80C166 supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

Parallel Ports

The SAB 80C166 provides up to 76 I/O lines which are organized into five input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. Port 0 and Port 1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A17/A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 2 is associated with the capture inputs or compare outputs of the CAPCOM unit and/or with optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$). Port 3 includes alternate functions of timers, serial interfaces, optional bus control signals ($\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{READY}}$) and the system clock output (CLKOUT). Port 5 is used for the analog input channels to the A/D converter. All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with identical functionality, Asynchronous/Synchronous Serial Channels ASC0 and ASC1.

They are upward compatible with the serial ports of the Siemens SAB 8051x microcontroller family and support full-duplex asynchronous communication up to 625 Kbaud and half-duplex synchronous communication up to 2.5 Mbaud @ 20 MHz CPU clock.

Two dedicated baud rate generators allow to set up all standard baud rates without oscillator tuning. For transmission, reception, and erroneous reception 3 separate interrupt vectors are provided for each serial channel.

In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode).

In synchronous mode one data byte is transmitted or received synchronously to a shift clock which is generated by the SAB 80C166.

A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the CPU clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 25 μs and 420 ms can be monitored (@ 20 MHz CPU clock). The default Watchdog Timer interval after reset is 6.55 ms (@ 20 MHz CPU clock).

Bootstrap Loader

The SAB 80C166 provides a built-in bootstrap loader (BSL), which allows to start program execution out of the SAB 80C166's internal RAM. The program to be started is loaded via the serial interface ASC0 and does not require external memory or an internal ROM.

The SAB 80C166 enters BSL mode, when ALE is sampled high at the end of a hardware reset and if $\overline{\text{NMI}}$ becomes active directly after the end of the internal reset sequence. BSL mode is entered independent of the bus mode selected via EBC0, EBC1 and $\overline{\text{BUSACT}}$.

After entering BSL mode the SAB 80C166 scans the RXD0 line to receive a zero byte, i.e. one start bit, eight '0' data bits and one stop bit. From the duration of this zero byte it calculates the corresponding baudrate factor with respect to the current CPU clock and initializes ASC0 accordingly. Using this baudrate, an acknowledge byte is returned to the host that provides the loaded data. The SAB 80C166 returns the value <55_H>.

The next 32 bytes received via ASC0 are stored sequentially into locations 0FA40_H through 0FA5F_H of the internal RAM. To execute the loaded code the BSL then jumps to location 0FA40_H. The loaded program may load additional code / data, change modes, etc.

The SAB 80C166 exits BSL mode upon a software reset (ignores the ALE level) or a hardware reset (remove conditions for entering BSL mode before).

Instruction Set Summary

The table below lists the instructions of the SAB 80C166 in a condensed way.

The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**C16x Family Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

Instruction Set Summary

| Mnemonic | Description | Bytes |
|-----------------|---|-------|
| ADD(B) | Add word (byte) operands | 2 / 4 |
| ADDC(B) | Add word (byte) operands with Carry | 2 / 4 |
| SUB(B) | Subtract word (byte) operands | 2 / 4 |
| SUBC(B) | Subtract word (byte) operands with Carry | 2 / 4 |
| MUL(U) | (Un)Signed multiply direct GPR by direct GPR (16-16-bit) | 2 |
| DIV(U) | (Un)Signed divide register MDL by direct GPR (16-/16-bit) | 2 |
| DIVL(U) | (Un)Signed long divide reg. MD by direct GPR (32-/16-bit) | 2 |
| CPL(B) | Complement direct word (byte) GPR | 2 |
| NEG(B) | Negate direct word (byte) GPR | 2 |
| AND(B) | Bitwise AND, (word/byte operands) | 2 / 4 |
| OR(B) | Bitwise OR, (word/byte operands) | 2 / 4 |
| XOR(B) | Bitwise XOR, (word/byte operands) | 2 / 4 |
| BCLR | Clear direct bit | 2 |
| BSET | Set direct bit | 2 |
| BMOV(N) | Move (negated) direct bit to direct bit | 4 |
| BAND, BOR, BXOR | AND/OR/XOR direct bit with direct bit | 4 |
| BCMP | Compare direct bit to direct bit | 4 |
| BFLDH/L | Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data | 4 |
| CMP(B) | Compare word (byte) operands | 2 / 4 |
| CMPD1/2 | Compare word data to GPR and decrement GPR by 1/2 | 2 / 4 |
| CMPI1/2 | Compare word data to GPR and increment GPR by 1/2 | 2 / 4 |
| PRIOR | Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR | 2 |
| SHL / SHR | Shift left/right direct word GPR | 2 |
| ROL / ROR | Rotate left/right direct word GPR | 2 |
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |

Instruction Set Summary (cont'd)

| Mnemonic | Description | Bytes |
|---------------------|---|-------|
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS | Move byte operand to word operand with sign extension | 2 / 4 |
| MOVBZ | Move byte operand to word operand. with zero extension | 2 / 4 |
| JMPA, JMPI, JMPR | Jump absolute/indirect/relative if condition is met | 4 |
| JMPS | Jump absolute to a code segment | 4 |
| J(N)B | Jump relative if direct bit is (not) set | 4 |
| JBC | Jump relative and clear bit if direct bit is set | 4 |
| JNBS | Jump relative and set bit if direct bit is not set | 4 |
| CALLA, CALLI, CALLR | Call absolute/indirect/relative subroutine if condition is met | 4 |
| CALLS | Call absolute subroutine in any code segment | 4 |
| PCALL | Push direct word register onto system stack and call absolute subroutine | 4 |
| TRAP | Call interrupt service routine via immediate trap number | 2 |
| PUSH, POP | Push/pop direct word register onto/from system stack | 2 |
| SCXT | Push direct word register onto system stack and update register with word operand | 4 |
| RET | Return from intra-segment subroutine | 2 |
| RETS | Return from inter-segment subroutine | 2 |
| RETP | Return from intra-segment subroutine and pop direct word register from system stack | 2 |
| RETI | Return from interrupt service subroutine | 2 |
| SRST | Software Reset | 4 |
| IDLE | Enter Idle Mode | 4 |
| PWRDN | Enter Power Down Mode (supposes NMI-pin being low) | 4 |
| SRVWDT | Service Watchdog Timer | 4 |
| DISWDT | Disable Watchdog Timer | 4 |
| EINIT | Signify End-of-Initialization on RSTOUT-pin | 4 |
| NOP | Null operation | 2 |

Special Function Registers Overview

The following table lists all SFRs which are implemented in the SAB 80C166 in alphabetical order. Bit-addressable SFRs are marked with the letter “b” in column “Name”.

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Special Function Registers Overview

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|-----------------|---------------------|-----------------|--|-------------------|
| ADCIC | b FF98 _H | CC _H | A/D Converter End of Conversion Interrupt Control Register | 0000 _H |
| ADCON | b FFA0 _H | D0 _H | A/D Converter Control Register | 0000 _H |
| ADDAT | FEA0 _H | 50 _H | A/D Converter Result Register | 0000 _H |
| ADDRSEL1 | FE18 _H | 0C _H | Address Select Register 1 | 0000 _H |
| ADEIC | b FF9A _H | CD _H | A/D Converter Overrun Error Interrupt Control Register | 0000 _H |
| BUSCON1 | b FF14 _H | 8A _H | Bus Configuration Register 1 | 0000 _H |
| CAPREL | FE4A _H | 25 _H | GPT2 Capture/Reload Register | 0000 _H |
| CC0 | FE80 _H | 40 _H | CAPCOM Register 0 | 0000 _H |
| CC0IC | b FF78 _H | BC _H | CAPCOM Register 0 Interrupt Control Register | 0000 _H |
| CC1 | FE82 _H | 41 _H | CAPCOM Register 1 | 0000 _H |
| CC1IC | b FF7A _H | BD _H | CAPCOM Register 1 Interrupt Control Register | 0000 _H |
| CC2 | FE84 _H | 42 _H | CAPCOM Register 2 | 0000 _H |
| CC2IC | b FF7C _H | BE _H | CAPCOM Register 2 Interrupt Control Register | 0000 _H |
| CC3 | FE86 _H | 43 _H | CAPCOM Register 3 | 0000 _H |
| CC3IC | b FF7E _H | BF _H | CAPCOM Register 3 Interrupt Control Register | 0000 _H |
| CC4 | FE88 _H | 44 _H | CAPCOM Register 4 | 0000 _H |
| CC4IC | b FF80 _H | C0 _H | CAPCOM Register 4 Interrupt Control Register | 0000 _H |
| CC5 | FE8A _H | 45 _H | CAPCOM Register 5 | 0000 _H |
| CC5IC | b FF82 _H | C1 _H | CAPCOM Register 5 Interrupt Control Register | 0000 _H |
| CC6 | FE8C _H | 46 _H | CAPCOM Register 6 | 0000 _H |
| CC6IC | b FF84 _H | C2 _H | CAPCOM Register 6 Interrupt Control Register | 0000 _H |
| CC7 | FE8E _H | 47 _H | CAPCOM Register 7 | 0000 _H |

Special Function Registers Overview (cont'd)

| Name | | Physical Address | 8-Bit Address | Description | Reset Value |
|---------------|----------|-------------------|-----------------|--|-------------------|
| CC7IC | b | FF86 _H | C3 _H | CAPCOM Register 7 Interrupt Control Register | 0000 _H |
| CC8 | | FE90 _H | 48 _H | CAPCOM Register 8 | 0000 _H |
| CC8IC | b | FF88 _H | C4 _H | CAPCOM Register 8 Interrupt Control Register | 0000 _H |
| CC9 | | FE92 _H | 49 _H | CAPCOM Register 9 | 0000 _H |
| CC9IC | b | FF8A _H | C5 _H | CAPCOM Register 9 Interrupt Control Register | 0000 _H |
| CC10 | | FE94 _H | 4A _H | CAPCOM Register 10 | 0000 _H |
| CC10IC | b | FF8C _H | C6 _H | CAPCOM Register 10 Interrupt Control Register | 0000 _H |
| CC11 | | FE96 _H | 4B _H | CAPCOM Register 11 | 0000 _H |
| CC11IC | b | FF8E _H | C7 _H | CAPCOM Register 11 Interrupt Control Register | 0000 _H |
| CC12 | | FE98 _H | 4C _H | CAPCOM Register 12 | 0000 _H |
| CC12IC | b | FF90 _H | C8 _H | CAPCOM Register 12 Interrupt Control Register | 0000 _H |
| CC13 | | FE9A _H | 4D _H | CAPCOM Register 13 | 0000 _H |
| CC13IC | b | FF92 _H | C9 _H | CAPCOM Register 13 Interrupt Control Register | 0000 _H |
| CC14 | | FE9C _H | 4E _H | CAPCOM Register 14 | 0000 _H |
| CC14IC | b | FF94 _H | CA _H | CAPCOM Register 14 Interrupt Control Register | 0000 _H |
| CC15 | | FE9E _H | 4F _H | CAPCOM Register 15 | 0000 _H |
| CC15IC | b | FF96 _H | CB _H | CAPCOM Register 15 Interrupt Control Register | 0000 _H |
| CCM0 | b | FF52 _H | A9 _H | CAPCOM Mode Control Register 0 | 0000 _H |
| CCM1 | b | FF54 _H | AA _H | CAPCOM Mode Control Register 1 | 0000 _H |
| CCM2 | b | FF56 _H | AB _H | CAPCOM Mode Control Register 2 | 0000 _H |
| CCM3 | b | FF58 _H | AC _H | CAPCOM Mode Control Register 3 | 0000 _H |
| CP | | FE10 _H | 08 _H | CPU Context Pointer Register | FC00 _H |
| CRIC | b | FF6A _H | B5 _H | GPT2 CAPREL Interrupt Control Register | 0000 _H |
| CSP | | FE08 _H | 04 _H | CPU Code Segment Pointer Register (2 bits, read only) | 0000 _H |
| DP0 | b | FF02 _H | 81 _H | Port 0 Direction Control Register | 0000 _H |
| DP1 | b | FF06 _H | 83 _H | Port 1 Direction Control Register | 0000 _H |
| DP2 | b | FFC2 _H | E1 _H | Port 2 Direction Control Register | 0000 _H |
| DP3 | b | FFC6 _H | E3 _H | Port 3 Direction Control Register | 0000 _H |
| DP4 | b | FF0A _H | 85 _H | Port 4 Direction Control Register (2 bits) | 00 _H |

Special Function Registers Overview (cont'd)

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|---------------|----------------------------|-----------------|--|-------------------|
| DPP0 | FE00 _H | 00 _H | CPU Data Page Pointer 0 Register (4 bits) | 0000 _H |
| DPP1 | FE02 _H | 01 _H | CPU Data Page Pointer 1 Register (4 bits) | 0001 _H |
| DPP2 | FE04 _H | 02 _H | CPU Data Page Pointer 2 Register (4 bits) | 0002 _H |
| DPP3 | FE06 _H | 03 _H | CPU Data Page Pointer 3 Register (4 bits) | 0003 _H |
| MDC | b FF0E _H | 87 _H | CPU Multiply / Divide Control Register | 0000 _H |
| MDH | FE0C _H | 06 _H | CPU Multiply / Divide Register – High Word | 0000 _H |
| MDL | FE0E _H | 07 _H | CPU Multiply / Divide Register – Low Word | 0000 _H |
| ONES | FF1E _H | 8F _H | Constant Value 1's Register (read only) | FFFF _H |
| P0 | b FF00 _H | 80 _H | Port 0 Register | 0000 _H |
| P1 | b FF04 _H | 82 _H | Port 1 Register | 0000 _H |
| P2 | b FFC0 _H | E0 _H | Port 2 Register | 0000 _H |
| P3 | b FFC4 _H | E2 _H | Port 3 Register | 0000 _H |
| P4 | b FFC8 _H | E4 _H | Port 4 Register (2 bits) | 00 _H |
| P5 | b FFA2 _H | D1 _H | Port 5 Register (read only) | XXXX _H |
| PECC0 | FEC0 _H | 60 _H | PEC Channel 0 Control Register | 0000 _H |
| PECC1 | FEC2 _H | 61 _H | PEC Channel 1 Control Register | 0000 _H |
| PECC2 | FEC4 _H | 62 _H | PEC Channel 2 Control Register | 0000 _H |
| PECC3 | FEC6 _H | 63 _H | PEC Channel 3 Control Register | 0000 _H |
| PECC4 | FEC8 _H | 64 _H | PEC Channel 4 Control Register | 0000 _H |
| PECC5 | FECA _H | 65 _H | PEC Channel 5 Control Register | 0000 _H |
| PECC6 | FEC _H | 66 _H | PEC Channel 6 Control Register | 0000 _H |
| PECC7 | FECE _H | 67 _H | PEC Channel 7 Control Register | 0000 _H |
| PSW | b FF10 _H | 88 _H | CPU Program Status Word | 0000 _H |
| S0BG | FEB4 _H | 5A _H | Serial Channel 0 Baud Rate Generator Reload Register | 0000 _H |
| S0CON | b FFB0 _H | D8 _H | Serial Channel 0 Control Register | 0000 _H |
| S0EIC | b FF70 _H | B8 _H | Serial Channel 0 Error Interrupt Control Register | 0000 _H |
| S0RBUF | FEB2 _H | 59 _H | Serial Channel 0 Receive Buffer Register (read only) | XX _H |

Special Function Registers Overview (cont'd)

| Name | | Physical Address | 8-Bit Address | Description | Reset Value |
|---------------|----------|-------------------|-----------------|--|----------------------|
| S0RIC | b | FF6E _H | B7 _H | Serial Channel 0 Receive Interrupt Control Register | 0000 _H |
| S0TBUF | | FEB0 _H | 58 _H | Serial Channel 0 Transmit Buffer Register (write only) | 00 _H |
| S0TIC | b | FF6C _H | B6 _H | Serial Channel 0 Transmit Interrupt Control Register | 0000 _H |
| S1BG | | FEBC _H | 5E _H | Serial Channel 1 Baud Rate Generator Reload Register | 0000 _H |
| S1CON | b | FFB8 _H | DC _H | Serial Channel 1 Control Register | 0000 _H |
| S1EIC | b | FF76 _H | BB _H | Serial Channel 1 Error Interrupt Control Register | 0000 _H |
| S1RBUF | | FEBA _H | 5D _H | Serial Channel 1 Receive Buffer Register (read only) | XX _H |
| S1RIC | b | FF74 _H | BA _H | Serial Channel 1 Receive Interrupt Control Register | 0000 _H |
| S1TBUF | | FEB8 _H | 5C _H | Serial Channel 1 Transmit Buffer Register (write only) | 00 _H |
| S1TIC | b | FF72 _H | B9 _H | Serial Channel 1 Transmit Interrupt Control Register | 0000 _H |
| SP | | FE12 _H | 09 _H | CPU System Stack Pointer Register | FC00 _H |
| STKOV | | FE14 _H | 0A _H | CPU Stack Overflow Pointer Register | FA00 _H |
| STKUN | | FE16 _H | 0B _H | CPU Stack Underflow Pointer Register | FC00 _H |
| SYSCON | b | FF0C _H | 86 _H | CPU System Configuration Register | 0xx0 _H *) |
| T0 | | FE50 _H | 28 _H | CAPCOM Timer 0 Register | 0000 _H |
| T01CON | b | FF50 _H | A8 _H | CAPCOM Timer 0 and Timer 1 Control Register | 0000 _H |
| T0IC | b | FF9C _H | CE _H | CAPCOM Timer 0 Interrupt Control Register | 0000 _H |
| T0REL | | FE54 _H | 2A _H | CAPCOM Timer 0 Reload Register | 0000 _H |
| T1 | | FE52 _H | 29 _H | CAPCOM Timer 1 Register | 0000 _H |
| T1IC | b | FF9E _H | CF _H | CAPCOM Timer 1 Interrupt Control Register | 0000 _H |
| T1REL | | FE56 _H | 2B _H | CAPCOM Timer 1 Reload Register | 0000 _H |
| T2 | | FE40 _H | 20 _H | GPT1 Timer 2 Register | 0000 _H |
| T2CON | b | FF40 _H | A0 _H | GPT1 Timer 2 Control Register | 0000 _H |
| T2IC | b | FF60 _H | B0 _H | GPT1 Timer 2 Interrupt Control Register | 0000 _H |

Special Function Registers Overview (cont'd)

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|---------------|----------------------------|-----------------|---|-------------------|
| T3 | FE42 _H | 21 _H | GPT1 Timer 3 Register | 0000 _H |
| T3CON | b FF42 _H | A1 _H | GPT1 Timer 3 Control Register | 0000 _H |
| T3IC | b FF62 _H | B1 _H | GPT1 Timer 3 Interrupt Control Register | 0000 _H |
| T4 | FE44 _H | 22 _H | GPT1 Timer 4 Register | 0000 _H |
| T4CON | b FF44 _H | A2 _H | GPT1 Timer 4 Control Register | 0000 _H |
| T4IC | b FF64 _H | B2 _H | GPT1 Timer 4 Interrupt Control Register | 0000 _H |
| T5 | FE46 _H | 23 _H | GPT2 Timer 5 Register | 0000 _H |
| T5CON | b FF46 _H | A3 _H | GPT2 Timer 5 Control Register | 0000 _H |
| T5IC | b FF66 _H | B3 _H | GPT2 Timer 5 Interrupt Control Register | 0000 _H |
| T6 | FE48 _H | 24 _H | GPT2 Timer 6 Register | 0000 _H |
| T6CON | b FF48 _H | A4 _H | GPT2 Timer 6 Control Register | 0000 _H |
| T6IC | b FF68 _H | B4 _H | GPT2 Timer 6 Interrupt Control Register | 0000 _H |
| TFR | b FFAC _H | D6 _H | Trap Flag Register | 0000 _H |
| WDT | FEAE _H | 57 _H | Watchdog Timer Register (read only) | 0000 _H |
| WDTCON | FFAE _H | D7 _H | Watchdog Timer Control Register | 0000 _H |
| ZEROS | b FF1C _H | 8E _H | Constant Value 0's Register (read only) | 0000 _H |

*) The system configuration is selected during reset.

Absolute Maximum Ratings

Ambient temperature under bias (T_A):

SAB 83C166-5M, SAB 80C166-M..... 0 to + 70 °C

SAB 83C166-5M-T3, SAB 80C166-M-T3 – 40 to + 85 °C

Storage temperature (T_{ST}) – 65 to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) – 0.5 to + 6.5 V

Voltage on any pin with respect to ground (V_{SS}) – 0.5 to $V_{CC} + 0.5$ V

Input current on any pin during overload condition – 10 to + 10 mA

Absolute sum of all input currents during overload condition |100 mA|

Power dissipation..... 1 W

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the SAB 80C166 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (Controller Characteristics):

The logic of the SAB 80C166 will provide signals with the respective timing characteristics.

SR (System Requirement):

The external system must provide signals with the respective timing characteristics to the SAB 80C166.

DC Characteristics

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$
 $T_A = 0\text{ to }+70\text{ }^\circ\text{C}$ for SAB 83C166-5M, SAB 80C166-M
 $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ for SAB 83C166-5M-T3, SAB 80C166-M-T3

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|--|--------------------------|--------------------|----------------------|---------------|---|
| | | min. | max. | | |
| Input low voltage | V_{IL} SR | -0.5 | $0.2 V_{CC} - 0.1$ | V | - |
| Input high voltage (all except \overline{RSTIN} and XTAL1) | V_{IH} SR | $0.2 V_{CC} + 0.9$ | $V_{CC} + 0.5$ | V | - |
| Input high voltage \overline{RSTIN} | V_{IH1} SR | $0.6 V_{CC}$ | $V_{CC} + 0.5$ | V | - |
| Input high voltage XTAL1 | V_{IH2} SR | $0.7 V_{CC}$ | $V_{CC} + 0.5$ | V | - |
| Output low voltage (Port 0, Port 1, Port 4, ALE, \overline{RD} , \overline{WR} , BHE, CLKOUT, RSTOUT) | V_{OL} CC | - | 0.45 | V | $I_{OL} = 2.4\text{ mA}$ |
| Output low voltage (all other outputs) | V_{OL1} CC | - | 0.45 | V | $I_{OL1} = 1.6\text{ mA}$ |
| Output high voltage (Port 0, Port 1, Port 4, ALE, \overline{RD} , \overline{WR} , BHE, CLKOUT, RSTOUT) | V_{OH} CC | $0.9 V_{CC} - 2.4$ | - | V | $I_{OH} = -500\text{ }\mu\text{A}$ $I_{OH} = -2.4\text{ mA}$ |
| Output high voltage (all other outputs) | V_{OH1} CC | $0.9 V_{CC} - 2.4$ | - | V V | $I_{OH} = -250\text{ }\mu\text{A}$ $I_{OH} = -1.6\text{ mA}$ |
| Input leakage current (Port 5) ¹⁾ | I_{OZ1} CC | - | ± 200 | nA | $0\text{ V} < V_{IN} < V_{CC}$ |
| Input leakage current (all other) | I_{OZ2} CC | - | ± 500 | nA | $0\text{ V} < V_{IN} < V_{CC}$ |
| \overline{RSTIN} pullup resistor | R_{RST} CC | 50 | 150 | k Ω | - |
| Read inactive current ⁴⁾ | I_{RH} ²⁾ | - | -40 | μA | $V_{OUT} = V_{OHmin}$ |
| Read active current ⁴⁾ | I_{RL} ³⁾ | -500 | - | μA | $V_{OUT} = V_{OLmax}$ |
| ALE inactive current ⁴⁾ | I_{ALEL} ²⁾ | - | 150 | μA | $V_{OUT} = V_{OLmax}$ |
| ALE active current ⁴⁾ | I_{ALEH} ³⁾ | 2100 | - | μA | $V_{OUT} = V_{OHmin}$ |
| XTAL1 input current | I_{IL} CC | - | ± 20 | μA | $0\text{ V} < V_{IN} < V_{CC}$ |
| Pin capacitance ⁵⁾ (digital inputs/outputs) | C_{IO} CC | - | 10 | pF | $f = 1\text{ MHz}$ $T_A = 25\text{ }^\circ\text{C}$ |
| Power supply current | I_{CC} | - | $50 + 5 * f_{CPU}$ | mA | Reset active f_{CPU} in [MHz] ⁶⁾ |
| Idle mode supply current | I_{ID} | - | $30 + 1.5 * f_{CPU}$ | mA | f_{CPU} in [MHz] ⁶⁾ |
| Power-down mode supply current | I_{PD} | - | 50 | μA | $V_{CC} = 5.5\text{ V}$ ⁷⁾ |

Notes

- 1) This specification does not apply to the analog input (Port 5.x) which is currently converted.
- 2) The maximum current may be drawn while the respective signal line remains inactive.
- 3) The minimum current must be drawn in order to drive the respective signal line active.
- 4) This specification is only valid during Reset, or during Hold-mode.
- 5) Not 100% tested, guaranteed by design characterization.
- 6) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{CCmax} and 20 MHz CPU clock with all outputs open.
- 7) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{CC} - 0.1$ V to V_{CC} , $V_{REF} = 0$ V, all outputs (including pins configured as outputs) disconnected.
A voltage of $V_{CC} \geq 2.5$ V is sufficient to retain the content of the internal RAM during power down mode.

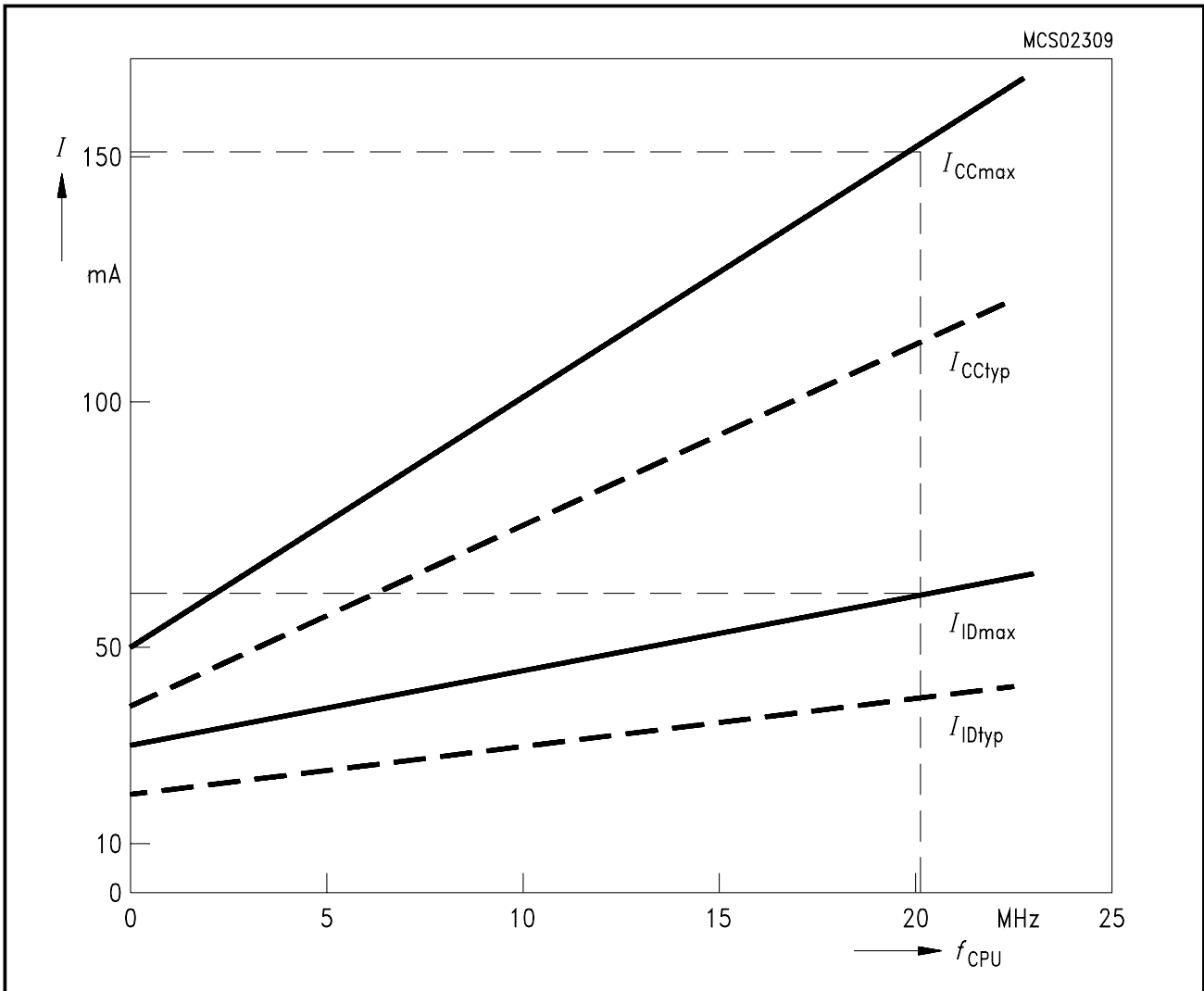


Figure 8
Supply/Idle Current as a Function of Operating Frequency

A/D Converter Characteristics

$$V_{CC} = 5 \text{ V} \pm 10 \% ; \quad V_{SS} = 0 \text{ V}$$

$$T_A = 0 \text{ to } +70 \text{ }^\circ\text{C} \quad \text{for SAB 83C166-5M, SAB 80C166-M}$$

$$T_A = -40 \text{ to } +85 \text{ }^\circ\text{C} \quad \text{for SAB 83C166-5M-T3, SAB 80C166-M-T3}$$

$$4.0 \text{ V} \leq V_{AREF} \leq V_{CC} + 0.1 \text{ V}; \quad V_{SS} - 0.1 \text{ V} \leq V_{AGND} \leq V_{SS} + 0.2 \text{ V}$$

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---------------|--------------|--------------------------|------------|-----------------------------------|
| | | min. | max. | | |
| Analog input voltage range | V_{AIN} SR | V_{AGND} | V_{AREF} | V | 1) |
| Sample time | t_S CC | – | $2 t_{SC}$ | | 2) 4) |
| Conversion time | t_C CC | – | $10 t_{CC} + t_S + 4TCL$ | | 3) 4) |
| Total unadjusted error | TUE CC | – | ± 2 | LSB | 5) |
| Internal resistance of reference voltage source | R_{AREF} SR | – | $t_{CC} / 250 - 0.25$ | k Ω | t_{CC} in [ns] ^{6) 7)} |
| Internal resistance of analog source | R_{ASRC} SR | – | $t_S / 500 - 0.25$ | k Ω | t_S in [ns] ^{2) 7)} |
| ADC input capacitance | C_{AIN} CC | – | 50 | pF | 7) |

Notes

- 1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.
- 2) During the sample time the input capacitance C_1 can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitors to reach their final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result. The value for the sample clock is $t_{SC} = TCL * 32$.
- 3) This parameter includes the sample time t_S , the time for determining the digital result and the time to load the result register with the conversion result. The value for the conversion clock is $t_{CC} = TCL * 32$.
- 4) This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.
- 5) TUE is tested at $V_{AREF} = 5.0\text{V}$, $V_{AGND} = 0 \text{ V}$, $V_{CC} = 4.8 \text{ V}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.
- 6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitors to reach their respective voltage level within t_{CC} . The maximum internal resistance results from the CPU clock period.
- 7) Not 100% tested, guaranteed by design characterization.

Testing Waveforms

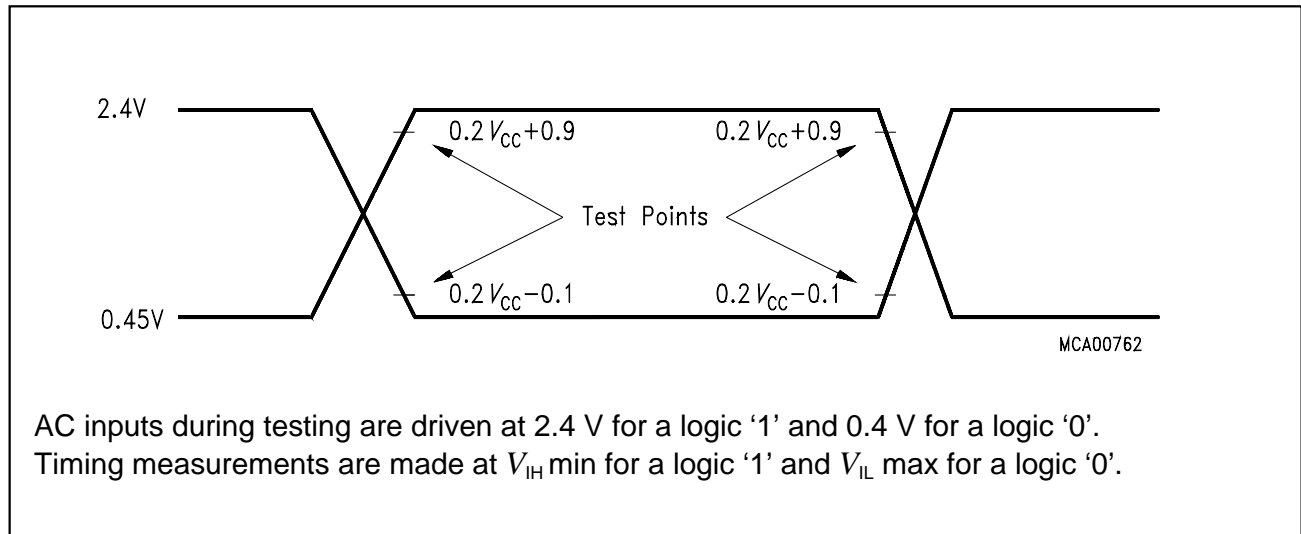


Figure 9
Input Output Waveforms

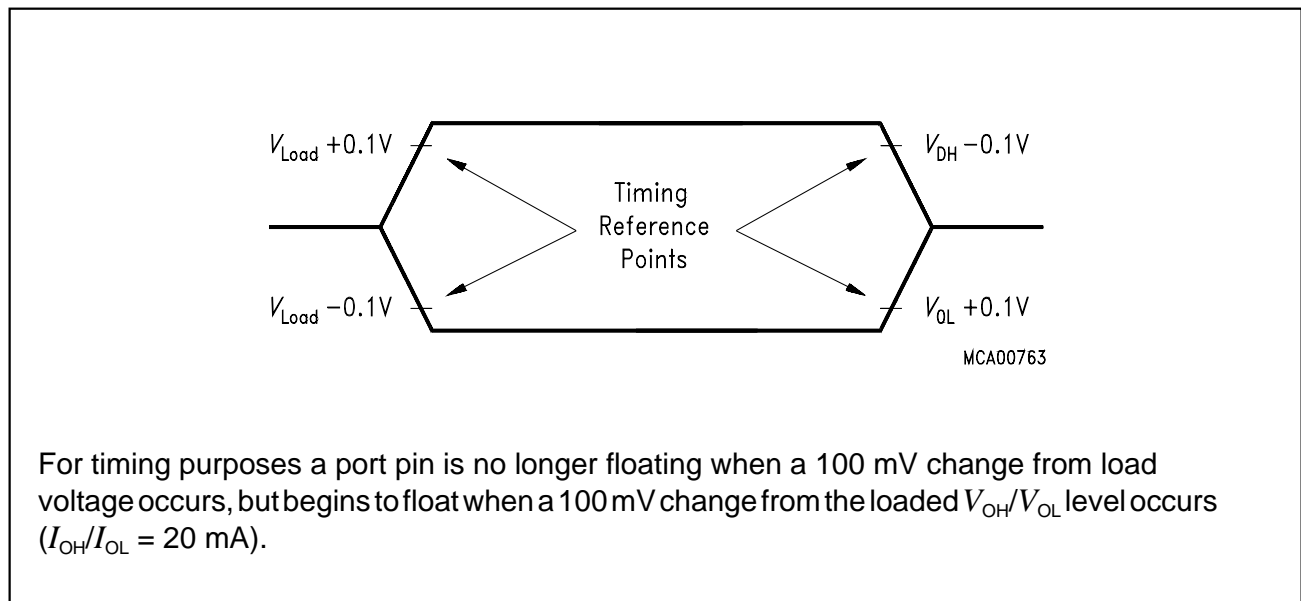


Figure 10
Float Waveforms

AC Characteristics

External Clock Drive XTAL1

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^\circ\text{C}$ for SAB 83C166-5M, SAB 80C166-M

$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ for SAB 83C166-5M-T3, SAB 80C166-M-T3

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|-------------------|----------|----------------------------|------|--|------|------|
| | | min. | max. | min. | max. | |
| Oscillator period | TCL SR | 25 | 25 | 25 | 500 | ns |
| High time | t_1 SR | 6 | – | 6 | – | ns |
| Low time | t_2 SR | 6 | – | 6 | – | ns |
| Rise time | t_3 SR | – | 5 | – | 5 | ns |
| Fall time | t_4 SR | – | 5 | – | 5 | ns |

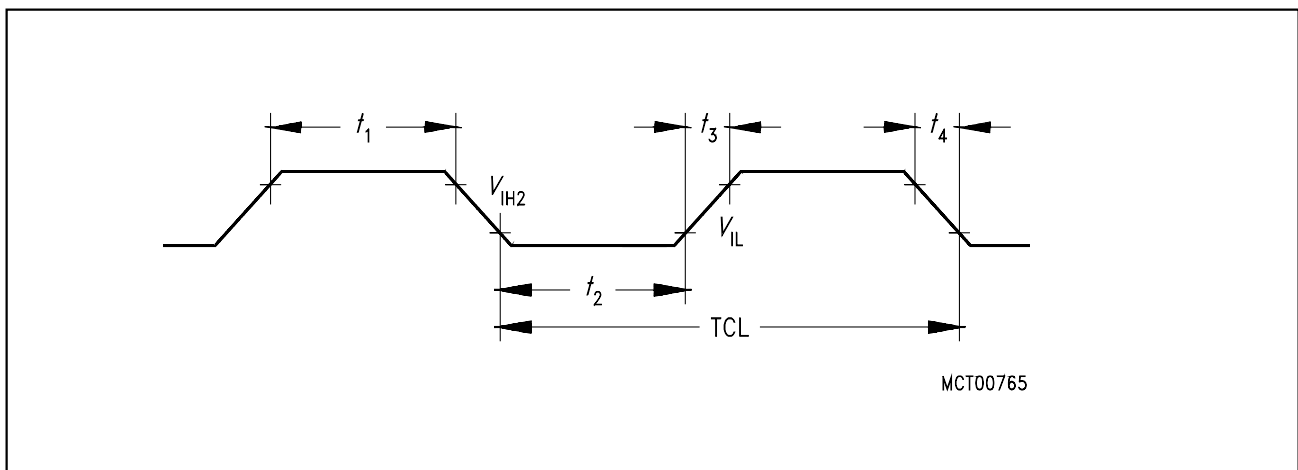


Figure 11
External Clock Drive XTAL1

Memory Cycle Variables

The timing tables below use three variables which are derived from registers SYSCON and BUSCON1 and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

| Description | Symbol | Values |
|------------------------------|--------|--------------------------------------|
| ALE Extension | t_A | $TCL * \langle ALECTL \rangle$ |
| Memory Cycle Time Waitstates | t_C | $2TCL * (15 - \langle MCTC \rangle)$ |
| Memory Tristate Time | t_F | $2TCL * (1 - \langle MTTC \rangle)$ |

AC Characteristics (cont'd)

Multiplexed Bus

$$V_{CC} = 5\text{ V} \pm 10\%; \quad V_{SS} = 0\text{ V}$$

$$T_A = 0\text{ to }+70\text{ }^\circ\text{C} \quad \text{for SAB 83C166-5M, SAB 80C166-M}$$

$$T_A = -40\text{ to }+85\text{ }^\circ\text{C} \quad \text{for SAB 83C166-5M-T3, SAB 80C166-M-T3}$$

$$C_L \text{ (for Port 0, Port 1, Port 4, ALE, } \overline{\text{RD}}, \overline{\text{WR}}, \overline{\text{BHE}}, \text{CLKOUT)} = 100\text{ pF}$$

$$\text{ALE cycle time} = 6\text{ TCL} + 2t_A + t_C + t_F \text{ (150 ns at 20-MHz CPU clock without waitstates)}$$

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|--|-------------|----------------------------|------------------------|--|--------------------------------------|------|
| | | min. | max. | min. | max. | |
| ALE high time | t_5 CC | $15 + t_A$ | – | $\text{TCL} - 10 + t_A$ | – | ns |
| Address setup to ALE | t_6 CC | $10 + t_A$ | – | $\text{TCL} - 15 + t_A$ | – | ns |
| Address hold after ALE | t_7 CC | $15 + t_A$ | – | $\text{TCL} - 10 + t_A$ | – | ns |
| ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay) | t_8 CC | $15 + t_A$ | – | $\text{TCL} - 10 + t_A$ | – | ns |
| ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay) | t_9 CC | $-10 + t_A$ | – | $-10 + t_A$ | – | ns |
| Address float after $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay) | t_{10} CC | – | 5 | – | 5 | ns |
| Address float after $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay) | t_{11} CC | – | 30 | – | $\text{TCL} + 5$ | ns |
| $\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (with RW-delay) | t_{12} CC | $40 + t_C$ | – | $2\text{TCL} - 10$ $+ t_C$ | – | ns |
| $\overline{\text{RD}}$ $\overline{\text{WR}}$ low time (no RW-delay) | t_{13} CC | $65 + t_C$ | – | $3\text{TCL} - 10$ $+ t_C$ | – | ns |
| $\overline{\text{RD}}$ to valid data in (with RW-delay) | t_{14} SR | – | $30 + t_C$ | – | $2\text{TCL} - 20$ $+ t_C$ | ns |
| $\overline{\text{RD}}$ to valid data in (no RW-delay) | t_{15} SR | – | $55 + t_C$ | – | $3\text{TCL} - 20$ $+ t_C$ | ns |
| ALE low to valid data in | t_{16} SR | – | 55 $+ t_A + t_C$ | – | $3\text{TCL} - 20$ $+ t_A + t_C$ | ns |
| Address to valid data in | t_{17} SR | – | 75 $+ 2t_A + t_C$ | – | $4\text{TCL} - 25$ $+ 2t_A + t_C$ | ns |
| Data hold after $\overline{\text{RD}}$ rising edge | t_{18} SR | 0 | – | 0 | – | ns |
| Data float after $\overline{\text{RD}}$ | t_{19} SR | – | $35 + t_F$ | – | $2\text{TCL} - 15$ $+ t_F$ | ns |
| Data valid to $\overline{\text{WR}}$ | t_{22} CC | $35 + t_C$ | – | $2\text{TCL} - 15$ $+ t_C$ | – | ns |

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|--|-------------|----------------------------|------|--|------|------|
| | | min. | max. | min. | max. | |
| Data hold after \overline{WR} | t_{23} CC | $35 + t_F$ | – | $2TCL - 15 + t_F$ | – | ns |
| ALE rising edge after \overline{RD} , \overline{WR} | t_{25} CC | $35 + t_F$ | – | $2TCL - 15 + t_F$ | – | ns |
| Address hold after \overline{RD} , \overline{WR} | t_{27} CC | $35 + t_F$ | – | $2TCL - 15 + t_F$ | – | ns |

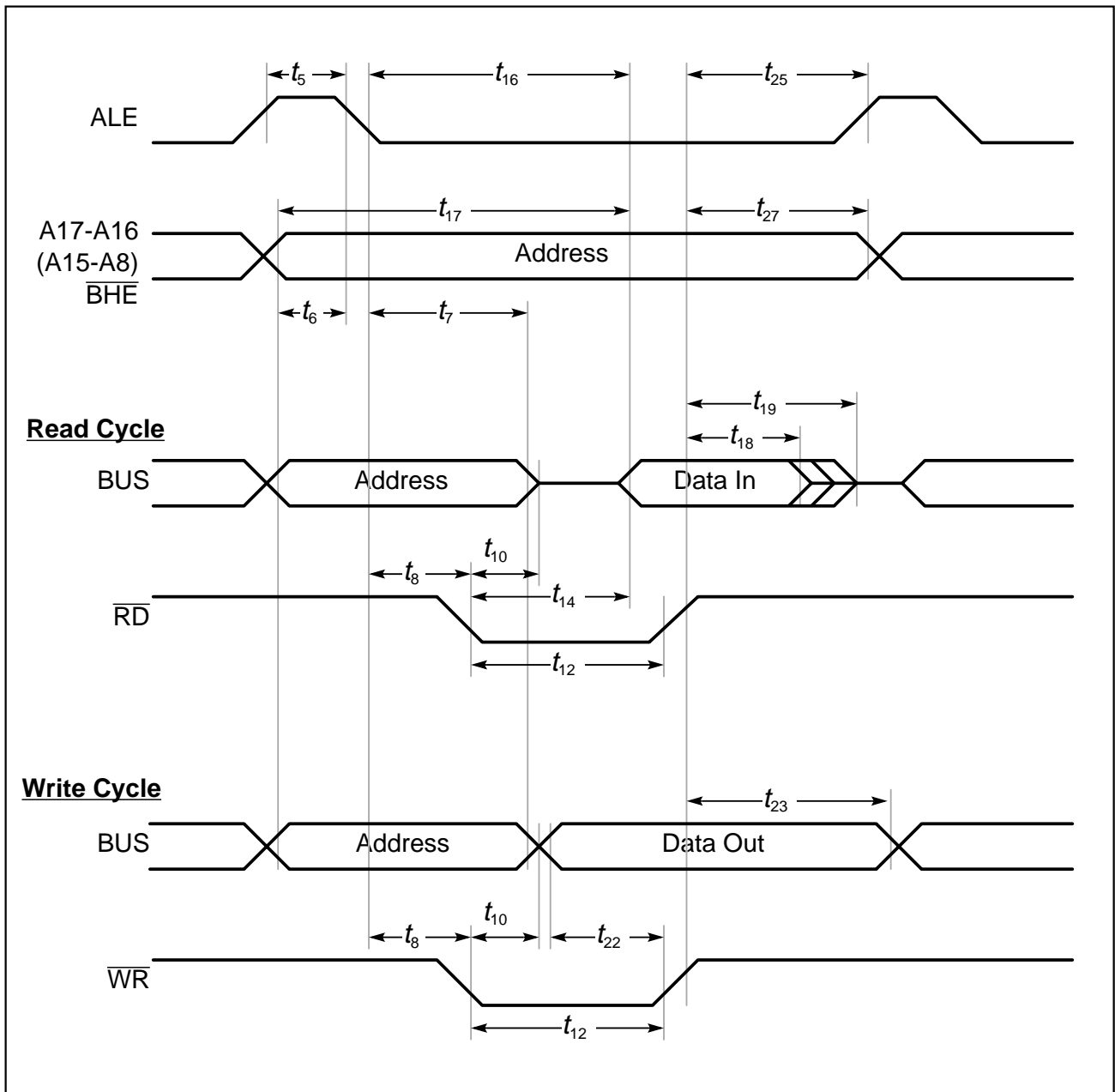


Figure 12-1
External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

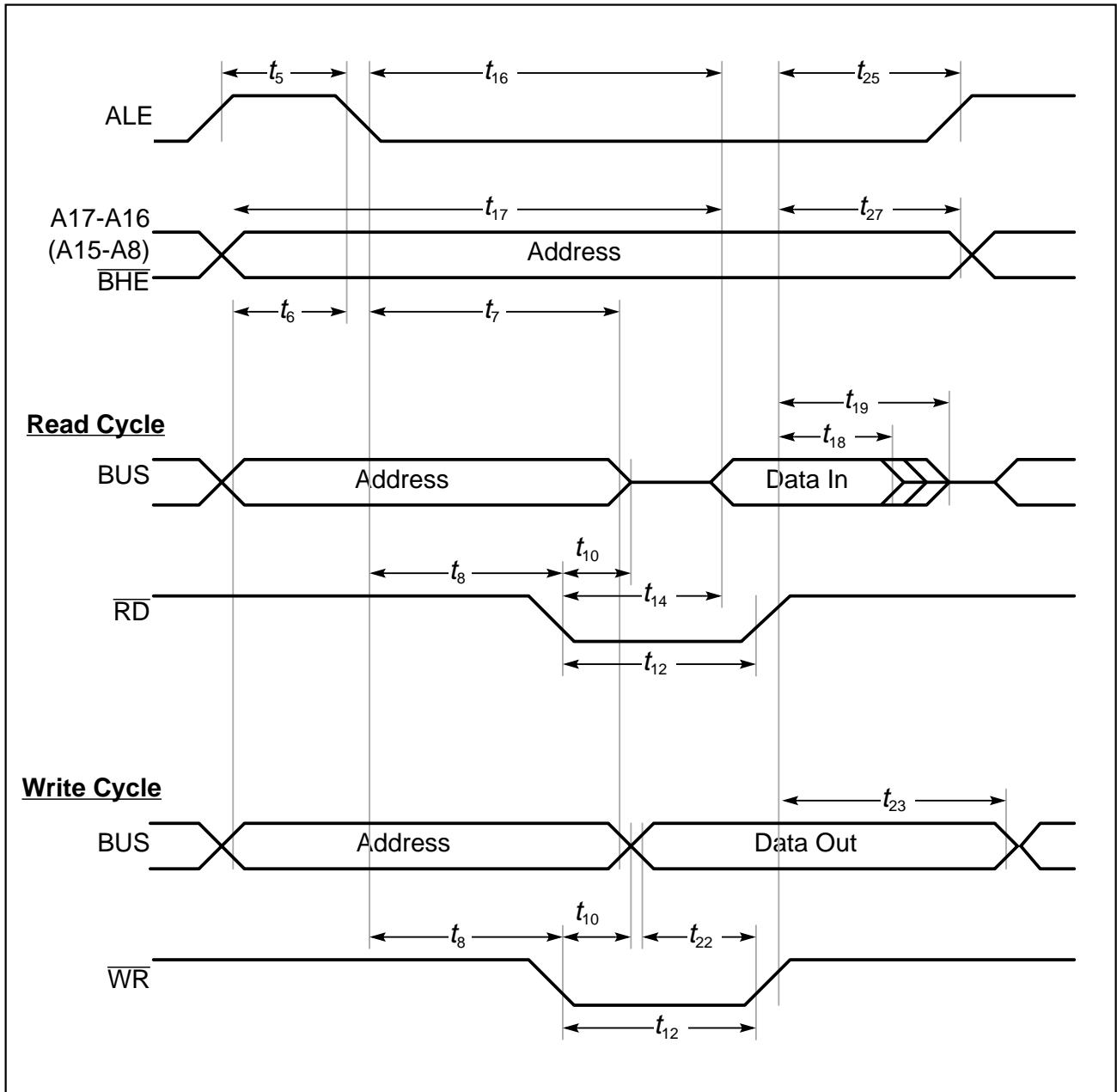


Figure 12-2
External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE

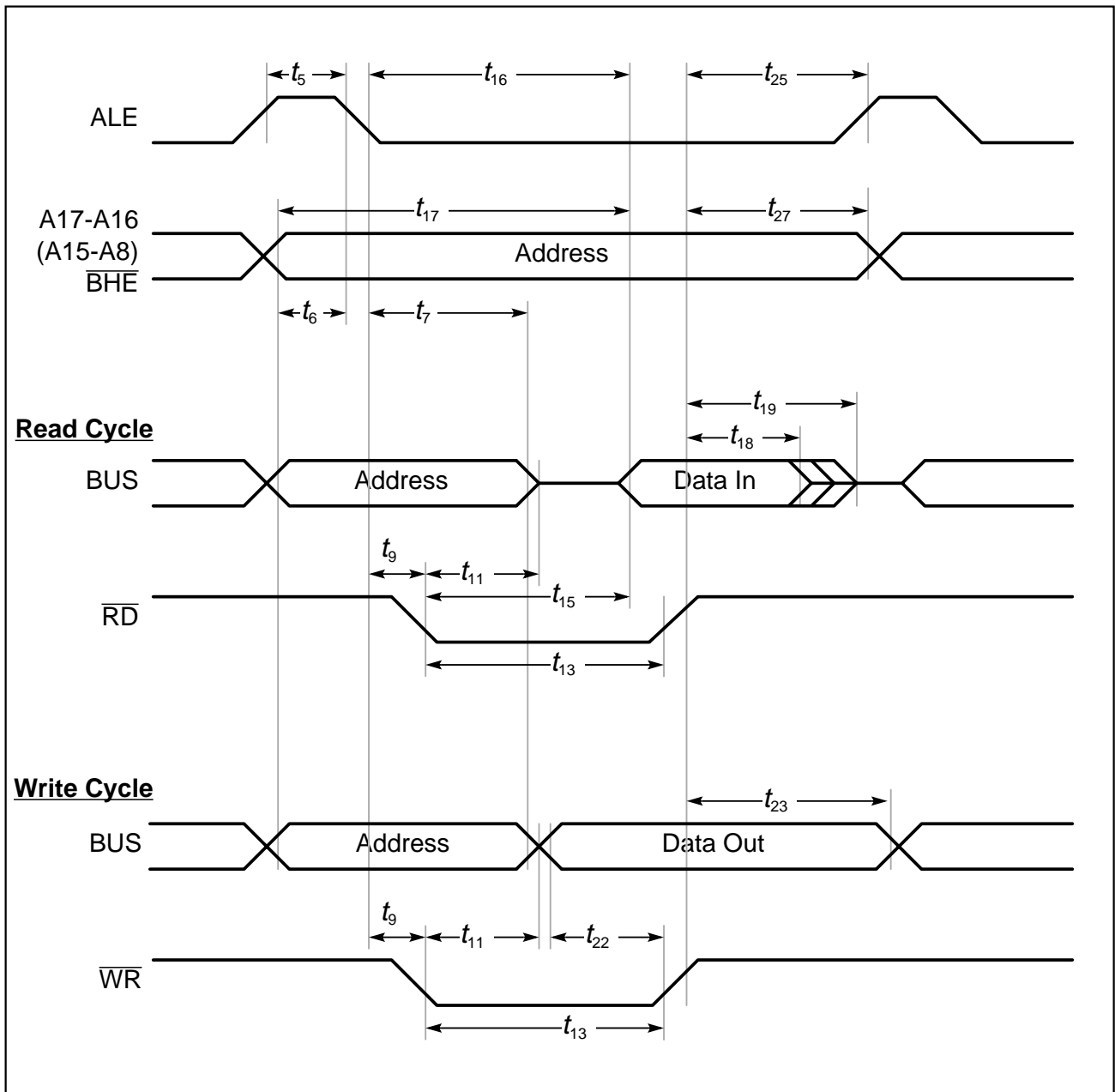


Figure 12-3
External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE

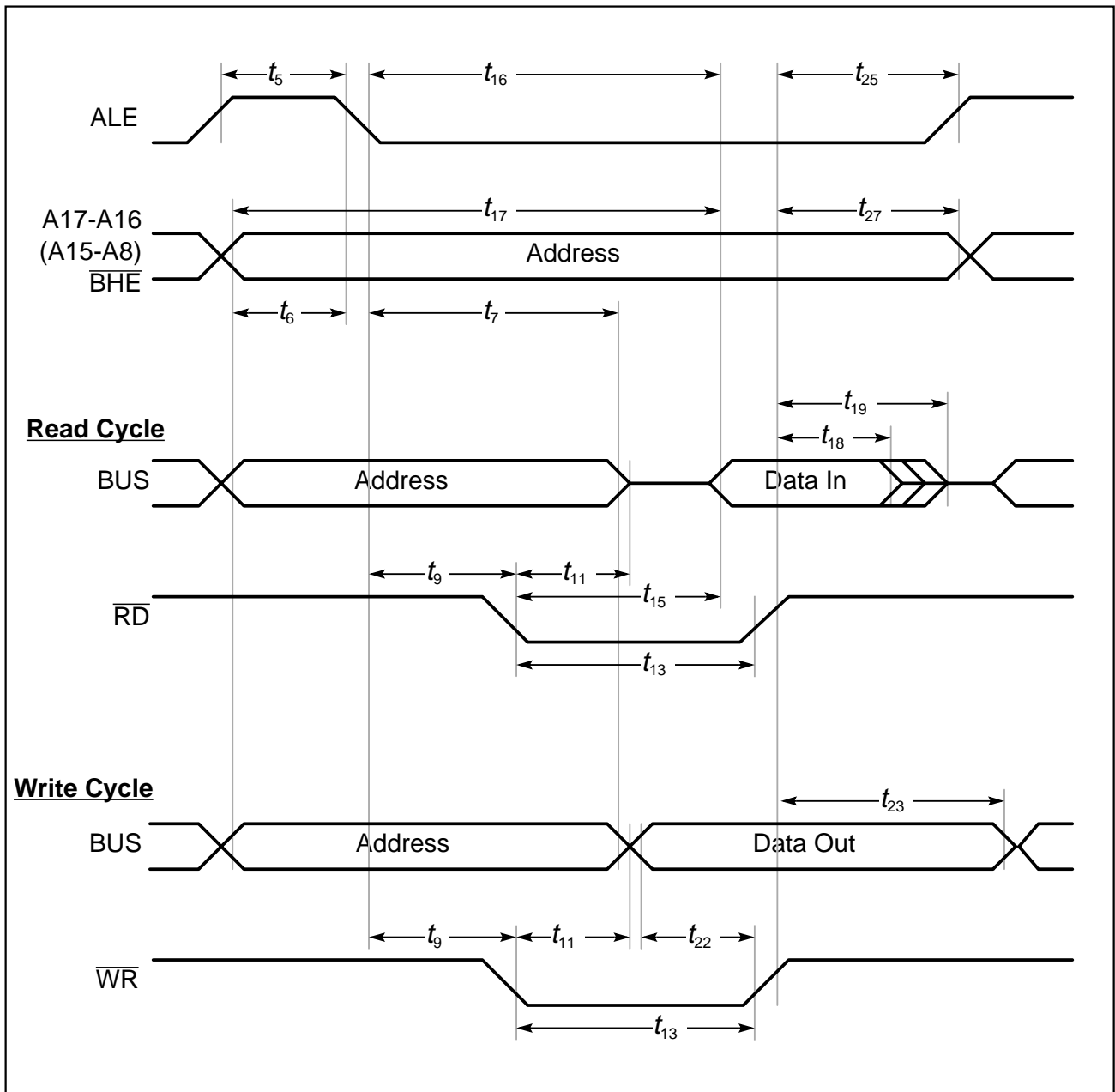


Figure 12-4
External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics (cont'd)

Demultiplexed Bus

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^\circ\text{C}$ for SAB 83C166-5M, SAB 80C166-M

$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ for SAB 83C166-5M-T3, SAB 80C166-M-T3

C_L (for Port 0, Port 1, Port 4, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT) = 100 pF

ALE cycle time = $4\text{ TCL} + 2t_A + t_C + t_F$ (100 ns at 20-MHz CPU clock without waitstates)

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|--|-------------|----------------------------|-------------------|--|---------------------------------|------|
| | | min. | max. | min. | max. | |
| ALE high time | t_5 CC | $15 + t_A$ | – | $\text{TCL} - 10 + t_A$ | – | ns |
| Address setup to ALE | t_6 CC | $10 + t_A$ | – | $\text{TCL} - 15 + t_A$ | – | ns |
| ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay) | t_8 CC | $15 + t_A$ | – | $\text{TCL} - 10 + t_A$ | – | ns |
| ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay) | t_9 CC | $-10 + t_A$ | – | $-10 + t_A$ | – | ns |
| $\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (with RW-delay) | t_{12} CC | $40 + t_C$ | – | $2\text{TCL} - 10 + t_C$ | – | ns |
| $\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (no RW-delay) | t_{13} CC | $65 + t_C$ | – | $3\text{TCL} - 10 + t_C$ | – | ns |
| $\overline{\text{RD}}$ to valid data in (with RW-delay) | t_{14} SR | – | $30 + t_C$ | – | $2\text{TCL} - 20 + t_C$ | ns |
| $\overline{\text{RD}}$ to valid data in (no RW-delay) | t_{15} SR | – | $55 + t_C$ | – | $3\text{TCL} - 20 + t_C$ | ns |
| ALE low to valid data in | t_{16} SR | – | $55 + t_A + t_C$ | – | $3\text{TCL} - 20 + t_A + t_C$ | ns |
| Address to valid data in | t_{17} SR | – | $75 + 2t_A + t_C$ | – | $4\text{TCL} - 25 + 2t_A + t_C$ | ns |
| Data hold after $\overline{\text{RD}}$ rising edge | t_{18} SR | 0 | – | 0 | – | ns |
| Data float after $\overline{\text{RD}}$ rising edge (with RW-delay) | t_{20} SR | – | $35 + t_F$ | – | $2\text{TCL} - 15 + t_F$ | ns |
| Data float after $\overline{\text{RD}}$ rising edge (no RW-delay) | t_{21} SR | – | $15 + t_F$ | – | $\text{TCL} - 10 + t_F$ | ns |
| Data valid to $\overline{\text{WR}}$ | t_{22} CC | $35 + t_C$ | – | $2\text{TCL} - 15 + t_C$ | – | ns |
| Data hold after $\overline{\text{WR}}$ | t_{24} CC | $15 + t_F$ | – | $\text{TCL} - 10 + t_F$ | – | ns |

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|--|-------------|----------------------------|------|--|------|------|
| | | min. | max. | min. | max. | |
| ALE rising edge after \overline{RD} , \overline{WR} | t_{26} CC | $-10 + t_F$ | – | $-10 + t_F$ | – | ns |
| Address hold after \overline{RD} , \overline{WR} | t_{28} CC | $0 + t_F$ | – | $0 + t_F$ | – | ns |

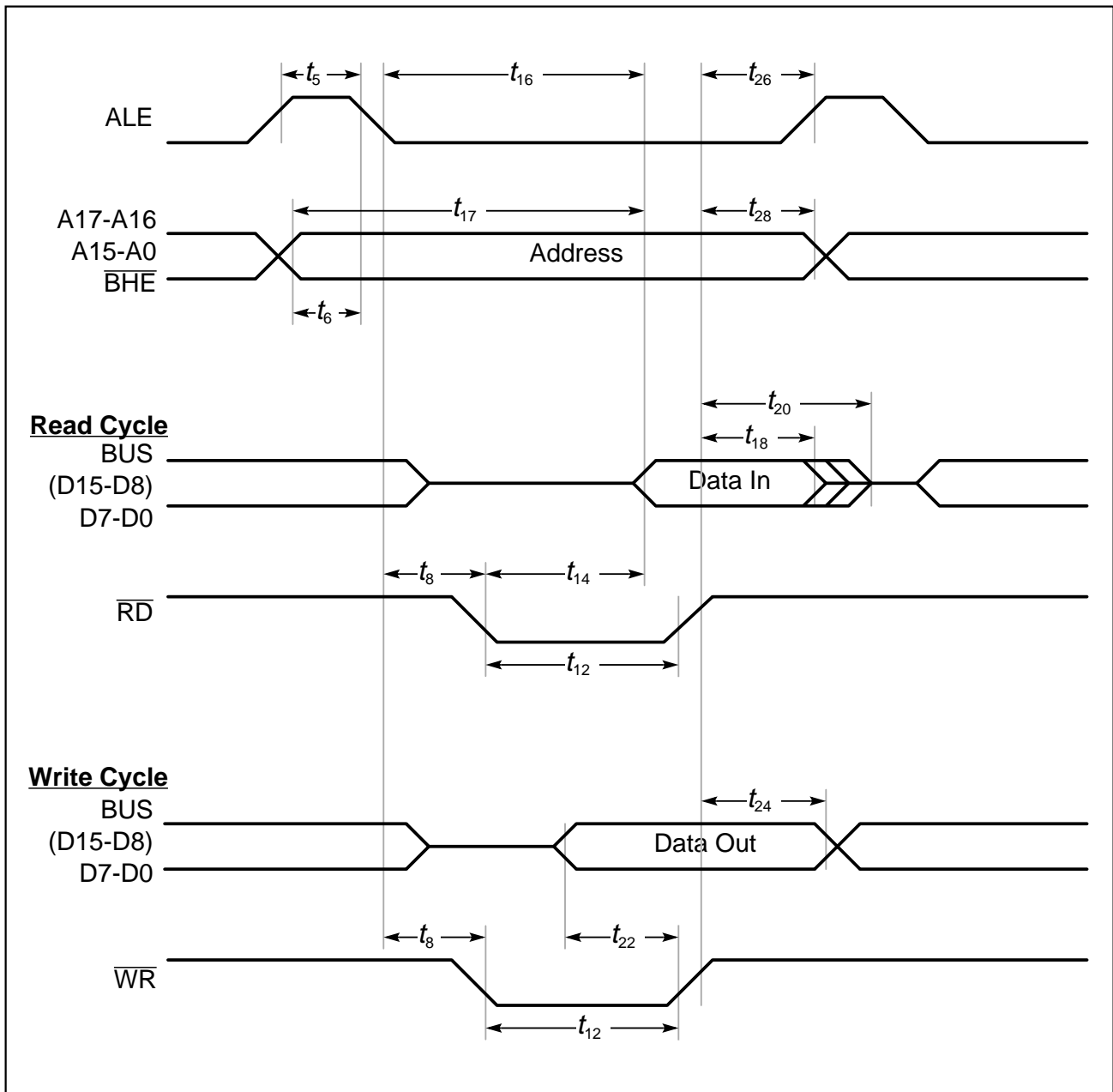


Figure 13-1
External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE

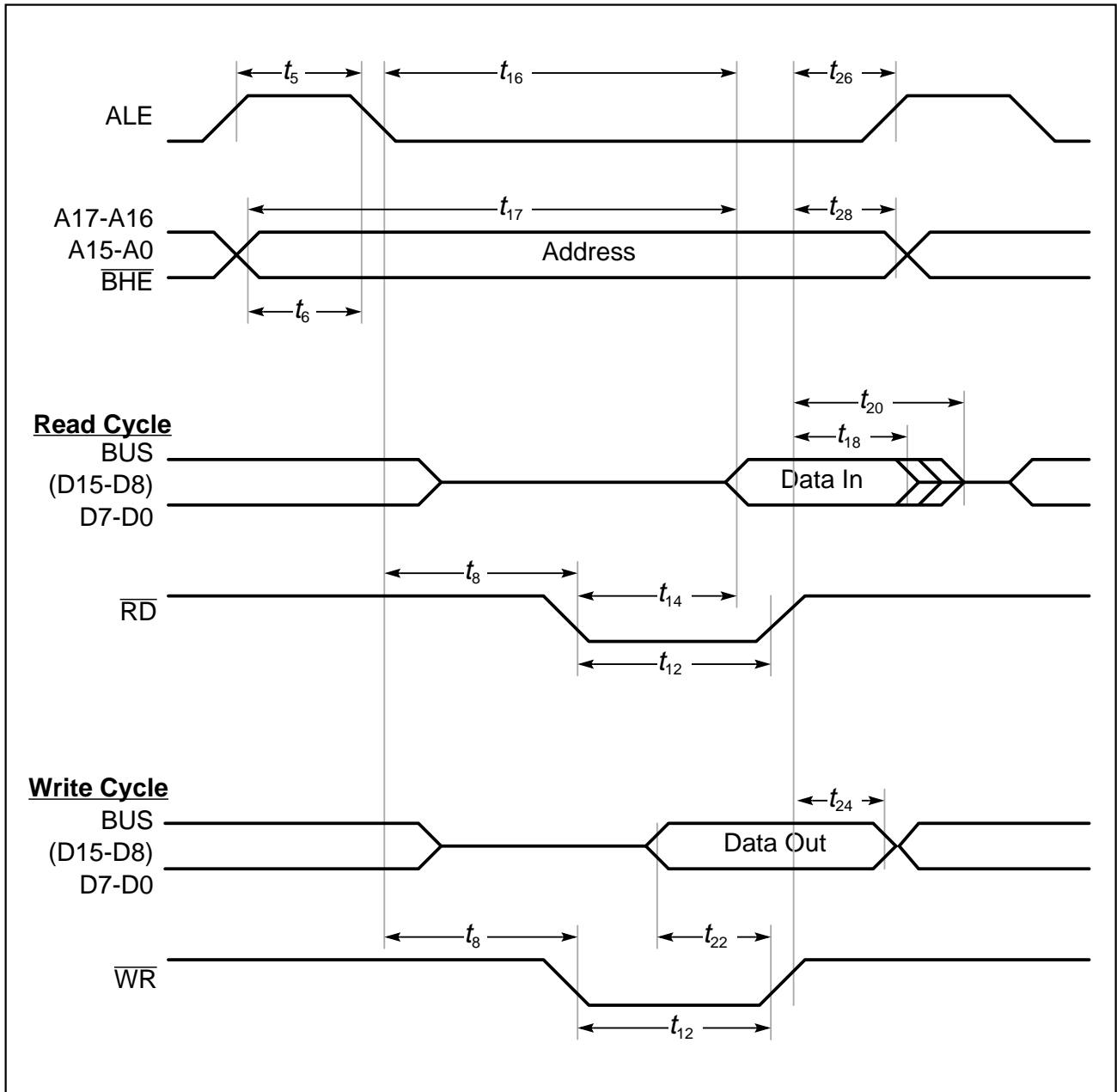


Figure 13-2
External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

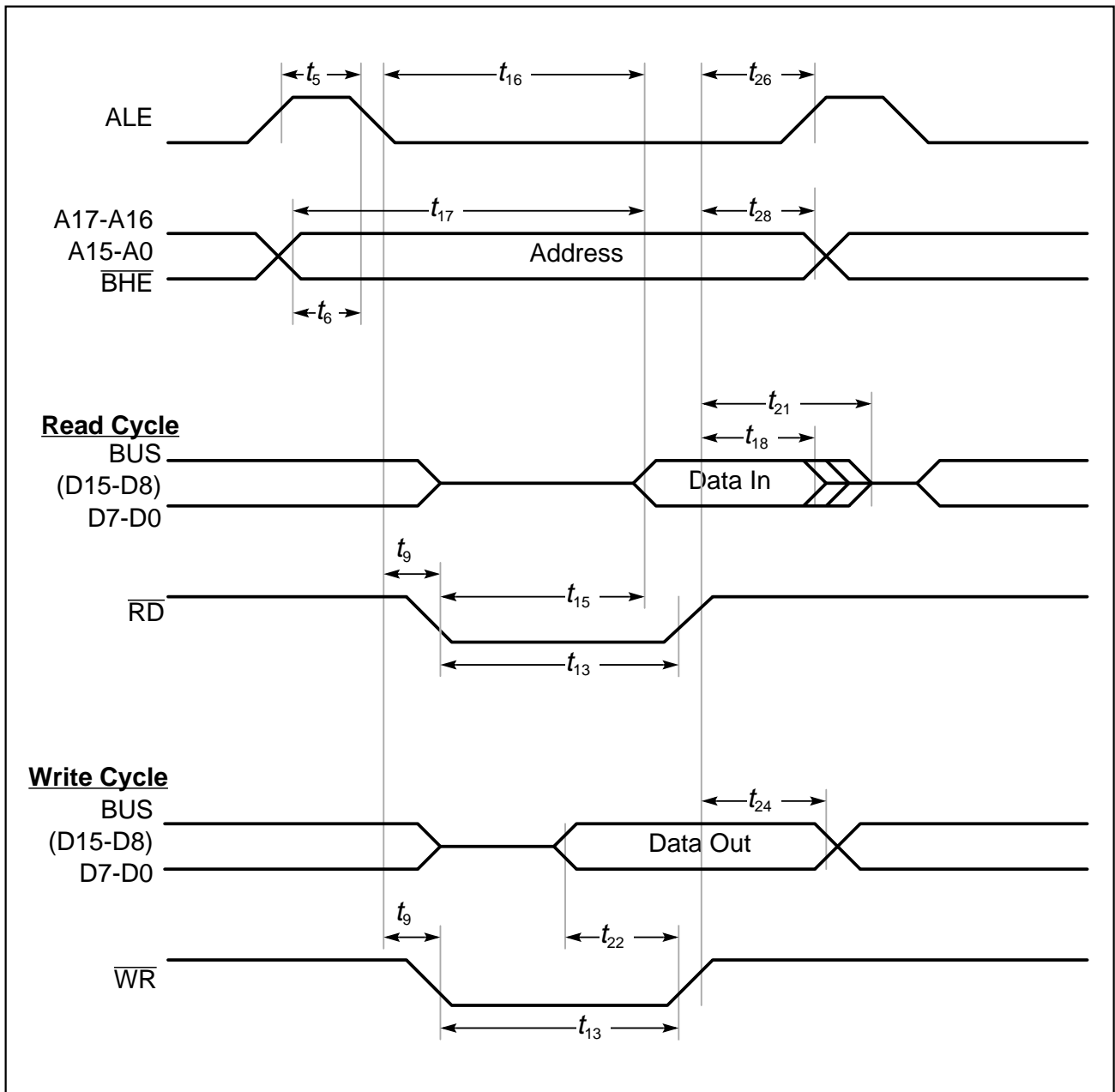


Figure 13-3
External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

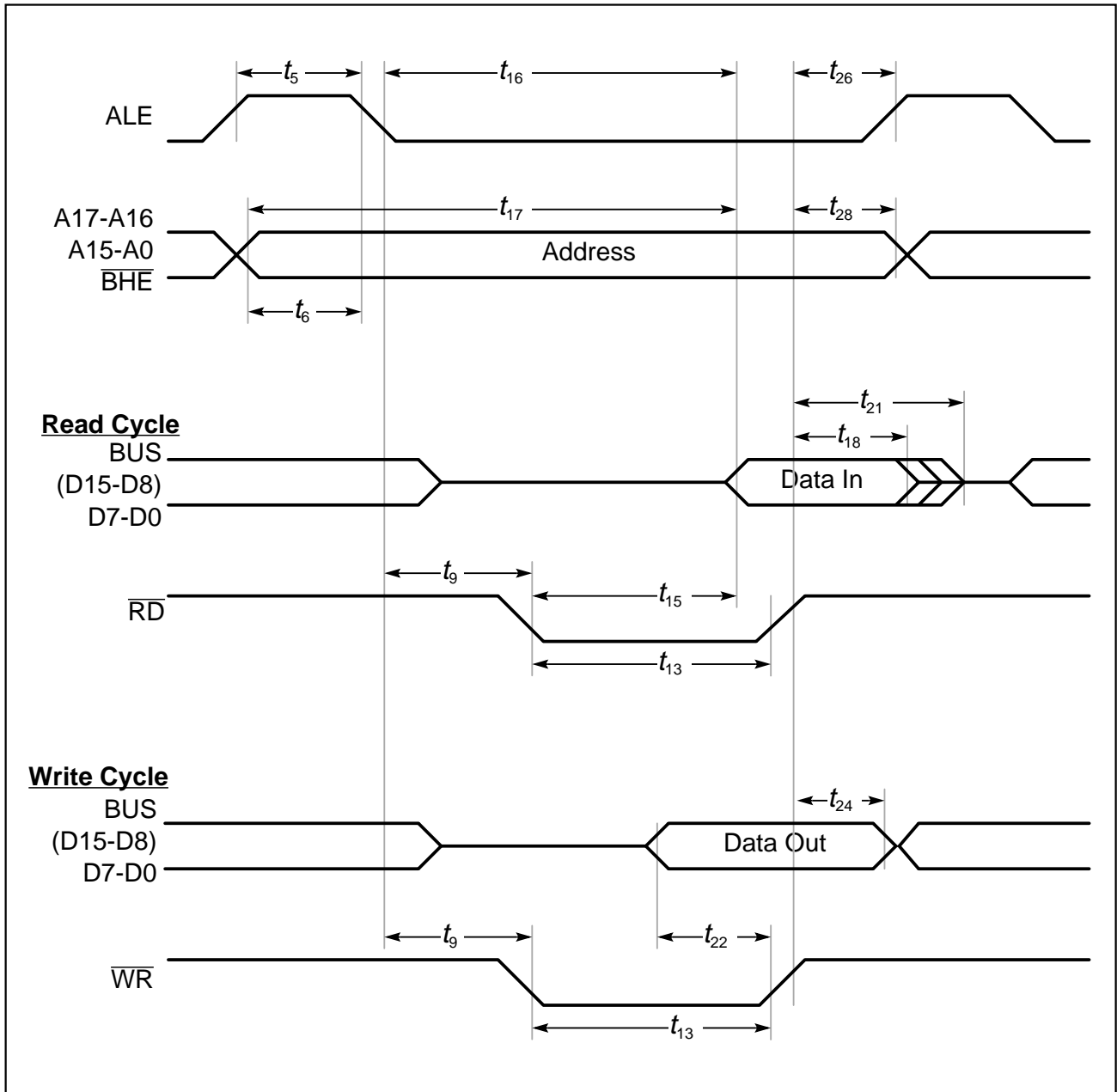


Figure 13-4
External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics (cont'd)

CLKOUT and READY

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^\circ\text{C}$ for SAB 83C166-5M, SAB 80C166-M

$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ for SAB 83C166-5M-T3, SAB 80C166-M-T3

C_L (for Port 0, Port 1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT) = 100 pF

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|---|-------------|----------------------------|-----------------------------------|--|---|------|
| | | min. | max. | min. | max. | |
| CLKOUT cycle time | t_{29} CC | 50 | 50 | 2TCL | 2TCL | ns |
| CLKOUT high time | t_{30} CC | 20 | – | TCL – 5 | – | ns |
| CLKOUT low time | t_{31} CC | 15 | – | TCL – 10 | – | ns |
| CLKOUT rise time | t_{32} CC | – | 5 | – | 5 | ns |
| CLKOUT fall time | t_{33} CC | – | 5 | – | 5 | ns |
| CLKOUT rising edge to ALE falling edge | t_{34} CC | $0 + t_A$ | $10 + t_A$ | $0 + t_A$ | $10 + t_A$ | ns |
| Synchronous $\overline{\text{READY}}$ setup time to CLKOUT | t_{35} SR | 10 | – | 10 | – | ns |
| Synchronous $\overline{\text{READY}}$ hold time after CLKOUT | t_{36} SR | 10 | – | 10 | – | ns |
| Asynchronous $\overline{\text{READY}}$ low time | t_{37} SR | 65 | – | 2TCL + 15 | – | ns |
| Asynchronous $\overline{\text{READY}}$ setup time ¹⁾ | t_{58} SR | 20 | – | 20 | – | ns |
| Asynchronous $\overline{\text{READY}}$ hold time ¹⁾ | t_{59} SR | 0 | – | 0 | – | ns |
| Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) ²⁾ | t_{60} SR | 0 | $0 + 2t_A + t_F$ ²⁾ | 0 | TCL - 25 $+ 2t_A + t_F$ ²⁾ | ns |

Notes

- 1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.
- 2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating READY.

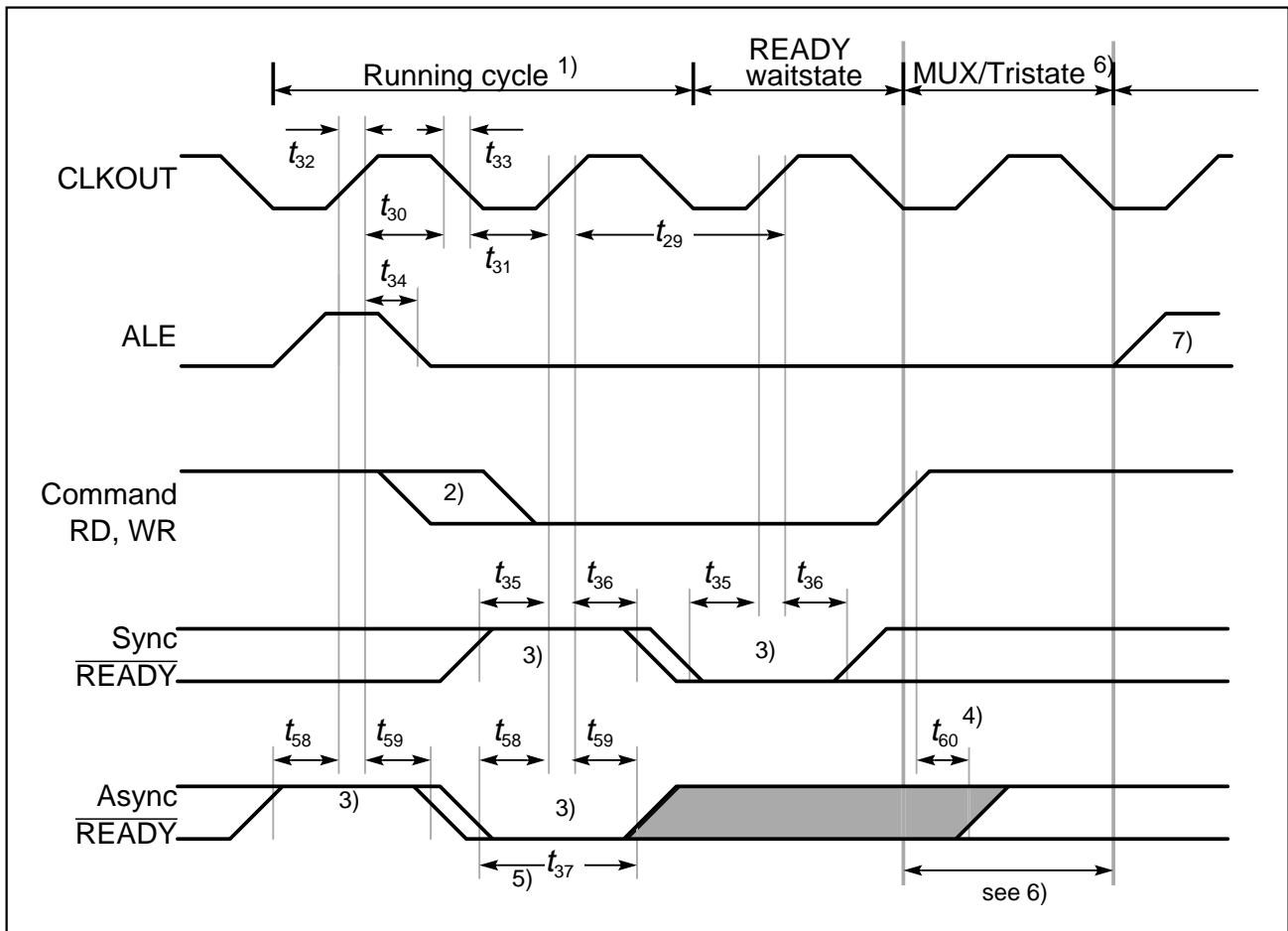


Figure 14
CLKOUT and $\overline{\text{READY}}$

Notes

- 1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
- 2) The leading edge of the respective command depends on RW-delay.
- 3) $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled waitstate, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
- 4) $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
- 5) If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if $\overline{\text{READY}}$ is removed in response to the command (see Note 4).
- 6) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
- 7) The next external bus cycle may start here.

AC Characteristics (cont'd)

External Bus Arbitration

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^\circ\text{C}$ for SAB 83C166-5M, SAB 80C166-M

$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ for SAB 83C166-5M-T3, SAB 80C166-M-T3

C_L (for Port 0, Port 1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT) = 100 pF

| Parameter | Symbol | | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|---|----------|----|----------------------------|------|--|------|------|
| | | | min. | max. | min. | max. | |
| HOLD input setup time to CLKOUT | t_{61} | SR | 20 | – | 20 | – | ns |
| CLKOUT to \overline{HLDA} high or \overline{BREQ} low delay | t_{62} | CC | – | 50 | – | 50 | ns |
| CLKOUT to \overline{HLDA} low or \overline{BREQ} high delay | t_{63} | CC | – | 50 | – | 50 | ns |
| Other signals release | t_{66} | CC | – | 25 | – | 25 | ns |
| Other signals drive | t_{67} | CC | -5 | 35 | -5 | 35 | ns |

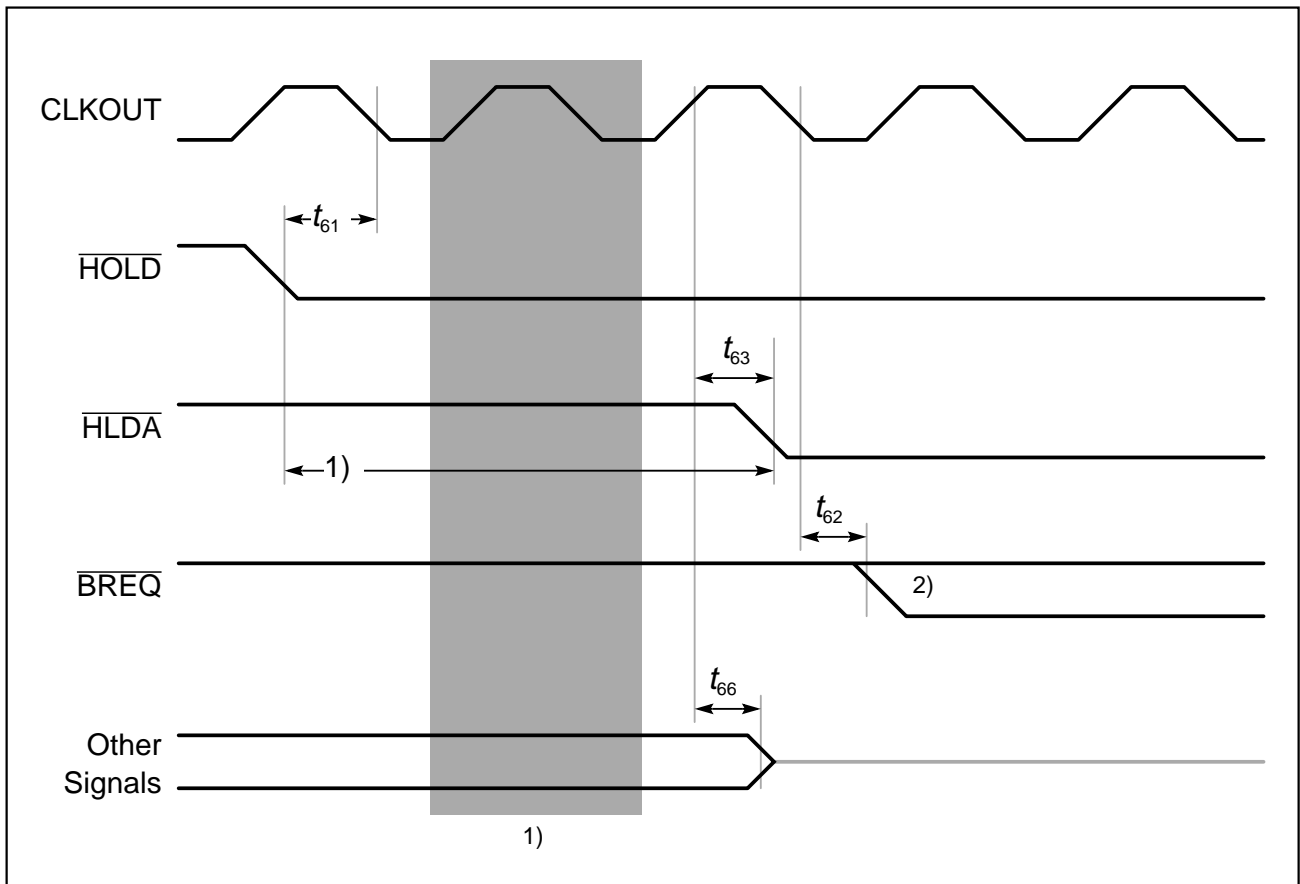


Figure 15
External Bus Arbitration, Releasing the Bus

Notes

- 1) The SAB 80C166 will complete the currently running bus cycle before granting bus access.
- 2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.

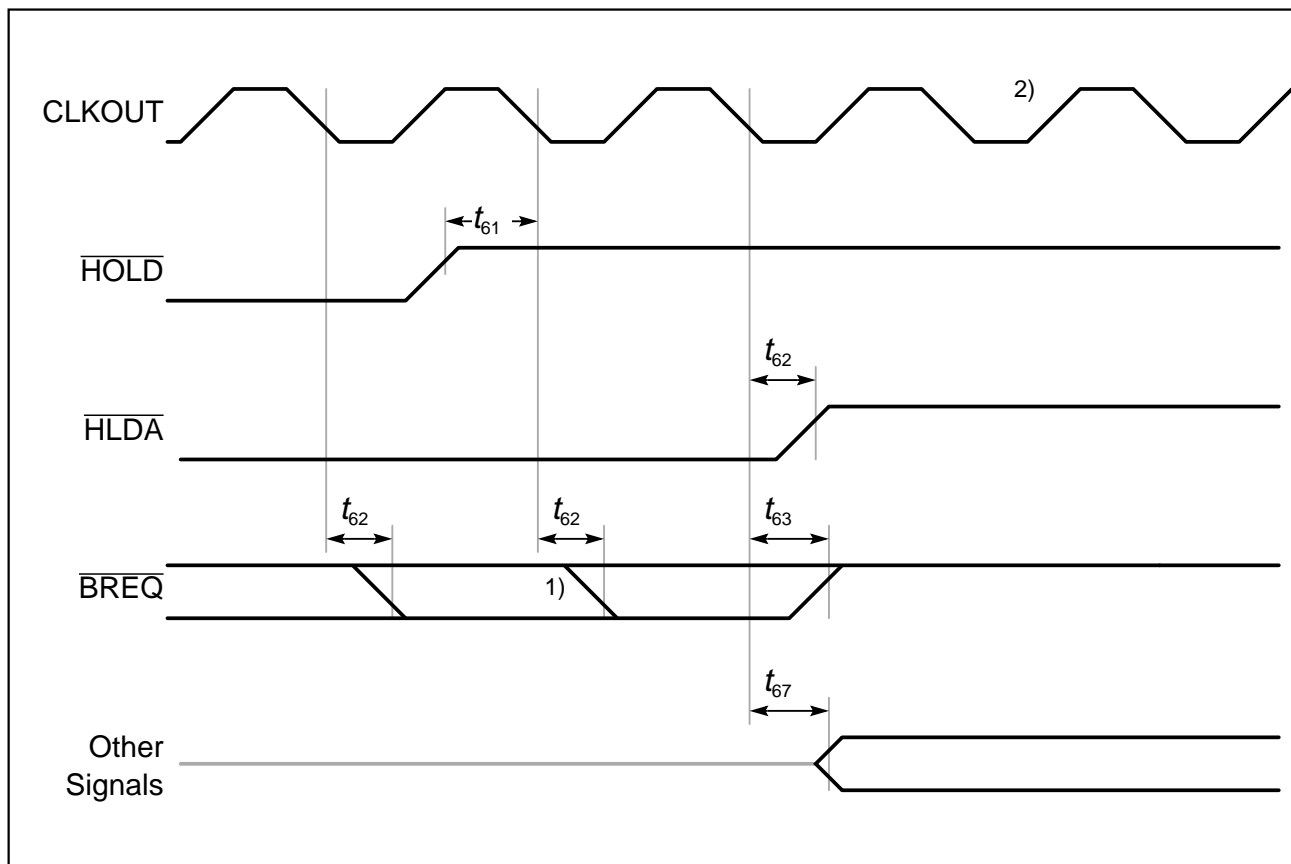


Figure 16
External Bus Arbitration, (Regaining the Bus)

Notes

- 1) This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence. Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high. Please note that $\overline{\text{HOLD}}$ may also be deactivated without the SAB 80C166 requesting the bus.
- 2) The next SAB 80C166 driven bus cycle may start here