Preliminary Version

SME5228BUPA-480

October 2000

UltraSPARC™-II CPU Module

DATA SHEET

480 MHz CPU, 8.0 Mbyte E-Cache

MODULE DESCRIPTION

The UltraSPARC™-II, 480 MHz CPU Module with an 8.0 Mbyte E-cache (SME5228BUPA-480), delivers high performance computing in a compact design. Based on the UltraSPARC™-II CPU, this module is designed using a small form factor board with an integrated external cache. It connects to the high bandwidth Ultra™ Port Architecture (UPA) bus via a high speed sturdy connector.

The UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache, can plug into any UPA 128M connector, saving system design costs and reducing the production time for new systems. Heatsinks are attached to components on the module board. Module design is geared towards ease of upgrade and field support.

Ease of System Design

- Small form factor board with integrated external cache and UPA interface
- JTAG boundary scan and performance instrumentation
- PCB provides a multi-power plane bypass, reducing systemboard design requirements

Performance

- High performance UltraSPARC™ CPU at 480 MHz
- Eight megabytes of external cache using high speed register-latch SRAMs
- Dedicated high bandwidth bus to processor

Glueless MP Support

- Supports one to four MP configuration
- Implements the high performance UPA interface
- Supports up to 32 Mbyte of external cache in a four-way MP system

Simplify System Qualifications by Complying with Industry and Government Standards

- Backwards compatibility with systems implementing a UPA interface
- Multi-layer PCB controls EMI radiation
- Edge connectors and ejectors
- Small form factor board
- On-board voltage regulator accepts 2.6 volts for the V_{DD_CORE}. It is compatible with existing systems.

CPU DESCRIPTION

UltraSPARC-II CPU

The UltraSPARC™-II, 480 MHz CPU is the second generation in the UltraSPARC™ s-Series microprocessor family.
A complete implementation of the SPARC™ V9 architecture, it has binary compatibility with all previous versions of the SPARC™ microprocessor family.

The UltraSPARC™-II, 480 MHz CPU is designed as a cost effective, scalable and reliable solution for high-end workstations and servers. Meeting the demands of mission critical enterprise computing, the UltraSPARC™-II, 480 MHz CPU runs enterprise applications requiring high data throughput. It is characterized by a high integer and floating point performance: optimally accelerating application performance, especially multimedia applications.

Delivering high memory bandwidth, media processing and raw compute performance, the UltraSPARC™-II, 480 MHz CPU incorporates innovative technologies which lower the cost of ownership.

CPU Features	*CPU Benefits*
Architecture	
•Thirty-two 64-bit integer registers	• 64-bit SPARC V9 architecture increases the network computing application's performance
•Superscalar/Superpipelined	• Allows applications to store data locally in the register files
•High performance memory interconnect	• Allows for multiple integer and floating point execution units leading to higher application performance
•Built-in Multiprocessing Capability	• Alleviating the bottleneck of bandwidth to main memory
•VIS multimedia accelerating instructions	• Delivering scalability at the system level, thus increasing the end user's return on investment
•100% binary compatibility with previous versions of SPARC™ architectures	• Reducing the system cost by eliminating the special purpose media processor
•Uses 0.25 micron technology and packaging	• Increasing the return on investment of software applications
	• Enhanced processor performance with decreased power consumption, thus increasing the reliability of the microprocessor
Performance	
•Integer	• 17.4 SPECint95: 19.7 Peak, 16.2 Base
•Floating Point	• 25.7 SPECfp95: 27.0 Peak, 23.9 Base
•Bandwidth (BW) to main memory	• 1.6 Gbyte/sec (peak) with a 100MHz UPA
Unique Features	
•Block load and store instructions	• Delivering high performance access to large datasets across the network
•JTAG Boundary Scan and Performance Instrumentation	• Enabling UltraSPARC™ based systems to offer features such as: power management, automatic error correction, and lower maintenance cost

MODULE COMPONENT OVERVIEW

The UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache, (SME5228BUPA-480), (see *Figure 1*), consists of the following components:

- UltraSPARC™-II, 480 MHz CPU
- UltraSPARC-II Data Buffer (UDB-II)
- Eight Megabyte E-cache, made up of eight (512K x 18) data SRAMs and one 128K x 36 Tag SRAM
- Clock Buffer: MC100LVE210
- DC-DC regulator (2.6V to 1.9V)

Block Diagram

The module block diagram for the UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache is illustrated in Figure 1.

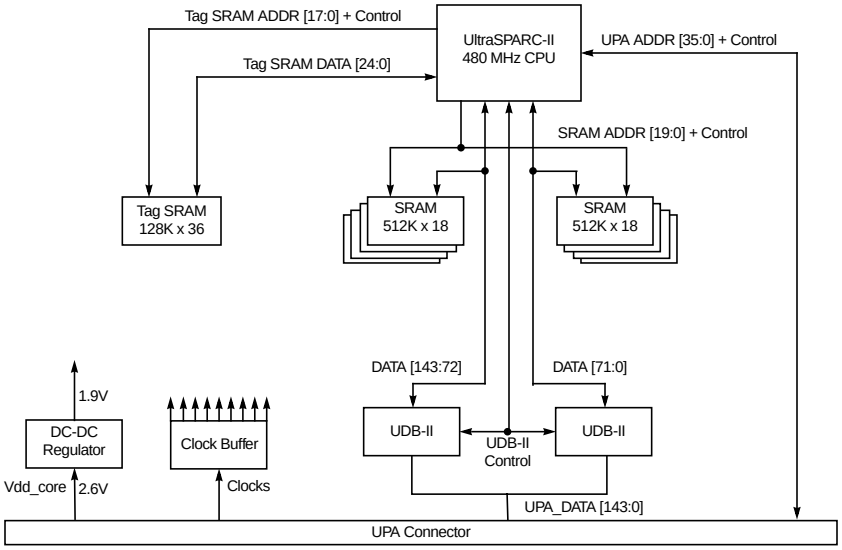


Figure 1. Module Block Diagram

DATA BUFFER DESCRIPTION

UltraSPARC-II Data Buffer (UDB-II)

The UltraSPARC™-II, 480 MHz CPU module has two UltraSPARC-II data buffers (UDB-II) - each a 256 pin BGA device - for a UPA Interconnect system bus width of 128 Data + 16 ECC.

There is a bidirectional flow of information between the external cache of the CPU and the 144-bit UPA interconnect. The information flow is linked through the UDB-II, it includes: cache fill requests, writeback data for dirty displaced cache lines, copyback data for cache entries requested by the system, non-cacheable loads and stores, and interrupt vectors going to and from the CPU.

Each UDB-II has a 64-bit interface plus eight parity bits on the CPU side, and a 64-bit interface plus eight error correction code (ECC) bits on the system side.

The CPU side of the UDB-II is clocked with the same clock delivered to UltraSPARC-II (1/2 of the CPU pipeline frequency).

EXTERNAL CACHE DESCRIPTION

The external cache is connected to the E-cache data bus. Nine SRAM chips are used to implement the eight megabyte cache. One SRAM is used as the tag SRAM and eight are used as data SRAMs. The tag SRAM is 128K x 36, while the data SRAMs are 512K x 18. All nine SRAMs operate in synchronous register-latch mode.

The SRAM interface to the CPU runs at one-half of the frequency of the CPU pipeline. The SRAM signals operate at 1.9V HSTL. The SRAM clock is a differential low-voltage HSTL input.[1]

1. PECL (Positive Emitter Coupled Logic) clocks are converted on the module to the HSTL clocks, for the E-cache interface.

SYSTEM INTERFACE

Figure 2 shows the major components of a UPA based uniprocessor system. The system controller[1] for the UPA bus arbitrates between the UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache, and the I/O bridge chip. The figure also illustrates a slave-only UPA graphics port for Sun graphics boards.

The module UPA system interface signals run at one-quarter of the rate of the internal CPU frequency.

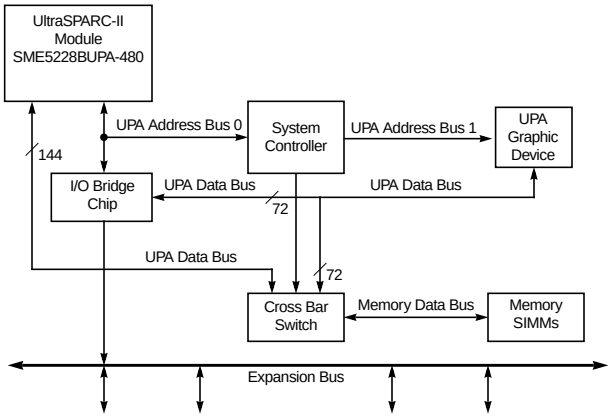


Figure 2. Uniprocessor System Configuration

UPA Connector Pins

The UPA edge connector provides impedance control. The pin assignments are shown with the physical module connector and are represented on page 26 and page 27.

UPA Interconnect

The UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache, (SME5228BUPA-480), supports full master and slave functionality with a 128-bit data bus and a 16-bit error correction code (ECC).

All signals that interface with the system are compatible with LVTTL levels. The clock inputs at the module connector, CPU_CLK, UPA_CLK0, and UPA_CLK1, are differential low-voltage PECL signals.

1. Only two megabytes of external cache are recognized and supported when using the Dual Processor System Controller (DSC, Marketing Part No.STP2202ABGA).

Module ID

Module IDs are used to configure the UPA address of a module. The UPA_PORT_ID[4:3] are hardwired on the module to “0”. UPA_PORT_ID[1:0] are brought out to the connector pins. Each module is hardwired in the system to a fixed and unique UPA address. This feature supports systems with four or fewer processors. For systems that need to support eight modules, UPA_SPEED[1] is connected to SYSID[2] in UDB-II to provide UPA_PORT_ID[2].

Systems which support more than eight modules must map the limited set of UPA_PORT_IDs from this module to the range of required UPA_PORT_IDs, by implementation-specific means in the system.

System firmware (Open Boot Prom) uses UPA_CONFIG_REG[42:39] for generating correct clocks to the CPU module and the UPA system ASICs. These bits are hardwired on the module and are known at MCAP[3:0] at the UltraSPARC-II pins. The 4-bit MCAP value for this module is A(1010).

Module Power

Two types of power are required for this module: V_{DD} at 3.3V, and V_{DD_CORE} at 2.6V. The V_{DD_CORE} supplies the DC-DC regulator which in turn supplies 1.9 volts to the core of the processor chip, the UDB-II external cache interface I/O, and the SRAM I/O. A resistor located on the module sends the program value to the power supply so it generates V_{DD_CORE} at 2.6V to the regulator.

JTAG Interface

The JTAG TCK signal is distributed to UDB-II, SRAMs and the CPU. For additional information about the JTAG interface, see "JTAG Testability," on page 24, and "JTAG (IEEE 1149.1) Timing," on page 25.

SIGNAL DESCRIPTION [1]

System Interface

Signal	Type	Name and Function
UPA_ADDR[35:0]	I/O	Packet switched transaction request bus. Maximum of three other masters and one system controller can be connected to this bus. Includes 1-bit odd-parity protection. Synchronous to UPA_CLK.
UPA_ADDR_VALID	I/O	Bidirectional radial UltraSPARC-II Bus signal between UltraSPARC-II CPU and the System. Driven by UltraSPARC-II to initiate UPA_ADDR transactions to the system. Driven by the system to initiate coherency, interrupt or slave transactions to UltraSPARC-II. Synchronous to UPA_CLK. Active high.
UPA_REQ_IN[2:0]	I	UltraSPARC-II system address bus arbitration request from up to three other UltraSPARC-II bus ports, which may share the UPA_ADDR. Used by the UltraSPARC-II for the distributed UPA_ADDR arbitration protocol. Connection to other UltraSPARC-II bus ports is strictly dependent on the Master ID allocation. Synchronous to UPA_CLK. Active high.
UPA_SC_REQ_IN	I	UltraSPARC-II system address bus arbitration request from the system. Used by the UltraSPARC-II CPU for the distributed UPA_ADDR arbitration protocol. Synchronous to UPA_CLK. Active high.
UPA_S_REPLY[4:0]	I	UltraSPARC-II system reply packet, driven by system controller to the UPA port. Synchronous to UPA_CLK. Active high. UPA_S_REPLY [4] is a no-connect.
UPA_DATA_STALL	I	Driven by system controller to indicate whether there is a data stall. Active high.
UPA_P_REPLY[4:0]	O	UltraSPARC-II system reply packet, driven by the UltraSPARC-II to the system. Synchronous to UPA_CLK. Active high.
UPA_DATA[127:0]	I/O	UPA interconnect data bus
UPA_ECC[15:0]	I/O	ECC bits for the data bus. 8-bit ECC per 64-bits of data.
UPA_ECC_VALID	I	Driven by the system controller to indicate that the ECC is valid for the data on the UPA interconnect data bus: active high.
UPA_REQ_OUT	I/O	Arbitration request from this module: active high.
UPA_PORT_ID[1:0]	I	Module's identification signals: active high. The UPA_SPEED[1] acts as a UPA_PORT_ID[2].

Clock Interface

Signal	Type	Name and Function
UPA_CLK[1:0]_POS UPA_CLK[1:0]_NEG	I	UPA interconnect clock, two copies are provided, one for the CPU and one for the UDBs.
CPU_CLK_POS CPU_CLK_NEG	I	Differential clock inputs to the clock buffer on the module.
UPA_RATIO	I	This is not used.
UPA_SPEED [0]	O	UPA_SPEED [0] is an output tied low on the module.
UPA_SPEED [1]	I/O	UPA_SPEED[1] is tied low with 510 ohms and high to 3.3V with 4.7k ohms. It is also connected to the SYSID [2] on each UDB-II.
UPA_SPEED [2]	O	UPA_SPEED [2] is tied high on the module.

1. For the modular connector pin assignments (UPA pin-out assignments) see page 26 and page 27.

JTAG/Debug Interface

Signal	Type	Name and Function
TDO	O	IEEE 1149 test data output. A three-state signal driven only when the TAP controller is in the shift-DR state.
TDI	I	IEEE 1149 test data input. This pin is internally pulled to logic one when not driven.
TCK	I	IEEE 1149 test clock input. This pin if not hooked to a clock source must always be driven to a logic 1 or a logic 0.
TMS	I	IEEE 1149 test mode select input. This pin is internally pulled to logic one when not driven. Active high.
TRST_L	I	IEEE 1149 test reset input (active low). This pin is internally pulled to logic one when not driven. Active low.

Initialization Interface

Signal	Type	Name and Function
UPA_RESET_L	I	Driven by the system controller for the POR (power-on) resets and the fatal system reset. Asserted asynchronously. Deasserted synchronous to UPA_CLK. Active low.
UPA_XIR_L	I	Driven to signal externally initiated reset (XIR). Actually acts like a non-maskable interrupt. Synchronous to UPA_CLK. Active low, asserted for one clock cycle.

Miscellaneous Signals

Signal	Type	Name and Function
TEMP_SENSE_NEG TEMP_SENSE_POS	O	Connected to a thermistor[1] next to the CPU package, see *Figure 6* on page 17.
POWER_SET_POS POWER_SET_NEG	O	POWER_SET_NEG is tied to GND on the module. POWER_SET_POS is connected to GND via a 1690-ohm resistor. Sets voltage of programmable supply.
POWER_OV	O	Connected to GND via a 1180-ohm resistor. Sets overvoltage level for programmable supply.

1. The thermistor used on this module (UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache) is manufactured by KOA. Operating at 27K the thermistor has KOA part number NT32BT273J.

UPA AND CPU CLOCKS

Module Clocks

The module receives three differential pair low voltage PECL (LVPECL) clock signals (CPU_CLK, UPA_CLK0 and UPA_CLK1) from the systemboard and terminates them. The CPU_CLK is unique in the system, but the UPA_CLKs are two of many UPA clock inputs in the system.

The CPU_CLK operates at one-half the CPU core frequency. The UPA_CLKs operate at the UPA bus frequency. The CPU to UPA clock ratios refer to the CPU core to UPA bus clock signal frequency. The CPU on the module will automatically sense the clock ratio driven by the systemboard as long as the module clock timing is satisfied.

The UltraSPARC-II CPU and UDB-II data buffers detect and support multiple CPU to UPA clock frequency ratios. The UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache is production tested in the 4:1 ratio (480 MHz CPU and 96 MHz UPA). It can be qualified at other ratios in specific systemboards.

UltraSPARC-II CPU Module	Tested CPU to UPA Frequency Ratio	Other supported CPU to UPA Frequency Ratios
UltraSPARC™-II, 480 MHz CPU	5:1	4:1, 6:1

System Clocks

The systemboard generates and distributes the CPU and UPA LVPECL clocks. The systemboard includes a frequency generator, frequency divider, clock buffers, and terminators.

The buffers fan-out the LVPECL clocks to the many UPA devices: the module, cross-bar data switches, system controller, FFB, and the system I/O bridge. The LVPECL clock trace pairs are routed source-to-destination. Each net is terminated at the destination. Most destinations are to single devices. The PCB traces for the differential clocks are balanced to provide a high degree of synchronous UPA device operation.

System Clock Distribution

The goal of this clock distribution is to deliver a quality clock to each system UPA device simultaneously and with the correct clock relationships to the module clocks. For a discussion on how to layout and balance the systemboard LVPECL clock signals and UPA bus signals, see the UPA Electrical Bus Design Note (Document Part Number: 805-0089).

The effective length of the CPU_CLK, UPA_CLK0, and UPA_CLK1 clocks signals on the module are provided in the UPA AC Timing Specification section of this data sheet.

The block diagram for the LVPECL clocks "Clock Signal Distribution," on page 10, illustrates a typical system clock distribution network. Each clock line is a parallel-terminated, dual trace LVPECL clock signal for the CPU, the UPA and the SRAM devices.

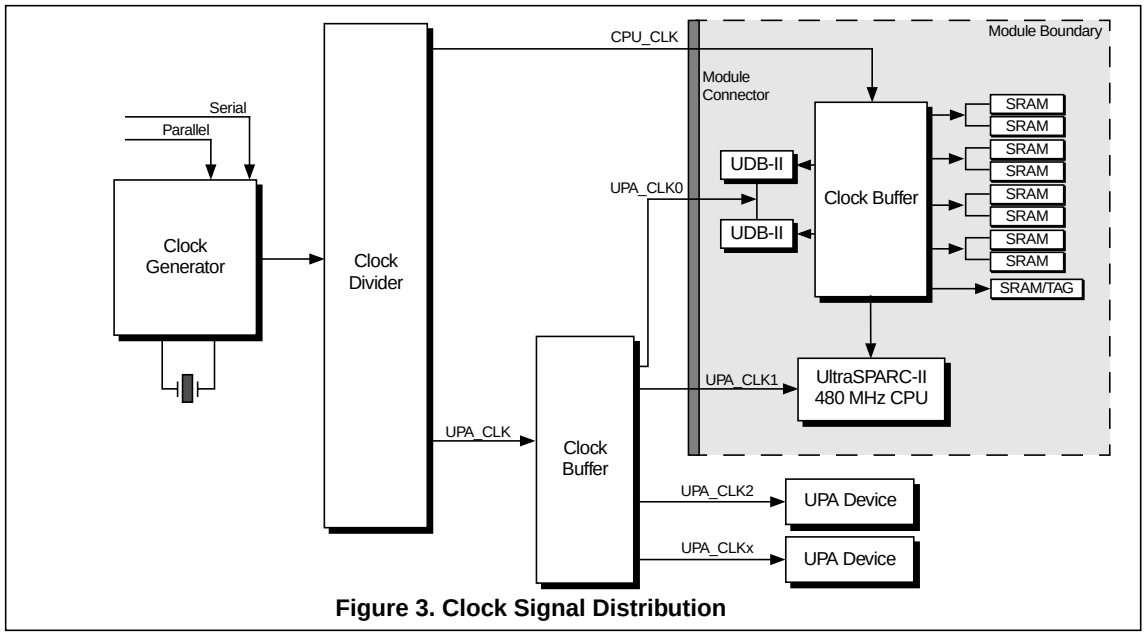


Figure 3. Clock Signal Distribution

LOW VOLTAGE PECL SIGNALS

Two trace signals compose each clock: one positive signal and one negative signal. Each signal is 180-degrees out of phase with the other. Signal timing is referenced to when the positive LVPECL signal transitions from low to high at the cross-over point, when the negative signal transitions from high to low. The trace-pair are routed side-by-side and use parallel termination, (specific routing techniques are require).

CPU CLOCK INPUT

The PLL in the CPU doubles the clock frequency presented at its clock pin. So, for a 480 MHz core CPU clock frequency, the CPU_CLK signal is 240 MHz. Therefore, for the CPU, actions will appear to occur at both transitions of the input CPU_CLK.

CLOCK TRACE DELAYS

The LVPECL propagation time is constant for all clock signals so all balancing is based on length rather than time. All LVPECL traces are striplines (dielectric and power planes top and bottom) with a fixed 180 ps per inch propagation time using the FR4, PCB Dielectric.

LVPECL CLOCK SIGNAL TRACES

Clock trace lengths originate at the clock divider and stop at the CPU module connector or the combined system ASIC pin and terminator loads. The UPA clock delays are relative to the CPU_CLK signal as shown in the following table:.

LVPECL Clock Signal Traces	*Systemboard Trace Length Requirements* [1]	*Time Relative to the CPU_CLK*
CPU_CLK	L Inches [2]	Reference
UPA_CLK + UPA_CLK0	(L + 9)" [3]	2.2 ns later
UPA_CLK + UPA_CLK1	(L + 9)" [3]	2.2 ns later
UPA_CLK + UPA_CLK[x:2]	(L + 18.0)" [3]	3.8 ns later

1. This is the length for traces only. The UPA clocks do not include the required clock buffer delay on the systemboard. A typical tolerance is plus or minus one inch, and is system dependent.
2. The trace lengths from the divider to the module connector.
3. The sum of the trace lengths from the divider to the buffer, plus the buffer to the module connector.

TRACE LENGTH ALLOCATIONS

The trace length guidelines in the above table are for the sum of the PCB trace links in the path for the clock divider to the module connector or systemboard device. The traces are lengthened on the PCB, in order to satisfy these guidelines.

The CPU_CLK trace length can be lengthened on the systemboard to allow for board routing of the longest LVPECL clock signal. See the figure "Clock Signal Distribution," on page 10. Clock traces to nearby devices are zig-zagged to satisfy the trace length requirements.

The UPA_CLK tracelength shown in the above table is common to multiple clock paths. The requirement is for the total length of all segments that make up the path from the clock divider to the reference point. A clock buffer (600ps delay) is assumed to also be in the clockpath of the UPA clocks. See the UPA Bus Design Note for additional layout details (Document Part Number: 805-0089).

SYSTEMBOARD TRACE LENGTH REQUIREMENTS [1]

This datasheet specifies systemboard trace length requirements. The new UPA bus specification guideline (for recommended new designs) advances the CPU and UPA clock signals relative to the systemboard UPA device clocking.

1. Datasheets prior to April 1999, *DID NOT* specify systemboard trace length requirements.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Units
V_{DD}	Supply voltage range for I/O	0 to 3.8	V
V_{DD_CORE} [2]	Supply voltage range for CPU core	0 to 3.0	V
V_I	Input voltage range [3]	-0.5 to V_{DD} + 0.5	V
V_O	Output voltage range	-0.5 to V_{DD} + 0.5	V
I_{IK}	Input clamp current	± 20	mA
I_{OK}	Output clamp current	± 50	mA
I_{OL}	Current into any output in the low state	50	mA
T_{STG}	Storage temperature (non-operating)	-40 to 90	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The V_{DD_CORE} supplies voltage to the onboard DC-DC regulator. The onboard DC-DC regulator then powers the CPU core and the SRAM I/O bus interface. The V_{DD_CORE} must be lower than V_{DD}, except when the CPU is being re-cycled, at which time the V_{DD} can be lower than V_{DD_CORE} for 30 ms or less, provided that the current is limited to twice thew maximum CPU rating.
3. Unless otherwise noted, all voltages are with respect to the V_{SS} ground.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage for I/O	3.14	3.30	3.46	V
V_{DD_CORE}	Supply voltage for the CPU core [1]	2.47	2.60	2.73	V
V_{SS}	Ground	–	0	–	V
V_{IH}	High-level input voltage	2.0	–	V_{DD} + 0.2	V
V_{IL}	Low-level input voltage	-0.3	–	0.8	V
I_{OH}	High-level output current	–	–	-4	mA
I_{OL}	Low-level output current	–	–	8	mA
T_J	Operating junction temperature	–	–	85	°C
T_A	Operating ambient temperature	–	–	– [2]	°C

1. A current of 2.6V supplies power to the DC-DC regulator which in turn supplies 1.9V to the CPU core.
2. Maximum ambient temperature is limited by airflow such that the maximum junction temperature does not exceed T_J. See the section "Thermal Definitions and Specifications," on page 21.

DC Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High-level output voltage	V_{DD} = Min, I_{OH} = Max	2.4	–	–	V
V_{IH}	High-level input voltage, PECL clocks,		2.28	–	–	V
	High-level input voltage, except PECL clocks		2.0	–	–	V
V_{IL}	Low-level input voltage, PECL clocks		–	–	1.49	V
	Low-level input voltage, except PECL clocks		–	–	0.8	V
V_{OL}	Low-level output voltage	V_{DD} = Min, I_{OL} = Max	–	–	0.4	V
I_{DD}	Supply current for V_{DD} [2] [3]	V_{DD} = Max, Freq.=Max	–	11.0	13.5	A
I_{DD_CORE}	Supply current for V_{DD_CORE} [4] [3]	V_{DD_CORE} = Max, Freq.=Max	–	12.2	13.7	A
I_{OZ}	High-impedance output current (Outputs without pull-ups)	V_{DD} = Max, V_O = 0.4V to 2.4V	–	–	30	µA
			–	–	-30	µA
	High-impedance output current (Outputs with pull-ups)	V_{DD} = Max, V_O = V_{SS} to V_{DD}	–	–	250	µA
I_I	Input current (inputs without pull-ups)	V_{DD} = Max, V_I = V_{SS} to V_{DD}	–	–	± 20	µA
	Input current (inputs with pull-ups)	V_{DD} = Max, V_I = V_{SS} to V_{DD}	–	–	-250	µA
I_{OH}	High level output current		4	–	–	mA
I_{OL}	Low level output current		8	–	–	mA

1. Note that this tables specifies the DC characteristics at the UPA 128M connector.
2. The supply current for the V_{DD} includes the supply current for the CPU, UDB-II, and the SRAMs.
3. The typical DC current values represent the current drawn at nominal voltage with a typical, busy computing load. Variations in the device, computing load, and system implementation affect the actual current. The maximum DC current values will rarely, if ever, be exceeded running all known computing loads over the entire operating range. The maximum values are based on simulations.
4. The supply current for the V_{DD_CORE} includes the supply current for the CPU, UDB-II, SRAMs, via the DC to DC regulator.

Module Power Consumption

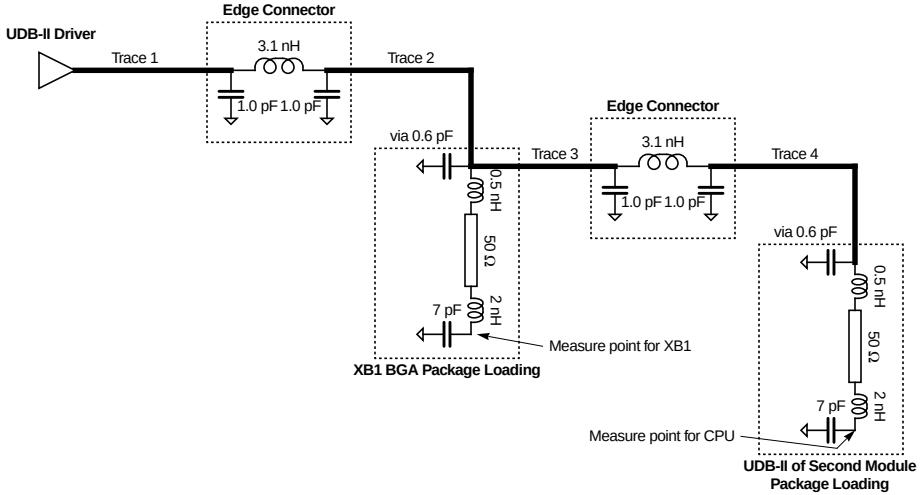
This UltraSPARC-II module requires two supply voltages. The required voltages (provided to the module) for the V_{DD} and V_{DD_CORE} are respectively 3.30V and 2.6V. The estimated *maximum* power consumption of the UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache (SME5228BUPA-480) is 81.68 watts at 480 MHz[1].

The estimated maximum power consumption includes the CPU, the SRAMs, the clock logic and the 8 watts consumed by the DC-DC regulator.

1. *Typical* power consumption for the UltraSPARC™–II, 480 MHz CPU module, 8.0 Mbyte E-cache (SME5228BUPA-480) is 56.24 watts at 480 MHz.

UPA Data Bus SPICE Model

A typical circuit for the UPA data bus and ECC signals is illustrated in *Figure 4*:.



Worst Case: $Z_0 = 60\Omega$, $T_P = 180$ ps / inch, Trace 1 Length = 4.4”, Trace 2 Length = 0.6”, Trace 3 Length = 1.2”, Trace 4 Length = 4.4”

Best Case: $Z_0 = 50\Omega$, $T_P = 160$ ps / inch, Trace 1 Length = 2.2”, Trace 2 Length = 0.2”, Trace 3 Length = 0.2”, Trace 4 Length = 2.2”

Figure 4. Module System Loading: Example for UPA_DATA, UPA_ECC

UPA AC TIMING SPECIFICATIONS

The UPA AC Timing Specifications are referenced to the UPA connector. The timing assumes that the clocks are correctly distributed, (see the section "System Clock Distribution," on page 9). The effective PCB clock trace lengths (CPU_CLK, UPA_CLK0 and UPA_CLK1) are used to calculate a balanced clock system.

UPA_CLK Module Clocks

All the UPA_CLKx trace pairs are the same length coming from the clock buffer and going to each load. To calculate UPA_CLK0 and UPA_CLK1 for the module, assume the trace lengths on the module are 9 inches, (which includes the module connector).

CPU_CLK Module Clock

The CPU_CLK trace on the system board is typically only a few inches long. It is the length of the traces used for the UPA_CLKs from the clock buffer plus the length of UPA_CLK from the clock divider to the clock buffer minus the effective trace length of CPU_CLK on the module, 18 inches, including the module connector.

Clock Buffers

The Clock buffer on the systemboard and the clock buffer on the module are assumed to have similar delays. The clock buffers have a 600 ps delay.

Timing References

The setup, hold and clock to output timing specifications are referenced at the module connector for the signal and at the system UPA device pin. There is no reference point associated with the module since the module trace lengths provided above are effective lengths only and may not represent actual traces.

The following table specifies the AC timing parameters for the UPA bus. For waveform illustrations see the illustration, "Timing Measurement Waveforms," on page 16.

Static signals consist of: UPA_PORT_ID[1:0], UPA_RATIO, and UPA_SPEED[2:0].

Setup and Hold Time Specifications

Symbol	Setup Signals and Hold Time Signals	Waveforms	480 MHz CPU 96 MHz UPA		Unit
			Min	Max	
t_{SU} Setup time	UPA_DATA [127:0]	1	3.4	–	ns
	UPA_ADDR [35:0] UPA_ADDR_VALID, UPA_REQ_IN [2:0], UPA_SC_REQ_IN, UPA_DATA_STALL, UPA_ECC_VALID, UPA_RESET_L, UPA_XIR_L	1	2.9	–	ns
	UPA_ECC [15:0]	1	3.4	–	ns
	UPA_S_REPLY [3:0]	1	3.4	–	ns

Setup and Hold Time Specifications

Symbol	Setup Signals and Hold Time Signals	Waveforms	480 MHz CPU 96 MHz UPA		Unit
			Min	Max	
t_H Hold time	UPA_DATA [127:0]	1	0.4	–	ns
	UPA_ADDR [35:0] UPA_ADDR_VALID, UPA_REQ_IN [2:0], UPA_SC_REQ_IN, UPA_DATA_STALL, UPA_ECC_VALID, UPA_RESET_L, UPA_XIR_L	1	0.4	–	ns
	UPA_ECC [15:0]	1	0.4	–	ns
	UPA_S_REPLY [3:0]	1	0.4	–	ns

The following table, "Propagation Delay, Output Hold Time Specifications," specifies the propagation delay and output hold times for the UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache.

Propagation Delay, Output Hold Time Specifications

Symbol	Clock-to-Out Signals and Output-Hold Signals	Waveforms	480 MHz CPU 96 MHz UPA		Unit
			Min	Max	
t_{PD} Clock-to-Out	UPA_DATA [127:0]	2	–	3.8	ns
	UPA_ADDR [35:0] UPA_ADDR_VALID, UPA_P_REPLY[4:0], UPA_REQ_OUT	2	–	3.1	ns
	UPA_ECC [15:0]	2	–	3.8	ns
t_{OH} Output-Hold	UPA_DATA [127:0]	2	1.1	–	ns
	UPA_ADDR [35:0] UPA_ADDR_VALID, UPA_P_REPLY[4:0]	2	1.1	–	ns
	UPA_ECC [15:0]	2	1.1	–	ns

Timing Measurement Waveforms

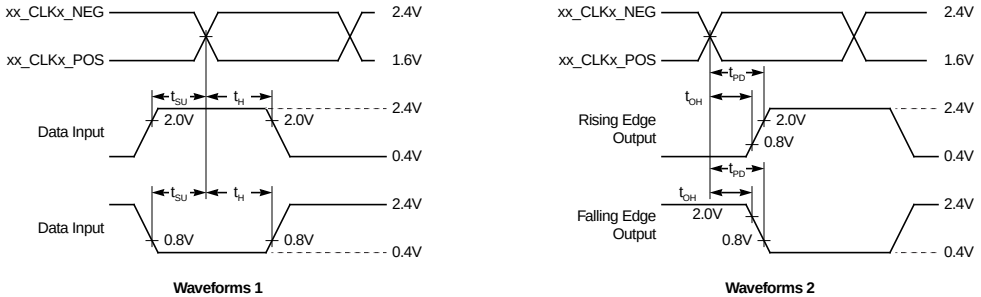


Figure 5. Timing Measurement Waveforms

MECHANICAL SPECIFICATIONS

The module components and dimensions are specified in *Figure 6*, *Figure 7*, *Figure 8* and *Figure 9*.

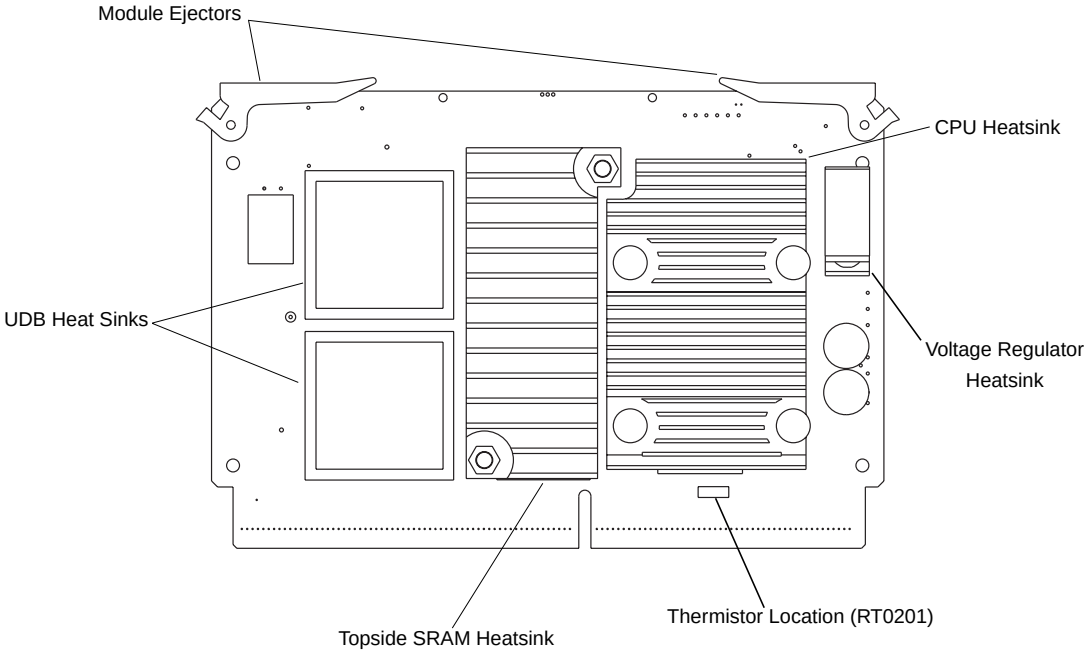


Figure 6. CPU Module (Components)

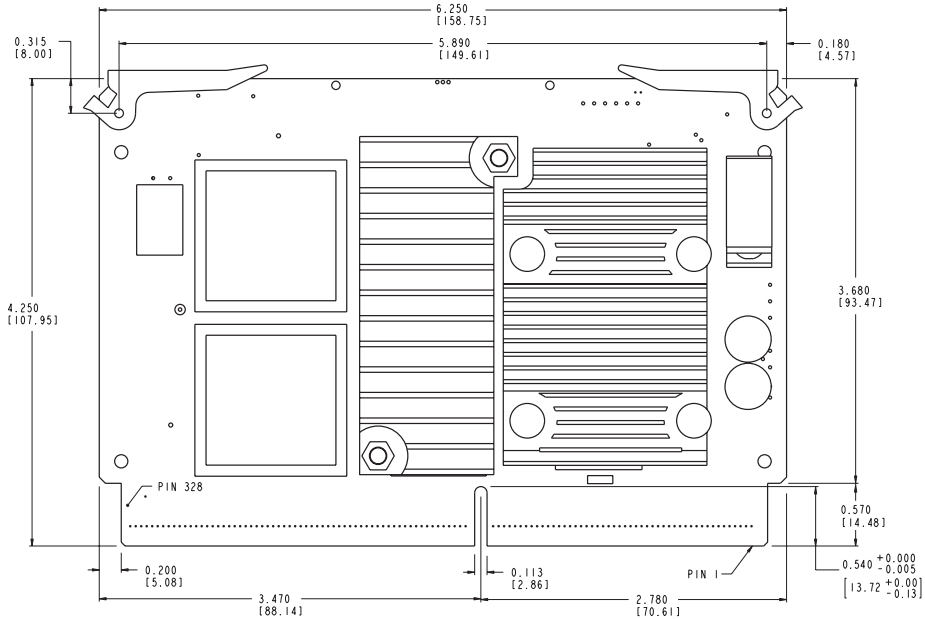


Figure 7. CPU Module (Component Dimensions)

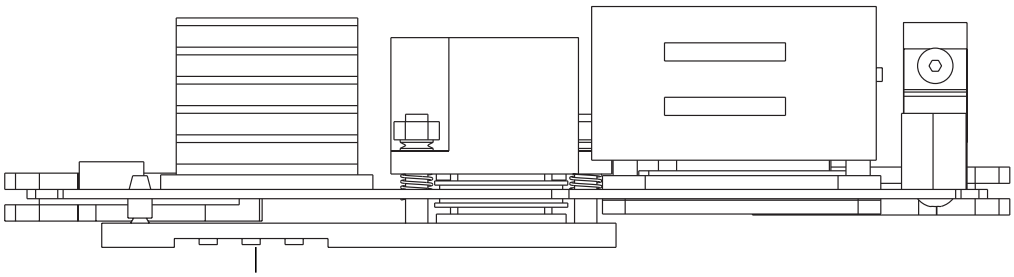
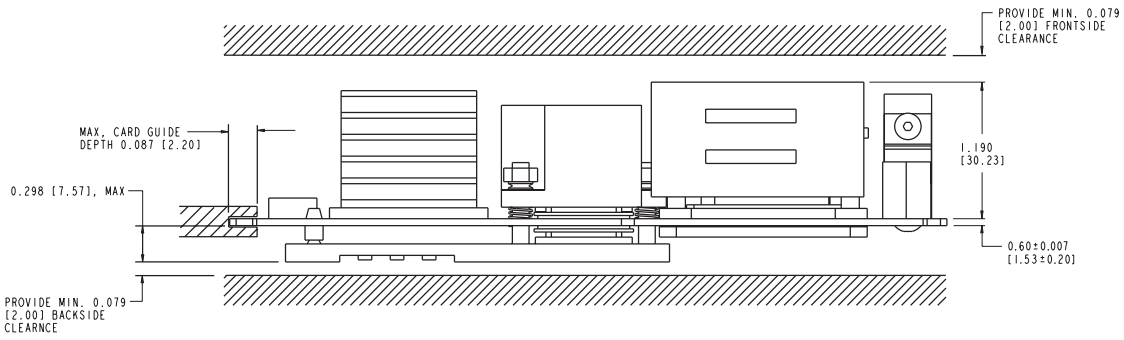


Figure 8. CPU Module Side View



Dimensions: inches [mm]

Figure 9. CPU Module Side View with Dimensions

Note: A minimum backside clearance is required for airflow cooling of the backside heatsink.

THERMAL SPECIFICATIONS

The maximum CPU operating frequency and I/O timing is reduced when the junction temperature (Tj) of the CPU device is raised. Airflow must be directed to the CPU heatsink to keep the CPU device cool. Correct airflow maintains the junction temperature within its operating range. The airflow directed to the CPU is usually sufficient to keep the surrounding devices on the topside of the module cool, including the SRAMs and clock circuitry. The cooling of the backside SRAMs is less critical, but still requires airflow according to the specifications found in the section "Airflow Bottomside," on page 22.

The CPU temperature specification is provided in terms of its junction temperature. It is related to the case temperature by the thermal resistance of the package and the power the CPU is dissipating.

The case temperature can be measured directly by a thermocouple probe, verifying that the CPU junction temperature is correctly maintained over the entire operating range of the system. This includes both the compute load and the environmental conditions for the system. If measuring the case temperature is problematic, then, measure the heatsink temperature and calculate the junction temperature. Both approaches for calculating junction temperature are explained in this section. Irrespective of which method is used, accurate measurement is required.

Two Step Approach to Thermal Design:

Step One determines the ducted airflow requirements based on the CPU power dissipation, the thermal characteristics of the CPU package, and the surrounding heatsink assembly.

See "Thermal Definitions and Specifications," on page 21 for the modules specifications. The specifications for the heatsinks are found in the table "Heatsink-to-Air Thermal Resistance," page 22.

Step Two verifies the cooling effectiveness of the design, by measuring the heatsink or case temperature and calculating the junction temperature. The junction temperature must not exceed the CPU specification. In addition, the lower the junction temperature, the higher the system reliability. The CPU temperature must be verified under a range of system compute loads and system environmental conditions, using one of the temperature measuring methods described herein.

Thermal Definitions and Specifications

Term	Definition	Specification	Comments
Tj	Maximum device junction temperature	85 °C	The Tj can't be measured directly by a thermocouple probe. It must always be estimated as Tj or less. Less is preferred.
Tc	Maximum case temperature	74.3 °C	Measurable at the top-center of the device. Requires a hole in the base of the heatsink to allow thermocouple to be in contact with the case. Maximum case is specified using a CPU device at its maximum power dissipation.
Ts	Maximum heatsink temperature	72.2 °C	Measurable as the temperature of the base of the heat-sink. The best approach is to embed a thermocouple in a cavity drilled in the heatsink base. An alternative approach is to place the thermocouple between the fins / pins of the heatsink (insulated from the airflow) and in contact with the base plate of the heatsink.
Ta	Module ambient air temperature	see page 22	The air temperature as it approaches the heatsink.
Pdt	Typical power dissipation of the CPU	20.72 W	Typical power consumption compute loads over the entire process range.
Pdm	Maximum power dissipation of the CPU	23.52 W	The worst case compute loads over the entire process range.
θjc	Maximum junction-to-case thermal resistance of the package	0.5°C / W	The specification for the UltraSPARC™–II, 480 MHz CPU in a ceramic LGA package.
θcs	Case-to-heatsink thermal resistance	0.1 °C / W	Accuracy of this value requires that good thermal contact is made between the package and the heatsink.
θsa	Heatsink-to-air thermal resistance	see page 22	This value is dependent on the heatsink design, the airflow direction, and the airflow velocity.
Va	Air Velocity	see page 22	The ducted airflow.

Temperature Estimating and Measuring Methods

The following methods can be used to estimate air cooling requirements and calculate junction temperature based on thermocouple temperature measurements.

Airflow Cooling Measurement Method

The relationship between air temperature and junction temperature is described in the following thermal equation:

$$Tj = Ta + [Pdt (\theta jc + \theta cs + \theta sa)]$$

Note: Testing is done with the worst-case power draw, software loading, and ambient air temperature.

Determination of the ambient air temperature (Ta) and the “free-stream” air velocity is required in order to apply the airflow method. The table "Heatsink-to-Air Thermal Resistance," illustrates the thermal resistance between the heatsink and air (θsa).

Note that the airflow velocity can be measured using a velocity meter. Alternatively it may be determined by knowing the performance of the fan that is supplying the airflow. Calculating the airflow velocity is difficult. It is subject to the interpretation of the term “free-stream.”

Note: The Airflow Cooling Estimate method is an estimate. Use it solely when an approximate value suffices. Thermal accuracy can only be assured using the Case Temperature measuring method or the Heatsink Temperature measuring method. Apply these methods to insure a reliable performance.

The following table, "Heatsink-to-Air Thermal Resistance," specifies the thermal resistance of the heatsink as a function of the air velocity.

Heatsink-to-Air Thermal Resistance

Air Velocity (ft/min)[1]	150	200	300	400	500	650	800	1000
θ_{SA} (°C/W)	1.21	1.05	0.91	0.84	0.78	0.72	0.67	0.64

1. Ducted airflow through the heatsinks.

Air Velocity Specifications

These specifications are recommended for a typical configuration:

Airflow Topside

150 LFM @25 °C up to 2,000 feet, altitude, maximum

300 LFM @ 40 °C up to 10,000 feet, altitude, maximum

Airflow Bottomside

150 LFM @ 25 °C up to 2,000 feet, altitude, minimum

150 LFM @ 40 °C up to 10,000 feet, altitude, minimum

Case Temperature Measuring Method

The relationship between case temperature and junction temperature is described in the following thermal equation.

If Tc is known, then Tj can be calculated:

$$Tj = Tc + (Pdt \times \theta jc)$$

Note: Testing is done with the worst-case power draw, software loading, and ambient air temperature.

There is good tracking between the case temperature and the heatsink temperature.

Heatsink Temperature Measuring Method

Measuring the heatsink temperature is sometimes easier than measuring the case temperature. This method provides accurate results for most designs. If the heatsink temperature (Ts) is known then the following thermal equation can be used to estimate the junction temperature:

$$Tj = Ts + [Pdt (\theta jc + \theta cs)]$$

JTAG TESTABILITY

The UltraSPARC™-II, 480 MHz CPU module, 8.0 Mbyte E-cache, (SME5228BUPA-480), implements the IEEE 1149.1 standard to aid in board level testing. Boundary Scan Description Language (BSDL) files are available for all the active devices on the module, except the clock buffer.

AC Characteristics - JTAG Timing

Symbol	Parameter	Signals	Conditions	480 MHz CPU 10 MHz TCK			Units
				Min	Typ	Max	
t_W($\overline{TRST}$)	Test reset pulse width	$\overline{TRST}$ [1]	–	–	–	–	ns
t_{SU}(TDI)	Input setup time to TCK	TDI	–	–	3	–	ns
t_{SU}(TMS)	Input setup time to TCK	TMS	–	–	4	–	ns
t_H(TDI)	Input hold time to TCK	TDI	–	–	1.5	–	ns
t_H(TMS)	Input hold time to TCK	TMS	–	–	1.5	–	ns
t_{PD}(TDO)	Output delay from TCK [2]	TDO	I_{OL} = 8 mA	–	6	–	ns
t_{OH}(TDO)	Output hold time from TCK [2]	TDO	I_{OH} = -4 mA C_L = 35 pF V_{LOAD} = 1.5V	3	–	–	ns

1. $\overline{TRST}$ is an asynchronous reset.
2. TDO is referenced from falling edge of TCK.

JTAG (IEEE 1149.1) TIMING

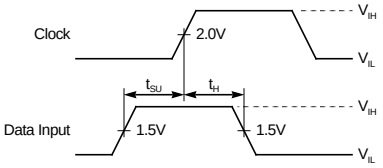


Figure 10. Voltage Waveforms - Setup and Hold Times

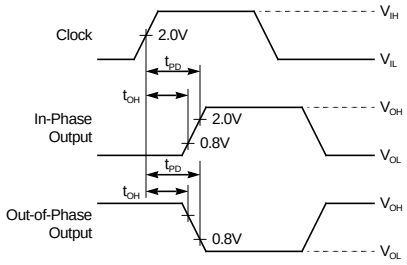
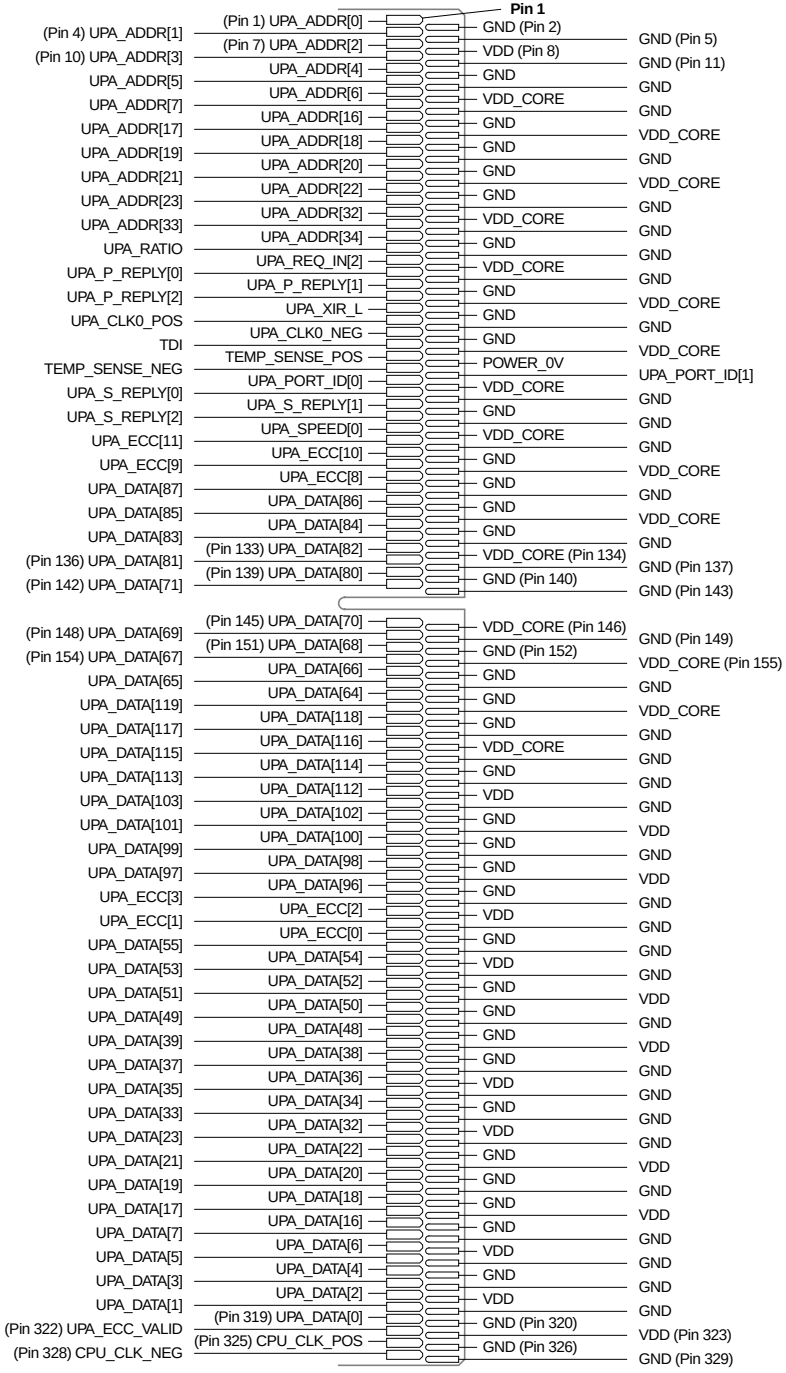
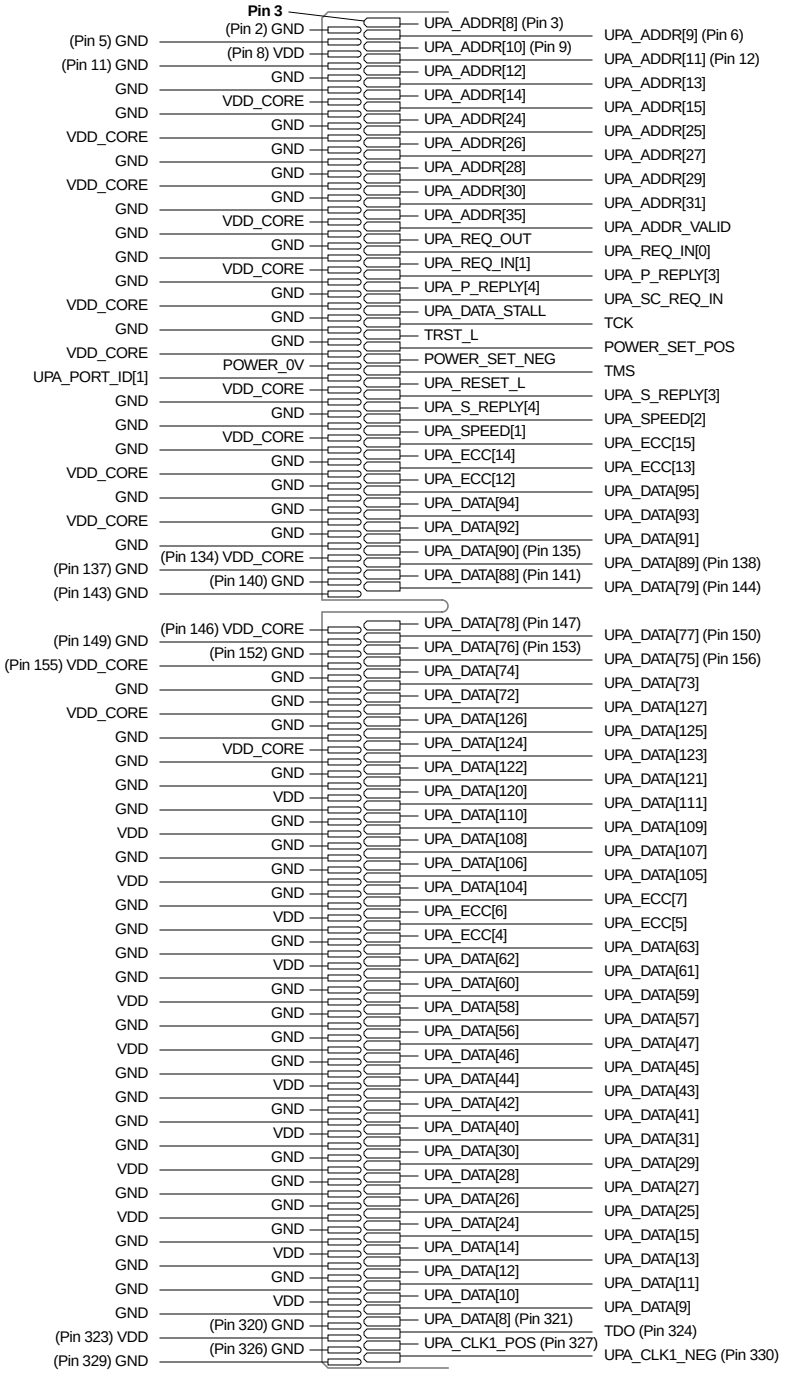


Figure 11. Voltage Waveforms - Propagation Delay Times

UPA CONNECTOR PIN ASSIGNMENTS (TOP VIEW)



UPA CONNECTOR PIN ASSIGNMENTS (BOTTOM VIEW)



STORAGE AND SHIPPING SPECIFICATIONS

Parameter	Conditions	Value			Unit
		Min.	Typ.	Max	
Temperature	Ambient	-40	–	90	°C
Temperature ramp	Ambient	–	–	10	°C/min.
Shock (shipping)	Drop height on to any edge, corner, or side of shipping box—single module package	–	–	21	inches
Shock (shipping)	Drop height on to any edge, corner, or side of shipping box—multi-module package	–	–	18	inches

HANDLING CPU MODULES

CAUTION: Handle a module by carefully holding it by its edges and by the large CPU heatsink. Do not bump or handle the SRAM heatsinks because this action can cause unseen damage to the solder connections. Always handle modules and other electronic devices in an ESD-controlled environment.

REVISION HISTORY

Date	Change
October 10, 2000	Change of datasheet to “Preliminary Version”. Correct marketing part number added: SME5228BUPA-480. The current URL for this datasheet is: http://www.sun.com/embedded/databook/pdf/datasheets/SME5228BUPA-480.pdf
September 1, 2000	Changes to illustrations and specifications to account for new thermal and mechanical information. Changes which state that this CPU module does not have a shroud. New calculations and specifications added for the maximum power dissipation of the module, see page 13.
April 28, 2000	This is the premiere edition of the SME5228BUPA-480 CPU module datasheet. It covers the latest version of the CPU and the changes made to this module to accommodate it.

Preliminary Version
SME5228BUPA-480

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