Who Said One Size Fits All?

In today’s world of enterprise computing, microprocessors are constantly driven to provide the optimal balance of performance, scalability, reliability, cost and power consumption for its intended range of target applications. Sun’s customer-focused design methodology and its tradition to innovate for real-world solutions has led to the development of a family of high-performance, 64-bit microprocessors that are conceived at multiple design points to address the challenging and unique workloads of the various tiers of enterprise computing. For high-performance microprocessors, one size never fits all.

As the latest member of the i-Series UltraSPARC® processor family, the UltraSPARC IIIi microprocessor powers systems used in applications such as web servers, application servers, CAD/CAM and high performance technical computing. While our flagship s-Series UltraSPARC III processor was designed to meet the needs of large SMP (symmetric multiprocessing)-based datacenter servers, the UltraSPARC IIIi processor was developed with a clear objective: to provide the real-world application performance, improved cost efficiency and robust RAS features mandated by volume servers and performance workstations.

The UltraSPARC IIIi processor leverages the core technologies from the UltraSPARC III processor, and further optimizes the microprocessor to exceed customer requirements. Features such as the 1 MB on-chip L2 cache, a high-speed JBus SMP system interface, 16 GB of main memory capacity and an integrated 266 MHz DDR-1 memory controller, provide the necessary application performance required for customer deployments at web/application servers and on the desktop. Additionally, the use of asynchronous design techniques to counter clock skew in the memory interface represents one of the several new design innovations in this microprocessor.

Designed and optimized in concert with the Solaris Operating Environment and Sun systems, the UltraSPARC IIIi processor offers impressive price/performance in its targeted tiers of applications. With 15 years of binary compatibility, and Sun’s determination to maintain it, customers should expect that their investments in the SPARC and Solaris platform can continue to pay dividends in the future.
UltraSPARC® IIIi Processor Technical Information

UltraSPARC® IIIi Processor Features

- L1 Cache: 64 KB (4-way) Data, 32 KB (4-way) Instruction, 2 KB Prefetch, 2 KB Write
- L2 cache: on-chip 1 MB (4-way, set-associative)
- System Bus: new cache coherent | Bus interface operating up to 200 MHz
- Integrated DDR1 SDRAM memory controller
- Clock frequency control for dynamically dropping frequency for low power modes (1/2 to 1/16)
- VIS SIMD Instruction Set

CPU Core Design

- 14-stage non-stalling pipeline
- 16,000 entry branch prediction table
- New byte mask and shuffle VIS instructions for media applications
- Jump target registration instruction to accelerate interpreted code like Java™ technology

Instruction Execution Features

- Sustainable 4-way Superscalar
- Six execution pipelines (2 integer, 2 FP/VIS, 1 load/store, 1 branch)
- Multiple outstanding block stores

JBus Features

- 183-bit, 150-200 MHz clock frequency
- System bus optimized for up to 4-way
- MOESI Coherence protocol
- Fully pipelined snooping protocol

Scalable System Performance

- Optimized system interface with peak bandwidth of 3.2 GB/s
- Processor memory bandwidth scales with number of processors

Distributed Main Memory

- Distributed memory control (at each CPU)
- Memory Interface: 266 MHz DDR1
- Memory Size: 16 GB per CPU
- Main memory bus bandwidth: 4.25 GB/s (peak)

Industry-leading RAS Features Include:

- L1 caches and tags are parity protected
- L2 data array ECC protected
- Memory bus is ECC protected
- JBus is parity protected

Enhanced Support from Solaris

- Multiprocessor (MP) support provided by Solaris OE
- System models for tightly coupled, shared memory and for large multi-processor clustered architectures (snoop and directory-based)

Physical Characteristics of UltraSPARC® IIIi 1 GHz

- 959 pin ceramic Micro Pin Grid Array (µPGA)
- Transistor Count: 52,7 million
- Maximum Power Dissipation: 52 W @1.28 GHz
- CMOS process: 0.13µ, 7-layer copper

DDR SDRAM (128b data, 9b ECC 80-122 MHz)

IBUS (128b data, 36b address, 120-200 MHz)