

TOSHIBA RISC PROCESSOR

TX9956CXBG-533/-600 (TX9956C)

(64-bit RISC MICROPROCESSOR)

1. GENERAL DESCRIPTION

The TX9956C is a 64-bit RISC (Reduced Instruction Set Computer) microprocessor that is a low-cost, low-power microprocessor developed for interactive consumer applications including set-top terminals, LBP(Laser Beam Printer), and video games.

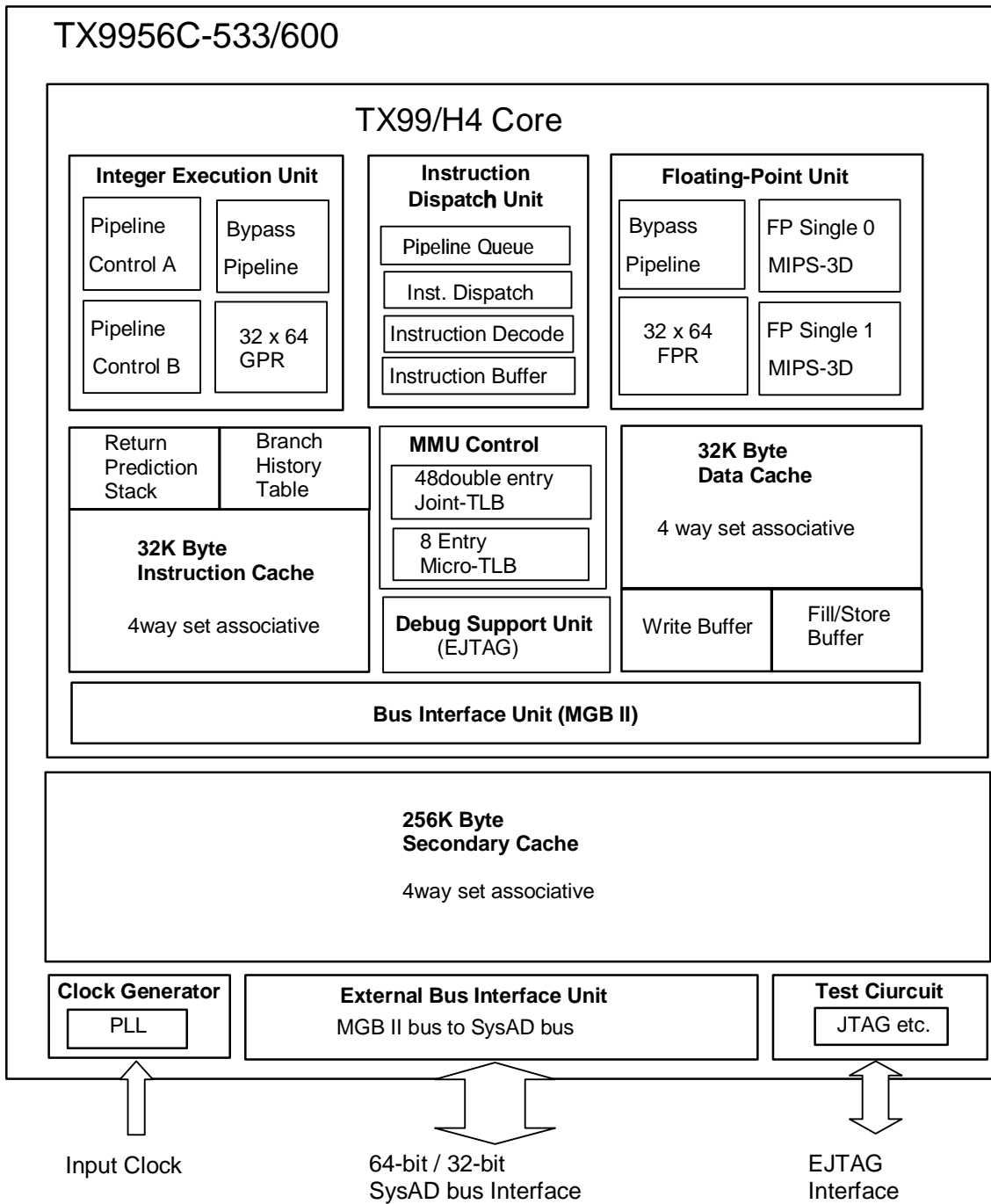
2. FEATURES

- True 64-bit microprocessor, with TX99/H4 core.
- 7-stage super-scalar pipeline
- 64bit System Address/Data bus (support 32bit bus mode)
- Single or double-precision Floating-Point Operation
- 36-bit physical address space and 64-bit virtual address space.
- 64-bit SysAD bus interface with R5000 compatible protocol
- On-chip 32-Kbyte Instruction Cache, 32-Kbyte Data Cache and 256KB Level 2 Cache.
- Low power consumption
 - 3.3V or 2.5V / 1.25V Dual power supply (I/O:3.3V or 2.5V, Internal:1.25V)
 - power management mode
- Memory management unit
 - contains 48-double entry JTLB, and 8-entry Data TLB
- Software compatibility with all MIPS processors
 - MIPS64 Instruction Set Architecture (ISA) and MIPS-3D ASE
- EJTAG (Enhanced JTAG) debug support
- Maximum operating frequency
 - Internal: 533 to 600MHz External:133Hz
- Package : 272-pin PBGA with 16-pin thermal balls, 27mm x 27mm, 1.27mm pitch

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3. SYSTEM CONFIGURATION

3.1 TX9956C BLOCK DIAGRAM



3.2 BLOCK FUNCTION

TX99/H4 Core

True 64-bit microprocessor

32, 64-bit integer general purpose registers

32, 64-bit floating point general purpose registers

7-stage super-scalar pipeline

Instruction Set

MIPS64 ISA

3D Graphic's instructions

On-chip 32-Kbyte Instruction Cache, 32-Kbyte Data Cache and 256KB Level2 Cache

4-way set associative and Lock function support : Primary cache

Data Cache: Write-back and Write-through support : Primary cache

256KB Secondary Cache

MMU

32-bit physical address space and 64-bit virtual address space

48-double-entry (even/odd) Joint TLB

8-entry Data TLB

IEEE754 compatible single and double precision FPU

Debug Support Unit (DSU) with EJTAG support

RP and Sleep mode

SysAD BUS I/F

Bus protocol conversion

It converts TX9956C Internal MGB II Read/Write request into outside SyAD Bus protocol.

Clock Generator

Generates the internal operating clock of the TX9901 from external crystal oscillator.

Debug Support Unit (DSU)

EJTAG function support

Consists of an Enhanced JTAG (EJTAG) Module and a Debug Support Unit (DSU). It can be used to provide single-step execution and hardware break-points for debugging processor systems. EJTAG utilizes JTAG interface and extends the ability to access the inside register contents, host system peripherals, and system memory.

4. PIN DESCRIPTION

4.1 Pin out

A1	Vss	B11	SysCmd2	D1	Reset*	F3	SysAD47	J17	Vss
A2	NC	B12	VccOK	D2	ColdReset*	F4	VccIO	J18	VccInt
A3	NC	B13	SysADC6	D3	TMODE	F17	Vss	J19	SysAD13
A4	SysADC4	B14	SysADC7	D4	Vss	F18	SysAD38	J20	SysAD12
A5	SysADC5	B15	ValidOut*	D5	VccInt	F19	SysAD37	K1	VccIO
A6	Int4*	B16	WrRdy*	D6	Vss	F20	VccIO	K2	SysAD22
A7	VccInt	B17	RdRdy*	D7	Vss	G1	VccInt	K3	SysAD21
A8	Vss	B18	NC	D8	VccIO	G2	SysAD49	K4	VccIO
A9	SysCmd8	B19	NC	D9	Vss	G3	VccInt	K9	Vss
A10	SysCmd5	B20	VccInt	D10	Vss	G4	Vss	K10	Vss
A11	SysCmd3	C1	NMI*	D11	VccIO	G17	Vss	K11	Vss
A12	Release*	C2	ExtRqst*	D12	Vss	G18	VccInt	K12	Vss
A13	VccIO	C3	VccIO	D13	VccIO	G19	SysAD36	K17	Vss
A14	Vss	C4	VccInt	D14	Vss	G20	Vss	K18	VccInt
A15	ValidIn*	C5	NC	D15	Vss	H1	Endian	K19	SysAD11
A16	Vss	C6	Int2*	D16	VccIO	H2	SysAD17	K20	SysAD10
A17	Vss	C7	VccInt	D17	Vss	H3	SysAD16	L1	Vss
A18	NC	C8	SysCmdP	D18	SysAD42	H4	VccIO	L2	SysAD23
A19	JTRST*	C9	SysCmd6	D19	SysAD41	H17	Vss	L3	VccInt
A20	Vss	C10	VccInt	D20	RP	H18	VccIO	L4	Vss
B1	VccInt	C11	SysCmd1	E1	SysAD46	H19	SysAD15	L9	Vss
B2	NC	C12	SysCmd0	E2	SysAD45	H20	SysAD14	L10	Vss
B3	NC	C13	NC	E3	SysAD44	J1	SysAD20	L11	Vss
B4	SysAD43	C14	VccInt	E4	Vss	J2	SysAD19	L12	Vss
B5	Int5*	C15	BSIZE64*	E17	Vss	J3	SysAD18	L17	VccIO
B6	Int3*	C16	VccInt	E18	VccIO	J4	Vss	L18	SysAD8
B7	Int1*	C17	Vss	E19	SysAD40	J9	Vss	L19	SysAD9
B8	Int0*	C18	VccIO	E20	SysAD39	J10	Vss	L20	VccInt
B9	SysCmd7	C19	NC	F1	Vss	J11	Vss	M1	SysAD26
B10	SysCmd4	C20	Sleep	F2	SysAD48	J12	Vss	M2	SysAD25

M3	SysAD24	P20	SysAD35	U9	Vss	V14	Vcclnt	W19	VccPLL
M4	VccIO	R1	Vss	U10	Vss	V15	SysAD62	W20	MasterClk
M9	Vss	R2	SysAD53	U11	Vss	V16	SysAD63	Y1	Vss
M10	Vss	R3	SysAD52	U12	VccIO	V17	EJDINT	Y2	SysDiv0
M11	Vss	R4	Vcclnt	U13	Vss	V18	VccIO	Y3	SysAD57
M12	Vss	R17	Vss	U14	Vss	V19	NC	Y4	Vcclnt
M17	Vss	R18	JTMS	U15	Vss	V20	Vss	Y5	Vss
M18	SysAD6	R19	SysAD32	U16	Vss	W1	Vcclnt	Y6	SysAD29
M19	SysAD7	R20	SysAD33	U17	Vss	W2	SysDiv1	Y7	SysAD31
M20	Vss	T1	SysAD55	U18	JTDO	W3	SysAD56	Y8	FMO
N1	SysAD27	T2	SysAD54	U19	BufSel	W4	SysAD58	Y9	VccIO
N2	SysAD51	T3	NC	U20	Vcclnt	W5	SysAD60	Y10	Vss
N3	SysAD50	T4	VccIO	V1	CoreDiv3	W6	SysAD28	Y11	SysADC1
N4	Vss	T17	VccIO	V2	SysDiv2	W7	SysAD30	Y12	SysAD1
N17	Vss	T18	JTCK	V3	VccIO	W8	FMRD	Y13	NC
N18	VccIO	T19	JTDI	V4	Vcclnt	W9	FMSI	Y14	Vss
N19	SysAD4	T20	Vss	V5	SysAD59	W10	SysADC3	Y15	Vcclnt
N20	SysAD5	U1	CoreDiv2	V6	SysAD61	W11	SysAD0	Y16	EJTRIG0
P1	Vcclnt	U2	CoreDiv1	V7	Vcclnt	W12	SysAD2	Y17	JtagSel
P2	Vss	U3	CoreDiv0	V8	FMCLK	W13	NC	Y18	BypassCoreCG
P3	Vcclnt	U4	Vss	V9	SysADC2	W14	NC	Y19	VssPLL
P4	Vss	U5	VccIO	V10	SysADC0	W15	NC	Y20	Vss
P17	Vss	U6	Vss	V11	Vcclnt	W16	EJTRIG1		
P18	Vcclnt	U7	Vss	V12	SysAD3	W17	L2Bypass		
P19	SysAD34	U8	VccIO	V13	NC	W18	BypassPLL		

4.2 PIN Layout

TOP View

	A	B	C	D	E	F	G	H	J	K
20	Vss	Vcclnt	Sleep	RP	SysAD39	VcclIO	Vss	SysAD14	SysAD12	SysAD10
19	JTRST*	NC	NC	SysAD41	SysAD40	SysAD37	SysAD36	SysAD15	SysAD13	SysAD11
18	NC	NC	VcclIO	SysAD42	VcclIO	SysAD38	Vcclnt	VcclIO	Vcclnt	Vcclnt
17	Vss	RdRdy*	Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss
16	Vss	WrRdy*	Vcclnt	VcclIO	Top View					
15	ValidIn*	ValidOut*	BSIZE64*	Vss						
14	Vss	SysADC7	Vcclnt	Vss						
13	VcclIO	SysADC6	NC	VcclIO						
12	Release*	VccOK	SysCmd0	Vss						
11	SysCmd3	SysCmd2	SysCmd1	VcclIO						
10	SysCmd5	SysCmd4	Vcclnt	Vss						
9	SysCmd8	SysCmd7	SysCmd6	Vss						
8	Vss	Int0*	SysCmdP	VcclIO						
7	Vcclnt	Int1*	Vcclnt	Vss						
6	Int4*	Int3*	Int2*	Vss						
5	SysADC5	Int5*	NC	Vcclnt						
4	SysADC4	SysAD43	Vcclnt	Vss	Vss	VcclIO	Vss	VcclIO	Vss	VcclIO
3	NC	NC	VcclIO	TMODE	SysAD44	SysAD47	Vcclnt	SysAD16	SysAD18	SysAD21
2	NC	NC	ExtRqst*	ColdReset*	SysAD45	SysAD48	SysAD49	SysAD17	SysAD19	SysAD22
1	Vss	Vcclnt	NMI*	Reset*	SysAD46	Vss	Vcclnt	Endian	SysAD20	VcclIO

Vss	Vss
Vss	Vss
Vss	Vss
Vss	Vss

L	M	N	P	R	T	U	V	W	Y									
VccInt	Vss	SysAD5	SysAD35	SysAD33	Vss	VccInt	Vss	MasterClk	Vss	20								
SysAD9	SysAD7	SysAD4	SysAD34	SysAD32	JTDI	BufSel	NC	VccPLL	VssPLL	19								
SysAD8	SysAD6	VccIO	VccInt	JTMS	JTCK	JTDO	VccIO	BypassPLL	Bypass CoreCG	18								
VccIO	Vss	Vss	Vss	Vss	VccIO	Vss	EJDINT	L2Bypass	JtagSel	17								
<table border="1" style="margin-left: 20px;"> <tr><td>Vss</td><td>Vss</td></tr> <tr><td>Vss</td><td>Vss</td></tr> <tr><td>Vss</td><td>Vss</td></tr> <tr><td>Vss</td><td>Vss</td></tr> </table>						Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss	SysAD63	EJTRIG1	EJTRIG0	16
						Vss	Vss											
						Vss	Vss											
						Vss	Vss											
						Vss	Vss											
						Vss	SysAD62	NC	VccInt	15								
						Vss	VccInt	NC	Vss	14								
						Vss	NC	NC	NC	13								
						VccIO	SysAD3	SysAD2	SysAD1	12								
						Vss	VccInt	SysAD0	SysADC1	11								
						Vss	SysADC0	SysADC3	Vss	10								
						Vss	SysADC2	FMSI	VccIO	9								
VccIO	FMCLK	FMRD	FMO	8														
Vss	VccInt	SysAD30	SysAD31	7														
Vss	SysAD61	SysAD28	SysAD29	6														
VccIO	SysAD59	SysAD60	Vss	5														
Vss	VccIO	Vss	Vss	VccInt	VccIO	Vss	VccInt	SysAD58	VccInt	4								
VccInt	SysAD24	SysAD50	VccInt	SysAD52	NC	CoreDiv0	VccIO	SysAD56	SysAD57	3								
SysAD23	SysAD25	SysAD51	Vss	SysAD53	SysAD54	CoreDiv1	SysDiv2	SysDiv1	SysDiv0	2								
Vss	SysAD26	SysAD27	VccInt	Vss	SysAD55	CoreDiv2	CoreDiv3	VccInt	Vss	1								

Top View

4.3 PIN FUNCTION

The following is a list of interface, interrupt, and miscellaneous pins available on the TX9956C.

SYSTEM INTERFACE

PIN NAME	I / O	FUNCTION
SysAD(63:0)	I / O	System address / data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysCmd(8:0)	I / O	System command / data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysADC(7:0)	I / O	System command/data check bus A 8-bit bus containing parity check bits for the SysAD bus during data cycles.
SysCmdP	I / O	Reserved for system command/data identifier bus parity For the TX9956C this signal is unused on input and zero on output.
ValidIn*	I	Valid input The external agent asserts ValidIn* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	O	Valid output The processor asserts ValidOut* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ExtRqst*	I	External request An external agent asserts ExtRqst* to request use of the System interface.
Release*	O	Release interface Signals that the system interface needs to submit an external request.
WrRdy*	I	Write Ready Signals that an external agent can now accept a processor write request.
RdRdy*	I	Read Ready Signals that an external agent can now accept a processor read request.

CLOCK / CONTROL INTERFACE

PIN NAME	I / O	FUNCTION
MasterClock	I	Master clock Master clock input that establishes the processor operating frequency.
CoreDiv(3:0)	I	Set the operational frequency of TX99H4 Core vs L2 Cache <u>CoreDiv(3:0) CPU Core : L2 Cache</u> 0000 Reserved 0001 2:1 0010 3:1 0011 4:1 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111 Reserved
SysDiv(2:0)	I	Set the operational frequency of MBG II bus vs SysAD Bus <u>SysDiv(2:0) MGB II bus : SysAD bus I/F</u> 000 Reserved 001 Reserved 010 2:1 011 3:1 100 4:1 101 Reserved 110 Reserved 111 Reserved
Sleep	O	Sleep mode
RP	O	RP mode
Endian	I	Endianess input Indicates the initial setting of the endian during a reset. 0 Little Endian 1 Big Endian
L2Bypass	I	L2 Cache Bypass Mode
BypassPLL	I	Test Mode
BypassCoreCG	I	Test Mode

INTERRUPT INTERFACE

PIN NAME	I / O	FUNCTION
Int(5:0)*	I	Interrupt Five general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register and visible as bits 15:10 of the Cause register.
NMI*	I	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.

JTAG and EJTAG INTERFACE

PIN NAME	I / O	FUNCTION
JTDI	I	JTAG data input / Debug interrupt input Run-time mode : input serial data to data/instruction register of JTAG. Real-time mode : interrupt line to change the debug unit state from real time mode to Run-time mode.
JTCK	I	JTAG clock input The processor receives a serial clock on JTCK. On the rising edge of JTCK, both JTDI and JTMS are sampled.
JTDO	O	JTAG data output / PC Trace output Run-time mode : output serial data from data/instruction register of JTAG. Real-time mode : output non-sequential program.
JTMS	I	JTAG command JTAG command signal, indicating the incoming serial data is command data.
EJDINT	I	Debug interrupt for EJTAG
EJTRIG(1:0)	O	Trigger output for EJTAG
JtagSel	I	JTAG Select
JTRST*	I	Test Reset input A reset input for a real-time debug system. When JTRST* is asserted, the debug support unit (DSU) is initialized.

INITIALIZATION INTERFACE

PIN NAME	I / O	FUNCTION						
VccOK	I	VccOK						
Reset*	I	Soft (Warm) Reset This signal must be asserted synchronously with MasterClock for a soft reset.						
ColdReset*	I	Cold reset This signal indicates to the processor that the +3.3V(I/O) and +1.2V(Internal) power supply is stable and the processor should initiate a cold reset sequence, resetting the PLL.						
BSIZE64*	I	Select the bus width of external SysAD bus interface <table border="0"> <tr> <td><u>BSIZE64*</u></td> <td><u>width</u></td> </tr> <tr> <td>0</td> <td>64-bit</td> </tr> <tr> <td>1</td> <td>32-bit</td> </tr> </table>	<u>BSIZE64*</u>	<u>width</u>	0	64-bit	1	32-bit
<u>BSIZE64*</u>	<u>width</u>							
0	64-bit							
1	32-bit							
BufSel	I	Select the output buffer size <table border="0"> <tr> <td><u>BufSel</u></td> <td><u>buffer size</u></td> </tr> <tr> <td>0</td> <td>16mA Buffer</td> </tr> <tr> <td>1</td> <td>8mA Buffer</td> </tr> </table>	<u>BufSel</u>	<u>buffer size</u>	0	16mA Buffer	1	8mA Buffer
<u>BufSel</u>	<u>buffer size</u>							
0	16mA Buffer							
1	8mA Buffer							

OTHERS

PIN NAME	I / O	FUNCTION
FMRD	I	Test Signal
FMSI	I	Test Signal
FMO	O	Test Signal
FMCLK	I	Test Signal
TMODE	I	Test Mode

POWER SUPPLY

PIN NAME	I / O	FUNCTION
VccPLL	I	Quiet V_{CC} for PLL Quiet V _{CC} for the internal phase locked loop. (1.25V)
VssPLL	I	Quiet V_{SS} for PLL Quiet V _{SS} for the internal phase locked loop.
VccIO	I	Vcc Power supply pin for IO.(3.3V or 2.5V)
VccInt	I	Vcc Power supply pin for internal.(1.25V)
Vss	I	Vss Ground pin

5. ELECTRICAL CHARACTERISTICS

Note: “Be careful of static”, please see “From Incoming to Shipping” of General Safety Precautions and Usage Considerations.

5.1 ABSOLUTE MAXIMUM RATINGS

$V_{SS} = 0 \text{ V (GND)}$

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage (for I/O)	$V_{CCIOMax}$	-0.5 to 3.9	V
Supply voltage (for internal)	$V_{CCIntMax}$	-0.5 to 3.0	V
Input voltage ^(*)	V_{IN}	-0.5 to $V_{CC} + 0.3$	V
Storage Temperature	T_{STG}	-40 to +125	°C

Note) If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended condition. If these conditions are exceeded, reliability of LSI may be adversely affected.

(*1) keep ($V_{CCIO} + 0.3V$) less than $V_{CCIOMax}$

5.2 RECOMMENDED OPERATING CONDITIONS

$V_{SS} = 0 \text{ V (GND)}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	Unit
Supply Voltage (for I/O)	V_{CCIO}	3.3V I/O	3.0	3.6	V
		2.5V I/O	2.1	2.7	V
Supply Voltage (for internal)	V_{CCInt}		1.118	1.32	V
Operating Case Temperature	T_C		-20	+85	°C

Note : The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC and DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

5.3 DC CHARACTERISTICS

5.3.1 DC CHARACTERISTICS

 $T_C = -20^{\circ}\text{C to } 85^{\circ}\text{C}, V_{ccInt} = 1.25 \pm 5\%, V_{ccIO} = 3.3\text{ V} \pm 0.2\text{V or } 2.5\text{V} \pm 0.2\text{V}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	$I_{OH} = -8\text{mA}$ (8mA Buffer)	$V_{ccIO} - 0.6$	-	V
		$I_{OH} = -16\text{mA}$ (16mA Buffer)			
Output Low Voltage	V_{OL}	$I_{OL} = 8\text{mA}$ (8mA Buffer)	-	0.4	V
		$I_{OL} = 16\text{mA}$ (16mA Buffer)			
Input High Voltage ^(*1)	V_{IH}		2	$V_{ccIO} + 0.3$	V
Input High Voltage	V_{IHC}	MasterClock	$0.8V_{ccIO}$	$V_{ccIO} + 0.3$	V
Input Low Voltage ^(*1)	V_{IL33}	3.3V I/O	-0.5	0.8	V
	V_{IL25}	2.5V I/O	-0.5	0.6	V
Input Low Voltage	V_{ILC}	MasterClock	-0.5	$0.2V_{ccIO}$	V
Input Leakage	I_{LI}	Except (*2), (*3)		± 10	μA
Input Leakage (Pull-up) ^(*2)	I_{LIu}		-70	-10	μA
Input Leakage (Pull-down) ^(*3)	I_{LId}		10	70	μA
Output Leakage	I_{LO}			± 20	μA
Input Capacitance	C_{IN}			10	pF

(*1) Except for MasterClock input

(*2) With pull-up resistor : Int(5:0)*, NMI*, JTMS, JTCK, JTDI

(*3) With pull-down resistor : JTRST*, EJDINT

5.3.2 OPERATING CURRENT

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNITS
Operating Current 1 (Internal : Normal Operating)	I_{CCInt1}	CPUCLK = 533MHz	3	A
		CPUCLK = 600MHz	3.5	A
Operating Current 2 (Internal : Drystone2.1 Operating)	I_{CCInt2}	CPUCLK = 533MHz	2.5	A
		CPUCLK = 600MHz	3	A
Operating Current 3 (Internal : Sleep mode)	I_{CCInt3}	CPUCLK = 533MHz	1.5	A
		CPUCLK = 600MHz	2	A
Operating Current 4 (Internal : MasterClock Stop)	I_{CCInt4}	MasterClock=0MHz CPUCLK = 0MHz	1	A
I/O Operating Current 1 (Using 3.3V I/O)	I_{CCIO33}	MasterCk=133MHz BufSel=1 50%(8mA Buffer) Load = 25pF	250	mA
		MasterCk=133MHz BufSel=1 50%(8mA Buffer) Load = 25pF	230	mA
I/O Operating Current 2 (Using 2.5V I/O)	I_{CCIO25}	MasterCk=133MHz BufSel=0 100%(16mA Buffer) Load = 25pF	200	mA
		MasterCk=133MHz BufSel=0 100%(16mA Buffer) Load = 25pF	180	mA

5.4 AC CHARACTERISTICS

5.4.1 CLOCK TIMING

$T_C = -20^{\circ}\text{C}$ to 85°C , $V_{ccInt} = 1.25\text{V} \pm 5\%$, $V_{ccIO} = 3.3\text{V} \pm 0.2\text{V}$ or $2.5\text{V} \pm 0.2\text{V}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
MasterClock High	t_{MCH}	Transition 5 ns	2		ns
MasterClock Low	t_{MCL}	Transition 5 ns	2		ns
MasterClock Frequency ^(*1)	f_{MCK}		80	133	MHz
Internal Operation Frequency		533MHz	320	533	MHz
		600MHz	320	600	MHz
MasterClock Period	t_{MCP}		7.5	12.5	ns
MasterClock Rise Time	t_{MCR}			2	ns
MasterClock Fall Time	t_{MCF}			2	ns

(*1) Operation of TX9956C is only guaranteed with the Phase Lock Loop enabled.

(*2) All output timings assume a 25 pF capacitive load.

5.4.2 SYSTEM INTERFACE

$T_C = -20^{\circ}\text{C}$ to 85°C , $V_{ccInt} = 1.25\text{V} \pm 5\%$, $V_{ccIO} = 3.3\text{V} \pm 0.2\text{V}$

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Data Output ^(*1,2,3)	t_{DO}	16mA Buffer Select	$1.0^{(*4)}$	4.0	ns
		8mA Buffer Select	$1.0^{(*4)}$	4.5	ns
Data Setup ^(*3)	t_{DS}		2.3		ns
Data Hold ^(*3)	t_{DH}		0.5		ns

$T_C = -20^{\circ}\text{C}$ to 85°C , $V_{ccInt} = 1.25\text{V} \pm 5\%$, $V_{ccIO} = 2.5\text{V} \pm 0.2\text{V}$

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Data Output ^(*1,2,3)	t_{DO}	16mA Buffer Select	$1.0^{(*4)}$	4.5	ns
		8mA Buffer Select	$1.0^{(*4)}$	5.0	ns
Data Setup ^(*3)	t_{DS}		2.5		ns
Data Hold ^(*3)	t_{DH}		0.5		ns

(*1) Timings are measured from 1.2V of the MasterClk to 1.2V of signal.

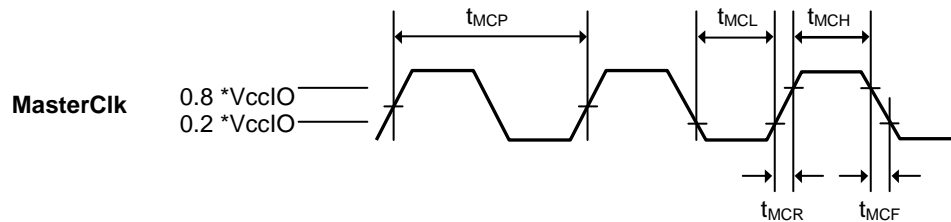
(*2) Capacitive load for all output timings is 25 pF.

(*3) Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the TX9956C on the system interface. Clocks are specified separately.

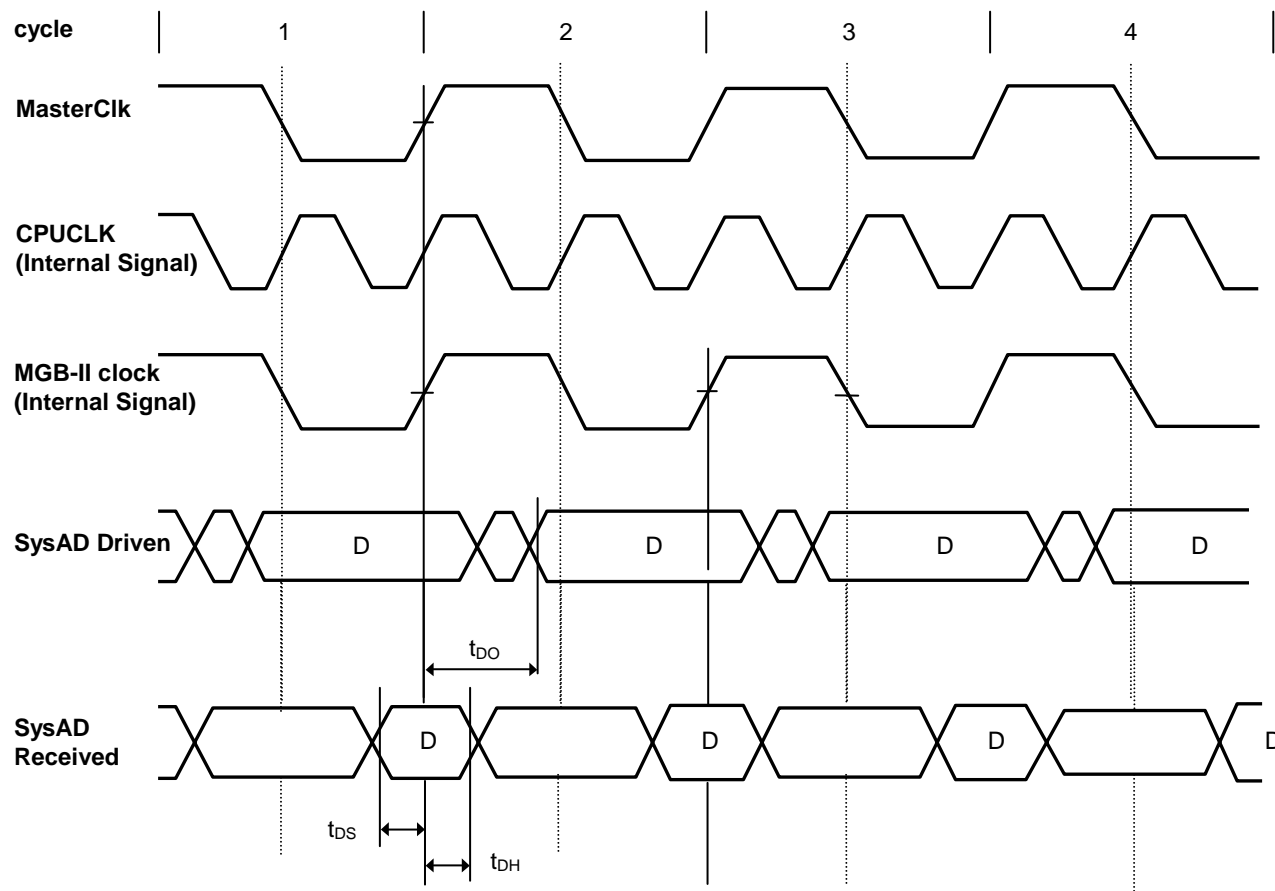
(*4) Guaranteed by the design.

5.5 TIMING DIAGRAMS

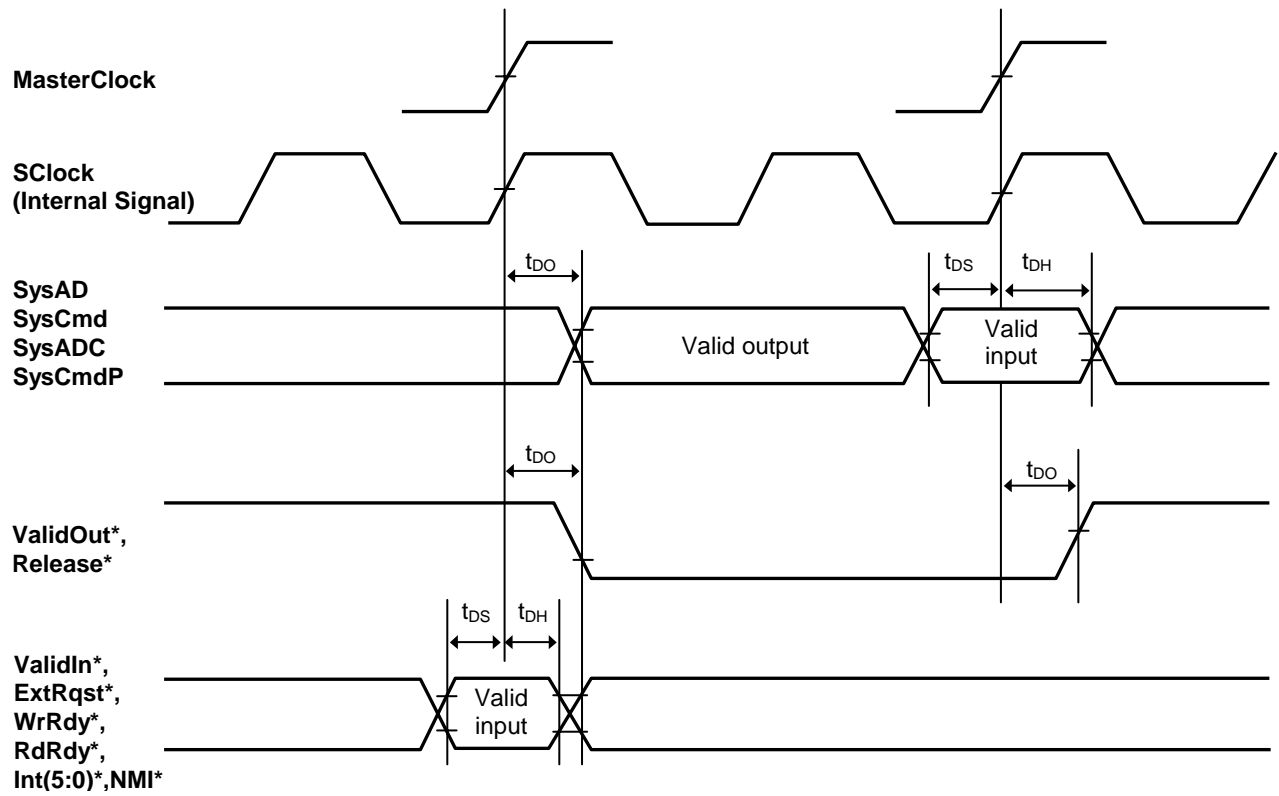
5.5.1 CLOCK TIMING



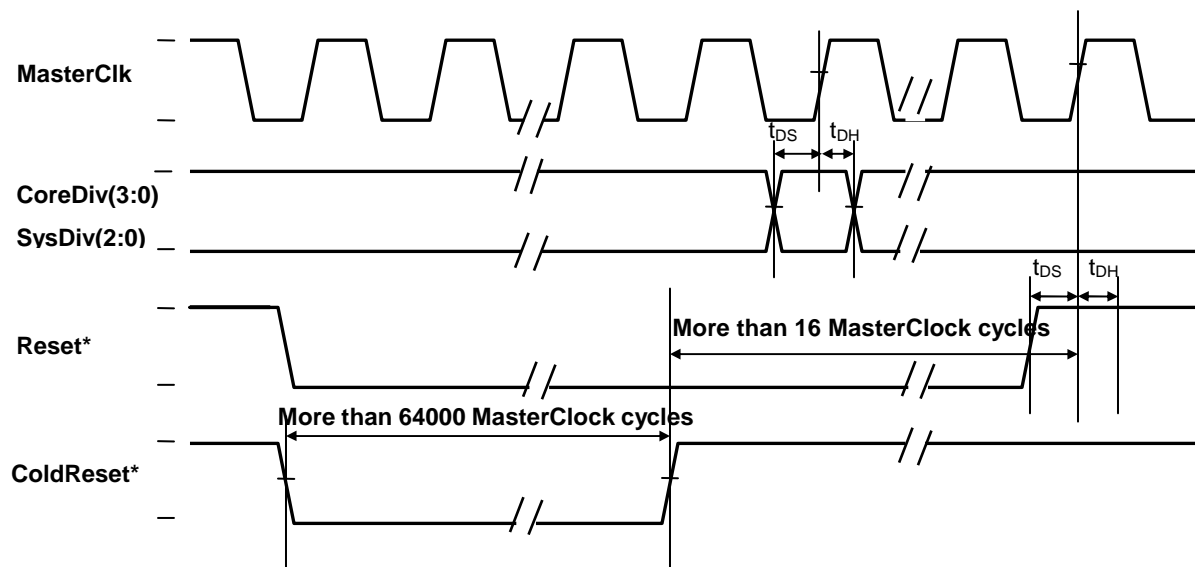
5.5.2 CPUCLK to MGB-II clock DIVISOR of 2



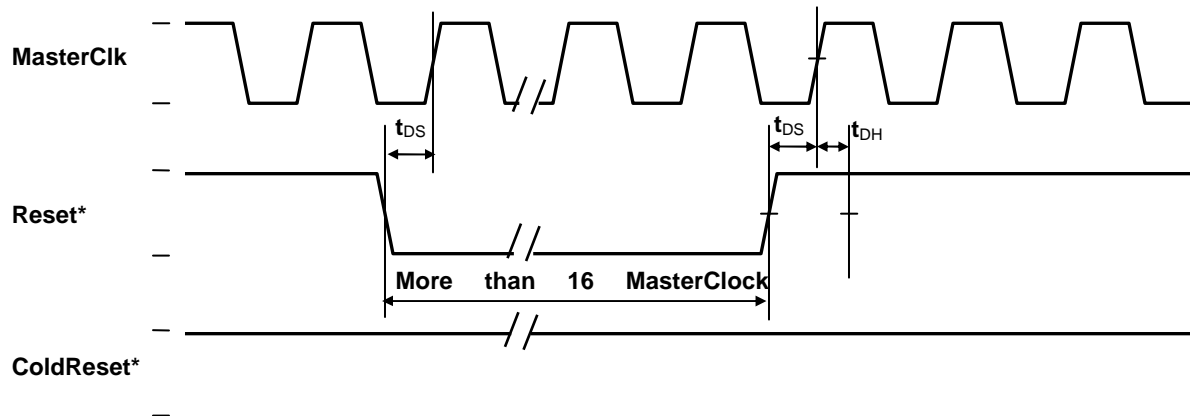
5.5.3 SYSTEM INTERFACE TIMING



5.5.4 COLD RESET TIMING



5.5.5 WARM RESET TIMING



7. PLL Passive Components

The Phase Locked Loop circuit requires several passive components for proper operation, which are connected to VccPLL, and VssPLL, as illustrated in Figure 1.

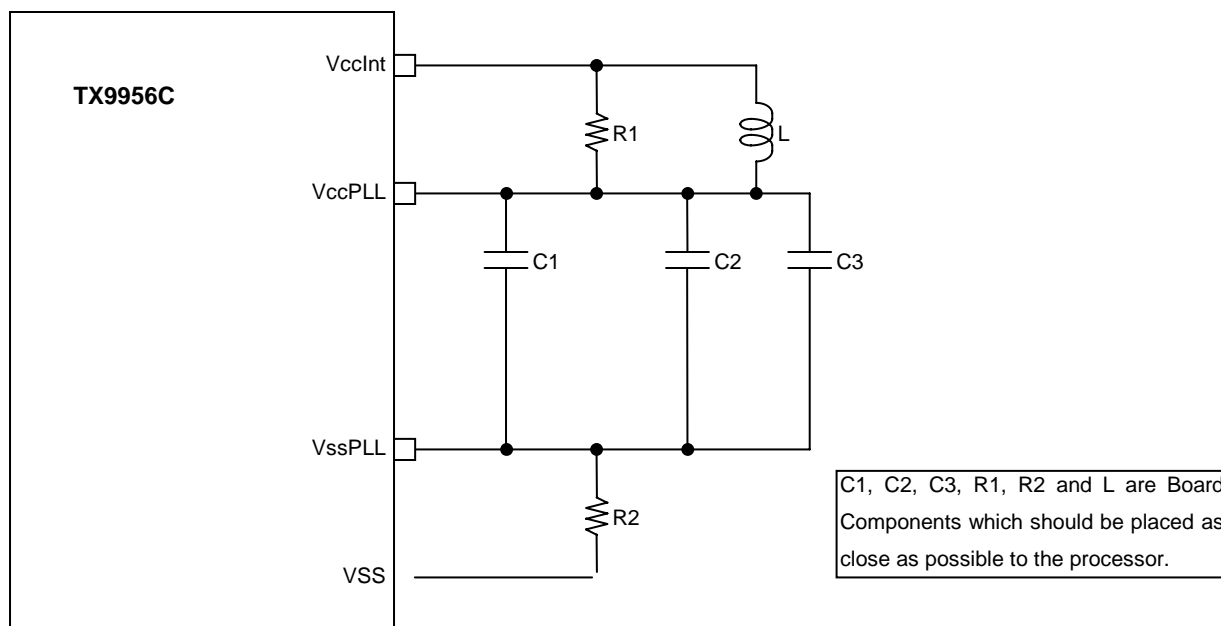


Figure 1 PLL Recommended Circuit

Reference Values:

$$R1 = 5.6 \Omega^{(*1)}$$

$$R2 = 0 \Omega^{(*1)}$$

$$L = 2.2 \mu\text{H}^{(*1)}$$

$$C1 = 1000 \text{ pF}^{(*1)}$$

$$C2 = 0.1 \mu\text{F}^{(*1)}$$

$$C3 = 10 \mu\text{F}^{(*1)}$$

$$V_{\text{ccInt}} = 1.25 \text{ V} \pm 5\%$$

Note *1 : Change to the suitable value on each board

The inductors (L) can be used as alternatives to the resistors (R) to filter the power supply.

It is essential to isolate the analog power and ground for the PLL circuit (VccPLL/VssPLL) from the regular power and ground (VccInt/Vss).

8. History

2002-1-29

2002-2-7 Added Level2 Cache.

2004-3-22 Added Pin-out and Pin Descriptions

2004-4-5 Modified Pin-out (B4)

2004-4-25 Modified Pin-out and AC/DC Specification

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.