

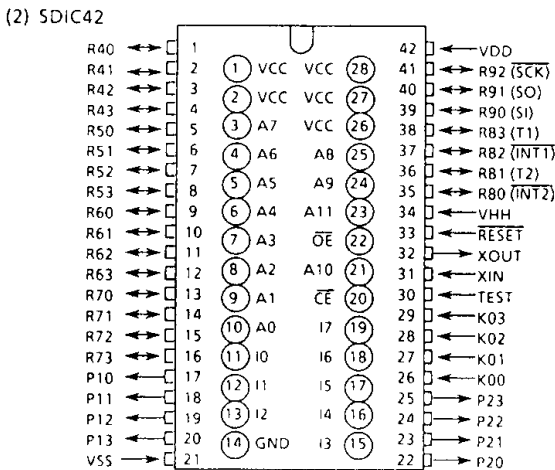
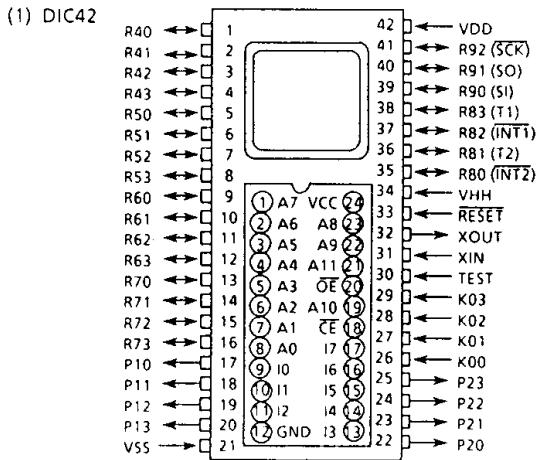
NMOS 4-BIT MICROCONTROLLER

TMP4799C  
TMP4799E

The 4799, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 4720/40 application systems (programs). The 4799C is pin compatible with the 4720/40P which are mask-programmed ROM devices. The 4799E is pin compatible with the 4720/40N. The 4799 which is equipped with an EPROM written the program operates like the 4720/40.

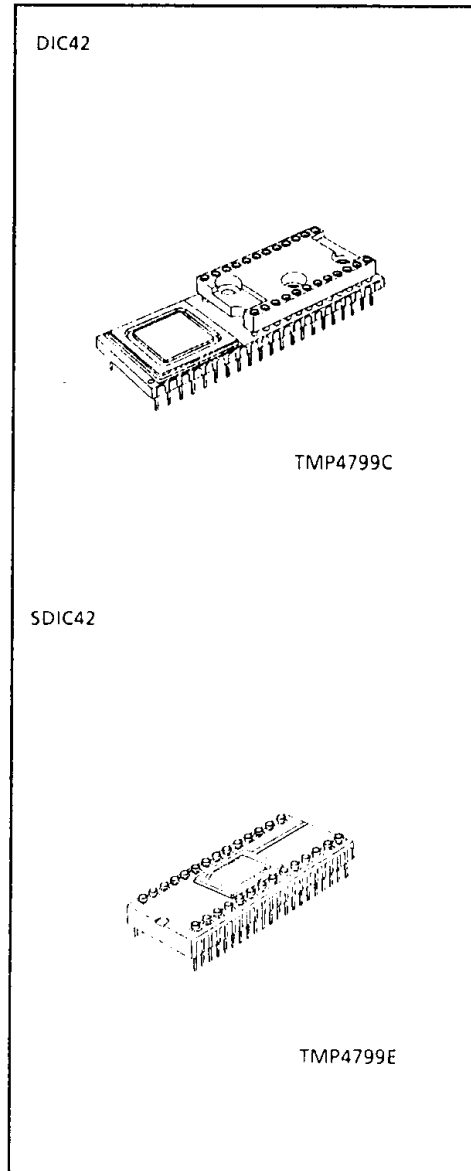
PART No.	ROM	RAM	PACKAGE
TMP4799C	4096 x 8-bit	256 x 4-bit	DIC42
TMP4799E	(External)		SDIC42

PIN ASSIGNMENT (TOP VIEW)



◆ Useable EPROM

- TMP4799C  
32K EPROM: TMM2732AD
- TMP4799E  
32K EPROM: TMM2732AD  
64K EPROM: TMM2764AD



PIN FUNCTION

(1) Top of the package

PIN NAME	Input / Output	FUNCTIONS
A11 - A0	Output	Program memory address output
I7 - I0	Input	Program memory data input
$\bar{C}E$	Output	Chip enable signal output
$\bar{O}E$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

(2) Bottom of the package

Pin compatible with the 4720/40. (As TEST pin does not have pull-down resistor, it must be fixed.)

NOTES FOR USE

(1) Program memory

The program area depends on the capacity of EPROM (See Figure 1).

When this chip is used as evaluator of the 4720A, data conversion table for [OUTB @HL] instruction must be allocated at two areas and they must be the same contents as shown in Figure 1 (a).

When 32K EPROM is used, the pins of 1, 2, 27, and 28 on the package are not used.

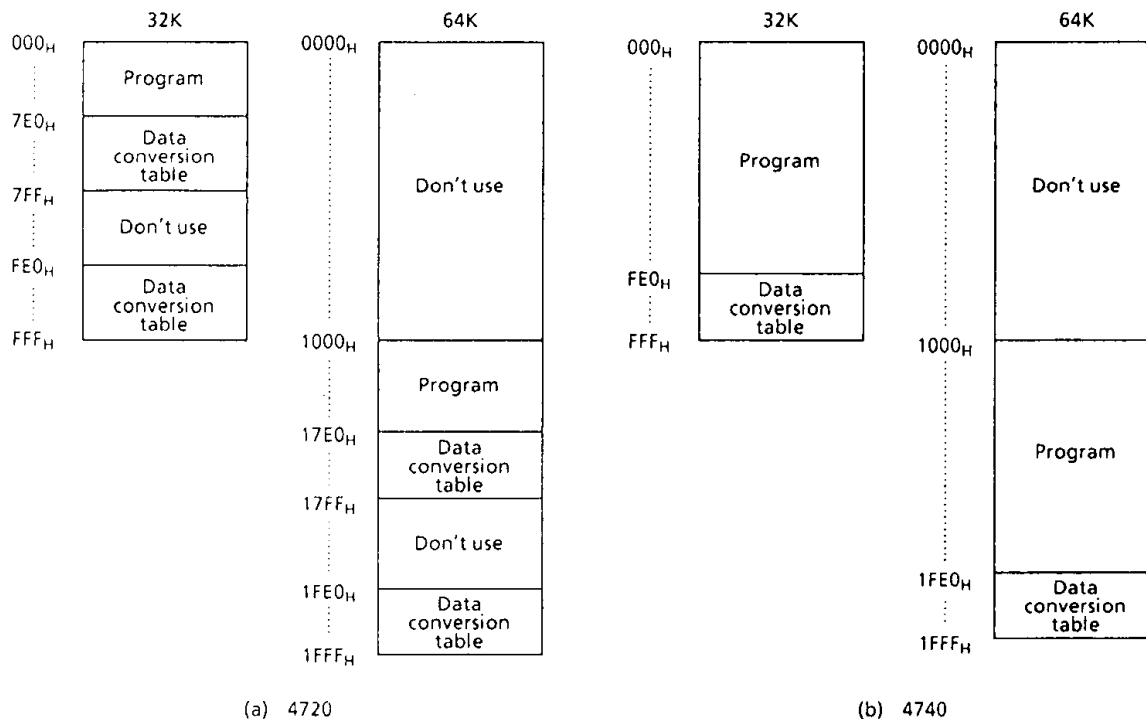


Figure 1. Capacity of EPROM and Program area

(2) Mount

The socket should be used for mounting 4799. When 4799 is soldered on the printed circuit board, the vent hole under the package must not be covered by the solder.

INPUT/OUTPUT CIRCUITRY

(1) Control pins

Control pins of the 4799 are similar to those of the 4720/40 except the following. The 4799 does not have pull-up resistor of  $\overline{\text{RESET}}$  pin (typ.300K $\Omega$ ) and pull-down resistor of TEST pin (typ.70K $\Omega$ ).

(2) I/O ports

The input/output circuitry of 4799 is the same as that of 4720/40 (code: AA). When used for evaluator of other codes (AE, AF, AH, AI), it is necessary to connect an external resistor.

As output latches of ports R4, R5 and R6 in 4799 are initialized to "H", caution is required when using as evaluator of code AH or AI.

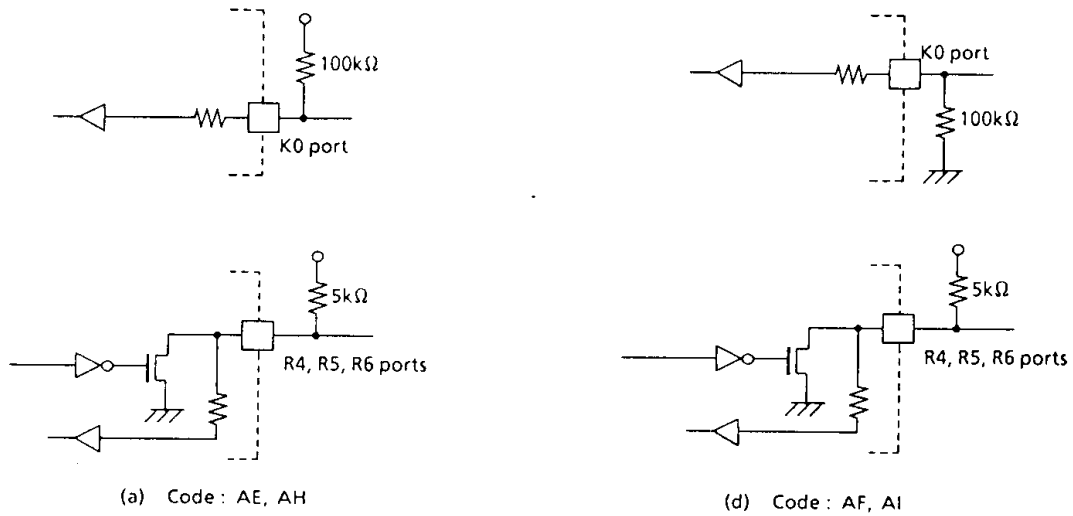


Figure 2. I/O code and external circuitry

## ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATING

 $(V_{SS} = 0V)$ 

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	$V_{DD}$		- 0.5 to 7	V
	$V_{HH}$			
Input Voltage	$V_{IN}$		- 0.5 to 7	V
Output Voltage	$V_{OUT1}$	Except sink open drain pin	- 0.5 to 7	V
	$V_{OUT2}$	Sink open drain pin	- 0.5 to 10	
Output Current (per 1 pin)	$I_{OUT}$	Ports P1, P2	30	mA
Power Dissipation [ $T_{opr} = 70^{\circ}C$ ]	PD		850	mW
Soldering Temperature (Time)	$T_{sld}$		260 (10sec)	$^{\circ}C$
Storage Temperature	$T_{stg}$		- 55 to 125	$^{\circ}C$
Operating Temperature	$T_{opr}$		- 30 to 70	$^{\circ}C$

## RECOMMENDED OPERATING CONDITIONS

 $(V_{SS} = 0V, T_{opr} = - 30 \text{ to } 70^{\circ}C)$ 

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	$V_{DD}$		in the Normal mode	4.5	5.5	V
	$V_{HH}$		in the memory holding mode	3.5		
Input High Voltage	$V_{IH1}$	Ports R4-R7		2.2	$V_{DD}$	V
	$V_{IH2}$	Except Ports R4-R7		3.0		
Input Low Voltage	$V_{IL1}$	Except Port K0		0	0.8	V
	$V_{IL2}$	Port K0			1.2	
Clock Frequency	fc			0.4	4.2	MHz

D.C. CHARACTERISTICS

( $V_{SS} = 0V$ ,  $T_{opr} = -30$  to  $70^{\circ}C$ )

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	$V_{HS}$	Hysteresis Input		—	0.5	—	V
Input Current	$I_{IN1}$	Port K0, $\overline{RESET}$ , $\overline{TEST}$	$V_{DD} = V_{HH} = 5.5V$ , $V_{IN} = 5.5V$	—	—	20	$\mu A$
	$I_{IN2}$	Ports R (open drain)	$V_{DD} = 5.5V$ , $V_{IN} = 5.5V$	—	—	20	
Input Low Current	$I_{IL}$	Ports R with pull-up resistor	$V_{DD} = 5.5V$ , $V_{IN} = 0.4V$	—	—	-2	mA
Output Leakage Current	$I_{LO}$	Open drain ports	$V_{DD} = 5.5V$ , $V_{OUT} = 5.5V$	—	—	20	$\mu A$
Output High Voltage	$V_{OH}$	Ports with pull-up resistor	$V_{DD} = 4.5V$ , $I_{OH} = -200\mu A$	2.4	—	—	V
Output Low Voltage	$V_{OL}$	Except XOUT and ports P1, P2	$V_{DD} = 4.5V$ , $I_{OL} = 1.6mA$	—	—	0.4	
Output Low Current	$I_{OL}$	Ports P1, P2	$V_{DD} = 4.5V$ , $V_{OL} = 1.0V$	—	20	—	mA
Supply Current (in the Normal mode)	$I_{DD} + I_{HH}$		$V_{DD} = V_{HH} = 5.5V$	—	70	120	mA
Supply Current (in the memory holding mode)	$I_{HH}$		$V_{DD} = V_{SS}$ , $V_{HH} = 3.5V$	—	5	10	

Note 1. *Typ. values show those at  $T_{opr} = 25^{\circ}C$ ,  $V_{DD} = 5V$ .*

Note 2. *Input Current  $I_{IN1}$ : The current flowing through resistor is not included, when the pull-up/pull-down resistor is contained.*

A.C. CHARACTERISTICS

( $V_{SS} = 0V$ ,  $V_{DD} = V_{HH} = 4.5$  to  $5.5V$ ,  $T_{opr} = -30$  to  $70^{\circ}C$ )

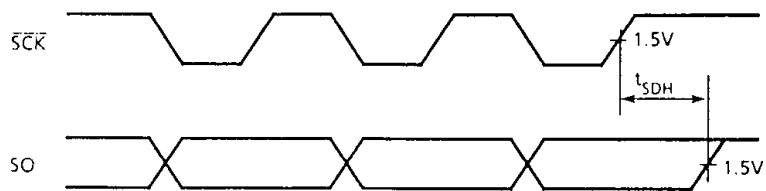
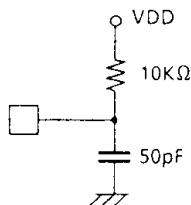
(1)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	$t_{cy}$	For external clock operation	1.9	—	20	$\mu s$
High level Clock Pulse Width	$t_{WCH}$		80	—	—	ns
Low level Clock Pulse Width	$t_{WCL}$		—	—	—	ns
Shift data Hold Time	$t_{SDH}$		$0.5t_{cy} - 300$	—	—	ns

Note. *Shift data Hold Time:*

External circuit for  $\overline{SCK}$  pin and SO pin

Serial port (completion of transmission)



(2)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	$t_{AD}$	$C_L = 100\text{pF}$	—	—	150	ns
Data Setup Time	$t_{IS}$		150	—	—	ns
Data Hold Time	$t_{IH}$		50	—	—	ns

## RECOMMENDED OSCILLATING CONDITIONS

 $(V_{SS} = 0\text{V}, V_{DD} = V_{HH} = 4.5 \text{ to } 5.5\text{V}, T_{opr} = -30 \text{ to } 70^\circ\text{C})$ 

Refer to technical data sheets for the 4720/40.

This datasheet has been downloaded from:

[www.DatasheetCatalog.com](http://www.DatasheetCatalog.com)

Datasheets for electronic components.