TM5500/TM5800 Data Book

June 26, 2002

TRANSMETA™

Crusoe™ Processor Model TM5500/TM5800
Data Book
Revision 0.3

Revision History:

0.1	Preliminary first draft
0.2	June 13, 2001 - first release
0.3	June 26, 2002 - added 867, 900 MHz SKUs, updated memory interface descriptions, updated LongRun tables

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Introduction

The Transmeta Crusoe™ processor model TM5500/TM5800 is a high performance, low power microprocessor based on a VLIW core architecture. When combined with Transmeta's x86 Code Morphing™ software, the TM5500/TM5800 processor provides x86-compatible code execution. TM5500/TM5800 processors deliver highly integrated, cost-effective processor solutions, incorporating L2 cache, support for single data rate (SDR) and double data rate (DDR) SDRAM, and a PCI controller. TM5500/TM5800 processors also provide power management controls, SMM and thermal monitoring capabilities, and operate at very voltage levels, making them ideal for mobile applications.

Crusoe™ Processor Model TM5500/TM5800 Features

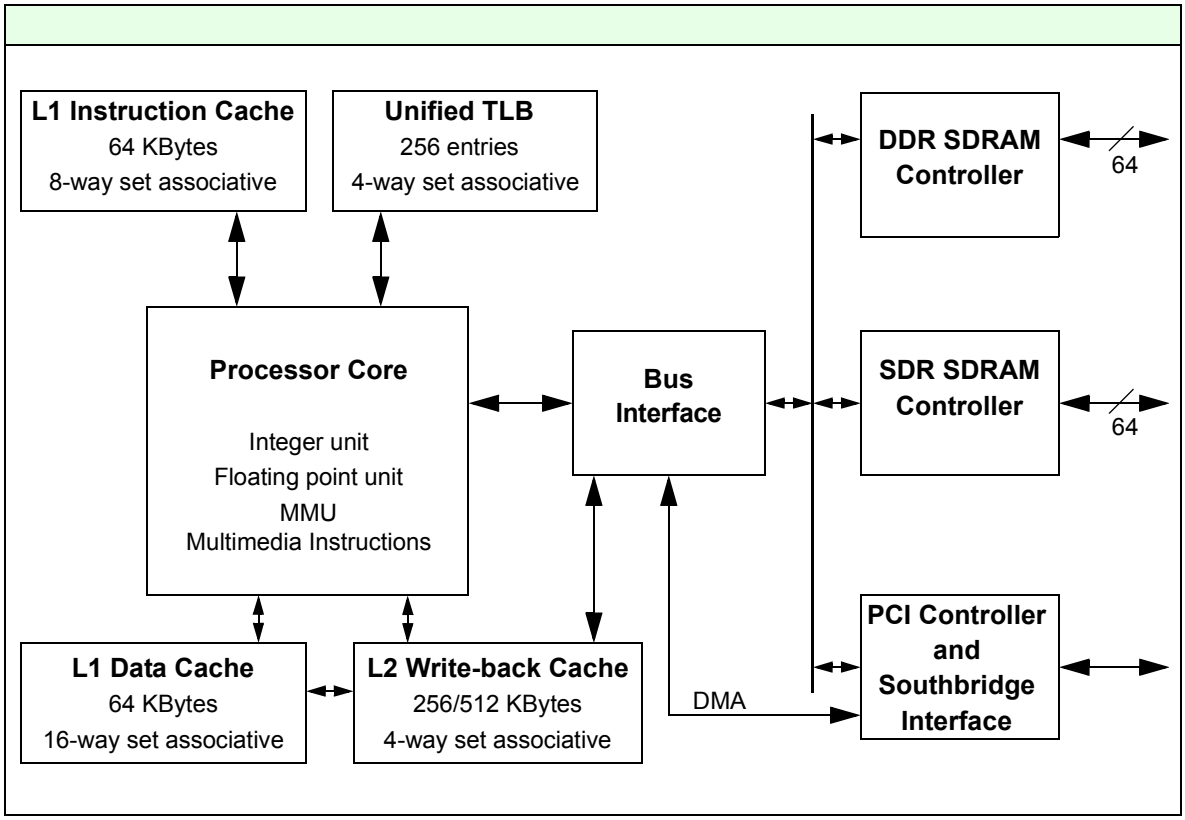
- VLIW processor and x86 Code Morphing™ software provides x86-compatible mobile platform solution
- 667, 700, 733, 800, 867, 900 MHz operating frequencies
- Integrated 64 KByte L1 instruction and data caches, and 256 KByte (TM5500) or 512 KByte (TM5800) L2 write-back cache
- Integrated northbridge core logic features facilitate compact system designs
  - DDR SDRAM memory controller with 83-133 MHz, 2.5 V interface
  - SDR SDRAM memory controller with 66-133 MHz, 3.3 V interface
  - PCI bus controller (PCI 2.1 compliant) with 33 MHz, 3.3 V interface
- LongRun™ advanced power management with ultra-low power operation extends battery life
  - < 1 W running typical multimedia applications
  - < 250 mW in deep sleep
- LongRun™ thermal management (CoolRun) dynamically adapts to system thermal environment
- Power management controls for ACPI-compliant modes
- Full System Management Mode (SMM) support
- Compact 474-contact ceramic ball-grid array (CBGA) package

The processor core operates from a 0.95-1.30 V supply, resulting in extremely low power consumption even at high operating frequencies. The processor typically consumes below 1 Watt under normal operating conditions. When operating in deep sleep, power consumption drops below 250 mW.

Architectural Overview

The Transmeta Crusoe processor model TM5500/TM5800 is an ultra-low power, high-speed microprocessor based on an advanced VLIW core architecture. When used in conjunction with Transmeta's x86 Code Morphing software, the TM5500/TM5800 processor provides x86-compatible software execution using dynamic binary code translation, without requiring code recompilation. In addition to the VLIW core, the processor incorporates separate 64 KByte L1 instruction and data caches, a large L2 write-back cache (256 KBytes on TM5500, 512 KBytes on TM5800), a 64-bit DDR SDRAM memory controller, a 64-bit SDR SDRAM memory controller, and a 32-bit PCI controller. These additional functional units, which are typically part of the chipset system logic that surrounds the microprocessor, allow the TM5500/TM5800 processor to provide a highly-integrated, cost-effective solution for x86 platforms requiring superior energy efficiency, low power consumption, and low thermal generation. Figure 1 shows a block diagram of the Crusoe TM5500/TM5800 processor.

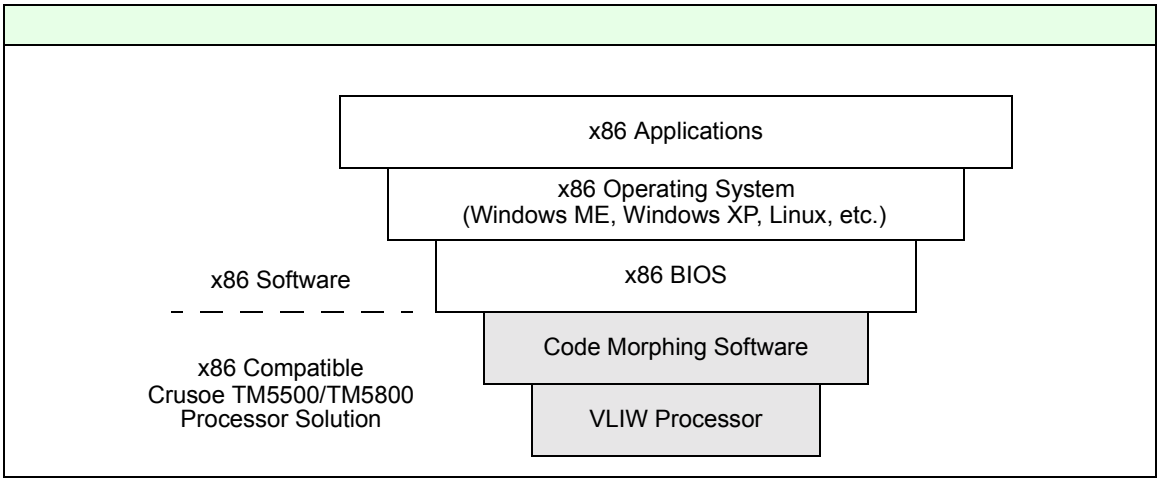
Figure 1: Crusoe TM5500/TM5800 Processor Block Diagram



The TM5500/TM5800 processor core is based on a Very Long Instruction Word (VLIW) instruction set of 64 or 128 bits. Within this VLIW architecture, the control logic of the processor is kept very simple, and software is used to control the scheduling of instructions. This allows a simplified and very straightforward hardware implementation with an in-order 7-stage integer pipeline and a 10-stage floating point pipeline. By streamlining the processor hardware and reducing control logic transistor count, the performance-to-power consumption ratio (energy efficiency) can be greatly improved over traditional x86 architectures.

In addition to having the execution hardware for logical, arithmetic, shift, and floating point instructions, as in conventional processors, the TM5500/TM5800 processor uses a combination of software and hardware to offer full x86 compatibility. The processor hardware generates the same condition codes as conventional x86 processors and operates on the same 80-bit floating point numbers. Also, the translation look-aside buffer (TLB) has the same protection bits and address mapping as x86 processors. The software component of this processor solution is used to emulate all other features of the x86 architecture. The software that converts x86 programs into the core VLIW instructions is called Code Morphing software. The combination of Code Morphing software and the VLIW core together act as an x86-compatible processor solution, as shown in Figure 2.

Figure 2: Crusoe TM5500/TM5800 Processor Software Hierarchy



The typical behavior of Code Morphing software is to execute a loop, which decodes and executes x86 instructions. The first few times a specific x86 code sequence is executed, Code Morphing software interprets the code by decoding the instructions one at a time and then dispatching execution to corresponding VLIW native instruction subroutines. Once the x86 code has been executed several times, Code Morphing software translates the x86 instructions into highly optimized and extremely fast native VLIW instructions, executes the translated code, and caches the native instruction translations for future use. If the same x86 code is required to execute again, the high-performance cached translations are executed immediately and no re-translation is required.

Reference Documents

The following documents should be used in conjunction with this specification:

- *TM5500/TM5800 Package Specifications and Manufacturing Guide*
- *TM5500/TM5800 System Design Guide*
- *TM5500/TM5800 Thermal Design Guide*
- *TM5500/TM5800 Development and Manufacturing Guide*
- *TM5500/TM5800 BSDL Test File*
- *TM5500/TM5800 IBIS Models*
- *TM5500/TM5800/Code Morphing Software Version 4.x BIOS Programmer's Guide*
- *TM5500/TM5800/Code Morphing Software Version 4.x Release Notes*
- *TM5500/TM5800/Code Morphing Software Version 4.x Errata*
- *PCI Local Bus Specification*

Chapter 1

Functional Interface Description

1.1 Power and Thermal Management

1.1.1 Power Management States

TM5500/TM5800 processors, in conjunction with Code Morphing software, support ACPI-compliant power management modes. Table 1 lists the state of the TM5500/TM5800 processor for each of the ACPI global system states. The power management states listed in Table 1 are defined in greater detail in Table 2 and the following paragraphs. TM5500/TM5800 processor power management states and state transitions are shown in Figure 3.

Table 1: System Power Management States

ACPI System State		Processor State	SDRAM	Clock Generator	Delay to Return to C0 State [1]
G0 / S0 / C0	Working	Normal	Normal	Running	-
G0 / S0 / C1	Auto Halt	Auto Halt	Normal/ self-refresh [2]	Running	< 260 nS
G0 / S0 / C2	Quick Start	Quick Start	Self-refresh	Running	< 2.8 µS
G0 / S0 / C3	Deep Sleep	Deep Sleep	Self-refresh	CLKIN stopped	< 20 µS
G1 / S1	Sleeping	Deep Sleep	Self-refresh	PLL shut down	< 20 µS
G1 / S3	Suspend-to-RAM	Off	Self-refresh	PLL shut down	10 mS + BIOS
G1 / S4	Suspend-to-Disk	Off	Off	Off	< 30 S
G2 / S5	Soft Off	Off	Off	Off	-
G3	Mechanical Off	Off	Off	Off	-

1. Delay times specified may vary depending on core operating frequency, memory type and speed, and system device response times.
2. In C1, SDR can be put into self-refresh if the OEM configuration variable pm_control has bit 2 set. DDR cannot be put into self-refresh in C1. See the *TM5500/TM5800 Development and Manufacturing Guide* for details.

Table 2: Processor Power Management States

Processor		SDRAM	PCI Controller	Entry Trigger	Snoops	Interrupts
State	Core					
Normal	Running	Running	Running	Normal operation	Serviced	Serviced
Auto Halt	Stopped	Running	Running	Executing a HLT instruction	Serviced	Serviced
Quick Start	Stopped	Self refresh	Running	Asserting STPCLK#	Serviced	Latched
Deep Sleep	Stopped	Self refresh	Stopped	Asserting SLEEP# and stopping CLKIN while in Quick Start state	Not allowed	Not allowed

Auto Halt

The Auto Halt state is a low-power mode entered through the execution of the HLT instruction. The Auto Halt state is exited upon an interrupt (INTR, INIT#, SMI# or NMI) or assertion of RESET#. Snoops are serviced while in the Auto Halt state.

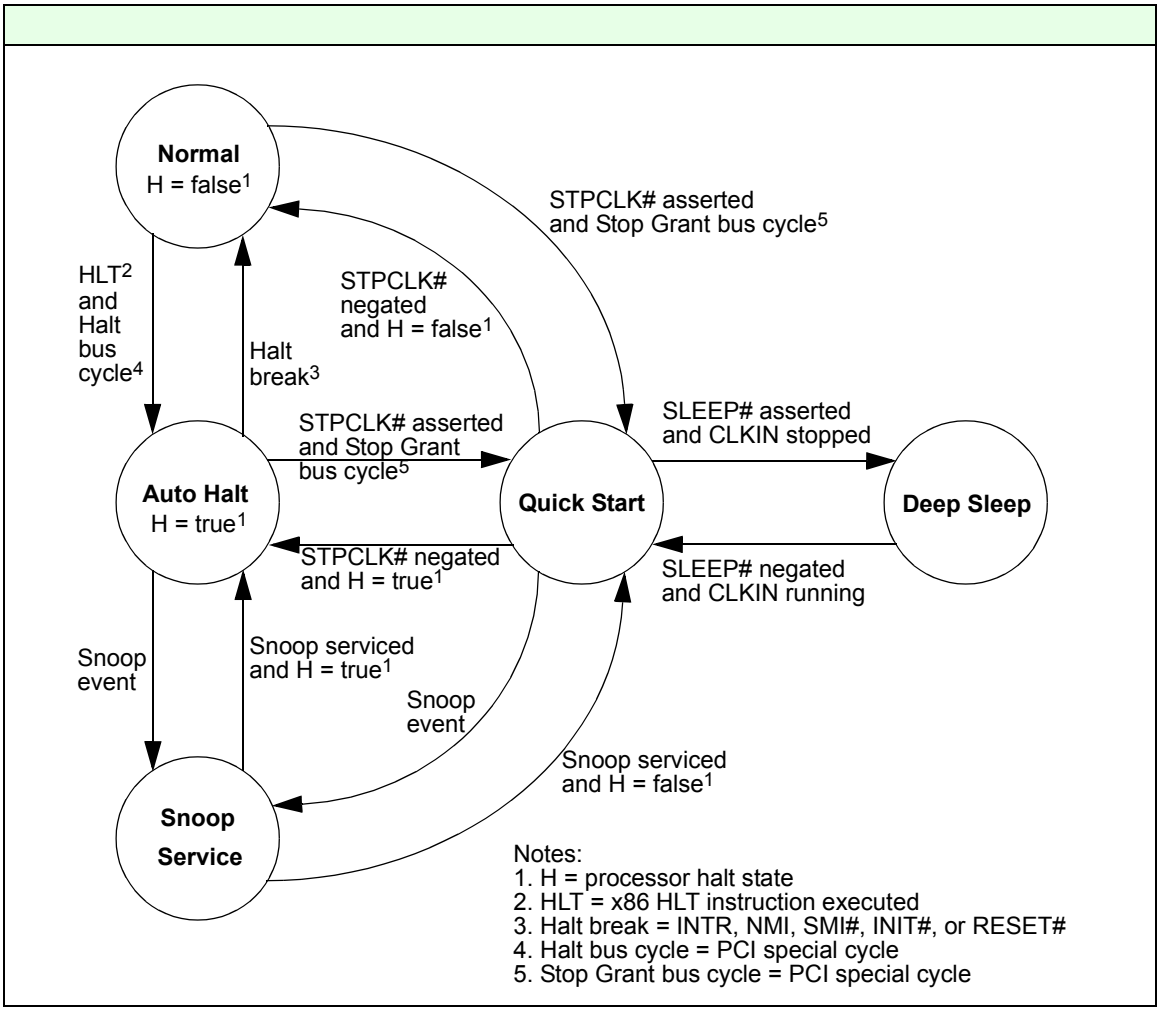
Quick Start

The Quick Start state is entered with the assertion of the STPCLK# input signal. While in Quick Start, snoops are serviced and interrupts are latched. Latched interrupts are serviced once the processor returns to the Normal state. Only one occurrence of an interrupt is latched while in Quick Start. If RESET# is asserted while in Quick Start, processor initialization occurs and then the processor returns to the Quick Start state if STPCLK# is still asserted.

Deep Sleep

The Deep Sleep state is a very low power state that the processor can enter while still maintaining its context. After entering the Quick Start state, the processor enters Deep Sleep when SLEEP# is asserted and the master clock input (CLKIN) is stopped. The PCI clock input (P_PCLK) may also be stopped. The processor internal PLL is shutdown while in Deep Sleep. Therefore, when the clocks are restarted to exit Deep Sleep, the system must allow time for PLL resynchronization. Snoops are not serviced and interrupts are neither serviced nor latched while in Deep Sleep. RESET# is ignored while in Deep Sleep.

Figure 3: Power Management State Diagram

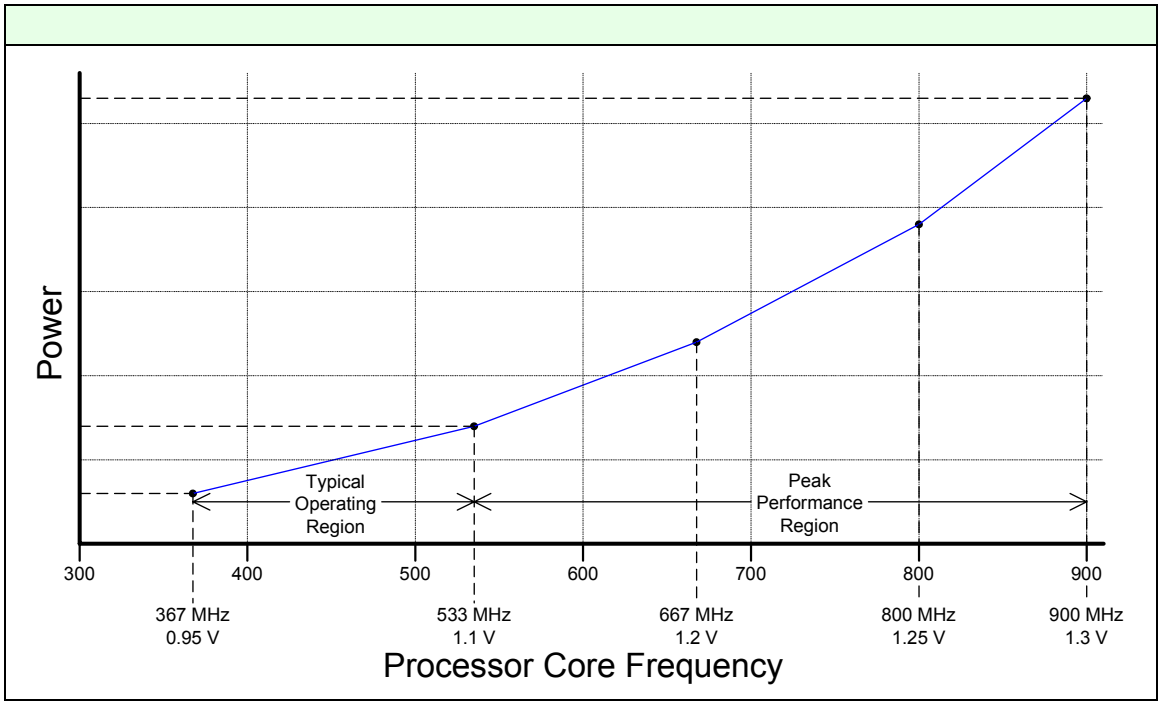


1.1.2 LongRun Power Management

LongRun power management technology provides Code Morphing software with the ability to adjust the TM5500/TM5800 processor core operating voltage and clock frequency dynamically, depending on the demands placed on the processor by software. Because power varies linearly with clock speed and by the square of voltage, adjusting both processor voltage and clock frequency can produce cubic reductions in power consumption, whereas conventional processors can adjust power linearly only by adjusting the effective operating frequency.

The LongRun policies are implemented within the Code Morphing software and can detect different workload scenarios based on runtime performance information, and then exploit these by adapting processor power usage accordingly. This ensures the processor delivers high performance when necessary and conserves power when demand on the processor is low. All power adjustments are transparent to the operating system, power management controller, and the user. LongRun power management uses a number of core frequency/voltage operating points, allowing TM5500/TM5800 processors to optimize for the lowest power and maximum performance along this curve, as shown in the figure below.

Figure 4: LongRun Power Management Operating Points



Most conventional x86 processors utilize ACPI policies to regulate their power consumption, the processor rapidly alternating between running at full-speed and being effectively turned off (called clock-throttling). This approach can potentially disable the processor just when a critical application needs it. In contrast, LongRun power management dynamically picks just the right clock speed and operating voltage needed to run the application, thereby allowing maximum energy efficiency. LongRun power management works in conjunction with ACPI. When the processor frequency and voltage scaling reaches the minimum LongRun power management setpoint, the processor transparently switches over to traditional power models, allowing policies such as ACPI to handle power management at very low power operating points.

During LongRun power management operation, the processor memory interface frequencies are also changed dynamically to keep the memory interfaces synchronized with the core frequency. LongRun power management core frequency, core voltage, and memory interface frequency configurations are provided in Table 3. Information on LongRun power management configuration is provided in *TM5500/TM5800 Development and Manufacturing Guide*.

Table 3: LongRun Power Management Specifications

Processor				Memory Interface				
	Core			DDR-266	DDR-200	SDR-133	SDR-125	SDR-100
SKU	MHz	V	T_j max	MHz	MHz	MHz	MHz	MHz
900	900	1.30	100 °C 90 °C [1]	129	100	129	113	100
	800	1.25		133	100	133	114	100
	667	1.2		133	95	133	111	95
	533	1.1		133	89	133	107	89
	367	0.95		122	92	122	122	92
867	867	1.30	100 °C 90 °C [1]	124	96	124	124	96
	800	1.25		133	100	133	114	100
	667	1.2		133	95	133	111	95
	533	1.1		133	89	133	107	89
	367	0.95		122	92	122	122	92
800	800	1.30	100 °C	133	100	133	114	100
	733	1.25		122	92	122	122	92
	667	1.2		133	95	133	111	95
	533	1.1		133	89	133	107	89
	367	0.95		122	92	122	122	92
733	733	1.30	100 °C	122	92	122	122	92
	667	1.25		133	95	133	111	95
	533	1.15		133	89	133	107	89
	400	1.05		133	100	133	100	100
	333	0.95		111	83	111	111	83
700	700	1.30	100 °C	117	100	117	117	100
	667	1.25		133	95	133	111	95
	533	1.15		133	89	133	107	89
	400	1.05		133	100	133	100	100
	333	0.95		111	83	111	111	83
667	667	1.30	100 °C	133	95	133	111	95
	600	1.25		120	100	120	120	100
	500	1.15		125	100	125	125	100
	367	1.0		122	92	122	122	92
	300	0.95		100	100	100	100	100

1. Maximum junction temperature specification depends on SKU. See *Package Marking Descriptions* on page 89 for details on device temperature package marking identifier.

1.1.3 LongRun Thermal Management

Thermal management of TM5500/TM5800 processors is integrated into the LongRun power management frequency/voltage ramp policies. The LongRun thermal management policy manages the TM5500/TM5800 processor thermal environment by using frequency/voltage shifts as a substitute for thermal throttling. In contrast to conventional thermal management techniques, LongRun thermal management delivers higher performance at the same die temperature, or the same performance at a lower die temperature. LongRun thermal management essentially expands the thermal budget of the processor. LongRun thermal management maximizes system performance and maintains safe processor operating temperatures within constrained thermal environments.

LongRun thermal management is recommended for all TM5500/TM5800 processor-based systems. Implementation details for LongRun thermal management are described in the TM5500/TM5800 technical bulletin *LongRun Thermal Management Implementation Guide*.

1.1.4 Processor Thermal Monitoring

TM5500/TM5800 processors provide an integrated on-die thermal diode. This 2-terminal (DIODE_ANODE, DIODE_CATHODE) thermal diode can be connected to an external temperature sensor and the processor junction temperature monitored by system BIOS and application software.

Thermal Diode Accuracy

The TM5500/TM5800 processor on-die thermal diode, when used in conjunction with a Maxim MAX1617MEE (standard part) temperature sensor, will provide a temperature accuracy of ± 3°C from 0 to 100°C.

1.1.5 SDRAM Power Saving Modes

In addition to the power management states defined in previous sections, TM5500/TM5800 processors provide additional power saving modes for DDR and SDR SDRAM. These power saving modes can be enabled during normal operation by programming processor-specific PSR configuration registers (CD_MISC for DDR SDRAM, SD_MISC for SDR SDRAM). In these power saving modes, the clock enable lines to the SDRAM are active only when the SDRAM is being accessed or refreshed. This decreases power dissipation, but increases the latency for a memory cycle by one SDRAM clock. Refer to the *TM5500/TM5800 BIOS Programmer's Guide* and the *TM5500/TM5800 Development and Manufacturing Guide* for power saving mode programming information.

1.2 Memory Interfaces

1.2.1 DDR SDRAM Interface

The DDR (double data-rate) SDRAM interface is the highest performance memory interface available on TM5500/TM5800 processors. The DDR controller supports only DDR SDRAM and transfers data at a rate that is twice the clock frequency of the interface. The DDR SDRAM controller supports the equivalent of one DIMM (one bank only) of DDR SDRAM using a 64-bit wide interface. The DDR SDRAM interface does not support parity bits.

The DDR SDRAM can be populated with 64-Mbit, 128-Mbit, 256-Mbit, or 512-Mbit devices. For the highest performance, it is recommended that the DDR SDRAM devices be soldered down to the circuit board, rather than incorporated on DIMMs. The DDR SDRAM interface supports only x8 or x16 devices. Table 4 shows possibleTM5500/TM5800 DDR SDRAM configurations.

Table 4: DDR SDRAM Memory Configurations

DDR Device Size (Mbits)	DDR Device Configuration	Number of Devices per Bank	Memory Size per Bank (MBytes)	Maximum Banks	Maximum Memory Size (MBytes)
64	4M x 16	4	32	1	32
	8M x 8	8	64	1	64
128	8M x 16	4	64	1	64
	16M x 8	8	128	1	128
256	16M x 16	4	128	1	128
	32M x 8	8	256	1	256
512	32M x 16	4	256	1	256
	64M x 8	8	512	1	512

The frequency setting for the DDR SDRAM interface is initialized during the boot sequence from data stored in the configuration ROM. Although the processor can be configured for a DDR interface frequency in the range of 1/2 to 1/15 of the core frequency, the supported interface frequency is restricted to a minimum of 83 MHz and a maximum of 133 MHz. DDR frequency settings vary at each LongRun power management step. DDR interface frequencies at various LongRun power management steps are shown in Table 3.

With LongRun power management enabled, the processor core frequency is lowered during times when peak performance is not required. When the core frequency changes, the DDR interface frequency is recalculated to match the new core frequency setting. For example, a 733 MHz device with a 122 MHz memory interface may have a LongRun setting of 533 MHz with a 133 MHz memory interface. Therefore, TM5500/TM5800 processor-based systems that use LongRun power management must support the entire DDR SDRAM interface frequency range of 83 MHz to 133 MHz.

1.2.2 DDR Memory Interface Constraints

- The DDR SDRAM interface cannot drive more than eight unbuffered loads (devices). See Table 6 for supported DDR memory configurations. Choose configurations that minimize the number of loads. Use the largest capacity devices possible for a given total memory size.
- Buffered or registered DDR memory DIMMs are not supported.
- All DDR SDRAM devices in the system must be configured the same. Mixing different speed, size, or geometry DDR devices is not supported.
- The maximum DDR SDRAM interface operating frequency is 133 MHz. Placing the DDR devices down on the motherboard is recommended for best high-speed signal integrity. Follow the DDR interface layout and routing guidelines in *TM5500/TM5800 System Design Guide*.
- DDR memory is not user expandable. SDR memory must be used for user-installed expansion memory.

1.2.3 SDR SDRAM Interface

The SDR SDRAM controller supports up to two 64-bit DIMMs (up to four banks) of single data rate SDRAM. The SDR SDRAM interface does not support parity bits. SDR DIMMs can be populated with 64-Mbit, 128-Mbit, 256-Mbit, or 512-Mbit devices. All DIMMs must use the same frequency SDRAMs, but there are no restrictions on mixing different DIMM configurations in the two DIMM slots. Table 5 shows possible SDR SDRAM configurations for a TM5500/TM5800-based system. The maximum memory size in Table 5 assumes two double-sided DIMMs of identical configuration and a maximum of 8 total devices per DIMM.

Table 5: SDR SDRAM Memory Configurations

SDR Device Size (Mbits)	SDR Device Configuration	Number of Devices per Bank	Memory Size per Bank (MBytes)	Maximum Banks	Maximum Memory Size (MBytes)
64	4M x 16	4	32	4	128
	8M x 8	8	64	2	
	16M x 4	16	128	1	
128	8M x 16	4	64	4	256
	16M x 8	8	128	2	
	32M x 4	16	256	1	
256	16M x 16	4	128	4	512
	32M x 8	8	256	2	
	64M x 4	16	512	1	
512	32M x 16	4	256	4	1024
	64M x 8	8	512	2	

The frequency setting for the SDR SDRAM interface is initialized during the boot sequence from data stored in the configuration ROM. Although the processor can be configured for an SDR interface frequency in the range of 1/2 to 1/15 of the core frequency, the supported interface frequency is restricted to a minimum of 66 MHz and a maximum of 133 MHz. SDR frequency settings vary at each LongRun power management step. SDR interface frequencies at various LongRun power management steps are shown in Table 3. It is also recommended that a maximum of 8 devices per DIMM be used in order to operate at the specified frequencies with the proper signal integrity.

With LongRun power management enabled, the processor core frequency is lowered during times when peak performance is not required. When the core frequency changes, the SDR interface frequency is recalculated to match the new core frequency setting. For example, a 733 MHz device with a 122 MHz memory interface may have a LongRun setting of 533 MHz with a 133 MHz memory interface. Therefore, TM5500/TM5800 processor-based systems that use LongRun power management must support the entire SDR SDRAM interface frequency range of 66 MHz to 133 MHz.

1.2.4 SDR Memory Interface Constraints

- The SDR SDRAM interface cannot drive more than sixteen unbuffered loads (devices). See Table 7 for supported SDR memory configurations. Choose configurations that minimize the number of loads. Use the largest capacity devices possible for a given memory size.
- Different SDR memory banks can have different size or geometry devices. The SDR memory interface will automatically be adjusted to run at the speed of the slowest installed SDR SDRAM memory. It is strongly recommended that all SDR memory installed in the system be the same speed.
- The maximum unbuffered SDR SDRAM interface operating frequency is 133 MHz. Follow the SDR interface layout and routing guidelines in *TM5500/TM5800 System Design Guide*.
- SDR SDRAM configurations requiring more than sixteen loads must use buffered SDR memory.
- The maximum industry-standard buffered SDR SDRAM operating frequency is 66 MHz. The maximum processor SDR SDRAM interface operating frequency is 133 MHz. Therefore, the processor SDR SDRAM interface operating frequency must be set below the standard LongRun power management table frequency values provided in this document and in the *TM5500/TM5800 Development and Manufacturing Guide*. Follow the SDR interface layout and routing guidelines in *TM5500/TM5800 System Design Guide*.
- SDR memory can be user expandable. SDR SDRAM is the only user-installed expansion memory option available for TM5500/TM5800 processors.

1.3 System Memory Configurations

Possible and recommended system memory configurations for TM5500/TM5800 processor-based systems are discussed in this section. As described previously, TM5500/TM5800 processors have two independent memory interfaces, a DDR SDRAM interface, and a SDR SDRAM interface. The DDR SDRAM interface offers higher performance and lower power operation compared to the SDR SDRAM interface.

1.3.1 Recommended Memory Configurations

The preferred memory configuration for TM5500/TM5800 processor-based systems is to use a fixed amount of DDR SDRAM for the system base memory configuration, with SDR SDRAM μDIMM/SODIMM/DIMM expansion memory slots. This provides the highest possible system performance, with a high degree of expansion memory flexibility. Table 6 and Table 7 below show possible DDR and SDR memory configurations, with recommended configurations **highlighted**.

DDR SDRAM Base Memory

Table 6: DDR SDRAM Base Memory Configurations

Device Size (Mbits)	Device Organization	Total Devices	Total Banks	Total Memory (MBytes)
64	4M x 16	4	1	32
	8M x 8	8	1	64
128	8M x 16	4	1	64
	16M x 8	8	1	128
256	**16M x 16**	**4**	**1**	**128**
	32M x 8	**8**	**1**	**256**
512	**32M x 16**	**4**	**1**	**256**
	64M x 8	**8**	**1**	**512**

SDR SDRAM Base or Expansion Memory

Table 7: SDR SDRAM Base or Expansion Memory Configurations

Slot 1					Slot 2				
Device Size (Mbits)	Device Organization	Total Devices	Total Banks	Total Memory (MBytes)	Device Size (Mbits)	Device Organization	Total Devices	Total Banks	Total Memory (MBytes)
64	4M x 16	8	2	64	64	4M x 16	8	2	64
	8M x 8	8	1	64		8M x 8	8	1	64
128	**8M x 16**	**4**	**1**	**64**	128	**8M x 16**	**4**	**1**	**64**
	8M x 16	**8**	**2**	**128**		**8M x 16**	**8**	**2**	**128**
	16M x 8	**8**	**1**	**128**		**16M x 8**	**8**	**1**	**128**
256	**16M x 16**	**4**	**1**	**128**	256	**16M x 16**	**4**	**1**	**128**
	16M x 16	**8**	**2**	**256**		**16M x 16**	**8**	**2**	**256**
	32M x 8	**8**	**1**	**256**		**32M x 8**	**8**	**1**	**256**
512	**32M x 16**	**4**	**1**	**256**	512	**32M x 16**	**4**	**1**	**256**
	32M x 16	**8**	**2**	**512**		**32M x 16**	**8**	**2**	**512**
	64M x 8	**8**	**1**	**512**		**64M x 8**	**8**	**1**	**512**
128	**8M x 16**	**16**	**4**	**256**					
	16M x 8	**16**	**2**	**256**					
256	**16M x 16**	**16**	**4**	**512**					
	32M x 8	**16**	**2**	**512**					
512	**32M x 16**	**16**	**4**	**1024**					
	64M x 8	**16**	**2**	**1024**					

1.3.2 Example Memory Configurations

Notebook PC

The memory requirements of the latest Microsoft operating systems, in combination with the widespread availability of low-cost DDR SDRAM memory, has resulted in base system memory configurations of 128 MBytes for notebook PCs. Additional memory expansion slots are usually provided for user-installed expansion memory. A typical TM5500/TM5800 processor-based notebook memory sub-system design configuration would be:

- Four 133 MHz (DDR-266) 256 Mbit (16M x 16) DDR SDRAM devices soldered down to the system motherboard, providing 128 MBytes of high-performance base system memory.
- Two 133 MHz SDR SDRAM memory expansion µDIMM sockets. These can be populated with a wide range of µDIMM memory modules, allowing incremental memory expansion of 64-512 MBytes.

High-Density Server

High-density server memory requirements typically favor very large memory configurations. The recommended TM5500/TM5800 memory configurations for these systems include the maximum amount of memory supported by the processor memory interfaces. An example high-density server memory sub-system design configuration would be:

- Eight 133 MHz (DDR-266) 512 Mbit (64M x 8) DDR SDRAM devices soldered down to the system motherboard, providing 512 MBytes of high-performance base system memory.
- One 133 MHz SDR SDRAM memory expansion DIMM socket. This can be populated with high-capacity DIMM memory modules with up to 1024 MBytes of SDR SDRAM.

1.3.3 Code Morphing Software Memory

Code Morphing software uses a portion (typically 16 MBytes) of the installed system memory for its working area and to store code translations. This portion of memory is completely isolated from the operating system-accessible (x86) memory area.

Code Morphing software memory is statically configured in the OEM configuration table. See the *TM5500/TM5800 Development and Manufacturing Guide* for detailed information on Code Morphing software memory configuration.

Systems with DDR Memory

If Code Morphing software detects DDR memory installed in the system, it allocates a portion of this DDR memory for its required memory area. This provides Code Morphing software the highest performance possible for the available memory resources in the system.

Systems without DDR Memory

If no DDR memory is installed in the system, Code Morphing software allocates a portion of the first bank of SDR memory for its required memory area. Because this first SDR memory bank must be used during the loading and initialization of Code Morphing software, it is hard-configured in the OEM configuration table, and thus cannot be located on a user-replaceable memory module.

Using SDR memory for the Code Morphing software memory space results in slower system performance than when DDR memory is used. For best overall system performance in SDR-only systems use the fastest possible SDR memory. If slower SDR memory is later added to the system, overall system performance will decrease because Code Morphing software automatically adjusts the SDR memory interface to the slowest installed memory speed.

1.4 PCI Interface

The TM5500/TM5800 PCI bus is revision 2.1 compliant. The PCI bus is 32 bits wide, operates at 33 MHz and is compatible with 3.3V levels (but is not 5V tolerant). The PCI controller on the TM5500/TM5800 provides a PCI host bridge, the central resource and a DMA controller.

The TM5500/TM5800 PCI bus can sustain 132 Mbytes/sec bursts for reads and writes on 4 KByte blocks. The PCI controller snoops ahead on PCI-to-DRAM reads and writes. The 16 DWORD processor-to-PCI write buffer converts sequential memory mapped I/O writes to PCI bursts. The DMA controller handles PCI-to-DRAM reads and writes. The 16 DWORD PCI-to-DRAM write buffer converts one 16 DWORD burst to eight separate address/data pairs. The 16 DWORD DRAM-to-PCI read ahead buffer permits continuation of read ahead after hitting in the buffer. The PCI controller tri-states the PCI bus when hot docking.

1.4.1 PCI Bus Commands

The TM5500/TM5800 PCI controller, in conjunction with the Code Morphing software, supports the PCI bus commands listed in Table 8. If the processor generates a shutdown, halt or stop grant condition, a PCI special cycle is generated. The shutdown cycle is propagated with 0000h in the message field, the halt cycle is propagated with 0001h in the message field, and the stop grant cycle is propagated with 0002h in the message field and 0012h in the message dependent data field.

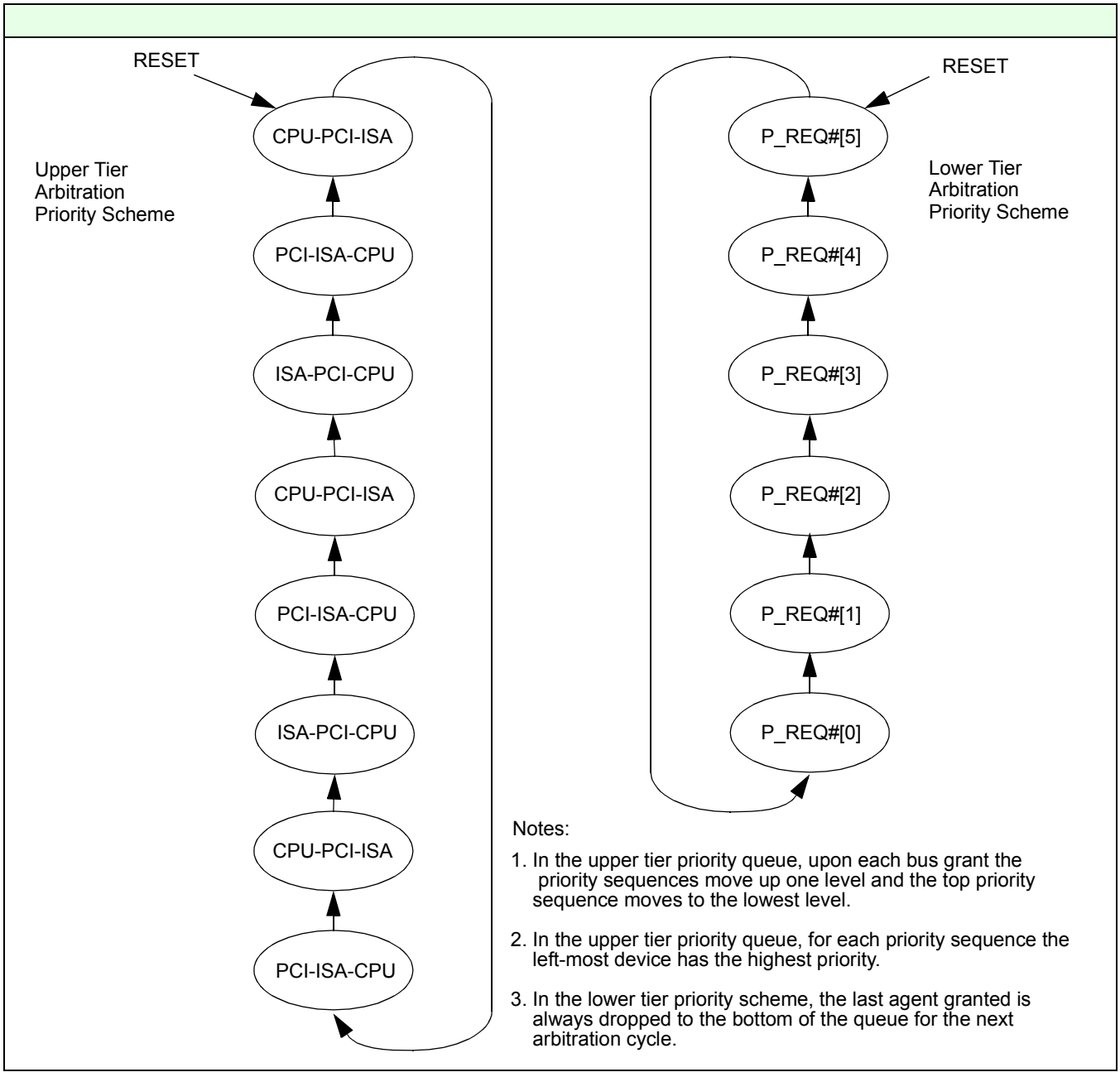
Table 8: PCI Bus Commands Supported

Command Encoding (P_C/BE#)	Command Type	Initiator Support	Target Support
0000	Interrupt Acknowledge	Yes	No
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	-	-	-
0101	-	-	-
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	-	-	-
1001	-	-	-
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	As a memory read
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	As a memory read
1111	Memory Write and Invalidate	No	As a memory write

1.4.2 Bus Arbitration

The PCI controller central resource includes an integrated arbiter which supports up to seven PCI masters, including a PCI-to-ISA bridge. The arbiter, in conjunction with Code Morphing software, implements a two-tier rotating priority-based scheme. The upper tier arbitrates among the three bus master categories of processor (CPU), PCI devices, and PCI-to-ISA bridge. The lower tier arbitrates among the requesting PCI devices. The arbitration priority scheme is shown in Figure 5.

Figure 5: PCI Arbitration Priority Scheme



When the PCI bus becomes idle, the arbiter “parks” the PCI bus on the processor. If the bus is parked and the processor and one or more other bus masters request the bus simultaneously, the processor is granted the bus regardless of the state of the upper tier priority queue.

P_REQ#[5:0] and P_GNT#[5:0] are the arbitration handshake signals used by PCI masters other than the PCI-to-ISA bridge. The PCI-to-ISA bridge uses the P_HOLD# and P_HLDA# signals.

1.5 Southbridge Sideband Signals

TM5500/TM5800 processors provide a variety of southbridge sideband signals: INIT#, RESET#, INTR, NMI, SMI#, FERR#, IGNNE#, STPCLK#, and SLEEP#. These signals are driven/monitored by a system southbridge device on the base platform and are used to guarantee PC-compatible functionality for resets, interrupts, floating point errors, processor clock control, and power management.

1.6 Serial Interfaces

The TM5500/TM5800 processor incorporates three separate serial interfaces:

Debug Serial Interface

The two-signal (S_SCLK, S_SDATA) debug interface can be used for debug purposes. Note that the serial debug interface is NOT an I2C or SMBus interface.

Configuration (Mode-Bit) ROM Serial Interface

The two-signal (CFG_SCLK, CFG_SDATA) configuration ROM interface is used to read data from a required serial ROM device. The serial configuration ROM contains hardware data that is used to initialize TM5500/TM5800 processor at power-up, and must be provided in the system design. The contents of the configuration ROM determines the settings for the processor and the SDRAM clocks, and the memory and PCI interface timing parameters. Once the PCI and SDRAM interfaces have been initialized, the configuration ROM controls the transfer of the Code Morphing software from the Code Morphing software flash memory to the SDRAM. Control is then transferred to the Code Morphing software and the configuration ROM is disabled. Programming information for the configuration ROM is available from Transmeta. The recommended ROM device is the 93LC56B-I/SN from Microchip Technology, Inc.

Code Morphing Software Boot ROM Serial Interface

The 5-signal (SROM_CS0#, SROM_CS1#, SROM_SCLK, SROM_SIN, SROM_SOUT) Code Morphing software boot ROM interface is used to read data from an optional serial flash ROM. This interface may also be used for in-system reprogramming. When used, the serial flash ROM device stores the Code Morphing software. During the boot process, the Code Morphing software is copied from the flash memory to the SDRAM. The Code Morphing software boot ROM interface supports up to 1 MByte of total storage using either two 512 KByte devices or a single 1 MByte device. Programming information for the Code Morphing software boot ROM is available from Transmeta.

1.7 Clocks

The TM5500/TM5800 processor input clock (CLKIN) is multiplied by the processor clock multiplier to generate the processor core clock. For currently defined TM5500/TM5800 SKUs, CLKIN is assumed to be 66.6 MHz. The CLKIN multipliers used for each available SKU and LongRun power management core clock frequency are provided in Table 9.

The processor core clock is divided down by the DDR and SDR clock dividers to generate the DDR SDRAM and SDR SDRAM interface clocks. See *Memory Interfaces* on page 19 for additional information on DDR frequency settings and *SDR SDRAM Interface* on page 21 for information on SDR frequency settings.

There is also a clock divider that must be initialized for the PCI interface. The PCI interface operates at 33.3 MHz. The processor core frequency divisors used to generate the 33.3 MHz PCI interface clock are shown in Table 9. The clock multiplier and divider values are programmed into the TM5500/TM5800 processor during initialization from data stored in the configuration ROM.

Table 9: Core Clock Multipliers and PCI Interface Divisors

Processor		66.6 MHz CLKIN Multiplier	33.3 MHz PCI Interface Divisor
SKU	Core Freq (MHz)		
900	900	13.5	27
	800	12	24
	667	10	20
	533	8	16
	367	5.5	11
867	867	13	26
	800	12	24
	667	10	20
	533	8	16
	367	5.5	11
800	800	12	24
	733	11	22
	667	10	20
	533	8	16
	367	5.5	11
733	733	11	22
	667	10	20
	533	8	16
	400	6	12
	333	5	10
700	700	10.5	21
	667	10	20
	533	8	16
	400	6	12
	333	5	10

Table 9: Core Clock Multipliers and PCI Interface Divisors (Continued)

Processor		66.6 MHz CLKIN Multiplier	33.3 MHz PCI Interface Divisor
SKU	Core Freq (MHz)		
667	667	10	20
	600	9	18
	500	7.5	15
	367	5.5	11
	300	4.5	9

1.8 JTAG Test Interface

TM5500/TM5800 processors provide a 5-signal JTAG interface that can be used for processor testing. This interface supports IEEE 1149.1, EXTEST, SAMPLE/PRELOAD, BYPASS, and HiZ instructions. The JTAG interface operates up to 50 MHz.

1.9 Supply Voltages

TM5500/TM5800 processors requires four supply voltages. The core supply voltage (CVDD) varies from 0.95-1.30 V (nominal). Two I/O supply voltages are required: IOVDD is 3.3 V (nominal), and IOVDD25 is 2.5 V (nominal). There is also a single supply connection for the PLL circuit, with a supply voltage (PLLVDD) that varies from 1.0-1.30 V (nominal).

1.10 Core Voltage Regulator VRDA Interface

TM5500/TM5800 processors provide a 5-signal open-drain interface (VRDA[4:0]) that is used by Code Morphing software LongRun power management to control the output voltage (CVDD) of the processor core voltage regulator module (VRM). The power-on default values for the VRDA signals are provided in Table 10.

Table 10: Power-On Default VRDA Output Values

VRDA Value						Low-Range VRM [1] Output	High-Range VRM Output
VRDA[4]	VRDA[3]	VRDA[2]	VRDA[1]	VRDA[0]	VRDA[4:0]		
0	1	1	1	0	0x0E	1.05 V	1.30 V

1. Low-Range VRMs, such as the Maxim MAX1718, are recommended for the TM5500/TM5800 core regulator device. See *TM5500/TM5800 System Design Guide* for more information on VRM circuit recommendations.

1.11 Power-On Sequence

The sequence of operations required to power-on TM5500/TM5800 processors is provided below.

1. **Apply power to the system.** Allow PLLVDD and CVDD to ramp up to their minimum operating levels. After CVDD reaches its minimum operating level, ramp up IOVDD and IOVDD25 to their respective minimum operating levels. The IOVDD and IOVDD25 supplies must not begin ramping up until CVDD has reached its minimum operating level or excessive surge currents can result on the I/O supply lines. See *Power On Specifications* on page 65 for additional information. RESET#, P_PCI_RST# and PWRGOOD should all be held low during this time. With PWRGOOD at a low level, the processor is in a self-protecting mode.

2. **Assert PWRGOOD.** Assert PWRGOOD after all power supplies reach their specified operating voltage levels following the required sequencing described in *Power On Specifications* on page 65.

3. **Begin toggling CLKIN.** At or before the assertion of PWRGOOD, begin toggling CLKIN.

4. **Deassert P_PCI_RST# and RESET#.** P_PCI_RST# must be held low until at least 1 ms after CLKIN begins to toggle. It also must be held low until at least 1 mS after the PWRGOOD rising edge.

5. **Processor mode bits are loaded from the configuration ROM.** Once P_PCI_RST# is deasserted, the processor begins reading data from the off-chip configuration ROM using the CFG_SCLK and CFG_SDATA signals. The frequency of CFG_SCLK is 920 KHz (CLKIN/72). The processor begins reading the configuration ROM by sending an eleven-bit sequence of 11000000000. This sequence tells the configuration ROM to begin supplying data starting at address 0. There is a 1 clock delay to allow the direction of the CFG_SDATA signal to change from driving to receiving. The processor then issues 112 CFG_SCLKs to read the contents of the configuration ROM. The entire sequence completes in approximately 130 µS.

6. **Complete internal reset sequence.** The processor internal reset sequence continues for approximately 800 ms plus an additional 64 internal clock cycles after the rising edge of RESET#. The processor then fetches its first instruction from either the serial boot ROM or from the PCI bus as determined by an internal mode bit.

Chapter 2

Signal Descriptions and Ballouts

This chapter contains signal descriptions, package footprint, and ballout assignments for TM5500/TM5800 processors.

2.1 Signal Descriptions

Table 11 provides a summary of TM5500/TM5800 processor signals. Table 12 through Table 25 describe the function of each signal on the processor. Signals that are designated as **Reserved** may have internal electrical connections. Unless specified otherwise in Table 23, there should be no external electrical connection to the reserved signals.

Table 11: Signal Summary

Signal Group	Quantity
DDR SDRAM Interface	109
SDR SDRAM Interface	102
PCI Interface	62
Southbridge Sideband Interface	8
Serial Interfaces	9
Thermal/Power/System Management	13
JTAG Interface and Debug	7
Reserved and No Connection	22
Core Voltage Sniff	2
Power	64
Ground	76
TOTAL	474

Table 12: DDR SDRAM Interface Signals

Signal Name	Type	Qty	Description
C_A[12:0]	O	13	**Memory Address** These signals carry row and column addressing information.
C_BA[1:0]	O	2	**Bank Address** These signals carry the bank address for the DDR SDRAM devices.
C_CAS#	O	1	**Column Address Strobe** When asserted low, enables latching of the column address on the positive edge of the next clock.
C_CKE[1:0]	O	2	**Clock Enable** When deasserted, the DDR SDRAMs enter power down mode. C_CKE[1] and C_CKE[0] are identical, and are provided to support loading requirements; each drives one block.
C_CLKA, C_CLKA#, C_CLKB, C_CLKB#	O	4	**SDRAM Clocks** Differential clocks for the multiple banks of DDR SDRAM. All DDR SDRAM operations are synchronized to the clock.
C_CS#[3:0]	O	4	**Chip Select** A DDR SDRAM row is selected when its C_CS# signal is asserted low.
C_DQ[63:0]	I/O	64	**Memory Data** This is the 64-bit data bus to the DDR SDRAMs.
C_DQMB[7:0]	O	8	**Data Mask** Used during read or write operations, one C_DQMB signal per data byte.
C_DQS[7:0]	I/O	8	**Data Strobe** Used to capture data at the processor and DDR SDRAM. When sending data to a DDR SDRAM, the strobe signal is aligned to the center of the data window to maintain timing margins. When receiving data from a DDR SDRAM, the strobe edge is aligned to the data at the processor pins.
C_RAS#	O	1	**Row Address Strobe** When asserted low, enables latching of the row address on the positive edge of the next clock.
C_VREF	I	1	**Voltage Reference** Reference voltage for the DDR SDRAM interface inputs. Used for SSTL_2 interface.
C_WE#	O	1	**Memory Write Enable** Enables write operations to the DDR SDRAMs.
Total Signals		109	

Table 13: Logical Alignment of DDR Byte Enables, Data Strobes and Data Bits

Byte Enable C_DQMB[7:0]	Data Strobe C_DQS[7:0]	Data Bits C_DQ[63:0]
C_DQMB[0]	C_DQS[0]	C_DQ[7:0]
C_DQMB[1]	C_DQS[1]	C_DQ[15:8]
C_DQMB[2]	C_DQS[2]	C_DQ[23:16]
C_DQMB[3]	C_DQS[3]	C_DQ[31:24]
C_DQMB[4]	C_DQS[4]	C_DQ[39:32]
C_DQMB[5]	C_DQS[5]	C_DQ[47:40]
C_DQMB[6]	C_DQS[6]	C_DQ[55:48]
C_DQMB[7]	C_DQS[7]	C_DQ[63:56]

Table 14: SDR SDRAM Interface Signals

Signal Name	Type	Qty	Description
S_A[12:0]	O	13	**Memory Address** These signals carry row and column addressing information for the SDR SDRAM.
S_BA[1:0]	O	2	**Bank Address** These signals carry the bank address for the SDR SDRAM.
S_CAS#	O	1	**Column Address Strobe** When asserted low, enables latching of the column address on the positive edge of the next clock.
S_CKE[1:0]	O	2	**Clock Enable** When deasserted, the SDR SDRAMs enter power down mode. Each S_CKE output drives up to 2 blocks.
S_CLK[3:0]	O	4	**SDRAM Clocks** Clocks for the multiple rows of SDR SDRAM. S_CLK[3:0] are identical, provided for loading; each drives one row.
S_CLKIN	I	1	**Clock input** Return of S_CLKOUT used to calibrate the board delay of S_CLK[3:0] to the actual SDR SDRAM devices.
S_CLKOUT	O	1	**Clock output** Clock output used in conjunction with S_CLKIN to calibrate the board delay of S_CLK[3:0] to the actual SDR SDRAM devices.
S_CS#[3:0]	O	4	**Chip Select** An SDR SDRAM block is selected when its S_CS# signal is asserted low. S_CS#[1:0] are used for slot 0, and S_CS#[3:2] are used for slot 1.
S_DQ[63:0]	I/O	64	**Memory Data** This is the 64-bit data bus to the SDR SDRAM.
S_DQMB[7:0]	O	8	**Data Mask** Used during read or write operations, one S_DQMB signal per data byte.
S_RAS#	O	1	**Row Address Strobe** When asserted low, enables latching of the row address on the positive edge of the next clock.
S_WE#	O	1	**Memory Write Enable** Enables write operations to SDR SDRAM.
Total Signals		102	

Table 15: Logical Alignment of SDR Clocks, Clock Enables, and Chip Selects

Clock	Clock Enable	Chip Select
Any S_CLK	S_CKE[0]	S_CS#[0]
Any S_CLK	S_CKE[0]	S_CS#[1]
Any S_CLK	S_CKE[1]	S_CS#[2]
Any S_CLK	S_CKE[1]	S_CS#[3]

Table 16: Logical Alignment of SDR Byte Enables and Data Bits

Byte Enable	Data Bits
S_DQMB[0]	S_DQ[7:0]
S_DQMB[1]	S_DQ[15:8]
S_DQMB[2]	S_DQ[23:16]
S_DQMB[3]	S_DQ[31:24]
S_DQMB[4]	S_DQ[39:32]
S_DQMB[5]	S_DQ[47:40]
S_DQMB[6]	S_DQ[55:48]
S_DQMB[7]	S_DQ[63:56]

Table 17 lists the memory address translations that correspond to the various SDRAM devices supported by TM5500/TM5800 processors.

Table 17: Memory Address Translations

SDRAM Device Config [1]	CS#	BS1	BS0	C10 [2]	C09	C08	C(07-00)	R12	R11	R(10-00)
64M / 4-Bank:										
4M x 16	A25	A23	A11	-	-	-	A(10-03)	-	A24	A(22-12)
8M x 8	A26	A23	A11	-	-	A25	A(10-03)	-	A24	A(22-12)
16M x 4	A27	A23	A11	-	A26	A25	A(10:03)	-	A24	A(22-12)
128M / 4-Bank:										
8M x 16	A26	A23	A11	-	-	A25	A(10-03)	A25	A24	A(22-12)
16M x 8	A27	A23	A11	-	A26	A25	A(10-03)	A25	A24	A(22-12)
32M x 4	A28	A23	A11	A27	A26	A25	A(10-03)	A25	A24	A(22-12)
256M / 4-Bank:										
16M x 16	A27	A23	A11	-	-	A26	A(10-03)	A25	A24	A(22-12)
32M x 8	A28	A23	A11	-	A27	A26	A(10-03)	A25	A24	A(22-12)
64M x 4	A29	A23	A11	A28	A27	A26	A(10-03)	A25	A24	A(22-12)
512M / 4-Bank:										
32M x 16	A28	A23	A11	-	-	A27	A(10-03)	A25	A24	A(22-12)
64M x 8	A29	A23	A11	-	A28	A27	A(10-03)	A25	A24	A(22-12)

1. SDRAM device configuration is as follows: nM, xB = n Mbits, x banks.
2. Column address 10 (C10) is sent out on address signal 11 during CAS cycle rather than address signal 10.

   Key: CS# = Chip select or side select
   Bn = Bank select
   Cnn = SDRAM column address
   Rnn = SDRAM row address
   Ann = Processor address nn

Table 18: PCI Interface Signals

Signal Name	Type	Qty	Description
P_AD[31:0]	I/O	32	**Address/Data** The address is driven with P_FRAME#, and data is written or read with subsequent clocks.
P_C/BE#[3:0]	I/O	4	**Command/Byte Enable** Command is driven with P_FRAME#. Byte enables correspond with the appropriate data on the PCI bus during read and write data cycles.
P_CLKRUN#	I/O	1	**Clock Run** This signal is open drain, and an external 2.7 KΩ resistor is required. When asserted low, the PCI clock is enabled to run.
P_DEVSEL#	I/O	1	**Device Select** Driven when a PCI initiator is accessing SDRAM.
P_FRAME#	I/O	1	**Frame** Asserted active low to indicate the beginning of a PCI access (address phase). Forced inactive high to indicate that another transfer is desired by the initiator of the cycle.
P_GNT#[5:0]	O	6	**Grant** Signals that permission is given for a master to use the PCI bus.
P_HLDA#	O	1	**PCI Hold Acknowledge** Driven to a bridge device in response to its P_HOLD# request to indicate that the bridge can take control of the PCI bus.
P_HOLD#	I	1	**PCI Hold** Asserted by an expansion bridge to request use of the PCI bus.
P_IRDY#	I/O	1	**Initiator Ready** Asserted by the initiator to indicate that it is ready for data transfer.
P_LOCK#	I/O	1	**Lock** While asserted, the currently accessed PCI resource is locked.
P_PAR	I/O	1	**Parity** Single bit representing the parity of lines P_AD[31:0] and P_C/BE#[3:0].
P_PCI_RST#	I/O	1	**Reset** Asynchronously resets the module PCI interface and northbridge, and puts all PCI signals into tristate.
P_PCLK	I	1	**PCI Clock** Clock signal for PCI interface.
P_PERR#	I/O	1	**PCI Parity Error** Signals/detects a parity error detected.
P_REQ#[5:0]	I	6	**PCI Request** A PCI master asserts this signal to request access to the PCI bus.
P_SERR#	I	1	**System error** Indicates a system error condition detected.
P_STOP#	I/O	1	**Stop** Asserted by a target device to request the master stop driving the PCI bus.
P_TRDY#	I/O	1	**Target Ready** Asserted by the target to indicate that it is ready for a data transfer.
Total Signals		62	

Table 19: Southbridge Sideband Interface Signals

Signal Name	Type	Qty	Description
FERR#	O	1	**Floating Point Unit Error** Driven by the processor when a floating point error is detected.
IGNNE#	I	1	**Ignore Numeric Error** Driven by the southbridge, this signal instructs the processor to ignore numeric exceptions and to continue to execute non-control floating point instructions.
INIT#	I	1	**Initialize** Asserted by the southbridge for system initialization. If INIT# is asserted, the processor resets internal integer registers.
INTR	I	1	**Interrupt** Driven by the southbridge to the processor to indicate that a maskable interrupt from a device is pending.
NMI	I	1	**Non-Maskable Interrupt** Forces a non-maskable interrupt to the processor.
SLEEP#	I	1	**Sleep** Used to put the processor into a low power Deep Sleep mode. Turns off PCI interface by stopping PCI clock and tri-stating PCI signals. Allows P_PCLK to be stopped.
SMI#	I	1	**System Management Interrupt** This input requests that an interrupt be serviced for system management functions such as power control.
STPCLK#	I	1	**Stop Clock** Stops all processor internal clocks except the internal master controller and the PCI controller.
Total Signals		8	

Table 20: Serial Interface Signals

Signal Name	Type	Qty	Description
S_SCLK	I/O	1	**Serial Clock** Clock for debug serial interface.
S_SDATA	I/O	1	**Serial Data** Data for debug serial interface.
CFG_SCLK	O	1	**Configuration (Mode-Bit) ROM Clock** Clock for the serial interface to the configuration ROM. Reading the configuration ROM is initiated by deassertion of P_RST# and is clocked at a frequency of CLKIN x 1/72.
CFG_SDATA	I/O	1	**Configuration (Mode-Bit) ROM Data** Data for the serial interface to the configuration ROM.
SROM_CS#[1:0]	O	2	**Code Morphing Software Boot ROM Chip Selects** When using two 512 KByte devices, SROM_CS#[0] selects the lower 512 KBytes and SROM_CS#[1] selects the upper 512 KBytes. When using a single 1 MByte device, only SROM_CS#[0] is used.
SROM_SCLK	O	1	**Code Morphing Software Boot ROM Clock** Clock from the processor to the Code Morphing software boot ROM.
SROM_SIN	I	1	**Code Morphing Software Boot ROM Serial Data In** Data from the Code Morphing software boot ROM to the processor.
SROM_SOUT	O	1	**Code Morphing Software Boot ROM Serial Data Out** Data from the processor to the Code Morphing software boot ROM.
Total Signals		9	

Table 21: Thermal/Power/System Management Signals

Signal Name	Type	Qty	Description
DIODE_ANODE	I	1	**Thermal Diode** Anode for the internal thermal diode used to monitor the processor junction temperature.
DIODE_CATHODE	O	1	**Thermal Diode** Cathode for the internal thermal diode used to monitor the processor junction temperature.
PWRGOOD	I	1	**Power Good** Indicates that the processor input clock and power supplies are stable and within operating range specifications.
VRDA[4:0]	O	5	**Voltage Regulator Control** These signals are used by Code Morphing software LongRun power management to control the processor core regulator power supply module output voltage (CVDD).
EPROMA[2:0]	O	3	**BIOS ROM Address Bits** EPROMA[2:1] are used as address bits [19:18] for the BIOS EPROM. EPROMA[0] is not used, and there should be no electrical connection to it.
RESET#	I	1	**Master Reset** Processor master reset input.
CLKIN	I	1	**Master Clock** Processor master clock input.
Total Signals		13	

Table 22: JTAG Interface and Debug Signals

Signal Name	Type	Qty	Description
TCK	I	1	**JTAG Test Clock** IEEE 1149.1 clock input.
TDI	I	1	**JTAG Test Data In** IEEE 1149.1 data input, has an internal pull-up.
TDO	O	1	**JTAG Test Data Out** IEEE 1149.1 data output.
TMS	I	1	**JTAG Test Mode Select** IEEE 1149.1 test mode select signal, has an internal pull-up.
TRST#	I	1	**JTAG Reset** IEEE 1149.1 reset signal, has an internal pull-up. This signal is an asynchronous input that resets the test logic in the processor. TRST# must be connected to RESET# if the JTAG interface signals are not going to be used.
DEBUG_INT	I	1	**Debug Interrupt Input** This signal is used for debugging purposes only. For proper operation, DEBUG_INT should be connected to GND through a 10 KΩ resistor.
DEBUG_NMI	I	1	**Debug NMI Input** This signal is used for debugging purposes only. For proper operation, DEBUG_NMI should be connected to GND through a 10 KΩ resistor.
Total Signals		7	

Table 23: Reserved and No Connection Signals

Signal Name	Type	Qty	Description
RSV	I	11	**Reserved Inputs** There should be no connection to these reserved signals.
RSV_E7	I	1	**Reserved Inputs** Connect to 10 KΩ pull-down resistor to GND.
RSV_G2	I	1	
RSV_G13	I	1	
RSV_F7	I	1	**Reserved Inputs** Connect to 10 KΩ pull-up resistor to IOVDD.
RSV_G1	I	1	
RSV_H5	I	1	
RSV_H6	I	1	
RSV_V1	I	1	
RSV_V2	I	1	
RSV_V3	I	1	
RSV_W6	I	1	
Total Signals		22	

Table 24: Core Voltage Sniff Signals

Signal Name	Qty	Description
SNIFF_CVDD	1	**Core Power Supply Sniff** Feedback signal for core voltage supply.
SNIFF_CVDDRTN	1	**Core Power Supply Sniff Return** Feedback signal for core voltage supply.
Total Signals	2	

Table 25: Power and Ground Signals

Signal Name	Qty	Description
CVDD	23	**Core Power Supply** CVDD = 0.95-1.30 V nominal.
IOVDD	28	**3.3 V I/O Power Supply** IOVDD = 3.3 V nominal.
IOVDD25	12	**2.5 V I/O Power Supply** IOVDD25 = 2.5 V nominal.
PLLVDD	1	**PLL Power Supply** PLLVDD = 1.0-1.30 V nominal.
GND	76	**Ground** Reference point for all single-ended signals and power supplies.
Total Signals	140	

2.2 I/O Signal Listings

The following tables summarize signal characteristics for each of the I/O signals. Table 26 lists the input signals, Table 27 lists the output signals and Table 28 lists the bidirectional signals.

Table 26: Input Only Signals

Signal Name	Internal Resistor	Active Level	Clock Domain	DC Specs	AC Specs
C_VREF	-	-	-	Table 32	-
CLKIN	-	-	-	Table 35	*Power On Specifications*,*Input Clocks*
DEBUG_INT	-	High	Asynchronous	Table 49	-
DEBUG_NMI	-	High	Asynchronous	Table 49	-
DIODE_ANODE	-	-	-	Table 38	-
IGNNE#	-	Low	Asynchronous	Table 35	*Southbridge Sidebands and Power Management Interface*
INIT#	-	Low	Asynchronous	Table 35	*Southbridge Sidebands and Power Management Interface*
INTR	-	High	Asynchronous	Table 35	*Southbridge Sidebands and Power Management Interface*
NMI	-	High	Asynchronous	Table 35	*Southbridge Sidebands and Power Management Interface*
P_HOLD#	-	Low	P_PCLK	Table 37	*PCI Interface*
P_PCLK	-	-	-	Table 37	*Power On Specifications*,*Input Clocks*,*PCI Interface*
P_SERR#	-	Low	P_PCLK	Table 37	*PCI Interface*
P_REQ#[5:0]	-	Low	P_PCLK	Table 37	*PCI Interface*
PWRGOOD	-	High	Asynchronous	Table 35	*Power On Specifications*,*Southbridge Sidebands and Power Management Interface*
RESET#	-	Low	Asynchronous	Table 35	*Power On Specifications*
S_CLKIN	-	-	-	Table 35	*Input Clocks*,*SDR SDRAM Interface*

Table 26: Input Only Signals (Continued)

Signal Name	Internal Resistor	Active Level	Clock Domain	DC Specs	AC Specs
SLEEP#	-	Low	Asynchronous	Table 35	*Southbridge Sidebands and Power Management Interface*
SMI#	-	Low	Asynchronous	Table 35	*Southbridge Sidebands and Power Management Interface*
SROM_SIN	-	-	SROM_SCLK	Table 35	*Code Morphing Software Boot ROM Interface*
STPCLK#	-	Low	Asynchronous	Table 35	*Southbridge Sidebands and Power Management Interface*
TCK	-	-	-	Table 35	*JTAG Interface*
TDI	Pull-up	High	TCK	Table 35	*JTAG Interface*
TMS	Pull-up	High	TCK	Table 35	*JTAG Interface*
TRST#	Pull-up	Low	Asynchronous	Table 35	*JTAG Interface*

Table 27: Output Only Signals

Signal Name	Signal Type	Active Level	Clock	Reset State	Doze State[1]	DC Specs	AC Specs
C_A[12:0]	Tri-state	-	C_CLK	1/0	Hi-Z	Table 36	*DDR SDRAM Interface*
C_BA[1:0]	Tri-state	High	C_CLK	1/0	Hi-Z	Table 36	*DDR SDRAM Interface*
C_CAS#	Tri-state	Low	C_CLK	1	Hi-Z	Table 36	*DDR SDRAM Interface*
C_CKE[1:0]	Tri-state	High	C_CLK	0	0	Table 36	*DDR SDRAM Interface*
C_CLKA, C_CLKA#, C_CLKB, C_CLKB#	Tri-state	-	-	Toggle	Hi-Z	Table 36	*DDR SDRAM Interface*
C_CS#[3:0]	Tri-state	Low	C_CLK	1	Hi-Z	Table 36	*DDR SDRAM Interface*
C_DQMB[7:0]	Tri-state	High	C_CLK	0	Hi-Z	Table 36	*DDR SDRAM Interface*
C_RAS#	Tri-state	Low	C_CLK	1	Hi-Z	Table 36	*DDR SDRAM Interface*
C_WE#	Tri-state	Low	C_CLK	1	Hi-Z	Table 36	*DDR SDRAM Interface*
CFG_SCLK	Tri-state	-	-	Hi-Z	Hi-Z	Table 35	*Configuration (Mode-bit) ROM Interface*
DIODE_CATHODE	Tri-state	-	-	Lo-Z	Lo-Z	Table 38	-
EPROMA[2:0]	Tri-state	High	Asynch.	0	Hi-Z	Table 35	-
FERR#	Open drain	Low	Asynch.	Hi-Z	Hi-Z	Table 35	-
P_GNT#[5:0]	Tri-state	Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
P_HLDA#	Tri-state	Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
S_A[12:0]	Tri-state	-	S_CLKIN	1	Hi-Z	Table 35	*SDR SDRAM Interface*
S_BA[1:0]	Tri-state	High	S_CLKIN	1	Hi-Z	Table 35	*SDR SDRAM Interface*
S_CAS#	Tri-state	Low	S_CLKIN	1	Hi-Z	Table 35	*SDR SDRAM Interface*
S_CKE[1:0]	Tri-state	High	S_CLKIN	0	0	Table 35	*SDR SDRAM Interface*
S_CLK[3:0]	Tri-state	-	-	Toggle	Hi-Z	Table 35	*SDR SDRAM Interface*
S_CLKOUT	Tri-state	-	-	Toggle	Hi-Z	Table 35	*SDR SDRAM Interface*
S_CS#[3:0]	Tri-state	Low	S_CLKIN	1	Hi-Z	Table 35	*SDR SDRAM Interface*
S_DQMB[7:0]	Tri-state	High	S_CLKIN	1	Hi-Z	Table 35	*SDR SDRAM Interface*

Table 27: Output Only Signals (Continued)

Signal Name	Signal Type	Active Level	Clock	Reset State	Doze State[1]	DC Specs	AC Specs
S_RAS#	Tri-state	Low	S_CLKIN	1	Hi-Z	Table 35	*SDR SDRAM Interface*
S_WE#	Tri-state	Low	S_CLKIN	1	Hi-Z	Table 35	*SDR SDRAM Interface*
SROM_CS#[1:0]	Tri-state	Low	SROM_SCLK	Hi-Z	Hi-Z	Table 35	*Code Morphing Software Boot ROM Interface*
SROM_SCLK	Tri-state	-	-	Hi-Z	Hi-Z	Table 35	*Code Morphing Software Boot ROM Interface*
SROM_SOUT	Tri-state	-	SROM_SCLK	Hi-Z	Hi-Z	Table 35	*Code Morphing Software Boot ROM Interface*
TDO	Tri-state	-	TCK	Hi-Z	Hi-Z	Table 35	*JTAG Interface*
VRDA[4:0]	Open drain	-	-	1/0	Lo-Z	Table 35	-

1. Doze state refers to the state of the signal during low-power modes when the specific interface is disabled. In the case of the SDRAM interfaces, the doze state refers to the state of the signal while the SDRAM is in self-refresh.

Table 28: Bidirectional Signals

Signal Name	Signal Type	Active Level	Clock	Reset State	Doze State[1]	DC Specs	AC Specs
C_DQ[63:0]		-	C_CLK	Hi-Z	Hi-Z	Table 36	*DDR SDRAM Interface*
C_DQS[7:0]		-	C_CLK	Hi-Z	Hi-Z	Table 36	*DDR SDRAM Interface*
CFG_SDATA		-	CFG_SCLK	Hi-Z	Hi-Z	Table 35	*Configuration (Mode-bit) ROM Interface*
P_AD[31:0]		-	P_PCLK	0	Hi-Z	Table 37	*PCI Interface*
P_C/BE#[3:0]		Low	P_PCLK	0	Hi-Z	Table 37	*PCI Interface*
P_CLKRUN#	Open drain	Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
P_DEVSEL#		Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
P_FRAME#		Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
P_IRDY#		Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
P_LOCK#		Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
P_PAR		High	P_PCLK	0	Hi-Z	Table 37	*PCI Interface*
P_PCI_RST#		Low	Asynch.	-	Hi-Z	Table 37	*Power On Specifications*, *PCI Interface*
P_PERR#		Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
P_STOP#		Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
P_TRDY#		Low	P_PCLK	Hi-Z	Hi-Z	Table 37	*PCI Interface*
S_DQ[63:0]		-	S_CLKIN	Hi-Z	Hi-Z	Table 35	*SDR SDRAM Interface*
S_SCLK	Open drain	-	-	Hi-Z	Hi-Z	Table 35	*Debug Interface*
S_SDATA	Open drain	-	S_SCLK	Hi-Z	Hi-Z	Table 35	*Debug Interface*

1. Doze state refers to the state of the signal during low-power modes when the specific interface is disabled. In the case of the SDRAM interfaces, the doze state refers to the state of the signal while the SDRAM is in self-refresh.

2.3 Footprint and Ballout Assignments

Figure 6 shows the TM5500/TM5800 processor package footprint. Figure 7 shows the processor package ball assignments. Table 29 and Table 30 list the ballout assignments for each signal on the processor.

Figure 6: Package Footprint - Top Down View

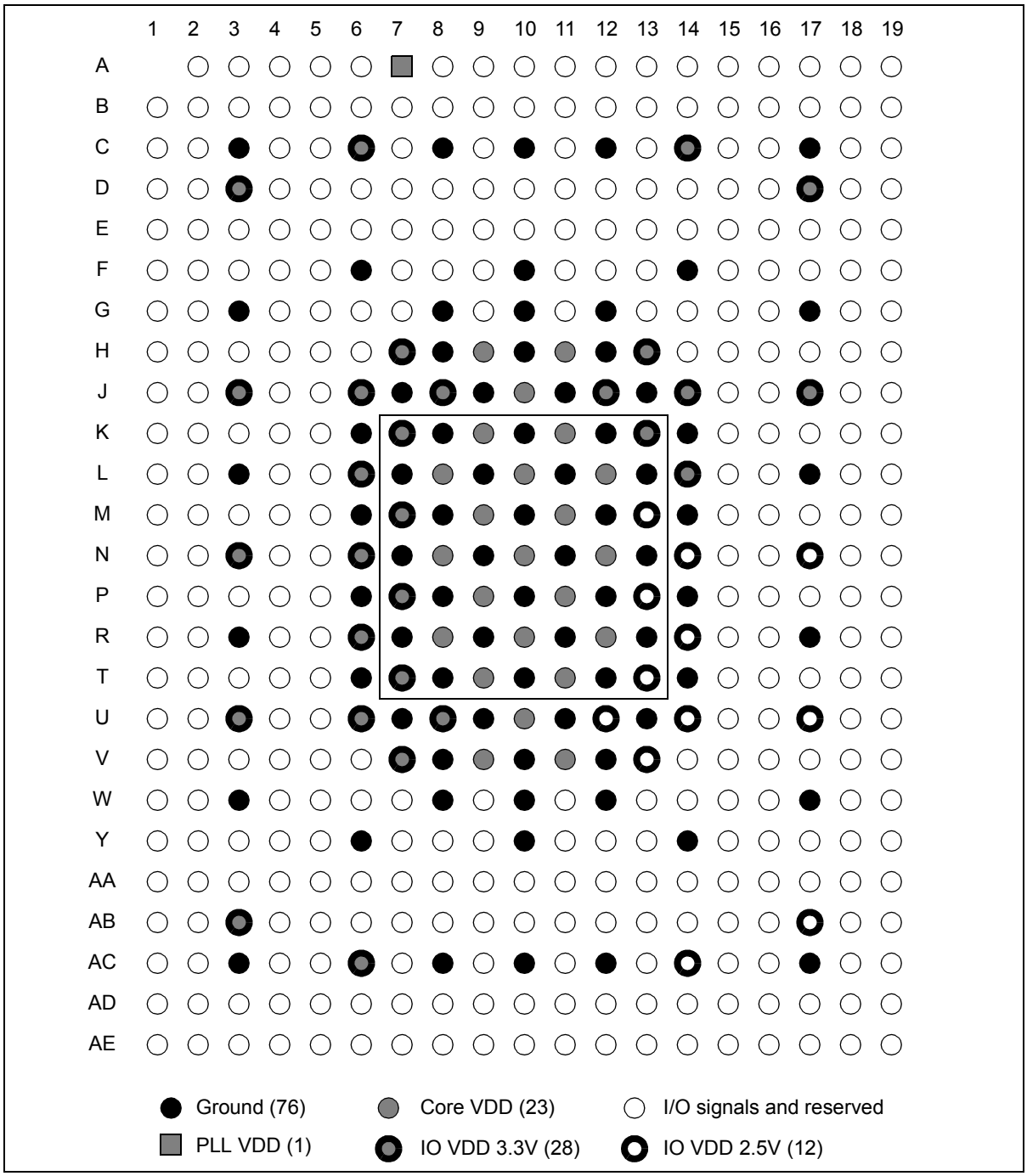


Figure 7: Package Ball-Signal Assignments - Top Down View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A		S_DQ59	S_DQ57	S_DQ60	S_DQ56	S_SCLK	PLLVDD	CFG_SDATA	P_AD30	P_AD31	P_CBE#2	P_CBE#0	P_FRAME#	P_LOCK#	P_GNT#3	P_GNT#1	P_DEVSEL#	DIODE_ANODE	TMS
B	S_DQ63	S_DQ62	S_DQ61	S_DQ58	S_DQ29	S_SDATA	CFG_SCLK	P_AD27	P_AD29	P_CBE#3	P_CBE#1	P_IRDY#	P_TRDY#	P_PAR	P_AD15	DIODE_CATHODE	P_AD3	P_AD2	P_AD0
C	S_DQ53	S_DQ55	GND	S_DQ31	S_DQ30	IOVDD	CLKIN	GND	P_AD28	GND	P_AD21	GND	P_STOP#	IOVDD	P_AD12	P_AD7	GND	P_AD1	P_HOLD#
D	S_DQ51	S_DQ54	IOVDD	S_DQ28	S_DQ21	S_DQ23	RSV	SLEEP#	P_AD26	P_AD23	P_AD19	P_AD20	P_SERR#	P_AD14	P_AD10	P_AD4	IOVDD	P_REQ#1	P_REQ#0
E	S_DQ50	S_DQ52	S_DQ26	S_DQ27	S_DQ22	S_DQ19	RSV_E7	P_PCI_RST#	P_AD25	P_AD22	P_AD18	P_AD16	P_HLDA#	P_AD13	P_AD9	P_AD5	P_AD6	P_REQ#3	P_REQ#2
F	S_DQ48	S_DQ49	S_DQ25	S_DQ24	S_DQ20	GND	RSV_F7	P_PCLK	P_AD24	GND	P_AD17	P_PERR#	P_GNT#2	GND	P_AD11	P_AD8	P_GNT#5	P_REQ#5	P_REQ#4
G	RSV_G1	RSV_G2	GND	S_DQ16	S_DQ18	S_DQ17	PWRGOOD	GND	TRST#	GND	RSV	GND	RSV_G13	SMI#	P_GNT#0	P_GNT#4	GND	INIT#	INTR
H	S_DQMB7	S_DQMB6	S_DQMB3	S_DQMB2	RSV_H5	RSV_H6	IOVDD	GND	CVDD	GND	CVDD	GND	IOVDD	DEBUG_INT	IGNNE#	FERR#	NMI	STPCLK#	RESET#
J	S_CKE1	S_CKE0	IOVDD	RSV	RSV	IOVDD	GND	IOVDD	GND	CVDD	GND	IOVDD	GND	IOVDD	EPROMA1	EPROMA0	IOVDD	P_CLKRUN#	EPROMA2
K	S_A11	S_A12	RSV	RSV	RSV	GND	IOVDD	GND	CVDD	GND	CVDD	GND	IOVDD	GND	SROM_CS#0	C_DQ32	SROM_SIN	SROM_SOUT	C_VREF
L	S_BA1	S_BA0	GND	S_CLK3	RSV	IOVDD	GND	CVDD	GND	CVDD	GND	CVDD	GND	IOVDD	SROM_CS#1	SROM_SCLK	GND	C_DQ31	C_DQ30
M	S_A5	S_A10	S_CLK0	S_CLK1	S_CLK2	GND	IOVDD	GND	CVDD	GND	CVDD	GND	IOVDD25	GND	C_DQ33	C_DQ34	C_DQ35	C_DQ29	C_DQ28
N	S_A7	S_A9	IOVDD	S_A1	S_A4	IOVDD	GND	CVDD	GND	CVDD	GND	CVDD	GND	IOVDD25	C_DQ36	C_DQ37	IOVDD25	C_DQ27	C_DQ26
P	S_A6	S_A8	S_A0	S_A3	S_WE#	GND	IOVDD	GND	CVDD	GND	CVDD	GND	IOVDD25	GND	C_DQ38	C_DQ39	C_DQS4	C_DQ25	C_DQ24
R	SNIFF_CVDDRTN	RSV	GND	RSV	S_RAS#	IOVDD	GND	CVDD	GND	CVDD	GND	CVDD	GND	IOVDD25	C_DQMB4	C_DQMB5	GND	C_DQS3	C_DQMB3
T	S_CS#2	S_CS#3	S_CS#1	S_CS#0	RSV	GND	IOVDD	GND	CVDD	GND	CVDD	GND	IOVDD25	GND	C_DQS5	C_DQ40	C_DQ41	C_DQMB2	C_DQS2
U	S_DQMB0	S_DQMB5	IOVDD	S_DQMB1	S_DQMB4	IOVDD	GND	IOVDD	GND	CVDD	GND	IOVDD25	GND	IOVDD25	C_DQ42	C_DQ43	IOVDD25	C_DQ23	C_DQ22
V	RSV_V1	RSV_V2	RSV_V3	S_CAS#	S_A2	S_CLKOUT	IOVDD	GND	CVDD	GND	CVDD	GND	IOVDD25	VRDA2	C_DQ44	C_DQ45	C_DQ46	C_DQ21	C_DQ20
W	S_DQ47	S_DQ46	GND	S_DQ15	S_DQ0	RSV_W6	TCK	GND	TDI	GND	DEBUG_NMI	GND	VRDA4	VRDA3	C_DQ47	C_DQ48	GND	C_DQ19	C_DQ18
Y	S_DQ45	S_DQ44	S_DQ14	S_DQ13	S_DQ4	GND	C_CKE1	C_CS#1	C_CS#2	GND	C_CS#3	VRDA0	VRDA1	GND	C_DQ49	C_DQ50	C_DQ51	C_DQ17	C_DQ16
AA	S_DQ43	S_DQ42	S_DQ12	S_DQ11	S_DQ3	S_DQ32	C_A7	C_A9	C_CLKB	C_CLKA	C_DQ62	C_DQ60	C_DQ57	C_DQS7	C_DQ52	C_DQ54	C_DQ53	C_DQ15	C_DQ14
AB	S_DQ41	S_DQ40	IOVDD	S_DQ1	S_DQ2	S_CLKIN	C_A6	C_A8	C_A12	C_CLKB#	C_DQ63	C_DQ61	C_DQ58	C_DQ56	C_DQMB6	C_DQ55	IOVDD25	C_DQ13	C_DQ12
AC	S_DQ9	S_DQ8	GND	S_DQ5	S_DQ33	IOVDD	C_A5	GND	C_A11	GND	C_CLKA#	GND	C_DQ59	IOVDD25	C_DQMB7	C_DQS6	GND	C_DQ11	C_DQ10
AD	S_DQ10	S_DQ7	S_DQ6	S_DQ35	S_DQ34	C_A4	C_A2	C_A0	C_BA1	C_CS#0	C_CAS#	C_DQ0	C_DQ2	C_DQ4	C_DQ6	C_DQS0	C_DQMB1	C_DQ9	C_DQ8
AE	TDO	S_DQ39	S_DQ36	S_DQ38	S_DQ37	C_CKE0	C_A3	C_A1	C_A10	C_BA0	C_RAS#	C_WE#	C_DQ1	C_DQ3	C_DQ5	C_DQ7	C_DQMB0	C_DQS1	SNIFF_CVDD

Table 29: Signal Ballout Assignments - Sorted by Ball Number

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	No Ball	C3	GND	E5	S_DQ[22]
A2	S_DQ[59]	C4	S_DQ[31]	E6	S_DQ[19]
A3	S_DQ[57]	C5	S_DQ[30]	E7	RSV_E7
A4	S_DQ[60]	C6	IOVDD	E8	P_PCI_RST#
A5	S_DQ[56]	C7	CLKIN	E9	P_AD[25]
A6	S_SCLK	C8	GND	E10	P_AD[22]
A7	PLLVDD	C9	P_AD[28]	E11	P_AD[18]
A8	CFG_SDATA	C10	GND	E12	P_AD[16]
A9	P_AD[30]	C11	P_AD[21]	E13	P_HLDA#
A10	P_AD[31]	C12	GND	E14	P_AD[13]
A11	P_C/BE#[2]	C13	P_STOP#	E15	P_AD[9]
A12	P_C/BE#[0]	C14	IOVDD	E16	P_AD[5]
A13	P_FRAME#	C15	P_AD[12]	E17	P_AD[6]
A14	P_LOCK#	C16	P_AD[7]	E18	P_REQ#[3]
A15	P_GNT#[3]	C17	GND	E19	P_REQ#[2]
A16	P_GNT#[1]	C18	P_AD[1]	F1	S_DQ[48]
A17	P_DEVSEL#	C19	P_HOLD#	F2	S_DQ[49]
A18	DIODE_ANODE	D1	S_DQ[51]	F3	S_DQ[25]
A19	TMS	D2	S_DQ[54]	F4	S_DQ[24]
B1	S_DQ[63]	D3	IOVDD	F5	S_DQ[20]
B2	S_DQ[62]	D4	S_DQ[28]	F6	GND
B3	S_DQ[61]	D5	S_DQ[21]	F7	RSV_F7
B4	S_DQ[58]	D6	S_DQ[23]	F8	P_PCLK
B5	S_DQ[29]	D7	RSV	F9	P_AD[24]
B6	S_SDATA	D8	SLEEP#	F10	GND
B7	CFG_SCLK	D9	P_AD[26]	F11	P_AD[17]
B8	P_AD[27]	D10	P_AD[23]	F12	P_PERR#
B9	P_AD[29]	D11	P_AD[19]	F13	P_GNT#[2]
B10	P_C/BE#[3]	D12	P_AD[20]	F14	GND
B11	P_C/BE#[1]	D13	P_SERR#	F15	P_AD[11]
B12	P_IRDY#	D14	P_AD[14]	F16	P_AD[8]
B13	P_TRDY#	D15	P_AD[10]	F17	P_GNT#[5]
B14	P_PAR	D16	P_AD[4]	F18	P_REQ#[5]
B15	P_AD[15]	D17	IOVDD	F19	P_REQ#[4]
B16	DIODE_CATHODE	D18	P_REQ#[1]	G1	RSV_G1
B17	P_AD[3]	D19	P_REQ#[0]	G2	RSV_G2
B18	P_AD[2]	E1	S_DQ[50]	G3	GND
B19	P_AD[0]	E2	S_DQ[52]	G4	S_DQ[16]
C1	S_DQ[53]	E3	S_DQ[26]	G5	S_DQ[18]
C2	S_DQ[55]	E4	S_DQ[27]	G6	S_DQ[17]

Table 29: Signal Ballout Assignments - Sorted by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
G7	PWRGOOD	J10	CVDD	L13	GND
G8	GND	J11	GND	L14	IOVDD
G9	TRST#	J12	IOVDD	L15	SROM_CS#[1]
G10	GND	J13	GND	L16	SROM_SCLK
G11	RSV	J14	IOVDD	L17	GND
G12	GND	J15	EPROMA[1]	L18	C_DQ[31]
G13	RSV_G13	J16	EPROMA[0]	L19	C_DQ[30]
G14	SMI#	J17	IOVDD	M1	S_A[5]
G15	P_GNT#[0]	J18	P_CLKRUN#	M2	S_A[10]
G16	P_GNT#[4]	J19	EPROMA[2]	M3	S_CLK[0]
G17	GND	K1	S_A[11]	M4	S_CLK[1]
G18	INIT#	K2	S_A[12]	M5	S_CLK[2]
G19	INTR	K3	RSV	M6	GND
H1	S_DQMB[7]	K4	RSV	M7	IOVDD
H2	S_DQMB[6]	K5	RSV	M8	GND
H3	S_DQMB[3]	K6	GND	M9	CVDD
H4	S_DQMB[2]	K7	IOVDD	M10	GND
H5	RSV_H5	K8	GND	M11	CVDD
H6	RSV_H6	K9	CVDD	M12	GND
H7	IOVDD	K10	GND	M13	IOVDD25
H8	GND	K11	CVDD	M14	GND
H9	CVDD	K12	GND	M15	C_DQ[33]
H10	GND	K13	IOVDD	M16	C_DQ[34]
H11	CVDD	K14	GND	M17	C_DQ[35]
H12	GND	K15	SROM_CS#[0]	M18	C_DQ[29]
H13	IOVDD	K16	C_DQ[32]	M19	C_DQ[28]
H14	DEBUG_INT	K17	SROM_SIN	N1	S_A[7]
H15	IGNNE#	K18	SROM_SOUT	N2	S_A[9]
H16	FERR#	K19	C_VREF	N3	IOVDD
H17	NMI	L1	S_BA[1]	N4	S_A[1]
H18	STPCLK#	L2	S_BA[0]	N5	S_A[4]
H19	RESET#	L3	GND	N6	IOVDD
J1	S_CKE[1]	L4	S_CLK[3]	N7	GND
J2	S_CKE[0]	L5	RSV	N8	CVDD
J3	IOVDD	L6	IOVDD	N9	GND
J4	RSV	L7	GND	N10	CVDD
J5	RSV	L8	CVDD	N11	GND
J6	IOVDD	L9	GND	N12	CVDD
J7	GND	L10	CVDD	N13	GND
J8	IOVDD	L11	GND	N14	IOVDD25
J9	GND	L12	CVDD	N15	C_DQ[36]

Table 29: Signal Ballout Assignments - Sorted by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
N16	C_DQ[37]	R19	C_DQMB[3]	V3	RSV_V3
N17	IOVDD25	T1	S_CS#[2]	V4	S_CAS#
N18	C_DQ[27]	T2	S_CS#[3]	V5	S_A[2]
N19	C_DQ[26]	T3	S_CS#[1]	V6	S_CLKOUT
P1	S_A[6]	T4	S_CS#[0]	V7	IOVDD
P2	S_A[8]	T5	RSV	V8	GND
P3	S_A[0]	T6	GND	V9	CVDD
P4	S_A[3]	T7	IOVDD	V10	GND
P5	S_WE#	T8	GND	V11	CVDD
P6	GND	T9	CVDD	V12	GND
P7	IOVDD	T10	GND	V13	IOVDD25
P8	GND	T11	CVDD	V14	VRDA[2]
P9	CVDD	T12	GND	V15	C_DQ[44]
P10	GND	T13	IOVDD25	V16	C_DQ[45]
P11	CVDD	T14	GND	V17	C_DQ[46]
P12	GND	T15	C_DQS[5]	V18	C_DQ[21]
P13	IOVDD25	T16	C_DQ[40]	V19	C_DQ[20]
P14	GND	T17	C_DQ[41]	W1	S_DQ[47]
P15	C_DQ[38]	T18	C_DQMB[2]	W2	S_DQ[46]
P16	C_DQ[39]	T19	C_DQS[2]	W3	GND
P17	C_DQS[4]	U1	S_DQMB[0]	W4	S_DQ[15]
P18	C_DQ[25]	U2	S_DQMB[5]	W5	S_DQ[0]
P19	C_DQ[24]	U3	IOVDD	W6	RSV_W6
R1	SNIFF_CVDDRTN	U4	S_DQMB[1]	W7	TCK
R2	RSV	U5	S_DQMB[4]	W8	GND
R3	GND	U6	IOVDD	W9	TDI
R4	RSV	U7	GND	W10	GND
R5	S_RAS#	U8	IOVDD	W11	DEBUG_NMI
R6	IOVDD	U9	GND	W12	GND
R7	GND	U10	CVDD	W13	VRDA[4]
R8	CVDD	U11	GND	W14	VRDA[3]
R9	GND	U12	IOVDD25	W15	C_DQ[47]
R10	CVDD	U13	GND	W16	C_DQ[48]
R11	GND	U14	IOVDD25	W17	GND
R12	CVDD	U15	C_DQ[42]	W18	C_DQ[19]
R13	GND	U16	C_DQ[43]	W19	C_DQ[18]
R14	IOVDD25	U17	IOVDD25	Y1	S_DQ[45]
R15	C_DQMB[4]	U18	C_DQ[23]	Y2	S_DQ[44]
R16	C_DQMB[5]	U19	C_DQ[22]	Y3	S_DQ[14]
R17	GND	V1	RSV_V1	Y4	S_DQ[13]
R18	C_DQS[3]	V2	RSV_V2	Y5	S_DQ[4]

Table 29: Signal Ballout Assignments - Sorted by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
Y6	GND	AB9	C_A[12]	AD12	C_DQ[0]
Y7	C_CKE[1]	AB10	C_CLKB#	AD13	C_DQ[2]
Y8	C_CS#[1]	AB11	C_DQ[63]	AD14	C_DQ[4]
Y9	C_CS#[2]	AB12	C_DQ[61]	AD15	C_DQ[6]
Y10	GND	AB13	C_DQ[58]	AD16	C_DQS[0]
Y11	C_CS#[3]	AB14	C_DQ[56]	AD17	C_DQMB[1]
Y12	VRDA[0]	AB15	C_DQMB[6]	AD18	C_DQ[9]
Y13	VRDA[1]	AB16	C_DQ[55]	AD19	C_DQ[8]
Y14	GND	AB17	IOVDD25	AE1	TDO
Y15	C_DQ[49]	AB18	C_DQ[13]	AE2	S_DQ[39]
Y16	C_DQ[50]	AB19	C_DQ[12]	AE3	S_DQ[36]
Y17	C_DQ[51]	AC1	S_DQ[9]	AE4	S_DQ[38]
Y18	C_DQ[17]	AC2	S_DQ[8]	AE5	S_DQ[37]
Y19	C_DQ[16]	AC3	GND	AE6	C_CKE[0]
AA1	S_DQ[43]	AC4	S_DQ[5]	AE7	C_A[3]
AA2	S_DQ[42]	AC5	S_DQ[33]	AE8	C_A[1]
AA3	S_DQ[12]	AC6	IOVDD	AE9	C_A[10]
AA4	S_DQ[11]	AC7	C_A[5]	AE10	C_BA[0]
AA5	S_DQ[3]	AC8	GND	AE11	C_RAS#
AA6	S_DQ[32]	AC9	C_A[11]	AE12	C_WE#
AA7	C_A[7]	AC10	GND	AE13	C_DQ[1]
AA8	C_A[9]	AC11	C_CLKA#	AE14	C_DQ[3]
AA9	C_CLKB	AC12	GND	AE15	C_DQ[5]
AA10	C_CLKA	AC13	C_DQ[59]	AE16	C_DQ[7]
AA11	C_DQ[62]	AC14	IOVDD25	AE17	C_DQMB[0]
AA12	C_DQ[60]	AC15	C_DQMB[7]	AE18	C_DQS[1]
AA13	C_DQ[57]	AC16	C_DQS[6]	AE19	SNIFF_CVDD
AA14	C_DQS[7]	AC17	GND		
AA15	C_DQ[52]	AC18	C_DQ[11]		
AA16	C_DQ[54]	AC19	C_DQ[10]		
AA17	C_DQ[53]	AD1	S_DQ[10]		
AA18	C_DQ[15]	AD2	S_DQ[7]		
AA19	C_DQ[14]	AD3	S_DQ[6]		
AB1	S_DQ[41]	AD4	S_DQ[35]		
AB2	S_DQ[40]	AD5	S_DQ[34]		
AB3	IOVDD	AD6	C_A[4]		
AB4	S_DQ[1]	AD7	C_A[2]		
AB5	S_DQ[2]	AD8	C_A[0]		
AB6	S_CLKIN	AD9	C_BA[1]		
AB7	C_A[6]	AD10	C_CS#[0]		
AB8	C_A[8]	AD11	C_CAS#		

Table 30: Signal Ballout Assignments - Sorted by Signal Name

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
C_A[0]	AD8	C_DQ[14]	AA19	C_DQ[54]	AA16
C_A[1]	AE8	C_DQ[15]	AA18	C_DQ[55]	AB16
C_A[2]	AD7	C_DQ[16]	Y19	C_DQ[56]	AB14
C_A[3]	AE7	C_DQ[17]	Y18	C_DQ[57]	AA13
C_A[4]	AD6	C_DQ[18]	W19	C_DQ[58]	AB13
C_A[5]	AC7	C_DQ[19]	W18	C_DQ[59]	AC13
C_A[6]	AB7	C_DQ[20]	V19	C_DQ[60]	AA12
C_A[7]	AA7	C_DQ[21]	V18	C_DQ[61]	AB12
C_A[8]	AB8	C_DQ[22]	U19	C_DQ[62]	AA11
C_A[9]	AA8	C_DQ[23]	U18	C_DQ[63]	AB11
C_A[10]	AE9	C_DQ[24]	P19	C_DQMB[0]	AE17
C_A[11]	AC9	C_DQ[25]	P18	C_DQMB[1]	AD17
C_A[12]	AB9	C_DQ[26]	N19	C_DQMB[2]	T18
C_BA[0]	AE10	C_DQ[27]	N18	C_DQMB[3]	R19
C_BA[1]	AD9	C_DQ[28]	M19	C_DQMB[4]	R15
C_CAS#	AD11	C_DQ[29]	M18	C_DQMB[5]	R16
C_CKE[0]	AE6	C_DQ[30]	L19	C_DQMB[6]	AB15
C_CKE[1]	Y7	C_DQ[31]	L18	C_DQMB[7]	AC15
C_CLKA	AA10	C_DQ[32]	K16	C_DQS[0]	AD16
C_CLKA#	AC11	C_DQ[33]	M15	C_DQS[1]	AE18
C_CLKB	AA9	C_DQ[34]	M16	C_DQS[2]	T19
C_CLKB#	AB10	C_DQ[35]	M17	C_DQS[3]	R18
C_CS#[0]	AD10	C_DQ[36]	N15	C_DQS[4]	P17
C_CS#[1]	Y8	C_DQ[37]	N16	C_DQS[5]	T15
C_CS#[2]	Y9	C_DQ[38]	P15	C_DQS[6]	AC16
C_CS#[3]	Y11	C_DQ[39]	P16	C_DQS[7]	AA14
C_DQ[0]	AD12	C_DQ[40]	T16	C_RAS#	AE11
C_DQ[1]	AE13	C_DQ[41]	T17	C_VREF	K19
C_DQ[2]	AD13	C_DQ[42]	U15	C_WE#	AE12
C_DQ[3]	AE14	C_DQ[43]	U16	CFG_SCLK	B7
C_DQ[4]	AD14	C_DQ[44]	V15	CFG_SDATA	A8
C_DQ[5]	AE15	C_DQ[45]	V16	CLKIN	C7
C_DQ[6]	AD15	C_DQ[46]	V17	CVDD	H9
C_DQ[7]	AE16	C_DQ[47]	W15	CVDD	H11
C_DQ[8]	AD19	C_DQ[48]	W16	CVDD	J10
C_DQ[9]	AD18	C_DQ[49]	Y15	CVDD	K9
C_DQ[10]	AC19	C_DQ[50]	Y16	CVDD	K11
C_DQ[11]	AC18	C_DQ[51]	Y17	CVDD	L8
C_DQ[12]	AB19	C_DQ[52]	AA15	CVDD	L10
C_DQ[13]	AB18	C_DQ[53]	AA17	CVDD	L12

Table 30: Signal Ballout Assignments - Sorted by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
CVDD	M9	GND	J11	GND	U13
CVDD	M11	GND	J13	GND	V8
CVDD	N8	GND	K6	GND	V10
CVDD	N10	GND	K8	GND	V12
CVDD	N12	GND	K10	GND	W3
CVDD	P9	GND	K12	GND	W8
CVDD	P11	GND	K14	GND	W10
CVDD	R8	GND	L3	GND	W12
CVDD	R10	GND	L7	GND	W17
CVDD	R12	GND	L9	GND	Y6
CVDD	T9	GND	L11	GND	Y10
CVDD	T11	GND	L13	GND	Y14
CVDD	U10	GND	L17	GND	AC3
CVDD	V9	GND	M6	GND	AC8
CVDD	V11	GND	M8	GND	AC10
DEBUG_INT	H14	GND	M10	GND	AC12
DEBUG_NMI	W11	GND	M12	GND	AC17
DIODE_ANODE	A18	GND	M14	IGNNE#	H15
DIODE_CATHODE	B16	GND	N7	INIT#	G18
EPROMA[0]	J16	GND	N9	INTR	G19
EPROMA[1]	J15	GND	N11	IOVDD	C6
EPROMA[2]	J19	GND	N13	IOVDD	C14
FERR#	H16	GND	P6	IOVDD	D3
GND	C3	GND	P8	IOVDD	D17
GND	C8	GND	P10	IOVDD	H7
GND	C10	GND	P12	IOVDD	H13
GND	C12	GND	P14	IOVDD	J3
GND	C17	GND	R3	IOVDD	J6
GND	F6	GND	R7	IOVDD	J8
GND	F10	GND	R9	IOVDD	J12
GND	F14	GND	R11	IOVDD	J14
GND	G3	GND	R13	IOVDD	J17
GND	G8	GND	R17	IOVDD	K7
GND	G10	GND	T6	IOVDD	K13
GND	G12	GND	T8	IOVDD	L6
GND	G17	GND	T10	IOVDD	L14
GND	H8	GND	T12	IOVDD	M7
GND	H10	GND	T14	IOVDD	N3
GND	H12	GND	U7	IOVDD	N6
GND	J7	GND	U9	IOVDD	P7
GND	J9	GND	U11	IOVDD	R6

Table 30: Signal Ballout Assignments - Sorted by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
IOVDD	T7	P_AD[21]	C11	PLLVDD	A7
IOVDD	U3	P_AD[22]	E10	PWRGOOD	G7
IOVDD	U6	P_AD[23]	D10	RSV	D7
IOVDD	U8	P_AD[24]	F9	RSV_E7	E7
IOVDD	V7	P_AD[25]	E9	RSV_F7	F7
IOVDD	AB3	P_AD[26]	D9	RSV_G1	G1
IOVDD	AC6	P_AD[27]	B8	RSV_G2	G2
IOVDD25	M13	P_AD[28]	C9	RSV	G11
IOVDD25	N14	P_AD[29]	B9	RSV_G13	G13
IOVDD25	N17	P_AD[30]	A9	RSV_H5	H5
IOVDD25	P13	P_AD[31]	A10	RSV_H6	H6
IOVDD25	R14	P_C/BE#[0]	A12	RSV	J4
IOVDD25	T13	P_C/BE#[1]	B11	RSV	J5
IOVDD25	U12	P_C/BE#[2]	A11	RSV	K3
IOVDD25	U14	P_C/BE#[3]	B10	RSV	K4
IOVDD25	U17	P_CLKRUN#	J18	RSV	K5
IOVDD25	V13	P_DEVSEL#	A17	RSV	L5
IOVDD25	AB17	P_FRAME#	A13	RSV	R2
IOVDD25	AC14	P_GNT#[0]	G15	RSV	R4
NMI	H17	P_GNT#[1]	A16	RSV	T5
P_AD[0]	B19	P_GNT#[2]	F13	RSV_V1	V1
P_AD[1]	C18	P_GNT#[3]	A15	RSV_V2	V2
P_AD[2]	B18	P_GNT#[4]	G16	RSV_V3	V3
P_AD[3]	B17	P_GNT#[5]	F17	RSV_W6	W6
P_AD[4]	D16	P_HLDA#	E13	RESET#	H19
P_AD[5]	E16	P_HOLD#	C19	S_A[0]	P3
P_AD[6]	E17	P_IRDY#	B12	S_A[1]	N4
P_AD[7]	C16	P_LOCK#	A14	S_A[2]	V5
P_AD[8]	F16	P_PAR	B14	S_A[3]	P4
P_AD[9]	E15	P_PCI_RST#	E8	S_A[4]	N5
P_AD[10]	D15	P_PCLK	F8	S_A[5]	M1
P_AD[11]	F15	P_PERR#	F12	S_A[6]	P1
P_AD[12]	C15	P_REQ#[0]	D19	S_A[7]	N1
P_AD[13]	E14	P_REQ#[1]	D18	S_A[8]	P2
P_AD[14]	D14	P_REQ#[2]	E19	S_A[9]	N2
P_AD[15]	B15	P_REQ#[3]	E18	S_A[10]	M2
P_AD[16]	E12	P_REQ#[4]	F19	S_A[11]	K1
P_AD[17]	F11	P_REQ#[5]	F18	S_A[12]	K2
P_AD[18]	E11	P_SERR#	D13	S_BA[0]	L2
P_AD[19]	D11	P_STOP#	C13	S_BA[1]	L1
P_AD[20]	D12	P_TRDY#	B13	S_CAS#	V4

Table 30: Signal Ballout Assignments - Sorted by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
S_CKE[0]	J2	S_DQ[29]	B5	S_DQMB[6]	H2
S_CKE[1]	J1	S_DQ[30]	C5	S_DQMB[7]	H1
S_CLK[0]	M3	S_DQ[31]	C4	S_RAS#	R5
S_CLK[1]	M4	S_DQ[32]	AA6	S_SCLK	A6
S_CLK[2]	M5	S_DQ[33]	AC5	S_SDATA	B6
S_CLK[3]	L4	S_DQ[34]	AD5	S_WE#	P5
S_CLKIN	AB6	S_DQ[35]	AD4	SLEEP#	D8
S_CLKOUT	V6	S_DQ[36]	AE3	SMI#	G14
S_CS#[0]	T4	S_DQ[37]	AE5	SNIFF_CVDD	AE19
S_CS#[1]	T3	S_DQ[38]	AE4	SNIFF_CVDDRTN	R1
S_CS#[2]	T1	S_DQ[39]	AE2	SROM_CS#[0]	K15
S_CS#[3]	T2	S_DQ[40]	AB2	SROM_CS#[1]	L15
S_DQ[0]	W5	S_DQ[41]	AB1	SROM_SCLK	L16
S_DQ[1]	AB4	S_DQ[42]	AA2	SROM_SIN	K17
S_DQ[2]	AB5	S_DQ[43]	AA1	SROM_SOUT	K18
S_DQ[3]	AA5	S_DQ[44]	Y2	STPCLK#	H18
S_DQ[4]	Y5	S_DQ[45]	Y1	TCK	W7
S_DQ[5]	AC4	S_DQ[46]	W2	TDI	W9
S_DQ[6]	AD3	S_DQ[47]	W1	TDO	AE1
S_DQ[7]	AD2	S_DQ[48]	F1	TMS	A19
S_DQ[8]	AC2	S_DQ[49]	F2	TRST#	G9
S_DQ[9]	AC1	S_DQ[50]	E1	VRDA[0]	Y12
S_DQ[10]	AD1	S_DQ[51]	D1	VRDA[1]	Y13
S_DQ[11]	AA4	S_DQ[52]	E2	VRDA[2]	V14
S_DQ[12]	AA3	S_DQ[53]	C1	VRDA[3]	W14
S_DQ[13]	Y4	S_DQ[54]	D2	VRDA[4]	W13
S_DQ[14]	Y3	S_DQ[55]	C2		
S_DQ[15]	W4	S_DQ[56]	A5		
S_DQ[16]	G4	S_DQ[57]	A3		
S_DQ[17]	G6	S_DQ[58]	B4		
S_DQ[18]	G5	S_DQ[59]	A2		
S_DQ[19]	E6	S_DQ[60]	A4		
S_DQ[20]	F5	S_DQ[61]	B3		
S_DQ[21]	D5	S_DQ[62]	B2		
S_DQ[22]	E5	S_DQ[63]	B1		
S_DQ[23]	D6	S_DQMB[0]	U1		
S_DQ[24]	F4	S_DQMB[1]	U4		
S_DQ[25]	F3	S_DQMB[2]	H4		
S_DQ[26]	E3	S_DQMB[3]	H3		
S_DQ[27]	E4	S_DQMB[4]	U5		
S_DQ[28]	D4	S_DQMB[5]	U2		

Chapter 3

Electrical Specifications

3.1 Absolute Maximum Ratings

Table 31: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum
CVDD	Core voltage	-0.2 V	1.5 V
IOVDD	3.3V I/O voltage	-0.2 V	3.6 V
IOVDD25	2.5V I/O voltage	-0.2 V	3.6 V
PLLVDD	PLL voltage	-0.2 V	1.5 V
-	IOVDD, IOVDD25 relative to CVDD, PLLVDD	0.0 V	3.465 V
V_{in}	Input voltage	-0.5 V	3.96 V
I_{in}	Input current	-100 mA	100 mA
$T_{storage}$	Storage temperature	-55 °C	150 °C

3.2 Recommended Operating Conditions

Table 32: Voltage and Temperature Specifications

Symbol	Description/Condition/SKU	Minimum	Nominal	Maximum
CVDD	Core voltage, maximum LongRun setting [1]			
	900 MHz	1.274 V [1]	1.30 V	1.365 V [1]
	867 MHz			
	800 MHz			
	733 MHz			
	700 MHz			
	667 MHz			
	Core voltage, intermediate LongRun settings			
	367-800 MHz	nom - 2% [1]	nom	nom + 5% [1]
	Core voltage, minimum LongRun setting			
	300/333/367 MHz	0.931 V [1]	0.95 V	0.998 V [1]
PLLVDD	PLL voltage, maximum LongRun setting			
	Clocks running	1.235 V	1.30 V	1.365 V
	PLL voltage, intermediate LongRun settings			
	Clocks running	See PLLVDD vs. CVDD tracking requirement		
	PLL voltage, minimum LongRun setting			
	Clocks running	0.95 V	1.0 V	1.05 V
IOVDD	3.3V I/O voltage	3.135 V	3.3 V	3.465 V
IOVDD25	2.5V I/O voltage	2.375 V	2.5 V	2.625 V
C_VREF	DDR SDRAM interface voltage reference	1.3 V	1.4 V	1.5 V
V_{in}	Input voltage	GND	-	IOVDD
T_j	Junction temperature			
	All operating points	0 °C	-	100 °C 90 °C [2]

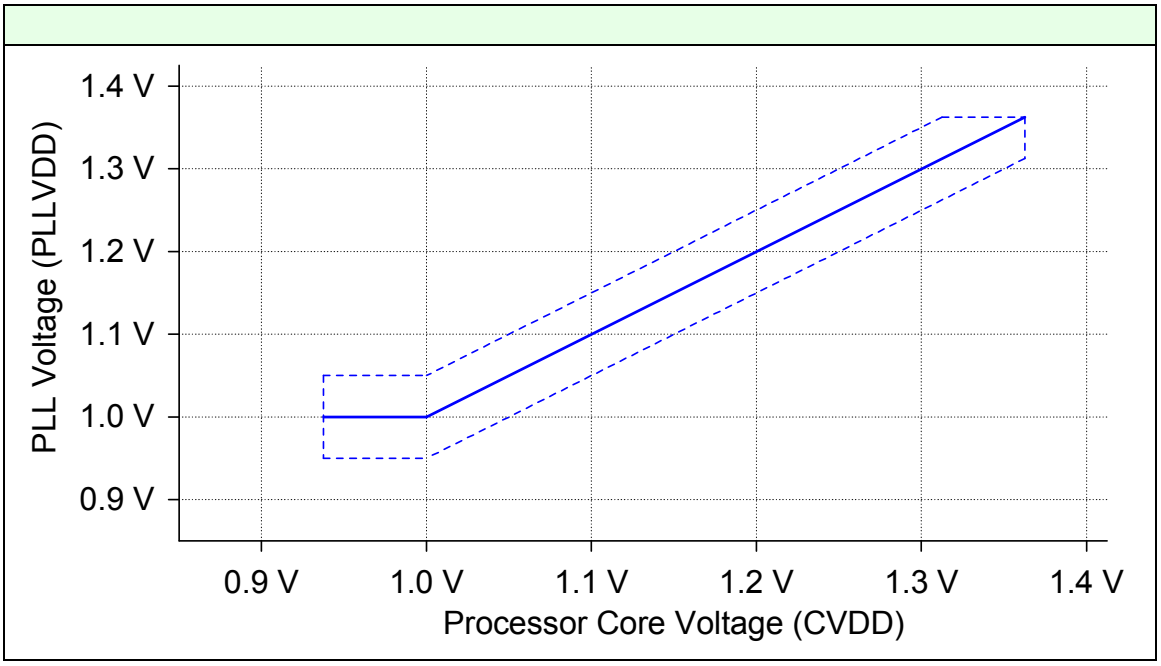
1. CVDD tolerance is +5/-2% from DC to 20 MHz and ±5% above 20 MHz.
2. Maximum junction temperature specification depends on SKU. See *Package Marking Descriptions* on page 89 for details on device temperature package marking identifier.

3.2.1 PLL Supply Core Voltage Tracking

PLLVDD must track the core supply voltage, CVDD, within ± 50 mV across a nominal core operating voltage range of 1.0 V to $CVDD_{max}$ V, while staying within the min/max voltage limits of each supply. PLLVDD must remain at 1.0 V ± 50 mV across a nominal core operating voltage range of 0.95 V to 1.0 V. The figure below graphically shows the TM5500/TM5800 PLL power supply tracking requirement.

For transitions in the core voltage (e.g. during LongRun power management voltage steps), PLLVDD must settle to within the ± 50 mV CVDD voltage tracking specification within ± 25 µS.

Figure 8: PLL/Processor Core Voltage Tracking



3.3 Power and Current Specifications

Table 33: Power Specifications

Specification		Test Conditions [1]			Power [1]	
Symbol	**SKU**	**MHz**	**CVDD**	**T_j**	**Typical**	**Maximum**
TDP	Thermal design power [2]					
	900	900	1.30 V	100 °C 90 °C [3]	-	6.8 W
	867	867				6.5 W
	800	800		100 °C		6.0 W
	733	733				5.5 W
	700	700				5.3 W
	667	667				5.0 W
P_{C1}	Auto Halt (ACPI C1) power [4]					
	900	367	0.95 V	50 °C	0.45 W	-
	867	367				
	800	367				
	733	333				
	700	333				
	667	300				
P_{C2}	Quick Start (ACPI C2) power [5]					
	900	367	0.95 V	50 °C	0.35 W	-
	867	367				
	800	367				
	733	333				
	700	333				
	667	300				
P_{C3}	Deep Sleep (ACPI C3) power [6]					
	900	-	0.95 V	35 °C	0.25 W	0.45 W
	867					
	800					
	733					
	700					
	667					

1. All power supplies at their nominal values. All power values are the total of core power and I/O power.
2. Thermal design power is the maximum average power dissipated over a 30 second interval while running publicly available application software at the maximum LongRun setting at maximum junction temperature (T_j). Thermal design power is the recommended thermal design point and is not the absolute maximum power under worst case conditions.
3. Maximum junction temperature specification depends on SKU. See *Package Marking Descriptions* on page 89 for details on device temperature package marking identifier.
4. Auto Halt (ACPI C1) is entered by executing a HLT instruction. Typical Auto Halt power is measured at the minimum LongRun setting at 50°C junction temperature.

5. Quick Start (ACPI C2) is entered by asserting STPCLK#. Typical Quick Start power is measured at the minimum LongRun setting at 50°C junction temperature.
6. Deep Sleep (ACPI C3) is entered by asserting SLEEP# and stopping CLKIN while in Quick Start. Processor clocks are stopped in Deep Sleep. Deep Sleep power is measured/specified at the minimum LongRun setting at 35°C junction temperature.

Table 34: Power Supply Current Specifications

Specification		Maximum Supply Voltage [1]	Current [2]
Symbol	**Description/SKU**		**Maximum**
I_{CVDD}	Processor core supply (CVDD) current		
	900	CVDD = 1.365 V	5.3 A
	867		5.1 A
	800		4.7 A
	733		4.3 A
	700		4.1 A
	667		3.9 A
I_{PLLVDD}	PLL supply (PLLVDD) current		
	900	PLLVDD = 1.365 V	20 mA
	867		
	800		
	733		
	700		
	667		
$I_{IOVDD25}$	2.5 V I/O supply (IOVDD25) current [3]		
	900	IOVDD25 = 2.625 V	400 mA
	867		
	800		
	733		
	700		
	667		
I_{IOVDD}	3.3 V I/O supply (IOVDD) current [4]		
	900	IOVDD = 3.465 V	500 mA
	867		
	800		
	733		
	700		
	667		

1. All supplies at their maximum values.
2. Specifications apply across full operating temperature range of processor.
3. The peak current specified for IOVDD25 (2.5 V I/O) is valid if the DDR interface is used. IOVDD25 current requirements are substantially reduced if the DDR interface is not used.
4. The peak current specified for IOVDD (3.3 V I/O) is valid if the SDR SDRAM interface is used. IOVDD current requirements are substantially reduced if the SDR SDRAM interface is not used.

3.4 DC Specifications for I/O Signals

Table 35: DC Specifications for All Signals Except PCI and DDR SDRAM Interfaces

Symbol	Description	Condition	Minimum	Maximum	Notes
V_{oh}	Output high voltage	I_{out} = -1 mA	2.4 V	-	
V_{ol}	Output low voltage	I_{out} = 1 mA	-	0.4 V	
V_{ih}	Input high voltage (excluding 2.5V inputs)		2.0 V	IOVDD	1
	Input high voltage for 2.5V inputs		1.7 V	IOVDD	
V_{il}	Input low voltage		-0.3 V	0.7 V	
I_{ih}	Input high leakage current	V_{in} = IOVDD	-	10 µA	2
I_{il}	Input low leakage current	V_{in} = 0 V	-	-100 µA	2
I_{ihz}	Hi-Z high leakage current	V_{in} = IOVDD	-	10 µA	2
I_{ilz}	Hi-Z low leakage current	V_{in} = 0 V	-	-10 µA	2
C_{in}	Input signal capacitance		-	10 pF	

1. The 2.5 V input signals are: CLKIN, IGNNE#, INTR, INIT#, NMI, SMI#, and STPCLK#. The 2.5 V input signals are 3.3 V tolerant.
2. Signals loaded at 2.4 pF.

Table 36: DC Specifications for DDR SDRAM Interface

Symbol	Description	Condition	Minimum	Maximum
V_{oh}	Output high voltage	I_{out} = -5.0 mA	1.85 V	-
V_{ol}	Output low voltage	I_{out} = 7.5 mA	-	0.35 V
V_{ih} [1]	Input high voltage		C_VREF + 0.18 V	IOVDD25 + 0.3 V
V_{il}	Input low voltage		-0.3 V	C_VREF - 0.18 V
I_{ih}	Input high leakage current	V_{in} = IOVDD25	-	10 µA
I_{il}	Input low leakage current	V_{in} = 0 V	-	-100 µA
C_{in}	Input signal capacitance		-	10 pF

1. The DDR SDRAM interface inputs are not 3.3 V tolerant.

Table 37: DC Specifications for PCI Interface

Symbol	Description	Condition	Minimum	Maximum
V_{oh}	Output high voltage	I_{out} = -0.5 mA	0.9 x IOVDD	-
V_{ol}	Output low voltage	I_{out} = 1.5 mA	-	0.1 x IOVDD
V_{ih}	Input high voltage (excluding P_PCLK)		0.5 x IOVDD	IOVDD + 0.5 V
	Input high voltage (P_PCLK only)		2.0 V	IOVDD + 0.5 V
V_{il}	Input low voltage (excluding P_PCLK)		-0.5 V	0.3 x IOVDD
	Input low voltage (P_PCLK only)		-0.5 V	0.8 V
I_{ih}	Input high leakage current	V_{in} = IOVDD	-	10 µA
I_{il}	Input low leakage current	V_{in} = 0 V	-	-100 µA
C_{in}	Input signal capacitance		-	10 pF

Table 38: Thermal Diode Specifications

Symbol	Description	Minimum	Typical	Maximum
V_{100} [1]	Forward biased diode drop forcing 100 µA	-	0.68 V	-
V_{10} [1]	Forward biased diode drop forcing 10 µA	-	0.62 V	-

1. V_{100} and V_{10} typical values are measured at 25°C while DIODE_CATHODE is biased at 0.7 V.

3.5 Timing Specifications for I/O Signals

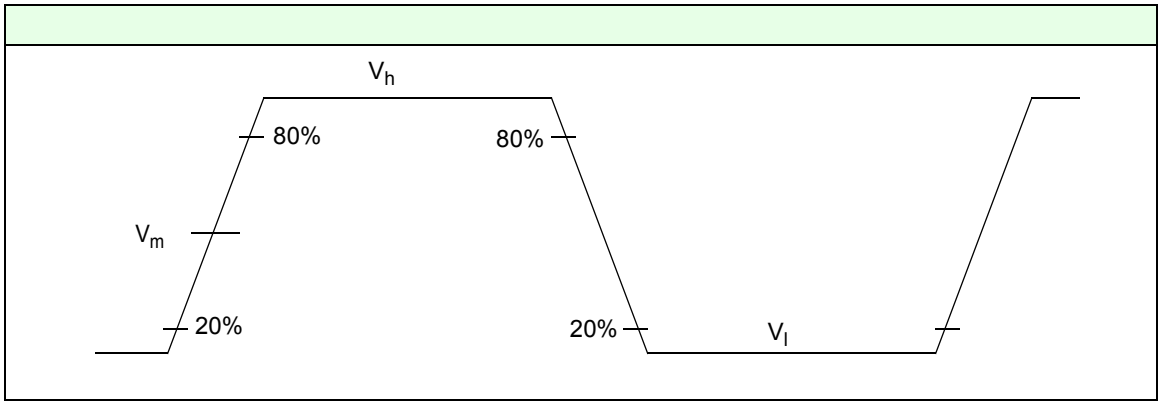
3.5.1 General AC Testing Conditions

Table 39 and Figure 9 specify the general AC test and measurement conditions. These conditions apply unless specified otherwise.

Table 39: General AC Testing Conditions

Parameter	Description	Value
V_l	3.3V input low drive level	0.4 V
	2.5V input low drive level	0.4 V
	DDR interface input low drive level	C_VREF - 0.35 V
V_h	3.3V input high drive level	2.4 V
	2.5V input high drive level	2.0 V
	DDR interface input high drive level	C_VREF + 0.35 V
V_m	3.3 V I/O timing specification measurement level	1.4 V
	2.5 V I/O timing specification measurement level	1.2 V
t_{edge}	Input signal edge rate specified between 20% and 80% of drive levels	1 V/nS

Figure 9: General AC Test and Measurement Conditions



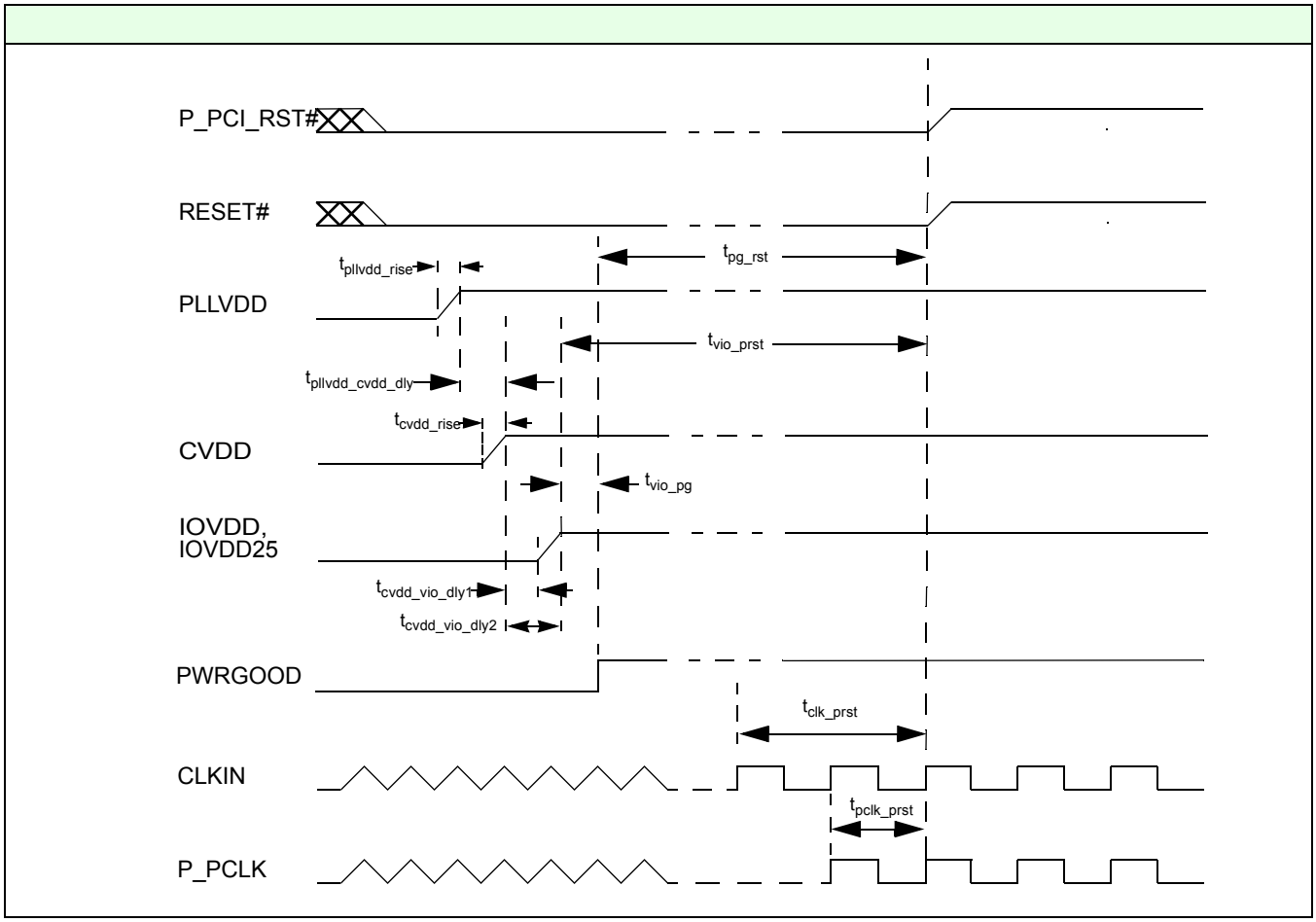
3.5.2 Power On Specifications

Table 40 and Figure 10 document the timing specifications for powering on the processor.

Table 40: Power On Specifications

Parameter	Description	Minimum	Maximum	Notes
t_{pllvdd_rise}	PLL power supply rise time	-	10 mS	
$t_{pllvdd\_cvdd\_dly}$	Required delay between PLLVDD valid and CVDD valid	-10 mS	10 mS	
t_{cvdd_rise}	Core power supply rise time	-	10 mS	
$t_{cvdd\_vio\_dly1}$	Required delay between CVDD valid and beginning of IOVDD/IOVDD25 power supply ramp-up	0 mS	<10 mS	Core supply voltage must reach minimum operating level before ramping I/O supplies to processor.
$t_{cvdd\_vio\_dly2}$	Required delay between CVDD valid and IOVDD/IOVDD25 valid	-	10 mS	
t_{vio_pg}	PWRGOOD asserted after I/O supplies reach valid operating levels	0 mS	-	P_PCI_RST# and RESET# should be active prior to PWRGOOD asserted.
t_{vio_prst}	All power supplies stable prior to P_PCI_RST# deasserted	1 mS	-	I/O supplies are last to reach valid operating levels.
t_{pg_rst}	PWRGOOD asserted to RESET#, P_PCI_RST# deasserted	1 mS	-	
t_{pclk_prst}	P_PCLK stable prior to P_PCI_RST# deasserted	100 µS	-	
t_{clk_prst}	CLKIN stable prior to P_PCI_RST# deasserted	1 mS	-	
t_{prst_rst}	P_PCI_RST# deasserted to RESET# deasserted	0 mS	-	
t_{pg_low}	PWRGOOD inactive pulse width	10 CLKINs	-	

Figure 10: Power On Timing



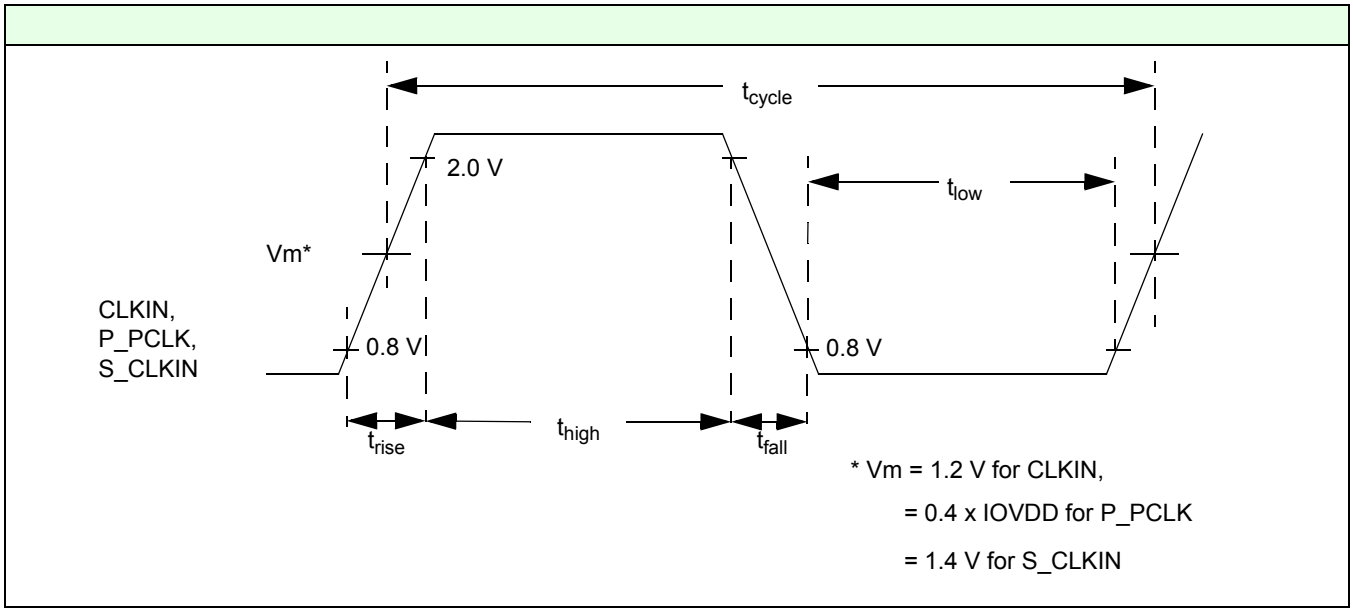
3.5.3 Input Clocks

Table 41 and Figure 11 document the timing specifications for the input clocks.

Table 41: Timing Specifications for Input Clocks

Parameter	Minimum	Maximum	Notes
f_{clk} (clock frequency)			
CLKIN	60.0 MHz	66.66 MHz	Clocks may be stopped. Not 100% tested. Guaranteed by design/characterization.
P_PCLK	30.0 MHz	33.33 MHz	
S_CLKIN	-	133.33 MHz	
t_{cycle} (clock period)			
CLKIN	15.0 nS	16.67 nS	
P_PCLK	30 nS	-	
S_CLKIN	7.5 nS	-	
t_{high} (clock high time)			
CLKIN	5.2 nS	-	Not 100% tested. Guaranteed by design/characterization.
P_PCLK	11 nS	-	
S_CLKIN	3.375 nS	-	
t_{low} (clock low time)			
CLKIN	5.0 nS	-	Not 100% tested. Guaranteed by design/characterization.
P_PCLK	11 nS	-	
S_CLKIN	3.375 nS	-	
t_{jitter} (clock jitter)			
CLKIN	-	250 pS	Spread spectrum clock generation (SSCG) is supported under the following conditions: 66.67 MHz nominal input frequency +0% / -0.6% maximum upspread / downspread 30 KHz maximum modulation frequency 250 pS max. clock jitter
P_PCLK	-	500 pS	
$t_{rise/fall}$ (clock rise and fall time)			
CLKIN	0.4 nS	1.6 nS	
P_PCLK	1.0 V/nS	4.0 V/nS	
t_{offset} (CLKIN to P_PCLK offset)	1.5 nS	4.0 nS	
t_{pll_lock} (PLL relock time)	-	20 µS	

Figure 11: Timing Specifications for Input Clocks



3.5.4 DDR SDRAM Interface

Table 42, Table 43, and Table 44, along with Figure 12 and Figure 13 document the timing specifications for the DDR SDRAM interface.

Table 42: Timing Specifications for DDR SDRAM Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	C_CLK frequency	-	133 MHz	
t_{cycle}	C_CLK period	7.5 nS	-	1
t_{low}, t_{high}	C_CLK low time, high time	0.45 bus clks	0.55 bus clks	1
t_{jitter}	C_CLK jitter	-	150 pS	1
V_x	Differential cross pt. voltage	1.1 V	1.4 V	1
t_{valid}	C_DQS output valid delay	0.75 bus clks	1.25 bus clks	2,4
t_{valid}	Output valid delay: Data signals CMD signals	 - -	 see Table 43 see Table 44	2,3,4
t_{ohold}	Output hold time: Data signals CMD signals	 see Table 43 see Table 44	 - -	2,3,4
t_{valid_dqs}	C_DQ, C_DQMB valid from C_DQS (writes)	-	3.05 nS	
t_{ohold_dqs}	C_DQ, C_DQMB hold from C_DQS (writes)	0.76 nS	-	
t_{dqs_skew}	C_DQS to C_DQ, C_DQMB skew	-0.76 nS	+0.76 nS	
t_{dqs_low}, t_{dqs_high}	C_DQS input low time, C_DQS input high time	0.45 bus clks	0.55 bus clks	
$t_{dqs\_preamble}$	C_DQS preamble valid time	0.9 bus clks	1.1 bus clks	
t_{off}	Active to float delay C_DQ C_DQS	 0 nS -0.5 nS	 2.5 nS +0.5 nS	2
n_{ras_cas}	C_RAS# to C_CAS# latency	1 bus clock	16 bus clocks	5
n_{cas_read}	C_CAS# to read latency	1 bus clock	16 bus clocks	5
n_{read_pchg}	Read precharge delay	1 bus clock	16 bus clocks	5
n_{wr_pchg}	Write precharge delay	1 bus clock	16 bus clocks	5
n_{row_pchg}	Row precharge time	1 bus clock	16 bus clocks	5,6
n_{idmrs}	Idle cycles after Mode Register Set (MRS) operation	2 bus clocks	17 bus clocks	5
n_{ras_ras}	Row cycle time	2 bus clocks	17 bus clocks	5,7
n_{burst}	Burst length	4 transfers	4 transfers	8
$n_{refresh}$	Refresh rate	128 bus clocks	16k bus clocks	5

1. Clock specifications apply to C_CLKA, C_CLKA#, C_CLKB, C_CLKB#. C_CLKA and C_CLKA# are 180° out of phase. C_CLKB and C_CLKB# are 180° out of phase. C_CLKA and C_CLKB are copies of each other.

2. The data parameters are specified relative to DQS signals and CMD parameters are specified relative to C_CLK/C_CLK# differential cross point voltage.
3. CMD signals are: C_A[12:0], C_BA[1:0], C_CAS#, C_CKE[1:0], C_CS#[3:0], C_RAS#, C_WE#.
4. Assumes 80 pF maximum load on each CMD signal and 10 pF maximum load on each of C_DQ[63:0].
5. These parameters are programmable within the processor.
6. Row precharge time is the number of bus clocks between the power on precharge and the next time RAS can be asserted.
7. Row cycle time is the number of bus clocks between refresh and the next time RAS can be asserted for other SDRAM operations. This also is the number of cycles the DDR SDRAM controller waits before starting any SDRAM access after it exits clock off mode.
8. The DDR SDRAM controller always performs burst operations.

Table 43 provides the DDR SDRAM interface output hold time (t_{ohold}) minimum timing and output valid delay (t_{valid}) maximum timing specifications for the data signals (relative to the DQS signals) for each processor SKU and LongRun step. The table covers three DDR memory speeds. Refer to *TM5500/TM5800 Development and Manufacturing Guide* for additional information on memory configuration.

Table 43: t_{ohold} and t_{valid} Timing for DDR SDRAM Data Signals

Processor			DDR Interface Frequency (MHz) / t_{ohold} min (nS) / t_{valid} max (nS)					
	Core		DDR266-CL2.5			DDR200-CL2.5		
SKU	MHz	V	Mclk	t_{ohold}	t_{valid}	Mclk	t_{ohold}	t_{valid}
900	900	1.30	129	0.75	2.09	100	0.75	2.09
	800	1.25	133	0.75	2.09	100	0.75	2.09
	667	1.20	133	0.75	1.90	95	0.75	1.90
	533	1.10	133	0.75	2.09	89	0.75	2.09
	367	0.95	122	0.75	2.35	92	0.75	2.35
867	867	1.30	124	0.75	2.09	96	0.75	2.09
	800	1.25	133	0.75	2.09	100	0.75	2.09
	667	1.20	133	0.75	1.90	95	0.75	1.90
	533	1.10	133	0.75	2.09	89	0.75	2.09
	367	0.95	122	0.75	2.35	92	0.75	2.35
800	800	1.30	133	0.75	1.83	100	0.75	1.83
	733	1.25	122	0.75	1.83	92	0.75	1.83
	667	1.20	133	0.75	1.90	95	0.75	1.90
	533	1.10	133	0.75	2.09	89	0.75	2.09
	367	0.95	122	0.75	2.35	92	0.75	2.35
733	733	1.30	122	0.75	1.83	92	0.75	1.83
	667	1.25	133	0.75	1.83	95	0.75	1.83
	533	1.15	133	0.75	1.90	89	0.75	1.90
	400	1.05	133	0.75	2.09	100	0.75	2.09
	333	0.95	111	0.75	2.35	83	0.75	2.35
700	700	1.30	117	0.75	1.83	100	0.75	1.83
	667	1.25	133	0.75	1.83	95	0.75	1.83
	533	1.15	133	0.75	1.90	89	0.75	1.90
	400	1.05	133	0.75	2.09	100	0.75	2.09
	333	0.95	111	0.75	2.35	83	0.75	2.35
667	667	1.30	133	0.75	1.83	95	0.75	1.83
	600	1.25	120	0.75	1.83	100	0.75	1.83
	500	1.15	125	0.75	1.90	100	0.75	1.90
	367	1.00	122	0.75	2.09	92	0.75	2.09
	300	0.95	100	0.75	2.35	100	0.75	2.35

Table 44 provides the DDR SDRAM interface output hold time (t_{ohold}) minimum timing and output valid delay (t_{valid}) maximum timing specifications for the CMD signals (relative to the clock signals) for each processor SKU and LongRun step. The table covers three DDR memory speeds. Refer to *TM5500/TM5800 Development and Manufacturing Guide* for additional information on memory configuration.

Table 44: t_{ohold} and t_{valid} Timing for DDR SDRAM CMD Signals

Processor			DDR Interface Frequency (MHz) / t_{ohold} min (nS) / t_{valid} max (nS)					
	Core		DDR266-CL2.5			DDR200-CL2.5		
SKU	MHz	V	Mclk	t_{ohold}	t_{valid}	Mclk	t_{ohold}	t_{valid}
900	900	1.30	129	1.84	3.42	100	1.84	3.42
	800	1.25	133	2.12	3.70	100	2.12	3.70
	667	1.20	133	1.87	3.85	95	1.87	3.85
	533	1.10	133	2.43	4.41	89	2.43	4.41
	367	0.95	122	2.10	4.73	92	2.10	4.73
867	867	1.30	124	1.93	3.51	96	1.93	3.51
	800	1.25	133	2.12	3.70	100	2.12	3.70
	667	1.20	133	1.87	3.85	95	1.87	3.85
	533	1.10	133	2.43	4.41	89	2.43	4.41
	367	0.95	122	2.10	4.73	92	2.10	4.73
800	800	1.30	133	2.12	3.70	100	2.12	3.70
	733	1.25	122	1.67	3.25	92	1.67	3.25
	667	1.20	133	1.87	3.85	95	1.87	3.85
	533	1.10	133	2.18	4.81	89	2.18	4.81
	367	0.95	122	1.60	4.90	92	1.60	4.90
733	733	1.30	122	1.67	3.25	92	1.67	3.25
	667	1.25	133	1.87	3.45	95	1.87	3.45
	533	1.15	133	2.43	4.41	89	2.43	4.41
	400	1.05	133	1.87	4.50	100	1.87	4.50
	333	0.95	111	1.83	5.13	83	1.83	5.13
700	700	1.30	117	1.76	3.34	100	1.76	3.34
	667	1.25	133	1.87	3.45	95	1.87	3.45
	533	1.15	133	2.43	4.41	89	2.43	4.41
	400	1.05	133	1.87	4.50	100	1.87	4.50
	333	0.95	111	1.83	5.13	83	1.83	5.13
667	667	1.30	133	1.87	3.45	95	1.87	3.45
	600	1.25	120	2.12	3.70	100	2.12	3.70
	500	1.15	125	2.43	4.41	100	2.43	4.41
	367	1.00	122	1.87	4.50	92	1.87	4.50
	300	0.95	100	2.10	5.40	100	2.10	5.40

Figure 12: Timing Specifications for DDR SDRAM Interface - Read Cycle

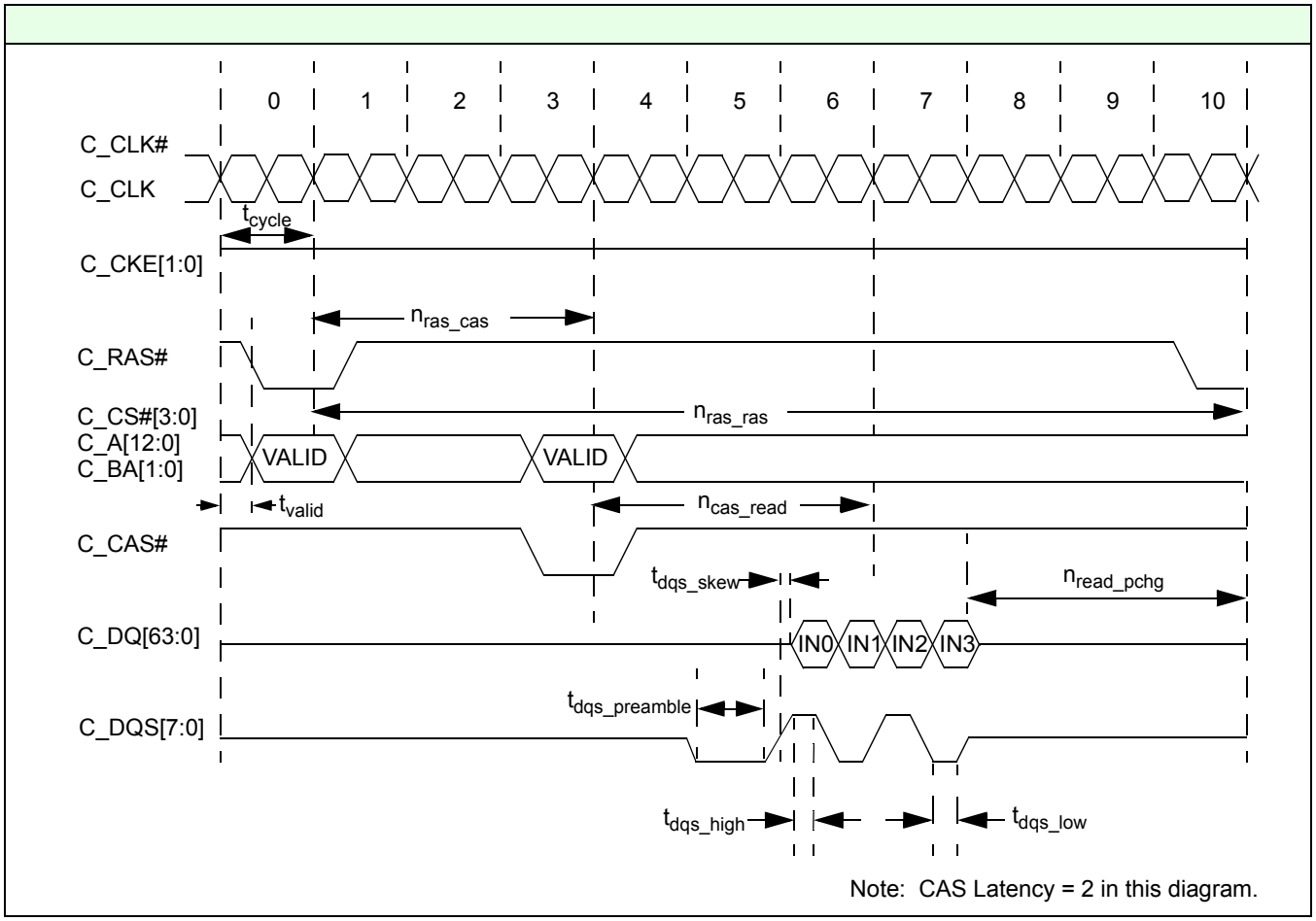
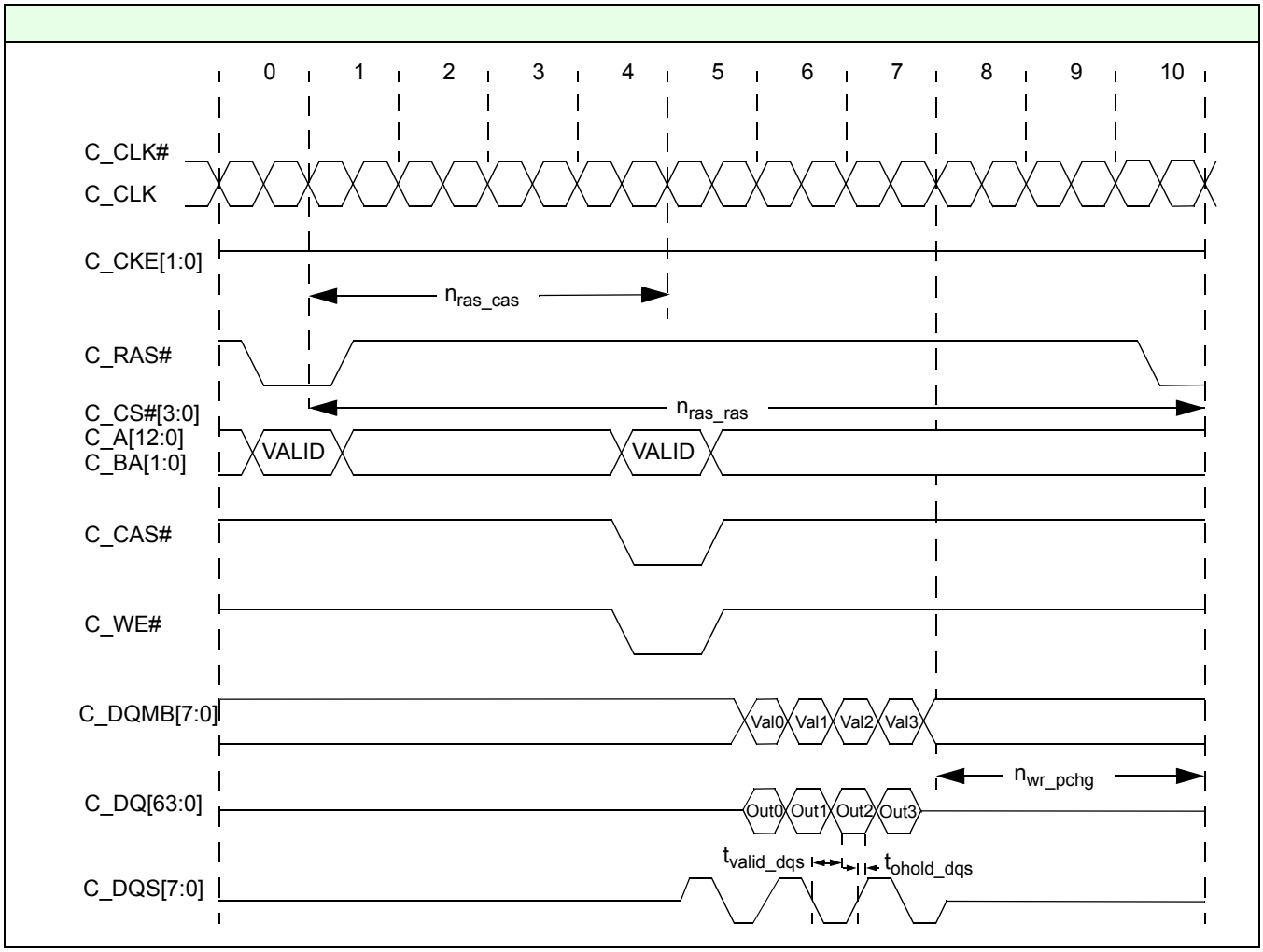


Figure 13: Timing Specifications for DDR SDRAM Interface - Write Cycle



3.5.5 SDR SDRAM Interface

Table 45 and Table 46, along withFigure 14, Figure 15, and Figure 16, document the timing specifications for the SDR SDRAM interface.

Table 45: Timing Specifications for SDR SDRAM Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	S_CLKIN, S_CLKOUT, S_CLK frequency	-	133 MHz	1
t_{setup}	Input setup time	1.7 nS	-	2, 3
t_{ihold}	Input hold time	1.9 nS	-	2, 3
t_{valid}	Output valid delay	-	see Table 46	2, 4, 5
t_{ohold}	Output hold time	see Table 46	-	2, 4, 5, 6
n_{ras_cas}	S_RAS# to S_CAS# latency	1 bus clock	16 bus clocks	6
n_{cas_read}	S_CAS# to read latency	1 bus clock	16 bus clocks	6
n_{read_pchg}	Read precharge delay	1 bus clock	16 bus clocks	6
n_{wr_pchg}	Write precharge delay	1 bus clock	16 bus clocks	6
n_{row_pchg}	Row precharge time	1 bus clock	16 bus clocks	6, 7
n_{idmrs}	Idle cycles after MRS	2 bus clocks	17 bus clocks	6, 8
n_{ras_ras}	Row cycle time	2 bus clocks	17 bus clocks	6, 9
n_{burst}	Burst length	4 transfers	4 transfers	10
$n_{refresh}$	Refresh rate	128 bus clocks	16K bus clocks	6

1. S_CLK[3:0] are copies of S_CLKOUT.
2. These parameters are specified relative to S_CLKIN rising edge at 1.4 V level.
3. Input signals are: S_DQ[63:0].
4. Output signals are:
   Data = S_DQ[63:0], S_DQMB[7:0]
   Address = S_A[12:0], S_BA[1:0], S_CAS#, S_RAS#, S_WE#
   Enables = S_CKE[1:0], S_CS#[3:0]
5. Assumes 50 pF load for output signals. For every 10 pF above a 50 pF load, add 170 pS for the data and enable signals, and 90 pS for the address signals. For every 10 pF below a 50 pF load, subtract 170 pS for the data and enable signals, and 90 pS for the address signals.
6. These parameters are programmable within the processor.
7. Row precharge time is the number of bus clocks between the power on precharge and the next time RAS can be asserted.
8. MRS stands for Mode Register Set operation.
9. Row cycle time is the number of bus clocks between refresh and the next time RAS can be asserted for other SDRAM operations. This also is the number of cycles the SDR SDRAM controller waits before starting any SDRAM access after it exits clock off mode.
10. The SDR SDRAM controller always performs burst operations.

Figure 14: SDR SDRAM Input Setup/Hold and Output Valid Delay/Hold Timing

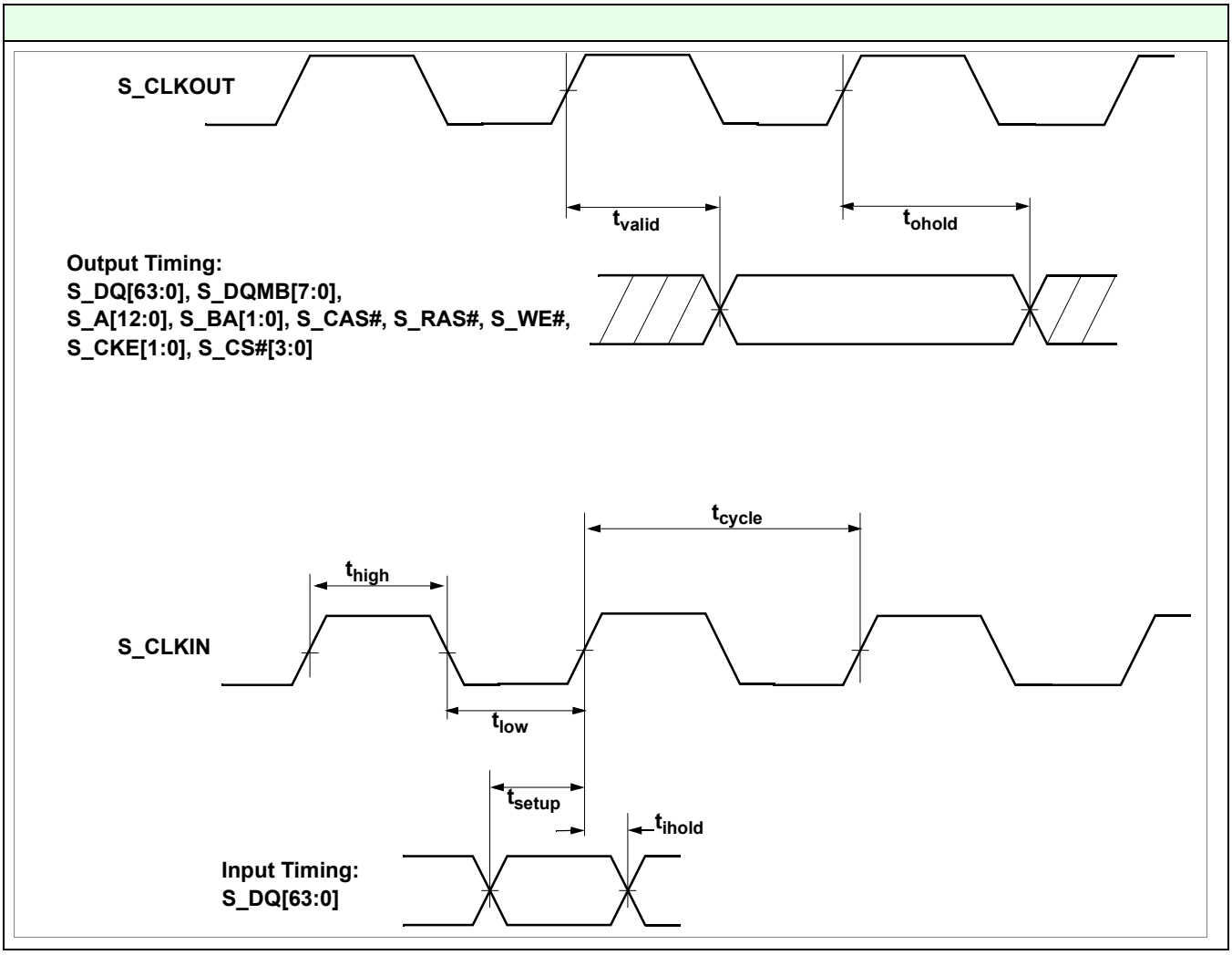


Table 46 provides the SDR SDRAM interface output hold time (t_{ohold}) minimum timing and output valid delay (t_{valid}) maximum timing specifications for each processor SKU and LongRun step. The table covers three SDR memory speeds. Refer to *TM5500/TM5800 Development and Manufacturing Guide* for additional information on memory configuration.

Table 46: t_{ohold} and t_{valid} Timing Specifications for SDR SDRAM Interface

Processor			SDR Interface Frequency (MHz) / t_{ohold} min (nS) / t_{valid} max (nS)								
	Core		SDR133-CL3			SDR125-CL3			SDR100-CL3		
SKU	MHz	V	Mclk	t_{ohold}	t_{valid}	Mclk	t_{ohold}	t_{valid}	Mclk	t_{ohold}	t_{valid}
900	900	1.30	129	1.72	3.72	113	1.72	3.72	100	1.72	3.72
	800	1.25	133	1.38	3.38	114	1.38	3.38	100	1.38	3.38
	667	1.20	133	1.65	3.95	111	1.65	3.95	95	1.65	3.95
	533	1.10	133	1.28	3.58	107	1.28	3.58	89	1.28	3.58
	367	0.95	122	1.88	4.83	122	1.88	4.83	92	1.88	4.83
867	867	1.30	124	1.23	3.23	124	1.23	3.23	96	1.23	3.23
	800	1.25	133	1.38	3.38	114	1.38	3.38	100	1.38	3.38
	667	1.20	133	1.65	3.95	111	1.65	3.95	95	1.65	3.95
	533	1.10	133	1.28	3.58	107	1.28	3.58	89	1.28	3.58
	367	0.95	122	1.88	4.83	122	1.88	4.83	92	1.88	4.83
800	800	1.30	133	1.38	3.38	114	1.38	3.38	100	1.38	3.38
	733	1.25	122	1.55	3.55	122	1.55	3.55	92	1.55	3.55
	667	1.20	133	1.65	3.95	111	1.65	3.95	95	1.65	3.95
	533	1.10	133	1.96	4.91	107	1.96	4.91	89	1.96	4.91
	367	0.95	122	1.50	4.90	122	1.50	4.90	92	1.50	4.90
733	733	1.30	122	1.55	3.55	122	1.55	3.55	92	1.55	3.55
	667	1.25	133	1.75	3.75	111	1.75	3.75	95	1.75	3.75
	533	1.15	133	1.28	3.58	107	1.28	3.58	89	1.28	3.58
	400	1.05	133	1.65	4.60	100	1.65	4.60	100	1.65	4.60
	333	0.95	111	1.73	5.13	111	1.73	5.13	83	1.73	5.13
700	700	1.30	117	1.64	3.64	117	1.64	3.64	100	1.64	3.64
	667	1.25	133	1.75	3.75	111	1.75	3.75	95	1.75	3.75
	533	1.15	133	1.28	3.58	107	1.28	3.58	89	1.28	3.58
	400	1.05	133	1.65	4.60	100	1.65	4.60	100	1.65	4.60
	333	0.95	111	1.73	5.13	111	1.73	5.13	83	1.73	5.13
667	667	1.30	133	1.75	3.75	111	1.75	3.75	95	1.75	3.75
	600	1.25	120	2.00	4.00	120	2.00	4.00	100	2.00	4.00
	500	1.15	125	1.28	3.58	125	1.28	3.58	100	1.28	3.58
	367	1.00	122	1.65	4.60	122	1.65	4.60	92	1.65	4.60
	300	0.95	100	2.00	5.40	100	2.00	5.40	100	2.00	5.40

Figure 15: Timing Specifications for SDR SDRAM Interface - Read Cycle

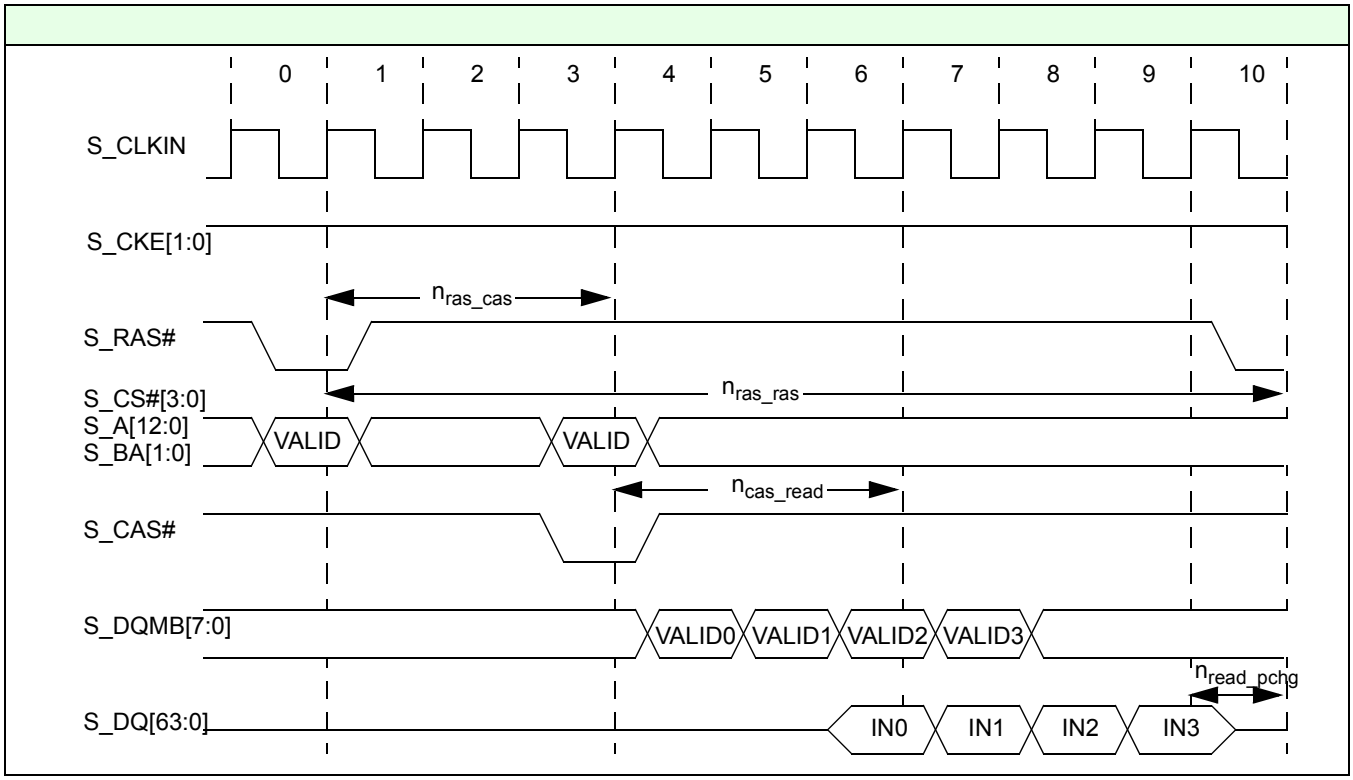
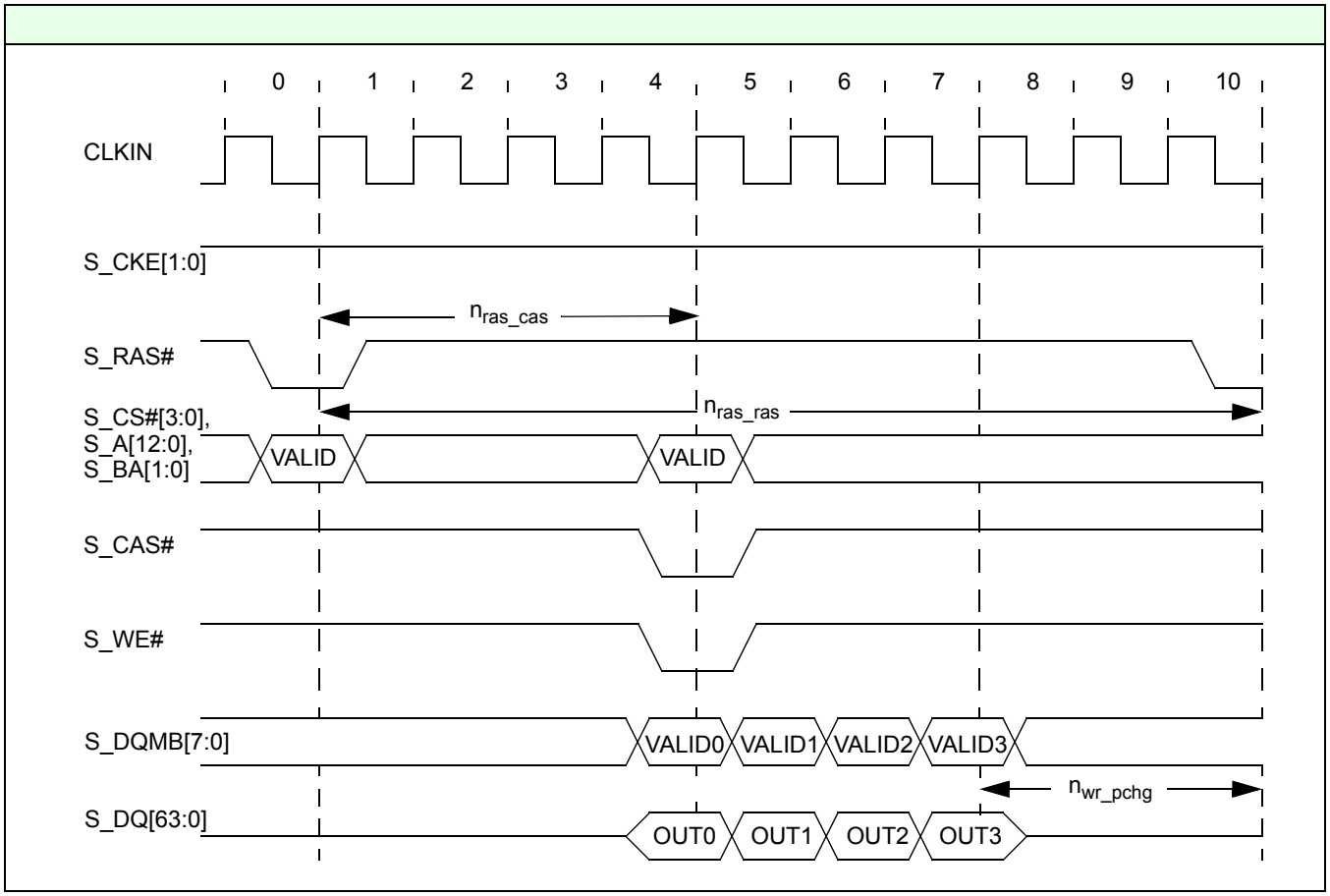


Figure 16: Timing Specifications for SDR SDRAM Interface - Write Cycle



3.5.6 PCI Interface

Table 47 documents the timing specifications for the PCI interface. The PCI interface is compliant with revision 2.1 of the PCI Local Bus Specification. Refer to the PCI specification for additional information.

Table 47: Timing Specifications for PCI Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	P_PCLK frequency	30.0 MHz	33.33 MHz	
t_{setup}	Input setup time			
	P_REQ#[5:0]	12 nS	-	1, 2
	All other inputs	7 nS	-	
t_{ihold}	Input hold time	0 nS	-	1, 2
t_{valid}	Output valid delay			
	P_GNT#[5:0]	2 nS	12 nS	1, 3
	All other outputs	2 nS	11 nS	
t_{off}	Active to float delay	-	28 nS	
t_{rst_off}	P_PCI_RST# asserted to output float delay	-	40 nS	

1. These parameters are specified relative to P_PCLK rising edge at 0.4*IOVDD level.
2. Input signals are: P_AD[31:0], P_C/BE#[3:0], P_CLKRUN#, P_DEVSEL#, P_FRAME#, P_HOLD#, P_IRDY#, P_LOCK#, P_PAR, P_PCI_RST#, P_PERR#, P_REQ#[5:0], P_SERR#, P_STOP#, P_TRDY#.
3. Output signals are: P_AD[31:0], P_C/BE#[3:0], P_CLKRUN#, P_DEVSEL#, P_FRAME#, P_GNT#[5:0], P_HLDA#, P_IRDY#, P_LOCK#, P_PAR, P_PERR#, P_STOP#, P_TRDY#.

3.5.7 Southbridge Sidebands and Power Management Interface

IGNNE#, INIT#, INTR, NMI, PWRGOOD, SLEEP#, SMI# and STPCLK# are asynchronous input signals. Therefore, these inputs are not required to meet any setup and hold specifications.

3.5.8 Debug Interface

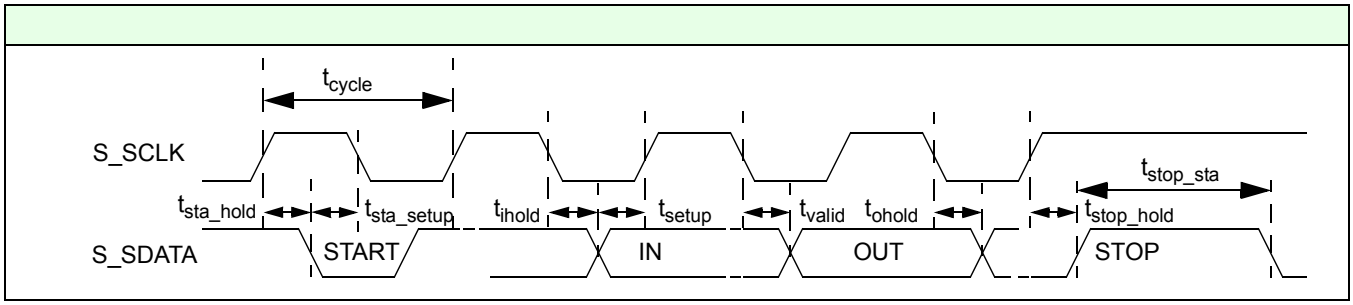
Table 48 and Figure 17 document the timing specifications for the debug serial interface.

Table 48: Timing Specifications for Debug Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	S_SCLK frequency	0	400 KHz	1
t_{cycle}	S_SCLK period	2.5 µS	-	
t_{high}	S_SCLK high time	600 nS	-	1
t_{low}	S_SCLK low time	1.3 µS	-	1
t_{rise}	S_SCLK, S_SDATA rise time	-	1 µS	2
t_{fall}	S_SCLK, S_SDATA fall time	-	300 nS	2
t_{stop_sta}	Bus free to new transaction	1.3 µS	-	
t_{sta_setup}	Start condition setup time	600 nS	-	3, 4
t_{sta_hold}	Start condition hold time	600 nS	-	3, 5
t_{stop_hold}	Stop condition setup time	600 nS	-	4, 6
t_{setup}	S_SDATA input setup time	100 nS	-	4
t_{ihold}	S_SDATA input hold time	0 nS	-	5
t_{valid}	S_SDATA output valid delay	-	350 nS	5
t_{ohold}	S_SDATA output hold time	250 nS	-	5

1. Not 100% tested. Guaranteed by design/characterization.
2. Rise and fall times are specified from 20% to 80%.
3. Start condition occurs when S_SDATA transitions from high to low while S_SCLK is high.
4. specified relative to S_SCLK rising edge at 1.5 V level. Assumed loading is 400 pF.
5. specified relative to S_SCLK falling edge at 1.5 V level. Assumed loading is 400 pF.
6. Stop condition occurs when S_SDATA transitions from low to high while S_SCLK is high.

Figure 17: Timing Specifications for Debug Interface



3.5.9 Code Morphing Software Boot ROM Interface

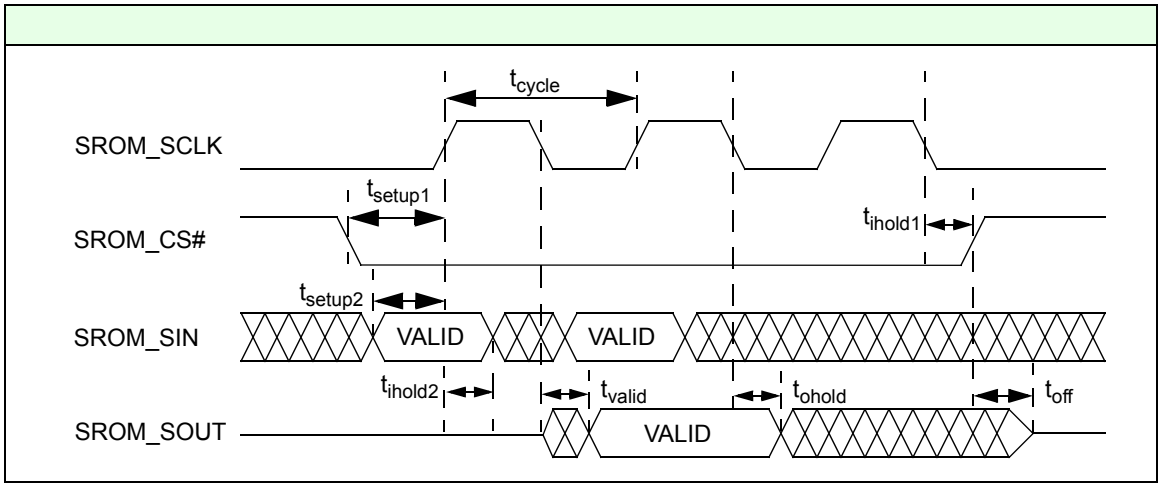
Table 49 and Figure 18 document the timing specifications for the Code Morphing software boot ROM serial interface.

Table 49: Code Morphing Software Boot ROM Interface Timing

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	SROM_SCLK frequency	-	11 MHz	
t_{cycle}	SROM_SCLK period	90 nS	-	
t_{high}	SROM_SCLK high time	40 nS	-	
t_{low}	SROM_SCLK low time	40 nS	-	
t_{setup1}	SROM_CS# input setup time	350 nS	-	1
t_{ihold1}	SROM_CS# input hold time	350 nS	-	2
t_{cs_high}	SROM_CS# high time	100 nS	-	
t_{setup2}	SROM_SIN input setup time	20 nS	-	1
t_{ihold2}	SROM_SIN input hold time	0 nS	-	1
t_{valid}	SROM_SOUT output valid delay	-	85 nS	2
t_{ohold}	SROM_SOUT output hold time	35 nS	-	2
t_{off}	SROM_SOUT active to float delay	-	100 nS	

1. These conditions are specified relative to SROM_SCLK rising edge at 1.4 V level.
2. These conditions are specified relative to SROM_SCLK falling edge at 1.4 V level.

Figure 18: Code Morphing Software Boot ROM Interface Timing



3.5.10 Configuration (Mode-bit) ROM Interface

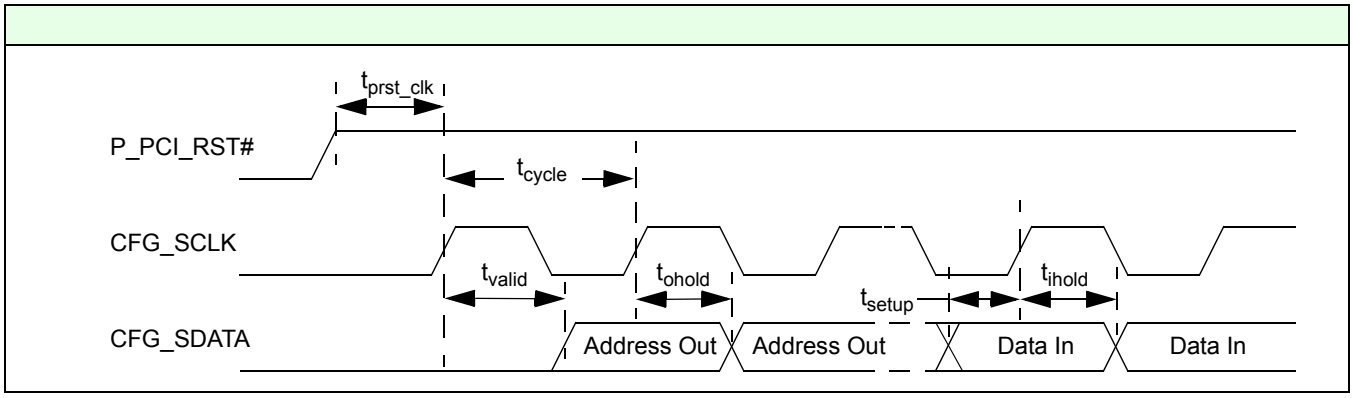
Table 50 and Figure 19 document the timing specifications for the configuration (mode-bit) ROM interface.

Table 50: Timing Specifications for Configuration ROM Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	CFG_SCLK frequency	-	2 MHz	
t_{cycle}	CFG_SCLK clock period	0.5 mS	2 mS	1
t_{high}	CFG_SCLK high time	250 nS	-	
t_{low}	CFG_SCLK low time	250 nS	-	
t_{prst_clk}	P_PCI_RST# to CFG_SCLK active high	100 nS	-	
t_{setup}	CFG_SDATA input setup time	600 nS	-	2
t_{ihold}	CFG_SDATA input hold time	0 S	-	2
t_{valid}	CFG_SDATA output valid delay	-	900 nS	2
t_{ohold}	CFG_SDATA output hold time	100 nS	-	2

1. CFG_SCLK period is CLKIN period × 72. For 66 MHz CLKIN, CFG_SCLK period is 1.08 mS.
2. These parameters are specified relative to CFG_SCLK rising edge at 1.4 V level.

Figure 19: Timing Specifications for Configuration ROM Interface



3.5.11 JTAG Interface

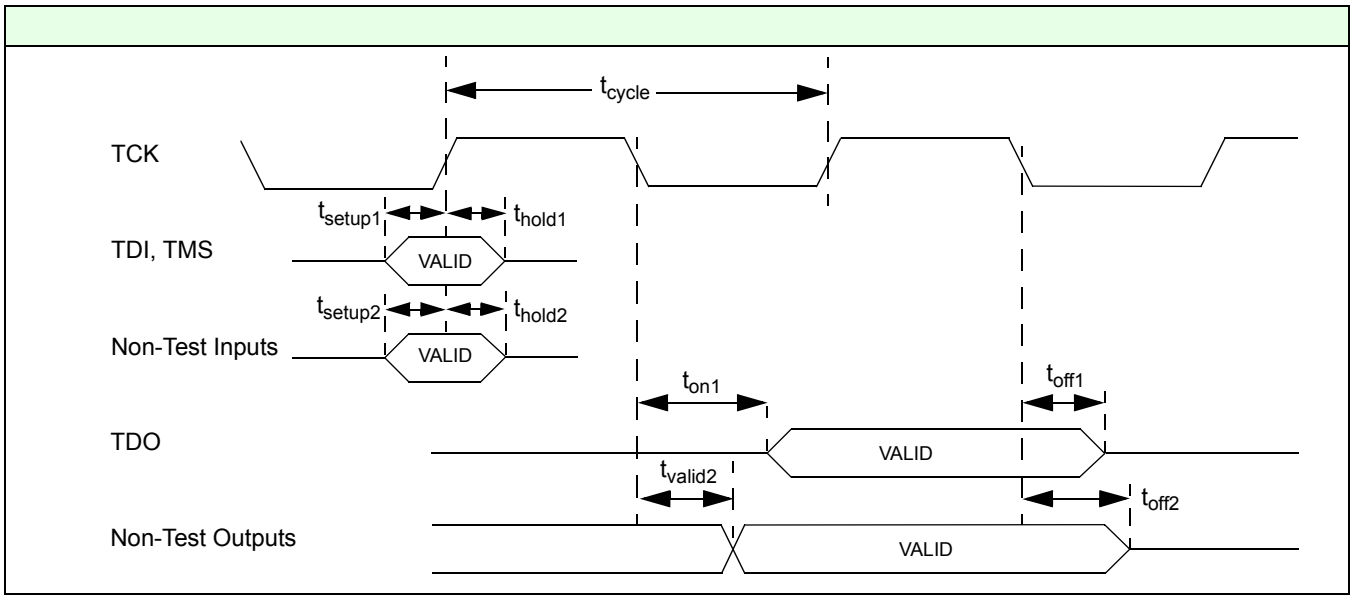
Table 51 and Figure 20 document the timing specifications for the JTAG interface. TRST# is an asynchronous signal. Therefore there is no setup or hold time specified for TRST# in Table 51.

Table 51: Timing Specifications for JTAG Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	TCK frequency		50 MHz	
t_{cycle}	TCK clock period	20 nS	-	
t_{low}	TCK low time	8 nS	-	
t_{high}	TCK high time	8 nS	-	
t_{rise}	TCK rise time	-	2 nS	
t_{fall}	TCK fall time	-	2 nS	
t_{reset}	TRST# pulse width	200 nS	-	
t_{setup1}	TDI, TMS input setup time	10 nS	-	1
t_{hold1}	TDI, TMS input hold time	10 nS	-	1
t_{on1}	TDO float to active delay	5 nS	10 nS	2
t_{off1}	TDO active to float delay	-	10 nS	2
t_{setup2}	Non-test inputs setup time	10 nS	-	1
t_{hold2}	Non-test inputs hold time	-	10 nS	1
t_{valid2}	Non-test outputs valid delay	-	10 nS	2
t_{off2}	Non-test outputs active to float delay	-	20 nS	2

1. These parameters are specified relative to TCK rising edge at 1.4 V level.
2. These parameters are specified relative to TCK falling edge at 1.4 V level.

Figure 20: Timing Specifications for JTAG Interface



Chapter 4

Mechanical Specifications

4.1 Thermal Specifications

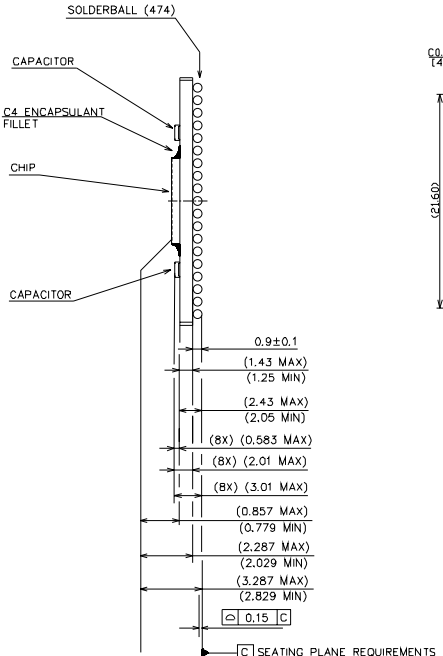
The maximum junction temperature for TM5500/TM5800 processors is 100 °C or 90 °C, depending on the SKU. See *Package Marking Descriptions* on page 89 for details on the device temperature package marking identifier.

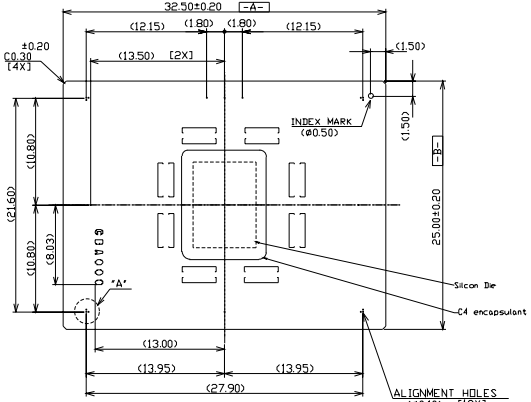
The junction-to-package top (exposed silicon die) thermal resistance (θ_{jp}) is 0.075 °C/W, and the junction-to-PCB thermal resistance (θ_{jb}) is 3.3 °C/W. For detailed information on processor thermal characteristics and thermal solution design, please refer to the *TM5500/TM5800 Thermal Design Guide*.

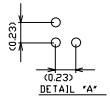
4.2 Package Dimensions

The TM5500/TM5800 processor is supplied in a 474-contact ceramic ball-grid array (CBGA) package. The dimensions for this package are shown in the drawings on the following pages. For more information on the TM5500/TM5800 package, see the *TM5500/TM5800 Package Specifications and Manufacturing Guide*.

REVISIONS/ENGINEERING CHANGE ORDER				
REV	ECO #	DESCRIPTION	DATE	BY
	-		01/01	BF







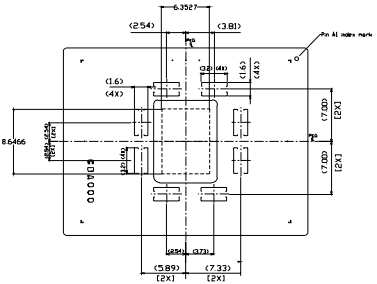
CONFIDENTIAL

Transmeta Corporation

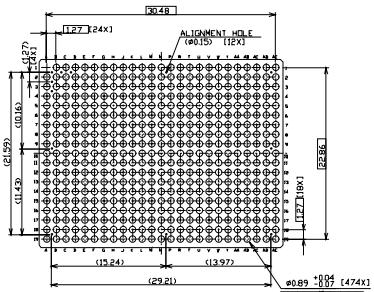
3940 FREEDOM CIRCLE SANTA CLARA, CALIFORNIA 95054

TOLERANCES UNLESS NOTED		TITLE: MODULE ASSEMBLY 25mm x 32.5mm
		SCALE: NONE
		PART NUMBER: 5232
LINEAR ±	0.5	SHEET: 1 OF 2
ANGLES ±	0° 30'	DESIGNER: Bruce Frederick
RADII UNLESS NOTED		CHECKED BY: BF
EDGE/CORNER OUTSIDE MAX		APPROVED: GB
BREAKS INSIDE MAX		ACAD#

REVISIONS/ENGINEERING CHANGE ORDER				
REV	ECO #	DESCRIPTION	DATE	BY
	–		01/01	BF



Capacitor Location Detail



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. THIS MODULE CONFORMS TO JEDEC REGISTRATION MO-157 REV. B.
3. SOLDER BALL COMPOSITION: 90 % LEAD/10% TIN.
4. SUBSTRATE BASE MATERIAL: ALUMINA (BLACK).

Transmeta Corporation

3940 FREEDOM CIRCLE SANTA CLARA, CALIFORNIA 95054

TOLERANCES UNLESS NOTED		TITLE: MODULE ASSEMBLY 25mm x 32.5mm	
		SCALE: NONE	PART NUMBER: 5232
LINEAR ±	0.5		SHEET: 2 OF 2
ANGLES ±	0° 30'	THIRD ANGLE PROJECTION	DESIGNER: Bruce Frederick
RADII UNLESS NOTED			CHECKED BY: BF
EDGE/CORNER BREAKS	OUTSIDE MAX INSIDE MAX		APPROVED: GB
		ACAD#	

4.3 Package Marking

Figure 21 shows the location of the TM5500/TM5800 processor package markings.

Figure 21: Package Marking Locations - Top View

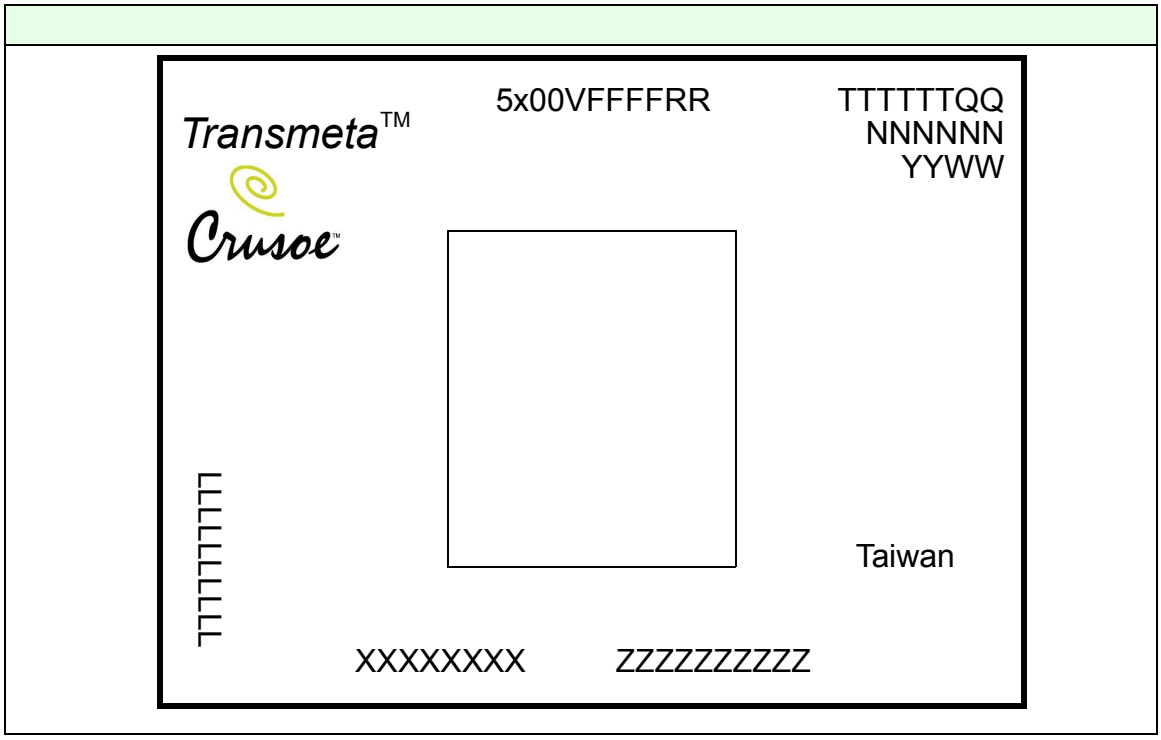


Table 52: Package Marking Descriptions

Field	Description	
5*x*00*VFFFFRR*	Part model, voltage, frequency, and version/revision identifier:	
	5x00	Model number: 5500 = Model TM5500 5800 = Model TM5800
	V	Operating voltage range and temperature: A = 0.95-1.30 V 100 °C L = 0.95-1.30 V 90 °C
	FFFF	Operating frequency (MHz): 0900 0867 0800 0733 0700 0667
	RR	Silicon version/revision identifier: 3 = Version 0.3 4 = Version 0.4 10 = Version 1.0
TTTTTTQQ	Transmeta tracking number and quality indicator:	
	TTTTTT	Transmeta tracking number
	QQ	Quality indicator: MS = Mechanical sample ES = Engineering sample Blank = Production level
NNNNNN	Lot number	
YYWW	Date code:	
	YY	Year
	WW	Work week
LLLLLLLLLL	Substrate part number	
XXXXXXXX *ZZZZZZZZZZ*	Transmeta tracking numbers	
Taiwan	Country of origin	