



TM5500/TM5800 Package Specifications and Manufacturing Guide

June 17, 2002

Crusoe™ Processor Model TM5500/TM5800

TM5500/TM5800 Package Specifications and Manufacturing Guide
Version 0.2

Revision History

- 0.1 Preliminary and first release version
- 0.2 Updated package marking specifications

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TM5500/TM5800 Package

TM5500/TM5800 processors utilize a 474-contact flip-chip ceramic BGA (FC-CBGA) package. This document provides package mechanical and thermal specifications, drawings, reflow guidelines, and assembly information.

1.0 Package Specifications

TM5500/TM5800 package thermal and mechanical specifications are provided below.

1.1 Thermal Specifications

The maximum junction temperature for TM5500/TM5800 processors is 100°C and 90°C. The junction-to-package top (exposed silicon die) thermal resistance (θ_{jp}) is 0.075°C/W, and the junction-to-PCB thermal resistance (θ_{jb}) is 3.3°C/W. For detailed information on processor thermal characteristics and thermal solution design, please refer to the *TM5500/TM5800 Thermal Design Guide*.

1.2 Mechanical Specifications

The maximum short-term heatsink attachment pressure, centered and normal to the FC-CBGA package, may not exceed 40 N/cm² (50 PSI). Under no circumstances shall the total load exceed 20 lbf (89 N).

Maximum short-term dynamic tensile force should not exceed 14.7 N (1.5 Kg equivalent).

Maximum short-term dynamic compressive force shall not exceed 69.7 N (7.1 Kg equivalent).

Long-term static tensile forces are not allowed.

Maximum long-term static compressive force on the package shall not exceed 46.5 N (4.75 Kg equivalent).

The maximum total mass of the FC-CBGA package with attached heatsink, without an auxiliary heatsink attachment mechanism, should not exceed 96 grams. Based on a component weight of 7.2 grams, this allows a heatsink assembly of up to 88.8 grams.

The package solder ball standoff height after reflow should be 0.89 +/- 0.10 mm.

2.0 Package Marking

The figure below shows the location of the TM5500/TM5800 package markings. The fields shown are described in detail in the table following the figure.

FIGURE 1 Package Marking Locations - Top View

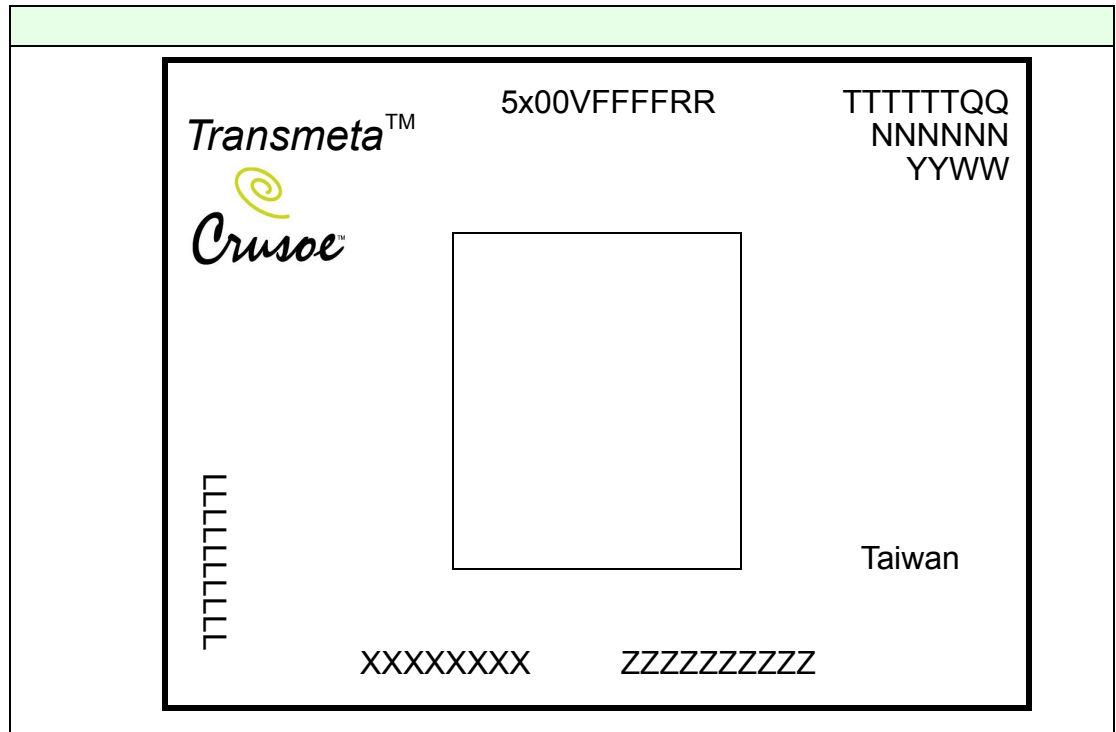
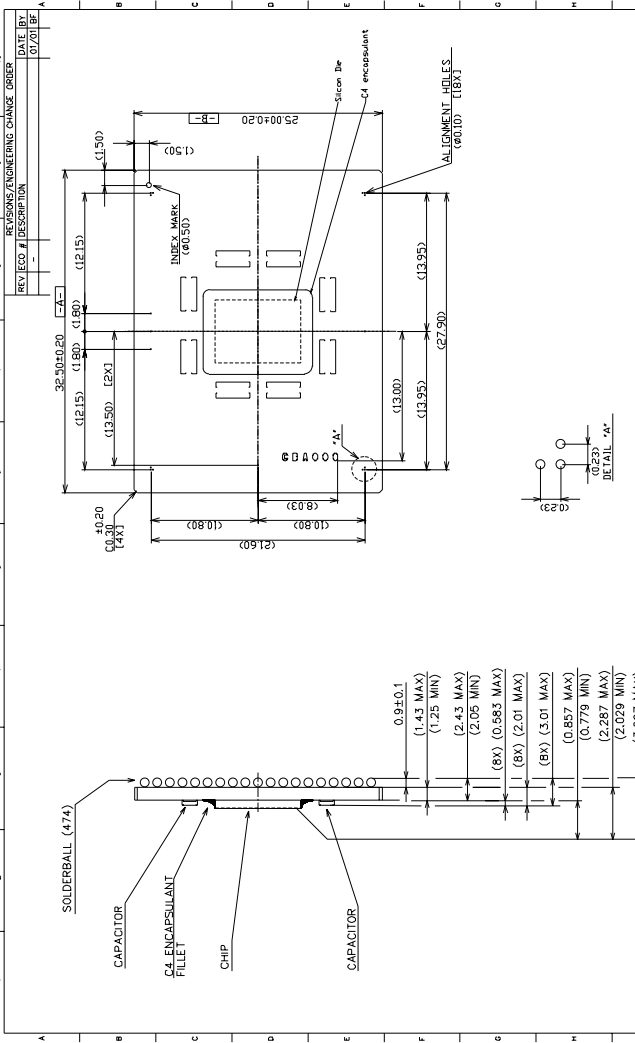


TABLE 1 Package Marking Descriptions

Field	Description	
5x00VFFFRR	Part model, voltage, frequency, and version/revision identifier:	
	5x00	Model number: 5500 = Model TM5500 5800 = Model TM5800
	V	Operating voltage range and temperature: A = 0.95-1.30 V 100 °C L = 0.95-1.30 V 90 °C
	FFFF	Operating frequency (MHz): 0900 0867 0800 0733 0700 0667
	RR	Silicon version/revision identifier: 3 = Version 0.3 4 = Version 0.4 10 = Version 1.0
TTTTTQQ	Transmeta tracking number and quality indicator:	
	TTTTT	Transmeta tracking number
	QQ	Quality indicator: MS = Mechanical sample ES = Engineering sample Blank = Production level
NNNNNN	Lot number	
YYWW	Date code:	
	YY	Year
	WW	Work week
LLLLLLLLLL	Substrate part number	
XXXXXXXXX ZZZZZZZZZZ	Transmeta tracking numbers	
Taiwan	Country of origin	

3.0 Package Drawings

Drawings for the TM5500/TM5800 FC-CBGA package are provided below.



REV		ECO #	DESCRIPTION	DATE	BY
				01/01	BF
REVISIONS/ENGINEERING CHANGE ORDER					

TOLERANCES UNLESS NOTED		TITLE: MODULE ASSEMBLY 25mm x 32.5mm
LINEAR #	SCALE: NONE	PART NUMBER: 5232
ANGLES #	0.5	SHEET: 1 OF 2
RADI UNLESS NOTED	Ø 20	DESIGNER: Bruce Frederick
EDGE / CORNER	OUTSIDE MAX	CHECKED BY: BF
BREAS	INSIDE MAX	APPROVED: GB
		AC/DF

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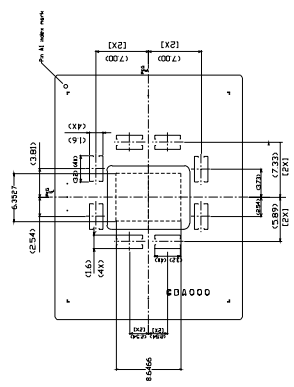
SEATING PLANE REQUIREMENTS

0.9 ± 0.1	(1.43 MAX)
(1.25 MIN)	(2.43 MAX)
(2.05 MIN)	(0.583 MAX)
(8X)	(2.01 MAX)
(8X)	(3.01 MAX)
(0.857 MAX)	(0.779 MIN)
(2.287 MAX)	(2.029 MIN)
(3.287 MAX)	(2.829 MIN)
0.15 [C]	

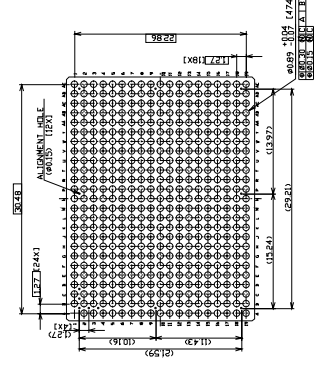
[C] SEATING PLANE REQUIREMENTS

CONFIDENTIAL

REVISIONS/ENGINEERING CHANGE ORDER	
REV	ECO # DESCRIPTION
01	01/01 BF



Capacitor Location Detail



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. THIS MODULE CONFORMS TO JEDEC REGISTRATION MO-157 REV. B.
3. SOLDER BALL COMPOSITION: 90 % LEAD/10% TIN.
4. SUBSTRATE BASE MATERIAL: ALUMINA (BLACK).

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TOLERANCES UNLESS NOTED	SCALE: NONE
TITLE: MODULE ASSEMBLY 25mm x 32.5mm	PART NUMBER: 5232
LINE # 0.5	SHEET: 2 OF 2
ANGLE #	DESIGNER: Bruce Frederick
RADI UNLESS NOTED	CHECKED BY: BF
EDGE/CORNER	APPROVED: CB
INSIDE MAX	AC/ADP

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4.0 Surface Mount Assembly and Rework Guidelines

The reflow profile guidelines below were developed to optimize FC-CBGA / mixed SMT technology assemblies used for TM5500/TM5800-based system designs. These guidelines can be used to achieve maximum solderability using no-clean (essentially RMA) type chemistries.

4.1 Overview

It is important to note that achieving a 'picture' perfect profile is not the objective. The objective is to maximize flux activation, reduce exposure to oxidation, and provide uniform solder paste melting and wetting across the total assembly surface during the reflow phase of the process.

The reflow profile guidelines provided below are intended as a starting point for determining the optimal profile for any given PCB assembly and manufacturing environment. The profile will need slight adjustments when using Palladium components, moving more toward the peak maximum temperature ranges. Final proof of a successful profile resides with the visual appearance of good wetting angles for every component on the assembly and the lack of appearance of grainy or disturbed solder joints.

4.2 Reflow Profile Guidelines

The table and figure below provide reflow profile guidelines for the TM5500/TM5800 FC-CBGA package. Note that the solder reflow process is highly dependent on factors such as oven type, solder paste selection, PCB thickness and density, component distribution on the PCB, etc. A specific thermal profile as provided below cannot suite all designs and manufacturing situations.

The information provided below is meant to be a guideline and not a firm rule. The ultimate determining factors in whether a specific reflow profile is acceptable should be visually good and mechanically sound solder joints.

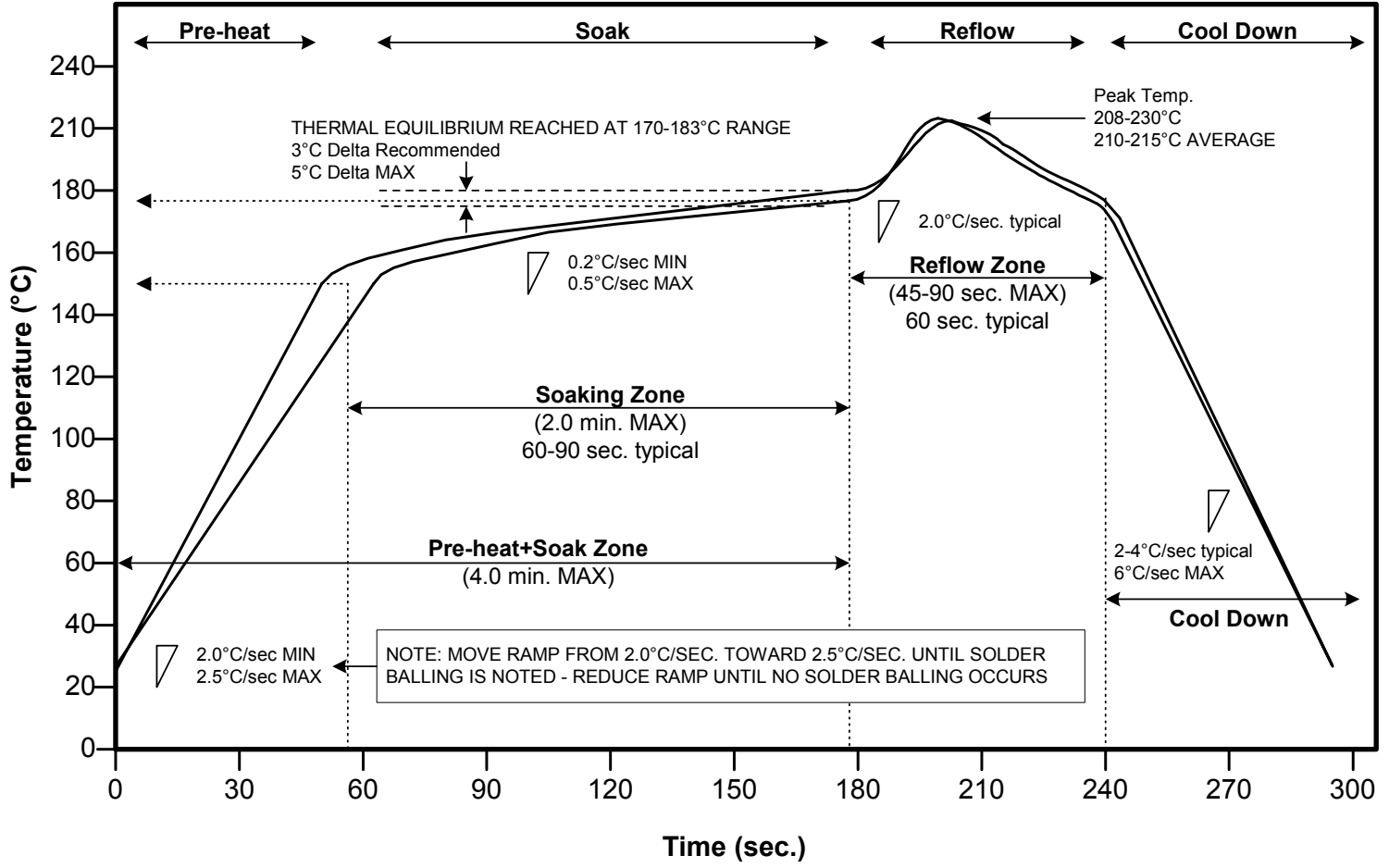
TABLE 2 TM5500/TM5800 FC-CBGA / Mixed SMT Reflow Recommendations

Zone	Temperature Range (begin/end, °C)	Ramp Range (°C/second)	Time (seconds)	Notes
Pre-heating	Beg: room temp	Min: 2.0°C/sec	Typ: ~ 90 sec	1
	End: 150°C	Max: 2.5°C/sec	Max: 120-240 sec	
Soaking	Beg: 150°C	Min: 0.2°C/sec	Typ: 60-90 sec	2
	End: 170-183°C	Max: 0.5°C/sec	Max: 120 sec	
Reflow	Beg: 170-183°C	Min: 2.0°C/sec	Typ: ~ 60 sec	3
	Peak: 208-230°C	Max:	Max: 45-90 sec	
	End: 170-183°C			
Cool-down	Beg: 170-183°C	Typ: 2-4°C/sec	Typ:	
	End: room temp	Max: 6°C/sec	Max:	

1. Pre-heating zone ramp from room temperature to 150°C: The overall objective is to minimize the time the assembly remains in the oven to avoid oxidation. The starting point to determine the correct ramp rate is recommended at 2.0°C/second. Then, increase the ramp rate incrementally to 2.5°C/second. If problems are noted, such as solder balls, then the ramp should be reduced until the defects are eliminated. PCB characteristics can contribute to solder balls and it is recommended to use a matt finish solder mask. The moisture content can also contribute to solder balls and should be managed appropriately.
2. Soaking zone ramp and thermal equilibrium: After reaching 150°C, slow the ramp rate to 0.2-0.5°C/second. The objective is to achieve thermal equilibrium across the assembly. The hottest and coldest measurements should not exceed 3°C (ΔT), minimum-to-maximum. The recommendation is to achieve the ΔT of 3°C in the range of a 170-183°C window. To minimize oxide build up, move out of the soaking zone into reflow immediately upon reaching equilibrium.
3. Reflow zone ramp: After reaching thermal equilibrium in the soaking zone, move the ramp from 0.5°C/second to a minimum of 2.0°C/second. Slow heating in the reflow area can result in tombstoning and/or grainy and uneven wetting visual characteristics. If the heating rate is too fast in the reflow area, solder balls (splatter) can develop.

4.3 Reflow Profile Diagram

A reflow profile diagram is provided in the figure below. This figure should be used in conjunction with the table above for developing optimal reflow processes for PCB assemblies containing TM5500/TM5800 FC-CBGA devices.



4.4 Other Assembly Issues

Paste Volume

The FC-CBGA solder wetting appearance, and subsequent second-level reliability, is subject to the amount of paste used. The volume used to mount the balls to ceramic is equivalent to using a 0.010-inch thick stencil and a 0.035-inch pad opening. While it may be difficult to achieve this actual solder volume on a production board populated with other fine-pitch components, this solder volume should be used as a goal for achieving optimal quality and reliability. It is important to maximize the stencil opening for the FC-CBGA to compensate for board warp and co-planarity changes from component-to-component.

Component Placement in Paste

CBGA ball deposition into the solder paste is a critical parameter for wetting. It is speculated that the surface area of the ball actually making contact with the paste provides the only active area available for cleaning. A controlled set of experiments is being conducted to optimize ball insertion into paste using Panasonic MPA equipment. Pending results of these experiments, a maximum placement setting will be recommended.

4.5 ESD

Although the Crusoe processor contains protective circuitry to resist damage from electrostatic discharge (ESD), the devices should only be used or handled at a static safeguarded work area. Do not ship or store the devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.