Transmeta™ Efficeon™ TM8300 Processor

The Transmeta Efficeon TM8300 processor is designed to address the ever-growing demand for x86 processing in value driven and energy conscious systems. Based upon a highly energy efficient design, the Efficeon TM8300 processor supports Transmeta’s LongRun power and thermal management technology and fully integrated Northbridge functionality. The I/O interfaces built into the Efficeon processor’s integrated Northbridge are matched with its high performance core, featuring support for DDR-400 memory, a 1.6 GB/s HyperTransport™ interconnect, and an AGP 4X graphics interface.

With the new Code Morphing Software for the Efficeon processor, Transmeta extends its leadership in power management, offering a solution that provides high performance while consuming less power for the same work. To maximize performance and responsiveness, the Efficeon TM8300 processor is based upon the same architecture and feature of the Efficeon TM8600 processor. Featuring a 256-bit wide VLIW engine that can execute up to 8 instructions per clock cycle, a 512KB L2 cache, and support for SSE & SSE2 instructions, the Efficeon TM8300 processor provides for a rich and compelling multimedia experience.

The result is a highly efficient x86 solution suitable for advanced web tablets, point of sale terminals (POS), high-end thin clients, notebooks and many other applications where an integrated, low power x86 processor is desirable.

HIGHLY INTEGRATED ARCHITECTURE

**Fully Integrated Northbridge Core Logic**
- On-chip DDR-400 memory interface
- Integrated AGP 2.0 compliant graphics interface for industry standard, high performance graphics solutions at 1X, 2X & 4X data rates
- On-chip 400 MHz HyperTransport™ interface, 8-bits wide in each direction, provides 12x the I/O throughput compared to 32-bit, 33 MHz PCI.
- Full support for ECC in L2 cache and northbridge memory controller enables expansion into the server market.

**Enables Small Form Factor Designs**
- Northbridge integration reduces system chip count, power consumption and PCB size

ENERGY EFFICIENT DESIGN

**Enhanced LongRun™ Dynamic Power Management**
- Enables longer battery life by dynamically adjusting operating frequency and voltage to match the performance requirements of application workloads
- Provides higher performance within smaller, thermally constrained environments

**Enhanced LongRun Thermal Management**
- Maximizes performance within a thermal envelope
- Low thermal characteristics enable fanless designs for quieter and more reliable systems

HIGH PERFORMANCE

**8 Instruction Issue, 256-Bit VLIW Engine**
- Fully Pentium 4-ISA compatible
- Up to eight instructions issued per clock cycle
- Up to 50% improvement in integer applications
- SSE and SSE2 multimedia extensions enables multimedia applications to run up to 80% faster per clock cycle than previous generation processors from Transmeta
- 512KB L2 cache improves processor performance

**Advanced Code Morphing Software**
- Improves performance and responsiveness over 1st generation Transmeta Crusoe technology
- Unique software based architecture is key to reducing power consumption and enabling future scalability and flexibility
- New generation Code Morphing Software technology leverages 256-bit VLIW hardware advances
- Enables quick, low cost improvements to performance and power
Transmeta Efficeon Processor Core
At the heart of the Transmeta Efficeon processor is a state-of-the-art VLIW (Very Long Instruction Word) hardware engine that uses a custom, efficient VLIW instruction set. Running on the processor is Transmeta’s proprietary Code Morphing Software (CMS), the Efficeon software component that dynamically optimizes and translates x86 instructions into VLIW native code. This unique combination of hardware and software allows the processor to be more efficient, and also adds intelligence to Efficeon not found in other x86 microprocessors to manage power consumption and heat.

Transmeta Enhanced LongRun Power Management
Unlike conventional x86 processors, Transmeta’s proprietary Enhanced LongRun power management technology is part of the Efficeon processor’s Code Morphing Software. This combination allows the Efficeon processor to seamlessly adjust its operating frequency and voltage up to hundreds of times per second — dramatically extending battery life, limiting heat dissipation yet providing rapid system responsiveness.

Transmeta Efficeon Processor

- On-die L1 Instruction Cache: 128KB
- On-die L1 Data Cache: 64KB
- On-die L2 Write-Back Cache: 512KB
- HyperTransport System Bus Speed: 800 MegaTransfers/s
- Aggregate HyperTransport Link Bandwidth: 1.6 GB/s
- MMX, SSE, SSE2 Instruction Support: Yes
- Fully Integrated Northbridge Functionality: Yes
- Integrated AGP 1X, 2X, and 4X graphics interface: Yes
- Support for DDR-266, 333, 400 memory: Yes
- Support for ECC memory: Yes
- Integrated Low Pin Count Bus (LPC): Yes
- Full x86 Software and OS Compatibility: Yes
- Enhanced LongRun Thermal Management: Yes
- Enhanced LongRun Power Management: Yes
- Package Size: 29mm x 29mm

For more information, visit www.transmeta.com