LongRun™ Power Management

Dynamic Power Management for Crusoe™ Processors

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Crusoe Processor Overview

In January of 2000, Transmeta Corporation introduced the Crusoe processor family, a series of x86-compatible solutions that combine strong performance with remarkably low power consumption. As might be expected, a new technology for designing and implementing microprocessors underlies the development of these processors. As might not be expected, the new technology is fundamentally *software*-based: the power savings come from replacing large numbers of transistors with software.

Crusoe processors consist of a hardware compute engine logically surrounded by a software layer. The engine is a very long instruction word (VLIW) processor core capable of executing up to four operations in each clock cycle. The VLIW processor's native instruction set bears no resemblance to the x86 instruction set; it has been designed purely for fast low-power operation using conventional CMOS fabrication. The surrounding software layer gives x86 programs the impression they are running on x86-compatible hardware. This software layer is called Code Morphing™ software because it dynamically "morphs" (transforms) x86 instructions into VLIW instructions. The Code Morphing software includes a number of advanced features to achieve excellent system-level performance. The underlying VLIW processor also includes support facilities that are specially designed to meet the needs of the Code Morphing software. In other words, Transmeta designers have judiciously rendered some functions in hardware and some in software, according to the product design goals and market requirements.

Power Management Basics

The principal goal of power management for mobile consumer devices is to prolong battery life. Other issues come into play that give users a better experience, like the avoidance of a built-in fan, weight reduction and cost reduction. In today's mobile market the primary requirement for a viable product solution is long battery life to meet the expectation of extended mobile operation.

Conventional Power Management

In a mobile setting, most conventional x86-compatible processors regulate their power consumption by rapidly alternating between running the processor at full speed and (in effect) turning the processor off. Different performance levels can be obtained by varying the on/off ratio (the "duty cycle") of the processor. The mobile x86 power management model defines one "on" state ("Normal" = 100% activity level) and multiple "off" states. Table 1describes these different power management states.

Table 1: Conventional Power Management States

State Name	ACPI [1] State Name	State Description
Normal	C0	In the Normal state, the processor is actively executing instructions.
AutoHALT	C1	The processor enters the AutoHALT state by executing the HLT instruction. In the AutoHALT state the processor stops its internal clocks in response to the HLT instruction.
Quick Start	C2	In the Quick Start state: • The processor stops its internal clocks in response to a STPCLK signal from the southbridge. • The processor maintains cache coherence (the processor caches continue to snoop system memory transactions).
Deep Sleep	C3	In the Deep Sleep state: • The southbridge stops the external clock input to the processor. • The system enforces cache coherency (the processor caches don't need to snoop system memory transactions). Deep Sleep realizes the maximum processor power savings without losing the processor context (internal state).

1. ACPI stands for *Advanced Configuration and Power Interface* and is a joint standard of Microsoft, Intel and Toshiba.

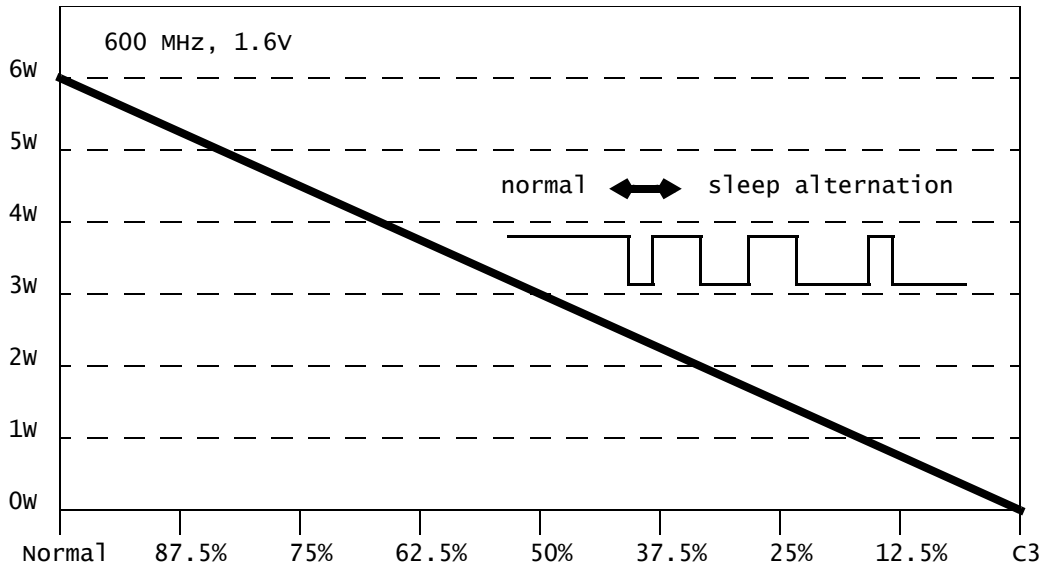
By continuously alternating between a normal operating state and one of these low-power states, the power consumption of conventional mobile x86-compatible processors responds proportionally to the actual performance level.

Linear Power Savings

Figure 1 illustrates the linear relationship between power consumption and apparent performance. By increasing the amount of time the processor spends in low power states, the processor has both lower power consumption and lower performance.

Also, with this approach, conventional processors deliver performance in discrete bursts, which tends to be unfavorable for smooth multimedia content, such as software-based DVD or MP3 playback. This may create artifacts, such as dropped frames during movie playback, that are perceptible to a user.

Figure 1: Linear Power Savings of Conventional Power Management Solutions (Power vs. Activity Level)



Crusoe processors are compatible with the conventional x86 power management model. However, there are more power savings to be gained through Crusoe processor-specific techniques that exploit new opportunities for power savings to extend battery life. The following sections give some background for the LongRun power management strategy by describing an equation that summarizes the major contributing components of active power consumption.

The Power Equation

In the active state, well over 90% of the total power dissipation for CMOS microprocessors can be approximated with the following equation:

$$\text{Power} = (\text{Capacitance} \times \text{Frequency} \times \text{Voltage}^2) / 2$$

Reducing any of the terms in this equation will lower the overall processor power consumption and extend battery life. The Crusoe processor architecture has taken some original approaches to make this happen.

Capacitance Reduction

Microprocessors are really large collections of logic transistors that are laid out in groups that perform specific functions. Each logic transistor adds to the total effective capacitance of the microprocessor. Of course, removing logic transistors reduces the microprocessor's effective capacitance. Therefore, to save power, the question is how to reduce the transistor count while retaining the complete functionality and performance of an x86-compatible processor. The answer lies in software.

Crusoe processor Code Morphing technology uses software to perform many functions that a conventional microprocessor performs with dedicated logic transistors. This allows a Crusoe processor to use a smaller number of logic transistors and thus gain a power efficiency advantage through lower effective capacitance.

An example of this software-based approach is instruction scheduling. In a conventional superscalar architecture, a special module manages the scheduling of the execution of a given block of instructions. Because the Crusoe processor performs its instruction scheduling in software, there is no need for a dedicated block of logic transistors to perform instruction scheduling. The resulting power savings translates into longer battery life for the user.

Frequency and Voltage Scaling

The 'dirty little secret' in the microprocessor world is that as an architecture evolves over time through a series of specific processors, most performance gains come from increasing the clock frequency and corresponding voltage levels. For desktop and server systems, this approach is usually acceptable. In a mobile device where every hour of battery life matters, however, it's a non-affordable luxury.

Only rarely does an application need a processor's maximum performance. The rest of the time, this unused extra performance represents wasted power. In the power equation above, the frequency and voltage terms represent potential areas of savings if the processor can match its active operating level to the performance requirements of the application.

To achieve this goal, the Crusoe processor architecture introduced an original approach to power management that dynamically manages the frequency and voltage (performance and power) levels at runtime to meet the needs of a given application.

LongRun Dynamic Power Management

LongRun power management technology is based on a combination of hardware capabilities in the Crusoe processor VLIW core that are controlled by a software module inside the Code Morphing software.

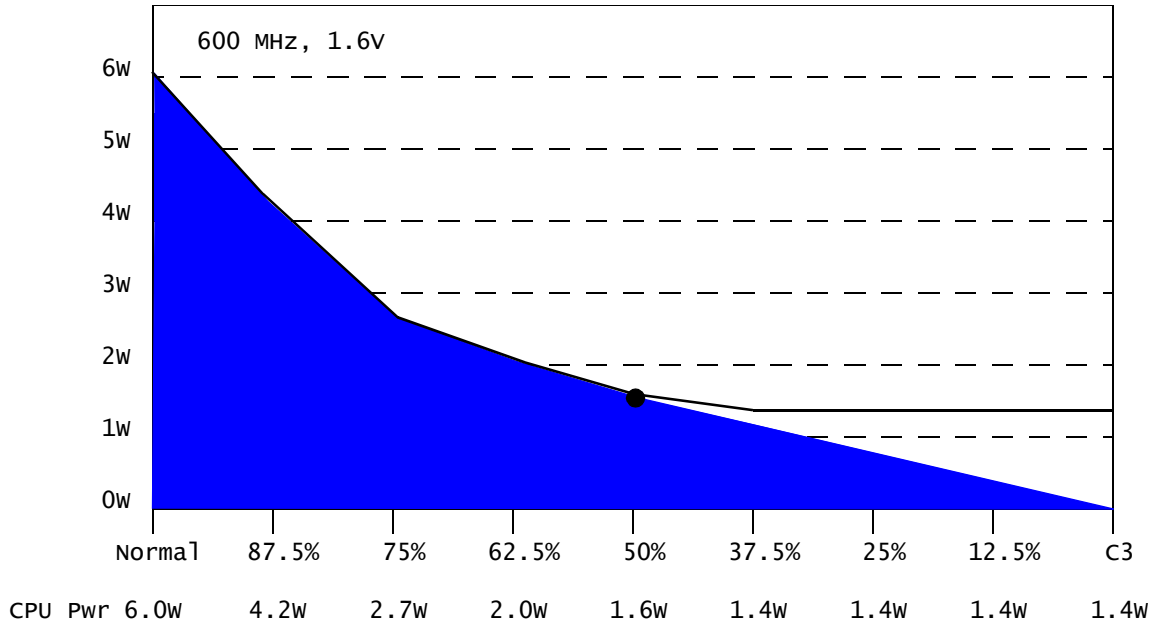
At a hardware level, the Crusoe processor VLIW engine can configure itself with the following adjustments:

- Frequency changes in steps of 33 MHz (within the hardware's operating range).
- Voltage changes in steps of 25 mV (depending on the voltage regulator), since at a lower operating frequency less voltage is needed.
- Up to 200 frequency/voltage changes per second.

These capabilities give LongRun power management a fine grained spectrum of voltage and frequency points to use for dynamic performance and power tuning. Because power varies linearly with clock frequency and by the square of the voltage, adjusting both can produce *cubic* (to the third power) reductions in power consumption, whereas conventional processors can scale power only linearly.

Figure 2 illustrates the LongRun power management effect of scaling both frequency and voltage on power consumption.

Figure 2: LongRun Power Profile (Power Consumption vs. Activity Level)



The curve in Figure 2 represents the cubic effects of LongRun power management. Eventually the frequency and voltage scaling ranges hit the limits of physics and the curve flattens out. In particular, with the current generation of Crusoe processors, the frequency/voltage floor is 300 MHz and 1.2 V. At this point, it is more efficient to switch over to traditional power management, i.e. alternating between Normal and Sleep states according to the actual performance demands of the system. This effect is made visible in Figure 2 by drawing a line that begins at the point where the power curve begins to flatten and ends at C3. This linear effect drives down the power consumption further, until it hits the minimum sleep power consumption (in this example: Deep Sleep). The result is the Crusoe processor power profile, shown in Figure 2.

The curve in Figure 2 tells only part of the story. It is the responsibility of the LongRun power management software to monitor the runtime performance needs of application software and to match those needs with the appropriate power/performance point on this curve. The LongRun power management algorithms tracks when it is advantageous to dynamically shift frequency/voltage levels and when it is best to use conventional power management techniques. LongRun power management takes full advantage of its integration with other runtime components of the Code Morphing software to maximize power savings and extend battery life.

To accomplish this, the LongRun power management code continuously monitors the application's performance needs and determines just how much processor performance is needed, and then dynamically adjusts its voltage and frequency (MHz) of operation. For example, assume an application program only requires 90% of the processor's speed. On a conventional processor, throttling back the processor by 10% cuts power by 10%, whereas under the same conditions, LongRun power management can reduce power by almost 30%—a noticeable advantage! The user will not perceive the change because the application behaves normally. As the performance needs of the application change,

the LongRun power management code will revise its power budget and select an appropriate frequency/ voltage combination.

Table 2 shows some estimates of LongRun power management benefits.

Table 2: LongRun Power Management vs. Conventional Power Management Benefits

Conventional Power Management			LongRun Power Management					
Perf Level	Clock Equiv	Power	Core			DDR (2.5 V I/O)		Total Power
			Clock	Voltage	Power	Clock	Power	
Normal	667 MHz	5.5 W	667 MHz	1.6 V	5.3 W	133 MHz	0.2 W	5.5 W
87.5	584	4.8	600	1.5	4.2	120	0.2	4.4
75.0	500	4.1	533	1.35	3.0	133	0.2	3.2
62.5	417	3.4	400	1.225	1.9	100	0.2	2.1
50.0	333	2.8	300	1.2	1.3	100	0.2	1.5
37.5	250	2.1						
25.0	167	1.4						

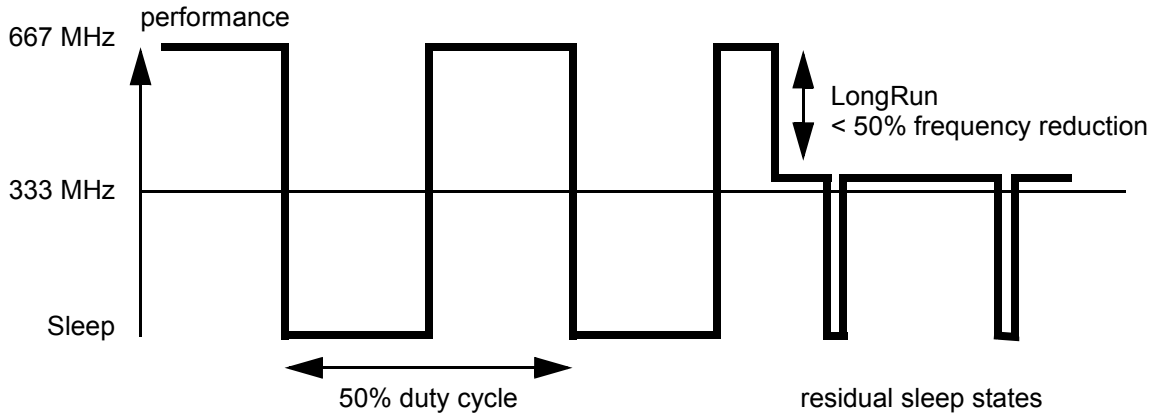
LongRun Power Management Policies

LongRun power management technology is an innovative power management solution. It's policies are implemented in processor-internal Code Morphing software, and it's mechanisms are implemented in both hardware and software. LongRun power management continuously scales both the frequency and voltage of the processor according to the instantaneous performance demands of the computer system. It determines the instantaneous performance demands by sampling the idle time of the system, which is represented by the time that the processor spends in the various sleep states. It can detect different operating scenarios based on runtime performance information and then exploit these by adapting its power usage accordingly.

The optional interfaces described in Table 3 and Table 5 provide methods for operating system and application-level software to interact with LongRun power management. LongRun power management does not require the BIOS, the operating system, device drivers or existing applications to use these interfaces. This independence promotes both portability and compatibility of x86 software. How can LongRun power management obtain a holistic perspective of the system's runtime performance requirements without requiring any software changes? The answer is that LongRun power management monitors the instantaneous system activity by sampling the traditional power management states. Monitoring these sleep states takes advantage of operating system knowledge.

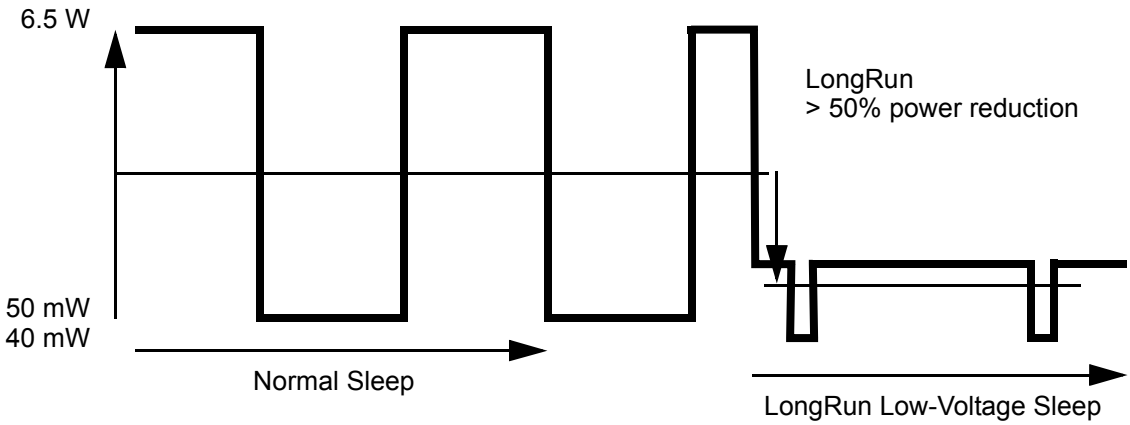
In particular, the LongRun power management policy heuristics track an equilibrium that absorbs the traditional sleep states. That is, LongRun power management always drives the processor frequency down to the point where the traditional sleep states almost disappear. For instance, when the processor spends 50% of its overall time in sleep states, LongRun power management can reduce the core frequency by almost 50% and still maintain the same effective performance level. Figure 3 illustrates this frequency reduction heuristic.

Figure 3: Frequency Reduction Heuristic



After the LongRun transition, the processor spends significantly less time in sleep states, and the effective performance remains the same. Figure 4 illustrates the corresponding power reduction:

Figure 4: Power Reduction



LongRun power management also enables low-power sleep states through voltage scaling. The reduced operating voltage used while the Crusoe processor is running at a reduced performance level results in reduced leakage current. Leakage current is the most significant contributor to power consumption while the processor is in the Deep Sleep state. Therefore, reducing the processor voltage also has significant power reduction effects in the sleep states.

If the processor spends most of its time idling, LongRun power management will have scaled down both the frequency and voltage. Hence, the more time the system spends in sleep, the more likely it is that it will spend it in a low-voltage sleep state. Probabilisticly, most sleep states on notebook computers will occur as low voltage sleep states.

LongRun Power Management Software Interface

The Crusoe processor LongRun power management interface supports both feature discovery, state queries and modification of the LongRun power management policy. Table 3 provides an overview of the LongRun power management interface in Code Morphing software version 4.1:

Table 3: LongRun Power Management Software Interface

Processor Identification Information	Register	Description
CPUID 8086 0001h	EDX:0	LongRun power management supported
	ECX	Nominal core frequency
CPUID 8086 0007h	EAX	Current core frequency
	EBX	Current core voltage
	ECX	Current performance percentage
MSR 8086 8010h	EDX	Upper boundary (% within min/max range, where 100 is max, 0 is min)
	EAX	Lower boundary (% within min/max range, where 100 is max, 0 is min)
MSR 8086 8011h	EAX:0	Economy/Performance mode

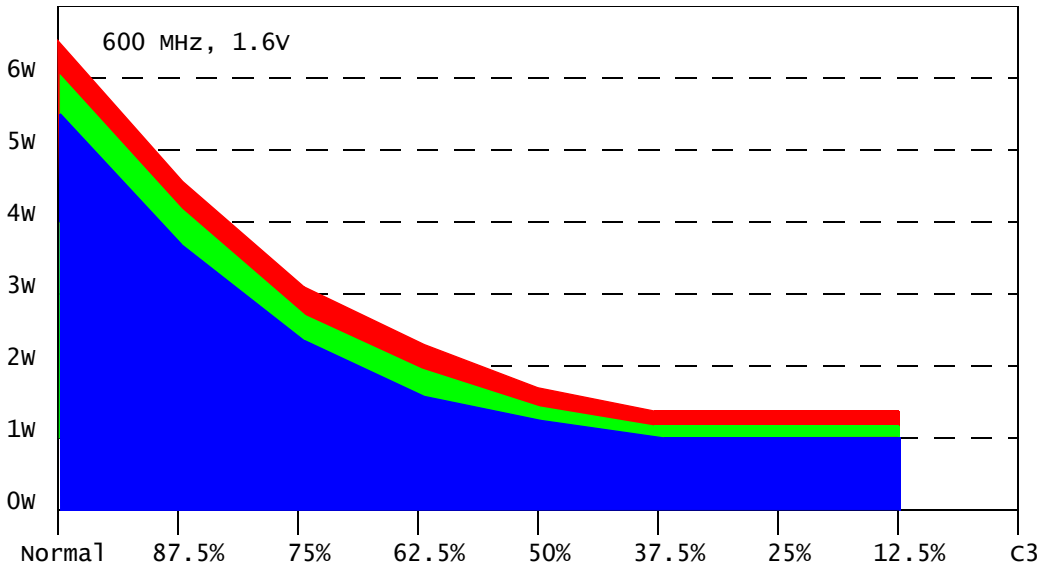
Crusoe Processor 'Virtual' Northbridge

A unique feature of the Crusoe processor is that it integrates the northbridge components of the chipset with the processor core on the same die. This includes the controller logic for the PCI bus and memory interfaces for both single data rate (SDR) and double data rate (DDR) SDRAM.

The memory interfaces themselves operate at a fixed voltage that matches the voltage of the installed memories. For DDR memory, it is 2.5 V and for SDR memory, it is 3.3V. However, the memory interfaces only allow frequency scaling within the range that the installed memories support. In the case of SDR memory, there is virtually no frequency floor, and the memory type (PC-100 and PC-133 memory) determines the frequency ceiling. DDR memory, in contrast, has its own DRAM phased lock loop (DLL), which determines its operating frequency range. The typical DDR frequency range is from 80 MHz up to the usual nominal memory frequencies, with a current maximum of 156 MHz.

In the final analysis, the linear power reduction of the memory interface is dominated by the cubic power reduction of the processor core and northbridge logic, since these also allow voltage scaling. Figure 5 graphically displays the dominance of the processor core cubic power savings of LongRun power management, and includes the power consumption of the integrated Crusoe processor northbridge and system memory.

Figure 5: Core + Northbridge Power Savings (Power Consumption vs. Activity Level)



SDR	0.5W	0.4W	0.4W	0.3W	0.2W	0.2W	0.2W	0.2W
DDR	0.5W	0.4W	0.4W	0.3W	0.3W	0.3W	0.3W	0.2W
Core+NB	5.5W	3.8W	2.3W	1.7W	1.3W	1.0W	1.0W	1.0W

A Paradox Explained

Another interesting observation is that the average power consumption of Crusoe processors actually tends to decrease with increasing maximum performance capability (e.g. larger cache size). This paradox can be explained as follows: at a given frequency/voltage setting, the TM5600 processor is faster than the TM5400, because of the larger L2 cache. Consequently, the TM5600 can deliver the same performance as the TM5400 at a lower frequency/voltage level. As a result, the TM5600 consumes less power on the average than the TM5400 (with the same workload).

In contrast, the power consumption of conventional processors will stay constant, at best, with increasing top speeds. An example: 50% $\times$ 10W = 5W; doubling the performance by frequency scaling yields only: 25% $\times$ 20W = 5W.

However, only scaling the frequency is not necessarily sufficient, because the voltage may need to be scaled correspondingly. The average power consumption of conventional processors thus tends to increase by improving maximum performance capability for a given core and process technology.

This is where LongRun power management technology really changes the rules. By running given workloads at a lower relative speed, the cubic power reduction effect of LongRun power management will allow faster processors to consume less average power. This result assumes identical core designs and process technologies, and even increased voltages at higher nominal speeds, which are rarely used in typical notebook workloads.

Thermal Design

An important part of the design of microprocessor-based consumer devices like notebooks and mobile Internet access products is the planning and management of how the device will generate and dispose of heat. As heat collects in a device, its operating temperature increases, and this can damage the device or affect its performance. System designers are careful to incorporate thermal solutions in their designs that allow their products to operate within a safe temperature range.

Conventional Thermal Throttling

Conventional thermal control solutions are often designed around a temperature measurement device and a clock throttling circuit. When the temperature goes into a range that is too high, the clock throttling circuit intervenes to reduce the amount of heat being generated. It does this by reducing the effective performance (and hence the power dissipation) of the chip by periodically shifting it from an active state to a sleep state, which gives the processor time for the heat to dissipate.

While this approach achieves the goal of maintaining a safe operating temperature, it does not make the most efficient use of power. The question is how to maximize battery life while maintaining a safe operating temperature. Again, the answer lies in software.

LongRun Power Management Thermal Extension

LongRun power management has both more control over processor performance and greater intelligence for handling different power management scenarios. Simply put, by integrating power management with thermal control, LongRun power management can optimize for both. By including a thermal model in the LongRun power management logic, Crusoe processors provide designers with a significantly reduced thermal footprint.

The Crusoe processor leverages LongRun power management technology as a substitute for thermal throttling with a system called LongRun power management thermal extension (LTX).

Because of the characteristic cubic LongRun power management advantage, LTX, in comparison to thermal throttling, delivers higher performance at the same die temperature, or the same performance at a lower die temperature. In other words, LTX allows expanding the thermal budget of the processor. As a result, LTX is a solution to optimally manage processor performance in thermally constrained environments.

Some Scenarios

There are two strategies of thermal design for most Crusoe processor-based systems:

- Increasing the thermal budget within a given thermal envelope, thus achieving higher performance.
- For an equivalent level of performance, reducing the thermal budget.

In practice, the issue of avoiding an active cooling solution (fan) is important. Fans increase power consumption, noise and cost. As conventional processor performance (and power) goes up, fans play a more prominent role in thermal control. Because they are electromechanical devices, fans can compromise the reliability of mobile system designs. Table 4 shows the performance improvement of LongRun power management thermal control (LTX) over conventional clock throttling thermal control.

Table 4: Performance Benefits of LongRun Power Management Thermal Control

Power Level	Conventional Performance	LongRun Performance	LongRun Performance Improvement
Normal = 100%	100%	100%	0%
75%	75%	91%	16%
50%	50%	80%	30%
25%	25%	63%	38%

For aggressive OEMs, pseudo-thermal throttling is acceptable to replace an active cooling solution like a fan because their thermal designs are based on the TDP_{TYP} of the processor. In fact, some aggressive OEMs use continuous thermal throttling by default! In these cases, LTX can reduce system weight and cost by eliminating the need for an active cooling solution, and provide substantially higher performance within the same thermal envelope.

Conservative OEMs, however, may not find this solution to replace a fan acceptable, because they prefer designing their thermal solutions to the TDP_{MAX} of the processor, as an additional safety measure. Though LTX doesn't completely remove the need for an active cooling solution in this scenario, it still delivers superior performance for a given thermal envelope.

LTX Northbridge Interface

LTX replicates the clock throttling register from the chipset southbridge, where it is usually located, into the integrated Crusoe processor northbridge. In general, the clock throttling register is only used for thermal throttling.

The BIOS must simply program the same values into the northbridge register that it normally would program into the corresponding southbridge register. To accomplish that, the BIOS ACPI active cooling handlers (`_AC[0:9]`) must be changed to use LongRun power management pseudo-throttling prior to passive thermal throttling. As a result, LTX and thermal throttling are complementary. Because of the way the LongRun power management heuristics work, thermal throttling pins the Crusoe processor to its lowest LongRun power management frequency so that LTX precedes thermal throttling.

In addition, while clock throttling requires the overhead of continuous STPCLK/Stop Grant handshaking between the southbridge and the processor via the PCI bus, LTX completely eliminates this additional, power consuming bus traffic, and allows the CLKRUN protocol to realize additional power savings.

The LTX northbridge interface supports both feature discovery and state queries. Table 5 provides an overview of the LTX northbridge interface in Code Morphing software version 4.1:

Table 5: LTX Northbridge Interface

Function 0, Register A8h		
Bit 4	Thermal management enabled	
Bits 1:3	Power reduction level:	
	Bits	**Mode**
	000	Reserved
	001	Reserved
	010	75.0%
	011	62.5%
	100	50.0%
	101	37.5%
	110	25.0%
	111	12.5%
Bit 0	LongRun power management supported	

Comparative Analysis

LongRun Power Management vs. Intel SpeedStep

LongRun power management operates dynamically and continuously, whether the system is running off AC line power or off battery power, to minimize power consumption and provide optimal processor performance. This is dramatically different than the static operation characteristic of Intel's SpeedStep technology, which only selects between two specific operating modes - high power AC line operation and slightly lower power battery operation. SpeedStep does not adjust operating performance or power based on application software needs.

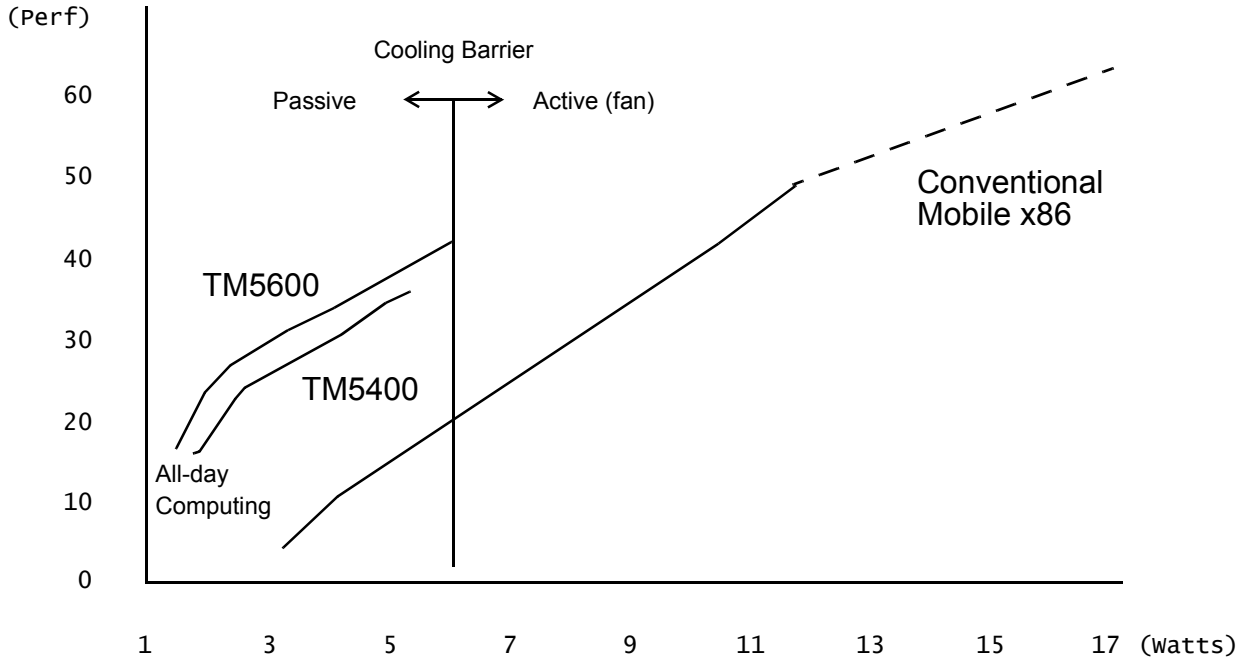
One aspect of Intel's SpeedStep technology is, in principle, similar to LongRun power management, although the benefits and implementations are very different. SpeedStep statically lowers its voltage/ frequency settings through a hardware-based approach with just two operating points. The lower granularity of this technique causes SpeedStep to miss opportunities for power savings that LongRun power management can exploit.

LongRun power management has two categories of advantages over SpeedStep: hardware and software. The Crusoe processor VLIW core has a finer granularity for controlling frequency shifts, voltage shifts and the rapid timing for these shifts. The LongRun power management software uses sophisticated algorithms for optimizing both performance, power and thermal control to extend battery life and remove the need for active cooling solutions.

Power Comparison

Figure 6 compares a conventional mobile x86 processor and the Crusoe processor family in power-constrained and thermally constrained environments.

Figure 6: Power Management Comparison (Performance vs. Power Consumption)



This diagram illustrates the following key points:

- The maximum performance of a conventional mobile x86-compatible processor is currently higher.
- Power consumption for the conventional mobile x86-compatible processor is significantly higher (compare 17W versus 6W for the TM5600).

In typical notebook computer environments, peak performance is rarely needed, and, when it is needed, it will typically only be used for short bursts. However, the thermal solutions are either dimensioned to absorb the maximum heat dissipation associated with peak performance levels, or the processor performance must be artificially constrained by thermal or clock throttling.

With that in mind, compare the actual/effective performance of the Crusoe processor family at 6W, which is about the maximum power dissipation that passive thermal solutions can absorb. In such constrained environments, which are typical for smaller notebook computers, Crusoe processors deliver significantly greater effective performance than conventional x86-compatible mobile solutions.

One of the results of this power comparison is that Crusoe processors deliver software-based DVD playback at the same power consumption that conventional x86-compatible processors uses in the Deep Sleep (C3) state (i.e., with its external bus clocks stopped and no work being done).

Table 6 summarizes the power consumption differences of conventional mobile x86-compatible processors vs. the Crusoe processor model TM5600:

Table 6: Power Consumption Differences

	Conventional Mobile x86 Solution			**Crusoe Processor Model TM5600 with Integrated Northbridge**
	Processor 600/500 MHz 1.35 / 1.1 V	Northbridge 3.3 V	Total 600/500 MHz 1.35 / 1.1 V	LongRun 600 ↔ 300 MHz 1.6 ↔ 1.2V
Normal (C0)	9.4 / 5.3 W	2.0 W	11.4 / 7.3 W	6.8 ↔ 0.7 W
AutoHalt (C1)	2.3 / 1.7 W	2.0 W	4.3 / 3.7 W	0.9 ↔ 0.3 W
Quick Start (C2)	2.0 / 1.4 W	2.0 W	4.0 / 3.4 W	0.6 ↔ 0.2 W
Deep Sleep (C3)	1.6 / 1.2 W	~1.0 W	2.6 / 2.2 W	0.2 ↔ 0.1 W

Future Directions

Different goals and market requirements for future products may result in different hardware-software partitioning than current Crusoe processors. Transmeta's Code Morphing technology changes the entire approach to designing microprocessors. By demonstrating that practical microprocessors can be implemented as hardware-software hybrids, Transmeta has expanded the design space that microprocessor designers can explore for optimal solutions. Microprocessor development teams may now enlist software experts and expertise, working largely in parallel with hardware engineers, to bring products to market faster. Upgrades to the software portion of a microprocessor can be rolled out independently from the processor hardware. Finally, decoupling the hardware design from the system and application software that use it frees hardware designers to evolve and eventually replace their designs without perturbing legacy software.

All Day Computing

Looking further ahead into the future of mobile computing, the user experience can be further enhanced by all-day computing. All-day computing, however, severely constrains the processors power envelope.

As an example: current battery capacities range from 17WH for ultra-lights to 70WH on 8-10 lb. full-featured notebooks. An average battery capacity of 40WH, stretched out over 8 hours, translates into a maximum system power consumption of 5W. The processor can obviously only consume a fraction of that. Hence an all-day computing power envelope of 1-2W for the processor is generous.

Whereas the Crusoe processor still delivers about 50% of its maximum performance in such extremely power constrained environments, traditional clock-throttling completely chokes the performance of conventional mobile x86-compatible processors. As a result, the Crusoe processor's effective performance profile makes it a superior choice for ultra-portable computer designs.

Summary

In 1995, Transmeta set out to expand the reach of microprocessors into new markets by dramatically changing the way microprocessors are designed. The initial market for Crusoe processors is mobile computing, in which complex power-hungry processors have forced users to give up either battery operating time or performance. Crusoe processor solutions have been designed for lightweight (two to four pound) mobile computers and Internet access products, such as handheld devices and web pads.

To design the Crusoe processor chips, Transmeta engineers did not resort to exotic fabrication processes. Instead, they rethought the fundamentals of microprocessor design. Rather than 'throwing hardware' at design challenges, they chose an innovative approach that employs a unique combination of hardware and software.

With regard to extending battery life, the innovative Crusoe processor approach provides the following benefits:

- Power consumption is between a factor of four (in AutoHALT) and a factor of thirty (in Deep Sleep) lower than the power consumption of conventional x86-compatible processors.
- In normal running mode, LongRun power management allows additional power savings between a factor of two to ten.
- Internet access devices can have PC capabilities and unplugged running times of up to a full day.

Transmeta's Code Morphing software and fast VLIW hardware, working together, achieve low power consumption without sacrificing high performance for real-world applications. Although the current Crusoe processor models are impressive first efforts, the significance of the Transmeta approach to microprocessor design is likely to become more apparent over the next several years. The technology is new and offers more freedom to innovate, in both hardware and software, than conventional hardware-only designs.