PowerPC 740 and PowerPC 750 Microprocessor Datasheet

CMOS 0.20 μm Copper Technology, PID-8p, PPC740L and PPC750L, dd3.2

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IBM Microelectronics Division

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Preface

The PowerPC 740™ and PowerPC 750™ are members of the PowerPC® family of reduced instruction set computer (RISC) microprocessors. The PPC740L and PPC750L microprocessors are the PID-8p implementations of the PowerPC 740 and PowerPC 750 in IBM CMOS 7S 0.20 µm copper technology. They are referred to in the body of this document as “740“ and “750.”

Information in this document does not apply to implementations of the PowerPC 740 and PowerPC 750 in other technologies, such as the PID-8t.

The information in this document is also specific to revision level dd3.2 of the (PID-8p) PPC740L and PPC750L, and does not apply to previous revisions.

This document is generally written in terms of the 750. Unless otherwise noted, information that applies to the 750 also applies to the 740. Exceptions are detailed.

The 740 uses the same die as the 750, but the 740 does not bring the L2 cache interface out to external package pins.

New Features for dd3.x

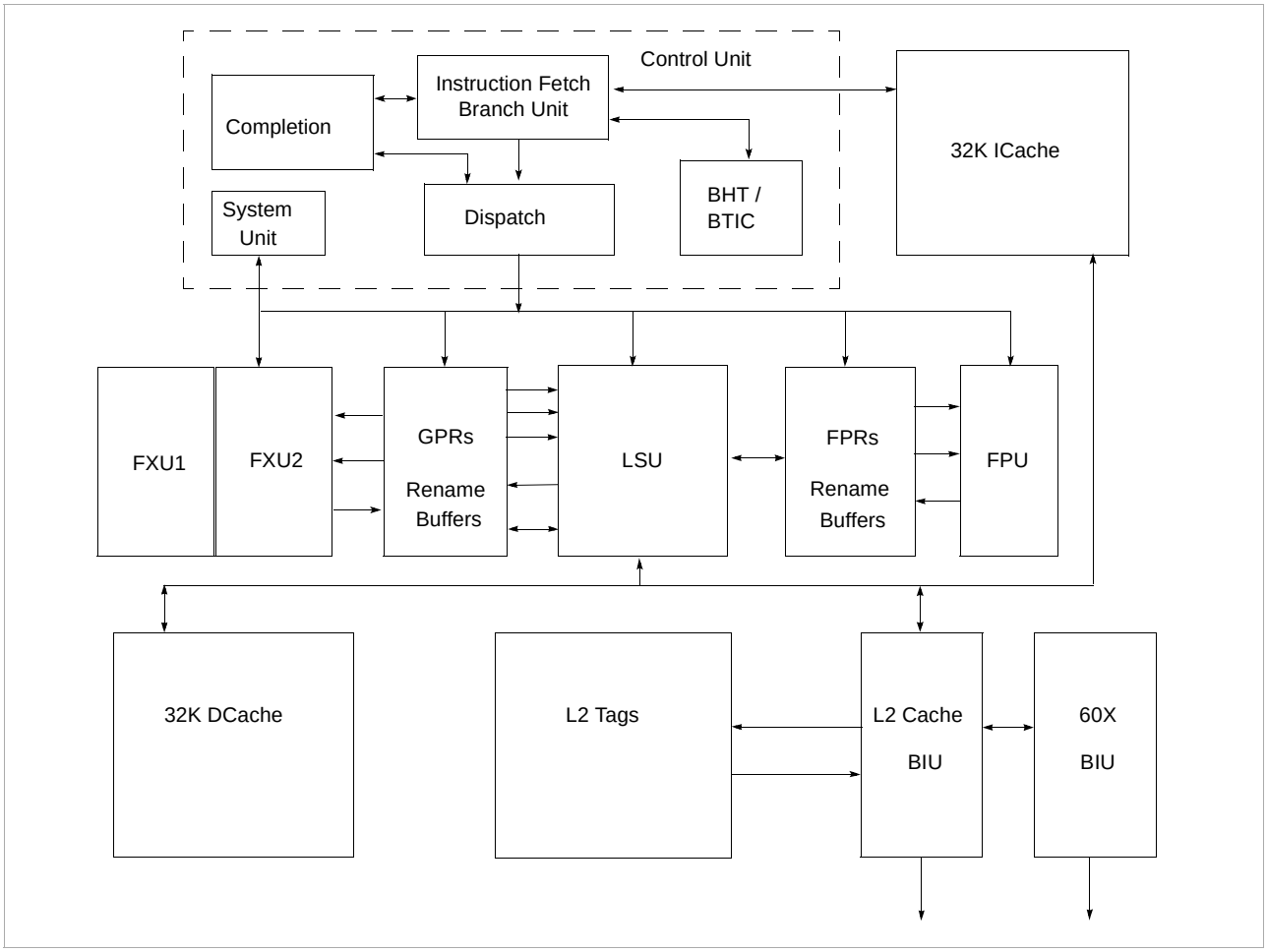
- Selectable I/O voltages on 60X bus and L2 bus. See ”Recommended Operating Conditions,” on page 11. Older revs must leave these pins “no connect” or “tied high” for 3.3v I/Os. AC timings are the same for all I/O voltages modes unless otherwise noted.
- 60X bus:core frequency ratios now also support the 10x ratio. See ”PLL Configuration,” on page 40.
- Extra output hold on the 60x bus by L2_TSTCLK pin tied low is no longer available. The L2_TSTCLK pin must now be tied to OV_{DD} for normal operation. See ”60X Bus Output AC Timing Specifications for the 750[1],” on page 18.

Overview

The 750 is targeted for high performance, low power systems and supports the following power management features: doze, nap, sleep, and dynamic power management. The 750 consists of a processor core and an internal L2 Tag combined with a dedicated L2 cache interface and a 60x bus. The L2 cache is not available with the 740.

Figure 1 shows a block diagram of the 750.

Figure 1. 750 Block Diagram



Features

This section summarizes features of the implementation of the PowerPC 750 architecture. For details, see the *PowerPC 740 and PowerPC750 User's Manual*.

- Branch processing unit
  - Four instructions fetched per clock.
  - One branch processed per cycle (plus resolving 2 speculations).
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch.
  - 512-entry branch history table (BHT) for dynamic prediction.
  - 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots.
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units).
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point).
  - Serialization control (predispatch, postdispatch, execution, serialization).
- Decode
  - Register file access.
  - Forwarding control.
  - Partial instruction decode.
- Load/store unit
  - One cycle load or store cache access (byte, half word, word, double word).
  - Effective address generation.
  - Hits under misses (one outstanding miss).
  - Single-cycle misaligned access within double word boundary.
  - Alignment, zero padding, sign extend for integer register file.
  - Floating-point internal format conversion (alignment, normalization).
  - Sequencing for load/store multiples and string operations.
  - Store gathering.
  - Cache and TLB instructions.
  - Big and little-endian byte addressing supported.
  - Misaligned little-endian support in hardware.
- Fixed-point units
  - Fixed-point unit 1 (FXU1); multiply, divide, shift, rotate, arithmetic, logical.
  - Fixed-point unit 2 (FXU2); shift, rotate, arithmetic, logical.
  - Single-cycle arithmetic, shift, rotate, logical.
  - Multiply and divide support (multi-cycle).
  - Early out multiply.
- Floating-point unit
  - Support for IEEE-754 standard single- and double-precision floating-point arithmetic.

- 3 cycle latency, 1 cycle throughput, single-precision multiply-add.
- 3 cycle latency, 1 cycle throughput, double-precision add.
- 4 cycle latency, 2 cycle throughput, double-precision multiply-add.
- Hardware support for divide.
- Hardware support for denormalized numbers.
- Time deterministic non-IEEE mode.

- System unit
  - Executes CR logical instructions and miscellaneous system instructions.
  - Special register transfer instructions.

- Cache structure
  - 32K, 32-byte line, 8-way set associative instruction cache.
  - 32K, 32-byte line, 8-way set associative data cache.
  - Single-cycle cache access.
  - Pseudo-LRU replacement.
  - Copy-back or write-through data cache (on a page per page basis).
  - Supports all PowerPC memory coherency modes.
  - Non-blocking instruction and data cache (one outstanding miss under hits).
  - No snooping of instruction cache.

- Memory management unit
  - 128 entry, 2-way set associative instruction TLB.
  - 128 entry, 2-way set associative data TLB.
  - Hardware reload for TLB's.
  - 4 instruction BAT's and 4 data BATs.
  - Virtual memory support for up to 4 exabytes (2^{52}) virtual memory.
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory.

- Level 2 (L2) cache interface (Not available on the 740)
  - Internal L2 cache controller and 4K-entry tags; external data SRAMs.
  - 256K, 512K, and 1 Mbyte 2-way set associative L2 cache support.
  - Copy-back or write-through data cache (on a page basis, or for all L2).
  - 64-byte (256K/512K) and 128-byte (l-Mbyte) sectored line size.
  - Supports flow-through (reg-buf) synchronous burst SRAMs, pipelined (reg-reg) synchronous burst SRAMs, and pipelined (reg-reg) late-write synchronous burst SRAMs with optional parity checking.
  - Supports Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, and ÷3. The 750 supports the L2 frequency range specified in Section “L2 Clock AC Specifications,” on page 20. For higher L2 frequencies, please contact ppcsupp@us.ibm.com.

- Bus interface
  - Compatible with 60x processor interface.
  - 32-bit address bus with optional parity checking.
  - 64-bit data bus (can be operated in 32-bit data bus mode) with optional parity checking.
  - Bus-to-core frequency multipliers from 2x to 10x. See the ”PLL Configuration,” on page 40.

- Integrated power management
  - Low-power 2.0/3.3V design.
  - Three static power saving modes: doze, nap, and sleep.
  - Automatic dynamic power reduction when internal functional units are idle.
- Integrated Thermal Management Assist Unit
  - On-chip thermal sensor and control logic.
  - Thermal Management Interrupts for software regulation of junction temperature.
- Testability
  - JTAG interface.

General Parameters

The following list provides a summary of the general parameters of the 750.

Technology	0.20μm CMOS (general lithography), six-layer copper metallization
	$0.12 \pm 0.04\mu m$ L_{eff}
Die Size	5.14mm x 7.78mm ($40mm^2$)
Transistor count	6.35 million
Logic design	Fully-static
Package	740: Surface mount 21x21mm, 255-lead ceramic ball grid array (CBGA)
	750: Surface mount 25x25mm, 360-lead ceramic ball grid array (CBGA)
PPC 740/PPC 750 core power supply	2V Nominal (see Application Conditions)
I/O power supply	3.3V 2.5V, or 1.8V (Nominal Selectable)

Electrical and Thermal Characteristics

DC Electrical Characteristics

The 750 60x bus power supply can be either 3.3V, 2.5V, or 1.8V nominal; likewise, the L2 power supply can be either 3.3V, 2.5V, or 1.8V nominal. See the pinout listing for more information

Absolute Maximum Ratings See Notes

Characteristic	Symbol	Value	Unit
Core supply voltage	V_{DD}	- 0.3 to 2.2	V
PLL supply voltage	AV_{DD}	- 0.3 to 2.2	V
L2 DLL supply voltage	$L2AV_{DD}$	- 0.3 to 2.2	V
60x bus supply voltage	$OV_{DD(3.3V)}$	- 0.3 to 3.6	V
	$OV_{DD(2.5V)}$	- 0.3 to 2.8	
	$OV_{DD(1.8V)}$	- 0.3 to 2.1	
L2 bus supply voltage	$L2OV_{DD}$	- 0.3 to 3.6	V
Input voltage	$V_{IN(3.3V)}$	- 0.3 to 3.6	V
	$V_{IN(2.5V)}$	- 0.3 to 2.8	
	$V_{IN(1.8V)}$	- 0.3 to 2.1	
Storage temperature range	T_{STG}	- 55 to 150	°C

Note:

1. Functional and tested operating conditions are given in Table ”Recommended Operating Conditions,” below. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{IN} must not exceed OV_{DD} by more than 0.3V at any time, including during power-on reset. This is a DC specification only. V_{IN} overshoot transients up to OV_{DD}+1V, and undershoots down to GND-1V (both measured with the 740 in the circuit) are allowed for up to 5ns.
3. **Caution:** OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0V at any time during normal operation. On power up and power down, OV_{DD} is allowed to exceed V_{DD}/AV_{DD} by up to 3.3V for up to 20 ms, or by up to 2.5V for 40 ms. Excursions beyond 40 ms or 3.3V are not allowed.
4. **Caution:** V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 0.4V during normal operation. On power up and power down, V_{DD}/AV_{DD} is allowed to exceed OV_{DD} by up to1.0V for up to 20 ms, or by up to 0.7V for 40 ms. Excursions beyond 40 ms or 1.0V are not allowed.

Recommended Operating Conditions

Characteristic	Symbol	Value	Unit	Notes
Core supply voltage	V_{DD}	See Note 2	V	1, 2
PLL supply voltage	AV_{DD}	V_{DD}	V	1
L2DLL supply voltage	$L2AV_{DD}$	V_{DD}	V	1
60x bus supply voltage, pin W1 tied high	$OV_{DD(3.3V)}$	3.135 to 3.465	V	1
60x bus supply voltage pin W1 tied to $\overline{\text{HRESET}}$	$OV_{DD(2.5V)}$	2.375 to 2.625	V	1
60x bus supply voltage, pin W1 tied to GND	$OV_{DD(1.8V)}$	1.71 to 1.89	V	1
L2 bus supply voltage, pin A19 tied high	$L2OV_{DD(3.3V)}$	3.135 to 3.465	V	1
L2 bus supply voltage, pin A19 tied to $\overline{\text{HRESET}}$	$L2OV_{DD(2.5V)}$	2.375 to 2.625	V	1
L2 bus supply voltage, pin A19 tied to GND	$L2OV_{DD(1.8V)}$	1.71 to 1.89	V	1
Input voltage (Under AC conditions, inputs must go rail-to-rail for maximum AC timing performance.)	$V_{IN(60X)}$	GND to OV_{DD}	V	1
	$V_{IN(L2)}$	GND to $L2OV_{DD}$	V	1
Die-junction temperature	T_J	-40 to 105	°C	1, 2

Note:

1. These are recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. V_{DD} and T_J are specified by the Application Conditions designator in the part number. See the Part Number Key on page 51 for more information.

Package Thermal Characteristics[1]

Characteristic	Symbol	740	750	Unit
Thermal resistance, junction-to-case (top surface of die) typical	θ_{JC}	0.03	0.03	°C/W
Thermal resistance, junction-to-balls, typical	θ_{JB}	3.8 - 7.1[2]	3.8 - 7.6[2]	°C/W
Thermal resistance, junction-to-ambient, at air-flow, no heat sink, typical	50 FPM	16.0	15.1	°C/W
	100 FPM	15.4	16.4	°C/W
	150 FPM	14.9	14.2	°C/W
	200 FPM	14.4	13.7	°C/W
Package Size		21 x 21	25 x 25	mm^2
Die Size		5.12 x 7.78	5.12 x 7.78	mm^2

Note:

1. Refer to Section “Thermal Management Information,” on page 45 for more information about thermal management.
2. 3.8°C/W is the theoretical θ_{JB} mounted to infinite heat sink. The larger number applies to a module mounted on a 1.8 mm thick, 2P card using 1 oz copper power/gnd planes, with an effective area for heat transfer of 75mm x 75mm.

The 750 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *PowerPC 740 and PowerPC 750 User’s Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in the table below.

Thermal Sensor Specifications

See System Design Section.

DC Electrical Specifications

See "Recommended Operating Conditions," on page 11, for operating conditions.

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	$V_{IH(3.3V)}$	2.0	3.465	V	1, 2
	$V_{IH(2.5V)}$	1.75	2.625		
	$V_{IH()1.8V}$	1.4	1.89		
Input low voltage (all inputs except SYSCLK)	$V_{IL(3.3V)}$	GND	0.8	V	
	$V_{IL(2.5V)}$	GND	0.7		
	$V_{IL()1.8V}$	GND	0.5		
SYSCLK input high voltage	$CV_{IH(3.3V)}$	2.0	3.465	V	1, 4
	$CV_{IH(2.5V)}$	2.0	2.625		
	$CV_{IH(1.8V)}$	1.5	1.89		
SYSCLK input low voltage	CV_{IL}	–	0.4	V	4
Input leakage current, $V_{IN} = OV_{DD}$	I_{IN}	–	20	μA	1, 2
Hi-Z (off state) leakage current, Vin = OV_{DD}	I_{TSI}	–	20	μA	1, 2
Output high voltage, I_{OH} = –6mA	$V_{OH(3.3V)}$	2.4	–	V	
Output high voltage, I_{OH} = –6mA	$V_{OH((2.5V))}$	1.9	–	V	
Output high voltage, I_{OH} = –3mA	$V_{OH(1.8V)}$	1.4	–	V	
Output low voltage, I_{OL} = 6mA	V_{OL}	–	0.4	V	
Capacitance, V_{IN} =0 V, f = 1MHz	C_{IN}	–	5.0	pF	2,3

Note:

1. For 60x bus signals, the reference is OV_{DD}, while $L2OV_{DD}$ is the reference for the L2 bus signals.
2. JTAG port signal levels are controlled by the BVSEL pin and are the same as those shown for the 60x bus. $\overline{\text{LSSD\_MODE}}$, L1_TSTCLK, and L2TSTCLK receiver voltage levels are those shown for OV_{DD} = 1.8V nominal, regardless of BVSEL. JTAG, $\overline{\text{LSSD\_MODE}}$, L1_TSTCLK, and L2TSTCLK values in this table are guaranteed by design and characterization, and are not tested.
3. Capacitance values are guaranteed by design and characterization, and are not tested.
4. SYSCLK input high and low voltage: I/O timings are measured using a "rail to rail" SYSCLK; I/O timing may be less favorable if SYSCLK does not travel from GND to OV_{DD}.

Power Consumption for 740 and 750

See Table "Recommended Operating Conditions," on page 11, for operating conditions

	Actual Processor CPU Frequency											Unit	Notes
	300	333	350	366	375	400	433	466	500A	500C	533D		
Full-On Mode													
Typical	3.7	4.0	4.1	4.3	4.4	4.5	5.0	5.5	6.0	6.3	6.75	W	1, 3, 4
Maximum	4.5	5.0	5.2	5.5	5.7	6.0	6.3	6.8	7.5	7.8	8.25	W	1, 2, 4
Doze Mode													
Maximum	1.7	1.7	1.7	1.8	1.8	1.9	2.1	2.2	2.5	3.3	3.3	W	1, 2, 4
Nap Mode													
Maximum	250	250	250	250	250	250	250	250	250	800	800	mW	1, 4
Sleep Mode													
Maximum	n/s	n/s	n/s	n/s	n/s	n/s	n/s	n/s	350	500	500	mW	1, 4

Note:

1. These values apply for all valid 60x bus and L2 bus ratios. The values do not include I/O Supply Power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically less than 10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15mW and $L2AV_{DD}$ = 15mW.
2. Maximum power is shown for a system executing worst case benchmark sequences at:
   - $V_{DD} = AV_{DD} = L2AV_{DD}$ = 2.1V (300 through 466, 500A, 500C)
   - $V_{DD} = AV_{DD} = L2AV_{DD}$ = 2.15V (533D)
   - $OV_{DD} = L2OV_{DD}$ = 3.3V
   - T_j = 65°C

   Maximum power at 85°C can be derived by adding 0.1 W to the maximum power shown at 65°C. Maximum power at 105°C can be derived by adding 0.3 W to the maximum power shown at 65°C.
3. Typical power is an average value shown for a system executing typical applications and benchmark sequences at:
   - $V_{DD} = AV_{DD} = L2AV_{DD}$ = 2.0V (300 through 400)
   - $V_{DD} = AV_{DD} = L2AV_{DD}$ = 2.05V (433 through 466, 500A, 500C)
   - $V_{DD} = AV_{DD} = L2AV_{DD}$ = 2.1V (533D)
   - $OV_{DD} = L2OV_{DD}$ = 3.3V
   - T_j = 45°C.
4. Guaranteed by design and characterization, and is not tested.
5. 500A column describes operation of the 500A part at 500 MHz.
   500C column describes operation of the 500C part at 500 MHz.
   533D column describes operation of the 533D part at 533 MHz.

AC Electrical Characteristics

This section provides the AC electrical characteristics for the 750. After fabrication, parts are sorted by maximum processor core frequency as shown in the Section “Clock AC Specifications,” on page 14, and tested for conformance to the AC specifications for that frequency. Parts are sold by maximum processor core frequency, subject to the specified application conditions. See ”Ordering Information,” on page 51. Unless otherwise noted, all timings apply for all I/O supply voltages.

Clock AC Specifications

The following table provides the clock AC timing specifications as defined in Figure 2.

Clock AC Timing Specifications

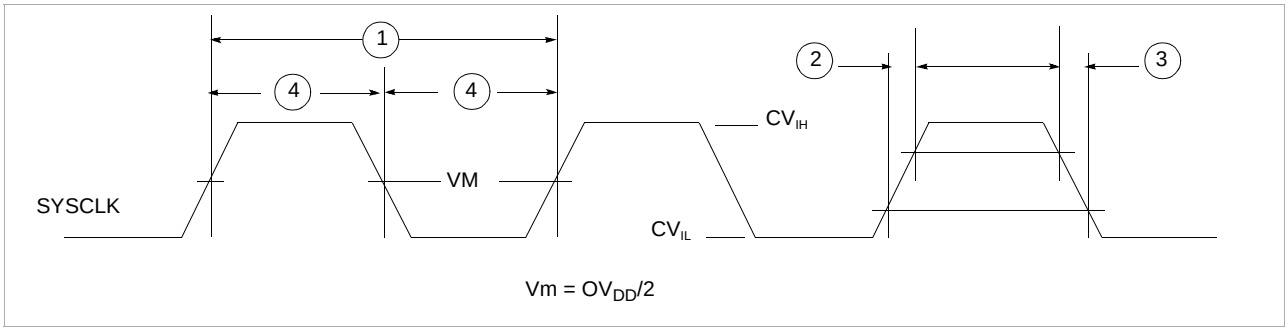
See ”Recommended Operating Conditions,” on page 11, for operating conditions.

Num	Characteristic	Fmax = 300-375MHz		Fmax ≥ 400MHz		Unit	Notes
		Min	Max	Min	Max		
	Processor frequency	250	As specified by part number	250	As specified by part number	MHz	6
	SYSCLK frequency	25	100	31	100	MHz	1
1	SYSCLK cycle time	10	40	10	32	ns	
2, 3	SYSCLK rise and fall time	–	1.0	–	1.0	ns	2, 3
4	SYSCLK duty cycle measured at Vm	40	60	40	60	%	3
	SYSCLK jitter, cycle-to-cycle	–	±150	–	±150	ps	4, 3
	Internal PLL relock time	–	100	–	100	µs	5

Note:

1. **Caution:** The SYSCLK frequency and the PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, and CPU (core) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section “PLL Configuration,” on page 40 for valid PLL_CFG[0:3] settings. Bus operation above 100 MHz is possible, but requires careful timing analysis. Contact IBM for details.
2. Rise and fall times for the SYSCLK input are measured from 0.5 to 1.5V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Short term jitter must be under ±150ps.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
6. Under certain conditions, operation at core frequencies below those stated is possible. Contact IBM for details.

Figure 2. SYSCLK Input Timing Diagram



Spread Spectrum Clock Generator (SSCG)

When designing with an SSCG, there are a number of issues that must be taken into account.

An SSCG creates a controlled amount of long-term jitter. In order for a receiving PLL in the 750 to function correctly with an SSCG, it must be able to accurately track the jitter.

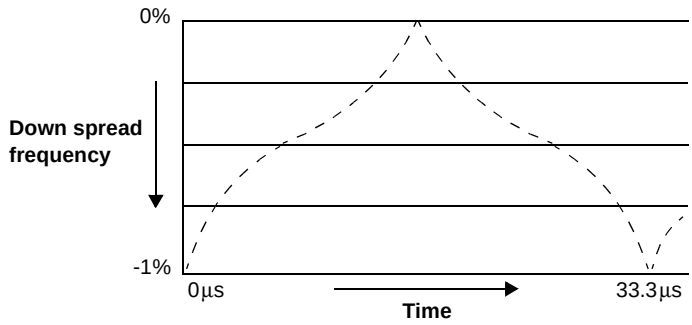
The accuracy with which the 750 PLL can track the SSCG is referred to as tracking skew. When performing system timing analysis, the tracking skew must be added to or subtracted from the I/O timing specifications, because the skew appears as a static phase error between the internal PLL and the SSCG.

To minimize the impact on I/O timing, the following SSCG configuration is recommended:

- Down-spread mode ≤ 0.5% of the maximum frequency
- Modulation frequency of 30 kHz
- Linear sweep modulation or a modulation profile (Hershey Kiss™ 1) as shown in Figure 3.

With this configuration, the tracking skew is less than 100 ps.

Figure 3. Linear Sweep Modulation Profile



60x Bus Input AC Specifications

The following table provides the 60X bus input AC timing specifications for the 750 as defined in Figure 4 and Figure 5. Input timing specifications for the L2 bus are provided in “L2 Bus Input AC Specifications,” on page 22.

60X Bus Input Timing Specifications[1]

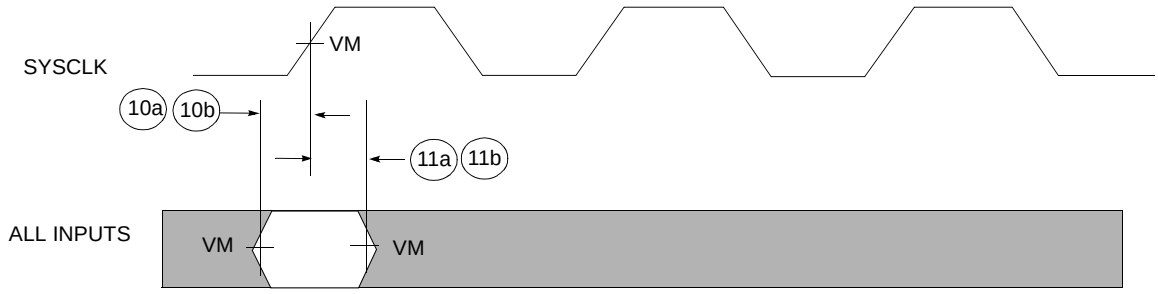
See ”Recommended Operating Conditions,” on page 11, for operating conditions.

Num	Characteristic	All Frequencies		Unit	Notes
		Minimum	Maximum		
10a	Address/Data/Transfer Attribute Inputs Valid to SYSCLK (Input Setup)	2.5	—	ns	2
10b	All Other Inputs Valid to SYSCLK (Input Setup)	2.5	—	ns	3
10c	Mode Select Input Setup to $\overline{\text{HRESET}}$ ($\overline{\text{DRTRY}}$,$\overline{\text{TLBISYNC}}$)	8	—	t_{sysclk}	4, 5, 6, 7
11a	SYSCLK to Address/Data/Transfer Attribute Inputs Invalid (Input Hold)	0.6	—	ns	2
11b	SYSCLK to All Other Inputs Invalid (Input Hold)	0.6	—	ns	3
11c	$\overline{\text{HRESET}}$ to mode select input hold ($\overline{\text{DRTRY}}$, $\overline{\text{TLBISYNC}}$)	0	—	ns	4, 6, 7

Note:

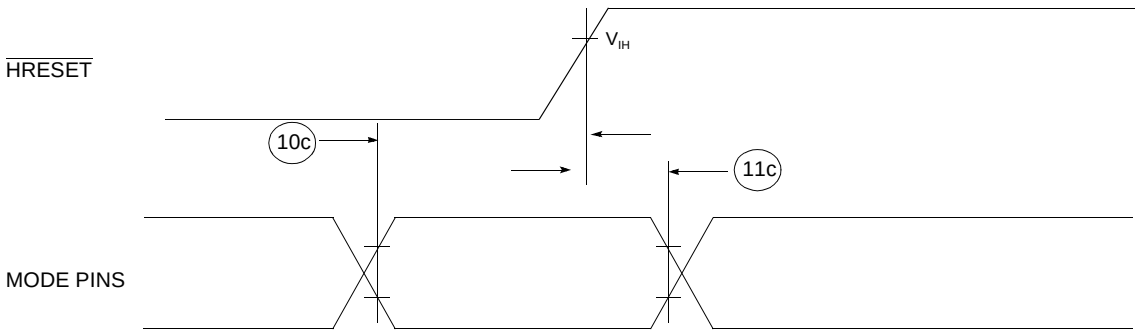
1. Input specifications are measured from the Vm of the signal in question to the Vm of the rising edge of the input SYSCLK. Input and output timings are measured at the pin (see Figure 4).
2. Address/Data Transfer Attribute inputs are composed of the following–A[0:31], AP[0:3], TT[0:4],$\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, DH[0:31], DL[0:31], DP[0:7].
3. All other signal inputs are composed of the following–$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{TBEN}}$, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 5).
5. t_{SYSCLK}, is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a *minimum of 255 bus clocks* after the PLL re-lock time during the power-on reset sequence.

Figure 4. Input Timing Diagram



Vm = 1.4 V for OV_{DD} = 3.3 V., else Vm = OV_{DD}/2

Figure 5. Mode Select Input Timing Diagram



V_{IH} = 2.0V

60x Bus Output AC Specifications

The following table provides the 60x bus output AC timing specifications for the 750 as defined in Figure 6. Output timing specification for the L2 bus are provided in the “L2 Bus Output AC Specifications,” on page 23.

60X Bus Output AC Timing Specifications for the 750[1]

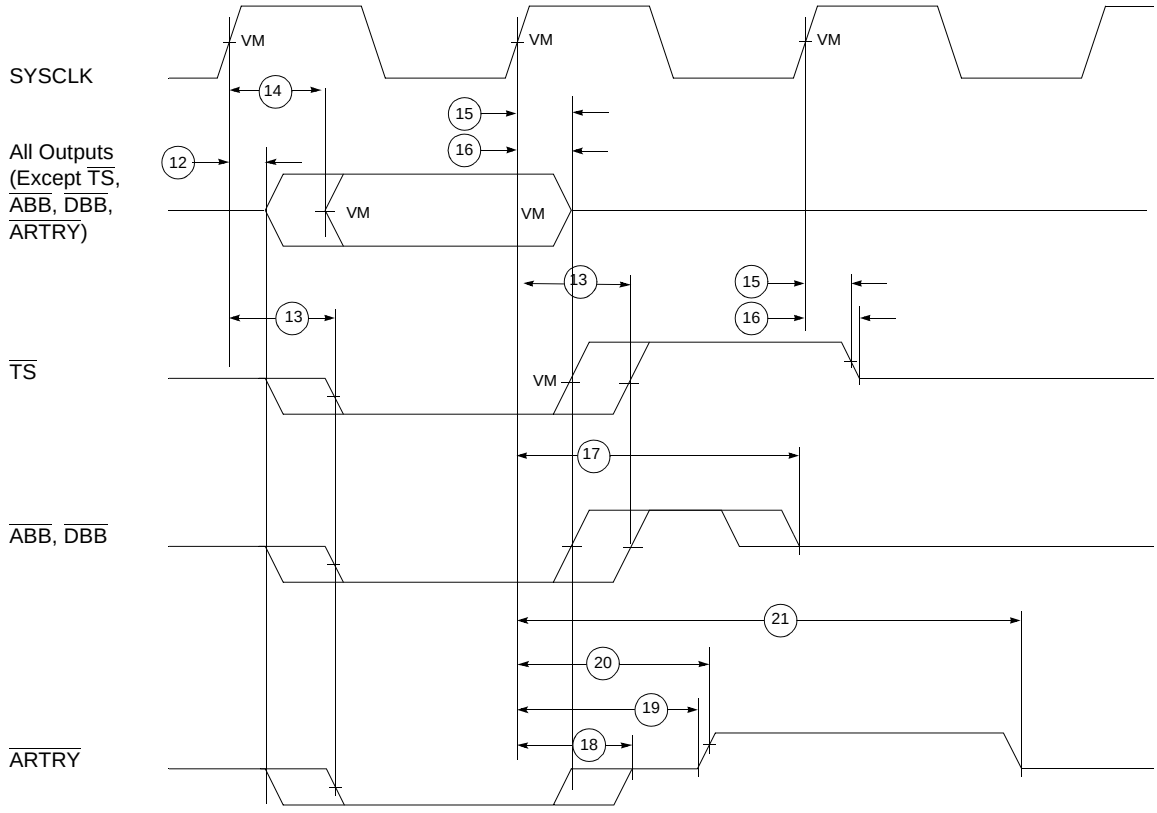
See ”Recommended Operating Conditions,” on page 11 for operating conditions, C_L = 50pF[2]

Num	Characteristic	All Frequencies		Unit	Notes
		Minimum	Maximum		
12	SYSCLK to Output Driven (Output Enable Time)	0.5		ns	8
13	SYSCLK to Output Valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$, and $\overline{TBST}$)	–	4.5	ns	5
14	SYSCLK to all other Output Valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$, and $\overline{TBST}$)	–	5.0	ns	5
15	SYSCLK to Output Invalid (Output Hold)	1.0		ns	3, 8, 9
16	SYSCLK to Output High Impedance (all signals except $\overline{ABB}$, $\overline{ARTRY}$, and $\overline{DBB}$)	–	6.0	ns	8
17	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ high impedance after precharge	–	1.0	t_{SYSCLK}	4, 6, 8
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	5.5	ns	8
19	SYSCLK to $\overline{ARTRY}$ precharge enable	$0.2 \times t_{SYSCLK} + 1.0$		ns	3, 4, 7
20	Maximum delay to $\overline{ARTRY}$ precharge		1	t_{SYSCLK}	4, 7
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge		2	t_{SYSCLK}	4, 7, 8

Note:

1. All output specifications are measured from Vm of the rising edge of SYSCLK to Vm of the signal in question. Both input and output timings are measured at the pin.
2. All maximum timing specifications assume C_L = 50pF.
3. This minimum parameter assumes CL = 0pF.
4. t_{SYSCLK} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
5. This footnote has been deleted.
6. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{SYSCLK}.
7. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}.
8. Guaranteed by design and characterization, and not tested.
9. Connecting L2_TSTCLK to GND no longer provides additional Output Hold. For new designs, L2_TSTCLK should be pulled up to OV_{DD}, but it can be left connected to GND in Legacy systems.

Figure 6. Output Timing Diagram



Vm = 1.4 V for OV_{DD} = 3.3 V., else Vm = OV_{DD}/2

L2 Clock AC Specifications

The following table provides the L2CLK output AC timing specifications for the 750 as defined in Figure 7.

L2CLK Output AC Timing Specifications

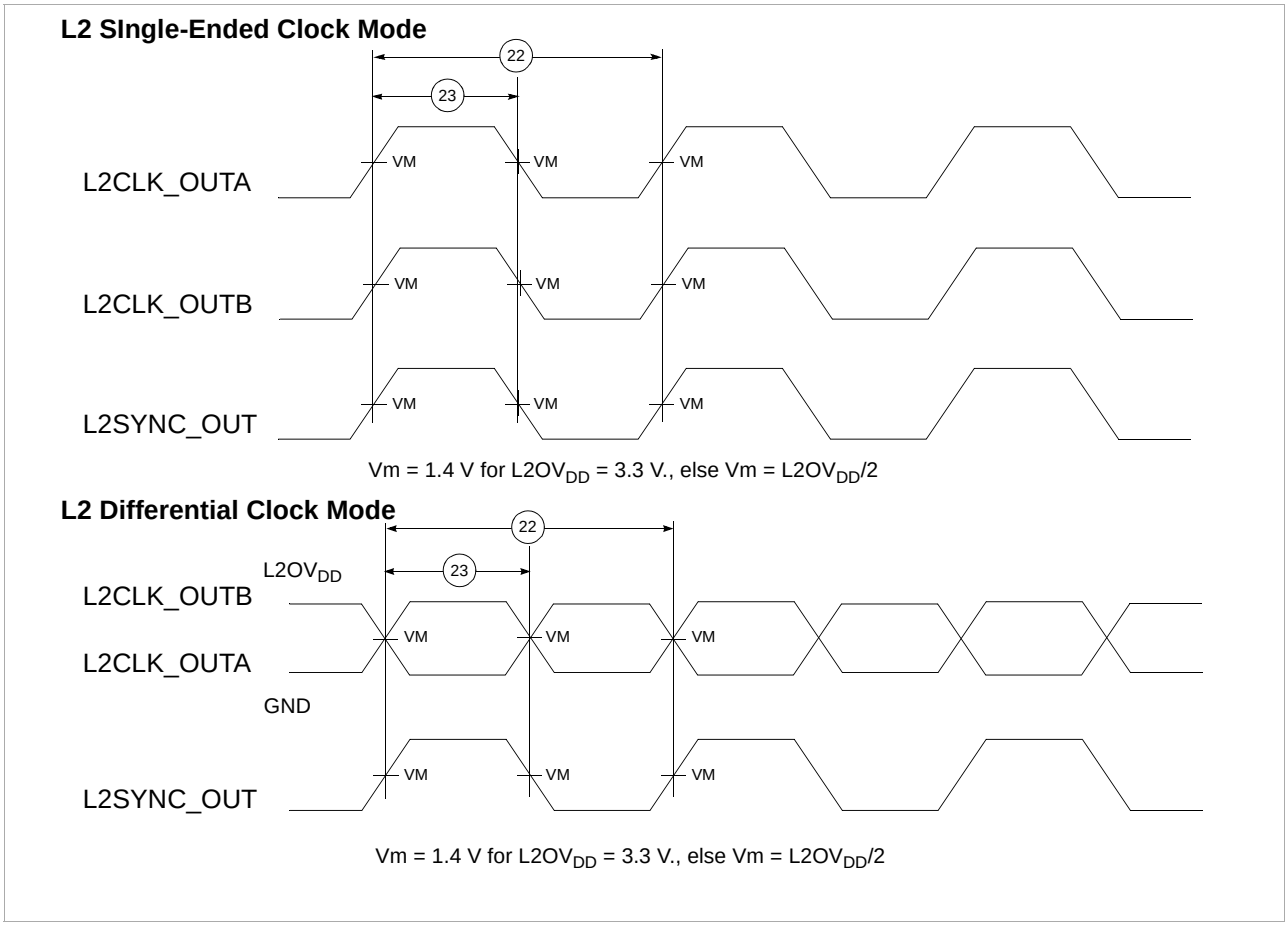
See ”Recommended Operating Conditions,” on page 11, for operating conditions.

Num	Characteristic	Min	Max	Unit	Notes
	L2CLK frequency	80	267	MHz	1, 5
22	L2CLK cycle time	3.75	12.5	ns	
23	L2CLK duty cycle	50		%	2
	Internal DLL-relock time	640	—	L2CLK	4
	L2CLK jitter	±	±150	ps	3, 6
	L2CLK skew		0	ps	7

Note:

1. L2CLK outputs are L2CLKOUTA, L2CLKOUTB and L2SYNC_OUT pins. The internal design supports higher L2CLK frequencies. Consult IBM PowerPC Application Engineering (ppcsupp@us.ibm.com) before operating the L2 SRAMs above core frequency/2. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. L2CLKOUTA and L2CLKOUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The major component of L2CLK jitter is passed through from SYSCLK. While SYSCLK jitter is less then ±150 ps, L2CLK jitter is also less than ±150 ps. SYSCLK jitter in excess of ±150 ps causes L2CLK jitter to exceed ±150 ps.
4. The DLL re-lock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in nanoseconds. Re-lock timing is guaranteed by design and characterization, and is not tested.
5. The L2CR [L2SL] bit should be set for L2CLK frequencies less than 110MHz.
6. Guaranteed by design and characterization, not tested.
7. Skew between the L2 output clocks is included in the other timing specs.

Figure 7. L2CLK_OUT Output Timing Diagram



L2 Bus Input AC Specifications

Some specifications are shown in the following table as a Function of Maximum Core Frequency (Fmax). These specifications refer to the effective Fmax of the part after derating for application conditions. For example, a nominal 450 MHz part running at application conditions that derate its Fmax to 400 MHz will meet or exceed the specifications shown for Fmax = 400 MHz.

L2 Bus Input Interface AC Timing Specifications

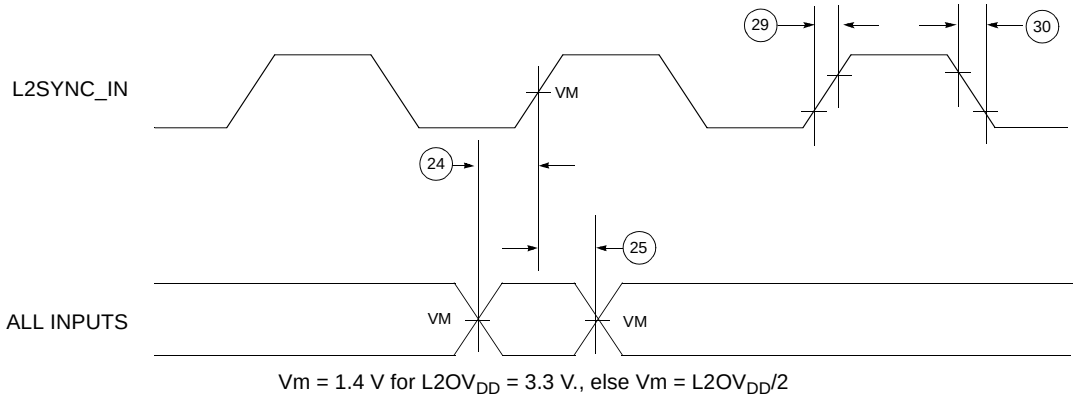
See "Recommended Operating Conditions," on page 11, for operating conditions.

Num	Characteristic	Min	Max	Unit	Notes
29,30	L2SYNC_IN rise and fall time	—	1.0	ns	2, 3
24	Data and parity input setup to L2SYNC_IN, Fmax up through 375 MHz.	1.5	—	ns	1
24	Data and parity input setup to L2SYNC_IN, Fmax = 400 MHz.	1.4	—	ns	1
24	Data and parity input setup to L2SYNC_IN, Fmax = 433 and 450 MHz.	1.1	—	ns	1
24	Data and parity input setup to L2SYNC_IN, Fmax = 466 and above.	1.0	—	ns	1
25	L2SYNC_IN to data and parity input hold	0.5	—	ns	1

Note:

1. All input specifications are measured from the Vm of the signal in question to the Vm of the rising edge of the input L2SYNC_IN. Input timings are measured at the pins (see Figure 8).
2. Rise and fall times for the L2SYNC_IN input are measured from 0.5 to 1.5V.
3. Guaranteed by design and characterization, and not tested.

Figure 8. L2 Bus Input Timing Diagrams



L2 Bus Output AC Specifications

L2 Bus Output Interface AC Timing Specifications[1]

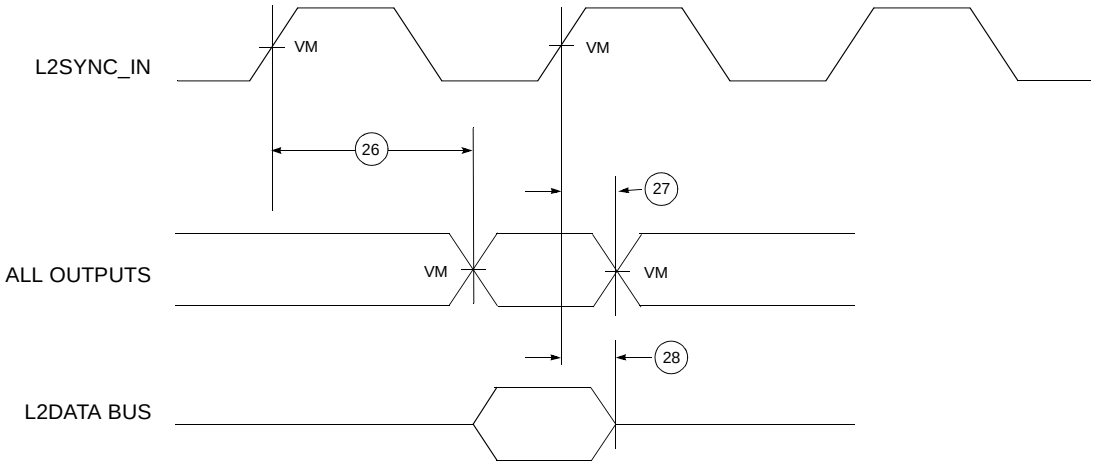
See "Recommended Operating Conditions," on page 11 for operating conditions, C_L = 20pF[3].

Num	Characteristic	L2CR[14:15] is equivalent to:								Unit	Notes
		00[2]		01		10		11			
		Min	Max	Min	Max	Min	Max	Min	Max		
26	L2SYNC_IN to output valid, Fmax[7] up through 375 MHz.	—	3.2	—	3.7	—	Rsv[5]	—	Rsv[5]	ns	
26	L2SYNC_IN to output valid, Fmax = 400 MHz.	—	3.0	—	3.5	—	Rsv[5]	—	Rsv[5]	ns	
26	L2SYNC_IN to output valid, Fmax = 433 and 450 MHz.	—	2.6	—	3.1	—	Rsv[5]	—	Rsv[5]	ns	
26	L2SYNC_IN to output valid, Fmax = 466 and above.	—	2.4	—	2.9	—	Rsv[5]	—	Rsv[5]	ns	
27	L2SYNC_IN to output hold	0.5	—	1.0	—	Rsv[5]	—	Rsv[5]	—	ns	4, 6
28	L2SYNC_IN to high impedance	—	3.5	—	4.0	—	Rsv[5]	—	Rsv[5]	ns	6

Note:

1. All outputs are measured from the Vm of the rising edge of L2SYNC_IN to the Vm of the signal in question. The output timings are measured at the pins (see Figure 9).
2. The outputs are valid for both single-ended and differential L2CLK modes. For flow-through and pipelined reg-reg synchronous burst SRAMs, L2CR[14:15] = 00 is recommended. For pipelined late-write synchronous burst SRAMs, L2CR[14:15] = 01 is recommended.
3. All maximum timing specifications assume C_L = 20pF.
4. This measurement assumes C_L = 5pF.
5. Reserved for future use.
6. Guaranteed by design and characterization, and not tested.
7. Specifications are shown as a Function of Maximum Core Frequency (Fmax). They refer to the effective Fmax of the part after derating for application conditions. For example, a nominal 450 MHz part running at application conditions that derate its Fmax to 400 MHz will meet or exceed the specifications shown for Fmax = 400 MHz.

Figure 9. L2 Bus Output Timing Diagrams



Vm = 1.4 V for $L2OV_{DD}$ = 3.3 V., else Vm = $L2OV_{DD}/2$

IEEE 1149.1 AC Timing Specifications

The table below provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 10, Figure 11, Figure 12, and Figure 13. The five JTAG signals are; TDI, TDO, TMS, TCK, and $\overline{\text{TRST}}$.

JTAG AC Timing Specifications (Independent of SYSCLK)

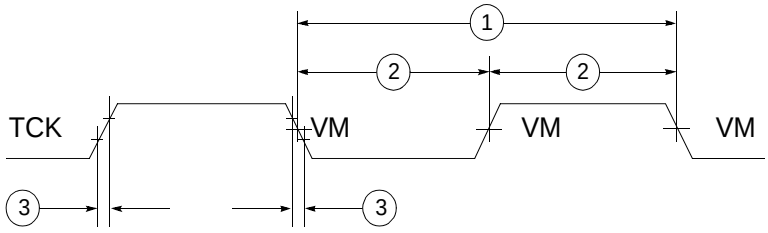
See "Recommended Operating Conditions," on page 11 for operating conditions, C_L = 50pF.

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at 1.4V	15	—	ns	
3	TCK rise and fall times	0	2	ns	4
4	spec obsolete, intentionally omitted				
5	$\overline{\text{TRST}}$ assert time	25	—	ns	1
6	Boundary-scan input data setup time	4	—	ns	2
7	Boundary-scan input data hold time	16	—	ns	2
8	TCK to output data valid	4	20	ns	3, 5
9	TCK to output high impedance	3	19	ns	3, 4
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	16	—	ns	
12	TCK to TDO data valid	2.5	12	ns	5
13	TCK to TDO high impedance	3	9	ns	4

Note:

1. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. Guaranteed by design.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by characterization and not tested.
5. Minimum spec guaranteed by characterization and not tested.

Figure 10. JTAG Clock Input Timing Diagram



Vm = 1.4 V for OV_{DD} = 3.3 V., else Vm = OV_{DD}/2

Figure 11. $\overline{\text{TRST}}$ Timing Diagram

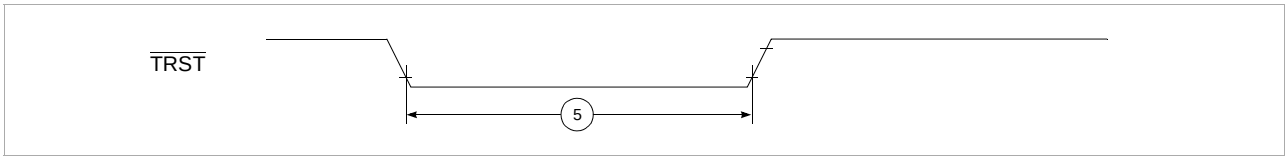


Figure 12. Boundary-Scan Timing Diagram

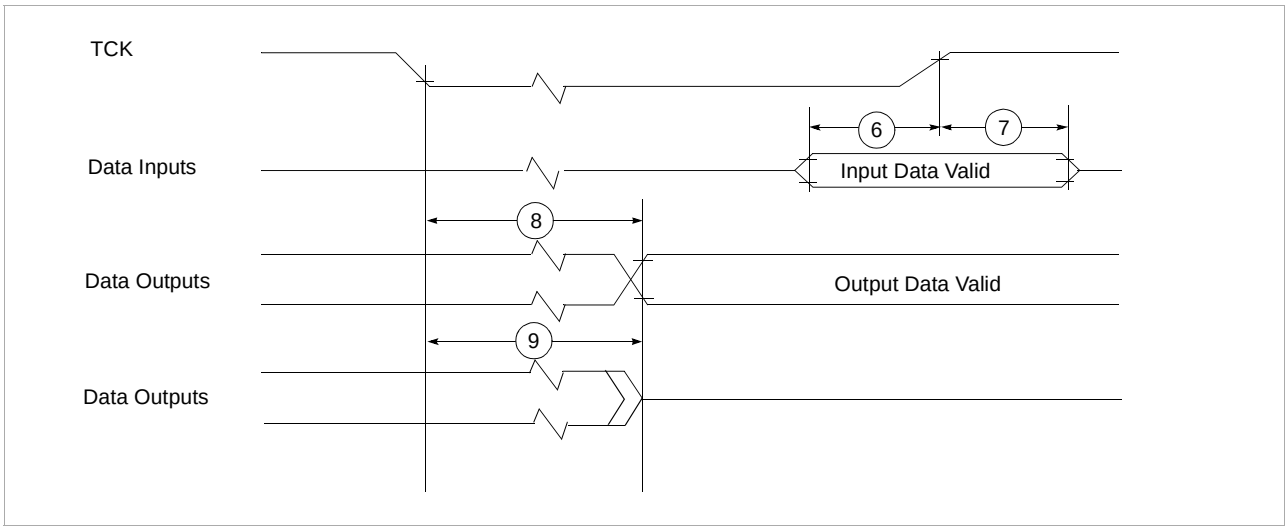
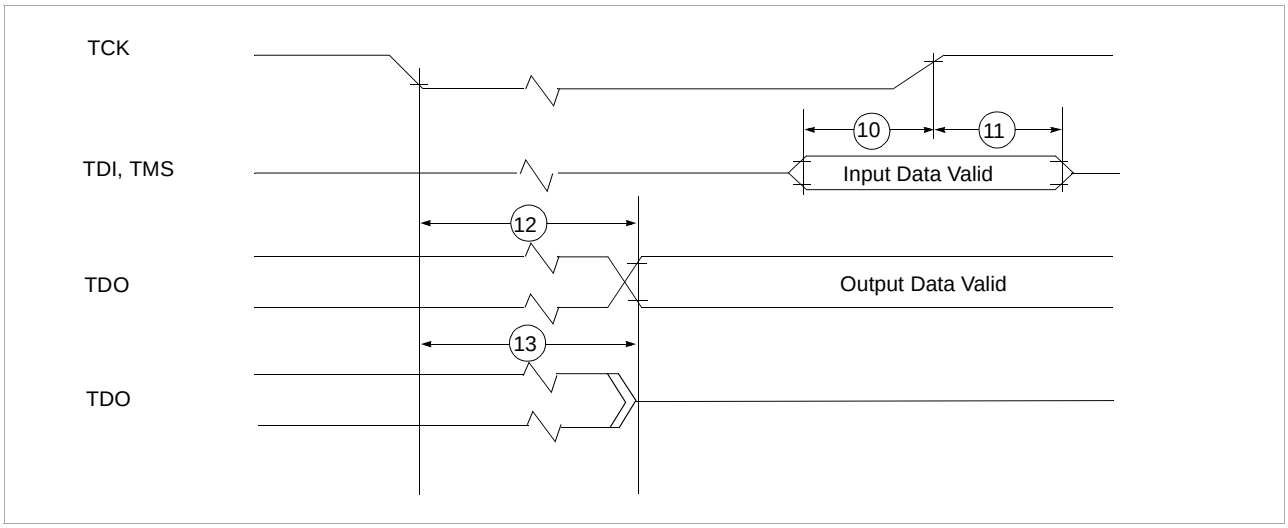


Figure 13. Test Access Port Timing Diagram



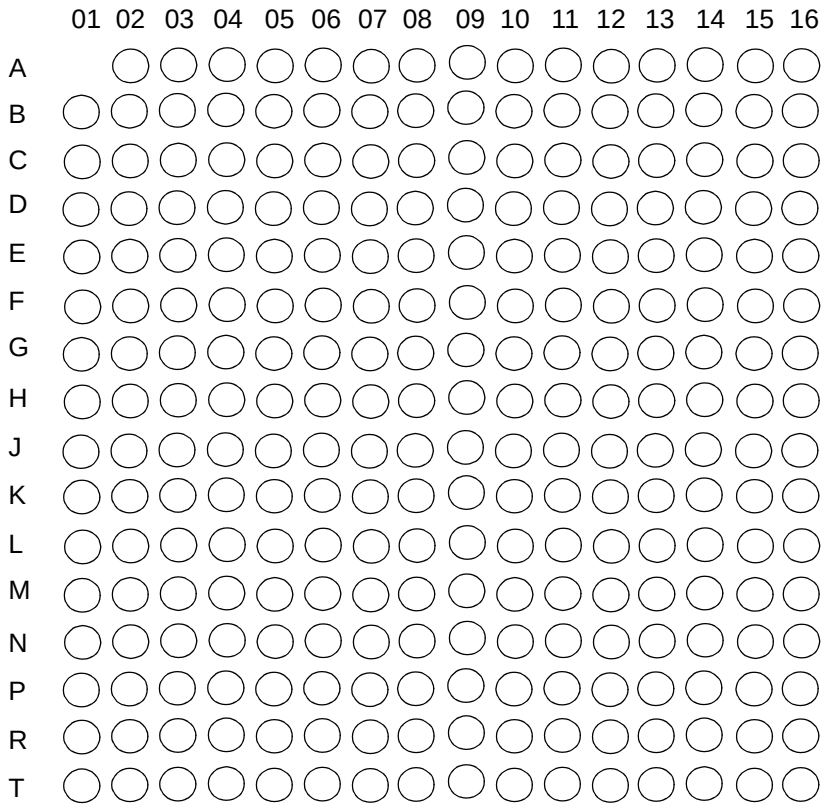
PowerPC 740 Microprocessor Pin Assignments

The following sections contain the pinout diagrams for the PowerPC 740, a 255 pin ceramic ball grid array (BGA) package.

Figure 14 (in part A) shows the pinout of the PPC 740, a 255 pin Ceramic Ball Grid Array (CBGA) package as viewed from the top surface. Part B shows the side profile.

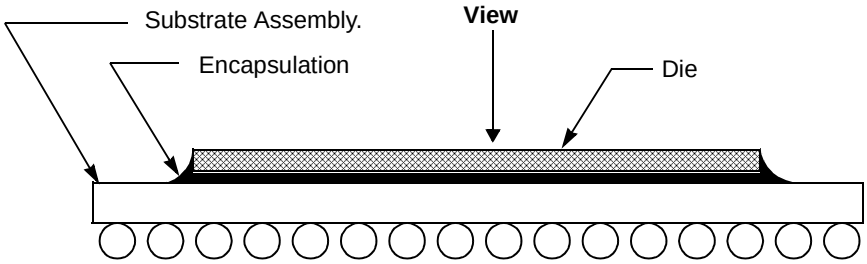
Figure 14. Pinout of the 740 255 CBGA Package as Viewed from the Top Surface

Part A



Not to Scale

Part B



Pinout Listing for the PowerPC 740 255 CBGA Package

Signal Name	Pin Number	Active	I/O
A[0:31]	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP[0:3]	C01, B04, B03, B02	High	I/O
$\overline{\text{ARTRY}}$	J04	Low	I/O
AVDD	A10	—	—
$\overline{\text{BG}}$	L01	Low	Input
$\overline{\text{BR}}$	B06	Low	Output
BVSEL[1]	H04		Input
$\overline{\text{CI}}$	E01	Low	Output
$\overline{\text{CKSTP\_IN}}$	D08	Low	Input
$\overline{\text{CKSTP\_OUT}}$	A06	Low	Output
CLK_OUT	D07	—	Output
$\overline{\text{DBB}}$	J14	Low	I/O
$\overline{\text{DBG}}$	N01	Low	Input
$\overline{\text{DBDIS}}$	H15	Low	Input
$\overline{\text{DBWO}}$	G04	Low	Input
DH[0:31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL[0:31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP[0:7]	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DRTRY}}$	G16	Low	Input
$\overline{\text{GBL}}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
$\overline{\text{HRESET}}$	A07	Low	Input
$\overline{\text{INT}}$	B15	Low	Input
L1_TSTCLK [2]	D11	High	Input
L2_TSTCLK [2]	D12	High	Input
$\overline{\text{LSSD\_MODE}}$ [2]	B10	Low	Input
$\overline{\text{MCP}}$	C13	Low	Input

Pinout Listing for the PowerPC 740 255 CBGA Package (cont.)

Signal Name	Pin Number	Active	I/O
NC (No-Connect)	B07, B08, C03, C06, C08, D05, D06, J16, A04, A05, A02, A03, B01, B05	—	—
OVDD	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—
PLL_CFG[0:3]	A08, B09, A09, D09	High	Input
$\overline{\text{QACK}}$	D03	Low	Input
$\overline{\text{QREQ}}$	J03	Low	Output
$\overline{\text{RSRV}}$	D01	Low	Output
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	—	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TCK	C11	High	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
$\overline{\text{TLBISYNC}}$	C04	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ[0:2]	A13, D10, B12,	High	Output
TT[0:4]	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
VDD [3]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—
VOLTDET[4]	F03	Low	Output

Note:

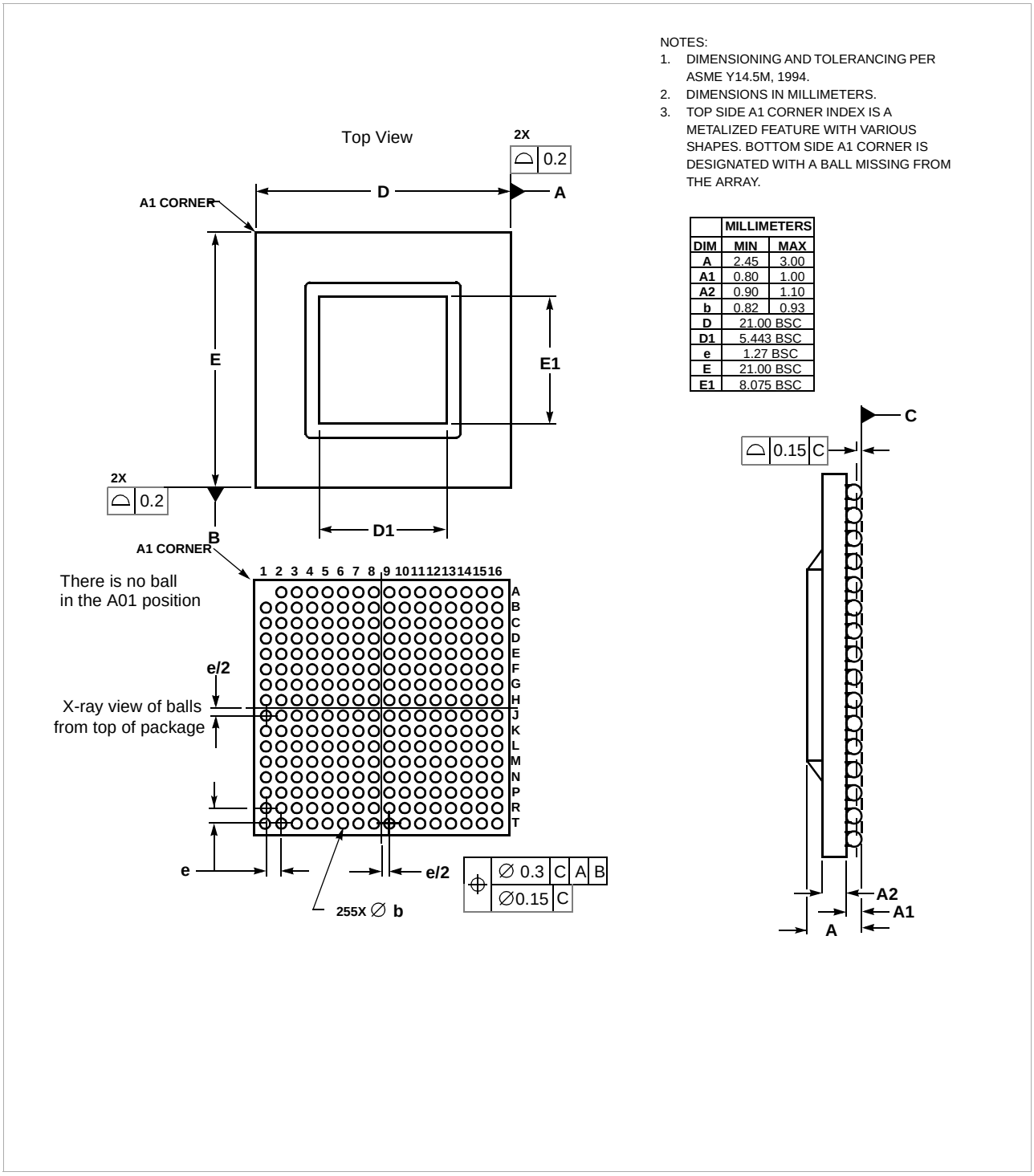
1. BVSEL Function:
   a. Unconnected or Pulled to OV_{DD} — OV_{DD} = 3.3 V nominal
   b. Connected to $\overline{\text{HRESET}}$ — OV_{DD} = 2.5 V nominal
   c. Connected to GND — OV_{DD} = 1.8 V nominal
   If BVSEL is connected to GND with a series resistor, the resistor value must be 10 Ω or less.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal operation.
3. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core.
4. Internally tied to GND in the 255 CBGA package. This is NOT a supply pin.

PowerPC 740 Package

Package Type	Ceramic Ball Grid Array (CBGA)
Package outline	21 x 21mm
Interconnects	255 (16 x 16 ball array - 1)
Pitch	1.27mm (50mil)
Minimum module height	2.45mm
Maximum module height	3.00mm
Ball diameter	0.89mm (35mil)

Mechanical Dimensions of the PowerPC 740 255 CBGA Package

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature of the 255 CBGA Package



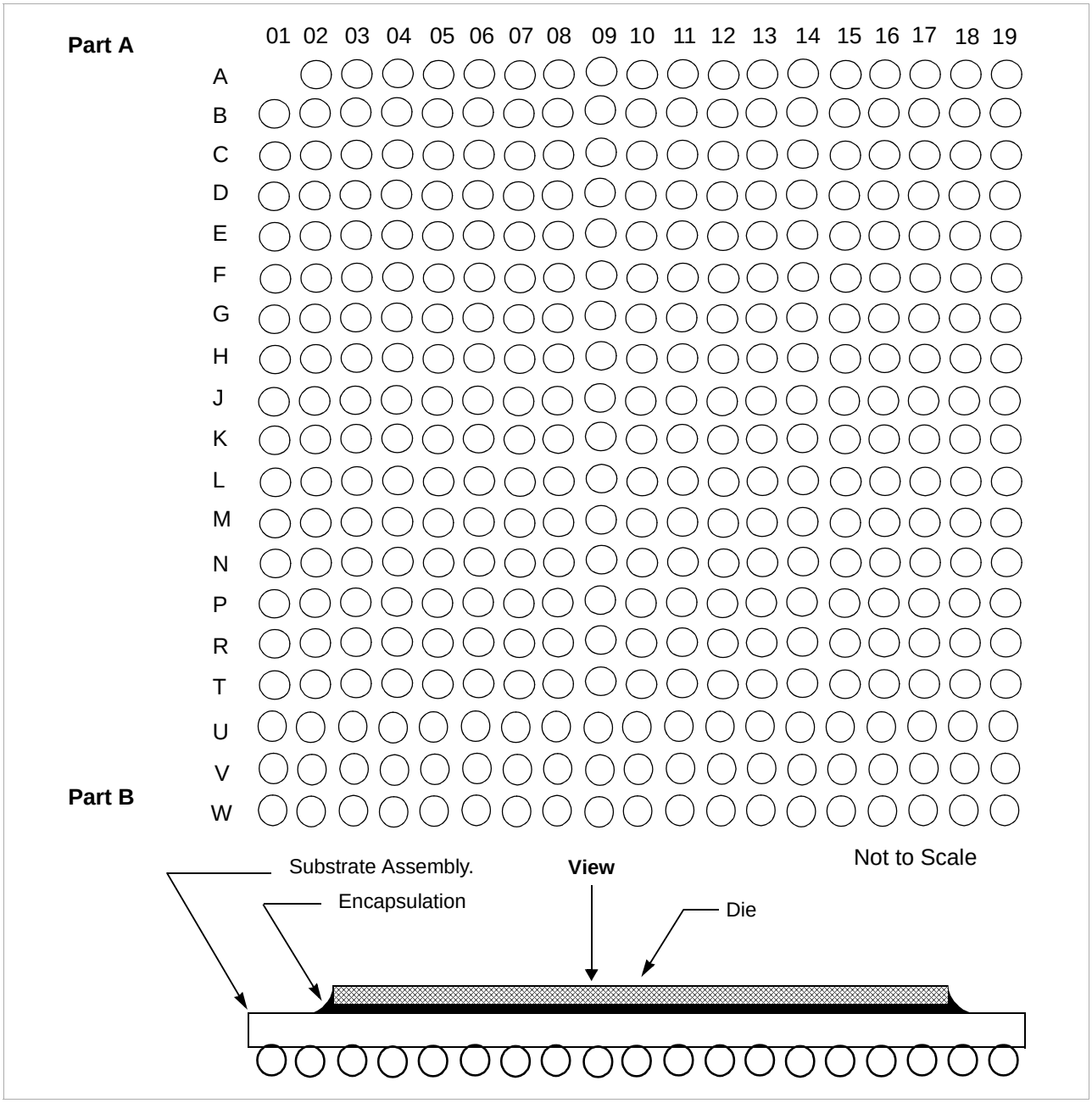
	MILLIMETERS	
DIM	MIN	MAX
A	2.45	3.00
A1	0.80	1.00
A2	0.90	1.10
b	0.82	0.93
D	21.00 BSC	
D1	5.443 BSC	
e	1.27 BSC	
E	21.00 BSC	
E1	8.075 BSC	

PowerPC 750 Microprocessor Pin Assignments

The following sections contain the pinout diagrams for the PowerPC 750 ceramic ball grid array 360 CBGA packages.

Figure 16 (in part A) shows the pinout of the 360 CBGA package as viewed from the top surface. Part B shows the side profile of the 360 CBGA package to indicate the direction of the top surface view.

Figure 16. Pinout of the 750 360 CBGA Package as Viewed from the Top Surface



Pinout Listing for the PowerPC 750 360 CBGA Package

Signal Name	Pin Number	Active	I/O
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O
$\overline{\text{AACK}}$	N3	Low	Input
$\overline{\text{ABB}}$	L7	Low	I/O
AP[0:3]	C4, C5, C6, C7	High	I/O
$\overline{\text{ARTRY}}$	L6	Low	I/O
AVDD [1]	A8	—	—
$\overline{\text{BG}}$	H1	Low	Input
$\overline{\text{BR}}$	E7	Low	Output
BVSEL[2]	W01[2]	—	Input
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output
$\overline{\text{CI}}$	C2	Low	Output
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input
CLKOUT	E3	—	Output
$\overline{\text{DBB}}$	K5	Low	I/O
$\overline{\text{DBDIS}}$	G1	Low	Input
$\overline{\text{DBG}}$	K1	Low	Input
$\overline{\text{DBWO}}$	D1	Low	Input
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O
$\overline{\text{DRTRY}}$	H6	Low	Input
$\overline{\text{GBL}}$	B1	Low	I/O
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—
$\overline{\text{HRESET}}$	B6	Low	Input
$\overline{\text{INT}}$	C11	Low	Input
L1_TSTCLK[3]	F8	High	Input
L2ADDR[0:16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output
L2AVDD	L13	—	—
$\overline{\text{L2CE}}$	P17	Low	Output
L2CLKOUTA	N15	—	Output

Pinout Listing for the PowerPC 750 360 CBGA Package (cont.)

Signal Name	Pin Number	Active	I/O
L2CLKOUTB	L16	—	Output
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	—	—
L2SYNC_IN	L14	—	Input
L2SYNC_OUT	M14	—	Output
L2_TSTCLK[3]	F7	High	Input
L2VSEL	A19[2]	—	Input
$\overline{\text{L2WE}}$	N16	Low	Output
L2ZZ	G17	High	Output
$\overline{\text{LSSD\_MODE}}$[3]	F9	Low	Input
$\overline{\text{MCP}}$	B11	Low	Input
NC (No-Connect)	B3, B4, B5, W19, K9, K11[4], K19[4]	—	—
OVDD [2]	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input
$\overline{\text{QACK}}$	B2	Low	Input
$\overline{\text{QREQ}}$	J3	Low	Output
$\overline{\text{RSRV}}$	D3	Low	Output
$\overline{\text{SMI}}$	A12	Low	Input
$\overline{\text{SRESET}}$	E10	Low	Input
SYSCLK	H9	—	Input
$\overline{\text{TA}}$	F1	Low	Input
TBEN	A2	High	Input
$\overline{\text{TBST}}$	A11	Low	I/O
TCK	B10	High	Input
TDI	B7	High	Input
TDO	D9	High	Output
$\overline{\text{TEA}}$	J1	Low	Input
$\overline{\text{TLBISYNC}}$	A3	Low	Input
TMS	C8	High	Input
$\overline{\text{TRST}}$	A10	Low	Input
$\overline{\text{TS}}$	K7	Low	I/O

Pinout Listing for the PowerPC 750 360 CBGA Package (cont.)

Signal Name	Pin Number	Active	I/O
TSIZ[0:2]	A9, B9, C9	High	Output
TT[0:4]	C10, D11, B12, C12, F11	High	I/O
$\overline{WT}$	C3	Low	Output
VDD [5]	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—
VOLTDET[6]	K13	High	Output

Note:

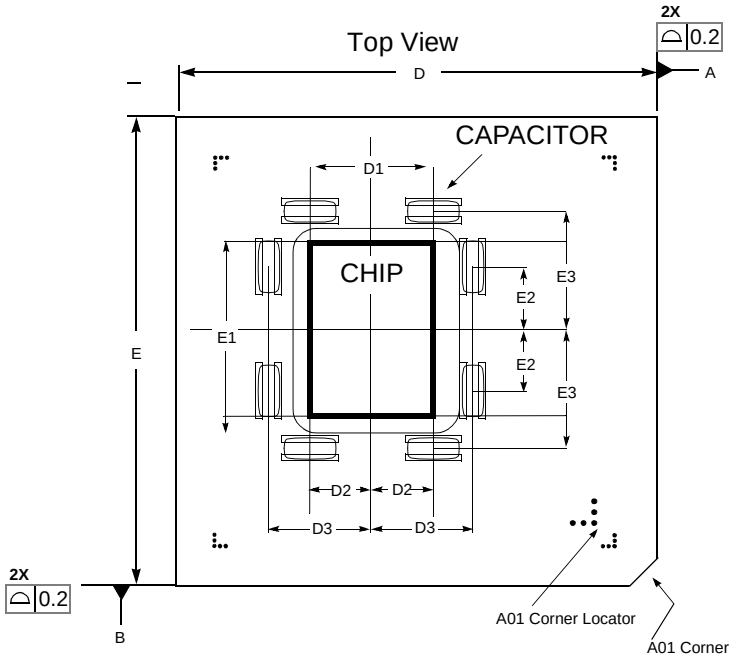
1. For dd3.x on the 750 only, AV_{DD} is no longer connected to the BGA pin. AV_{DD} is filtered on the module from V_{DD}. The 740 dd3.2 does require AV_{DD}.
2. BVSEL Function:
   a. Unconnected or Pulled to OV_{DD} — $L2OV_{DD}$ = 3.3 V nominal
   b. Connected to HRESET — OV_{DD} = 2.5 V nominal
   c. Connected to GND — OV_{DD} = 1.8 V nominal
   If BVSEL or L2VSEL is connected to GND with a series resistor, the resistor value must be 10 Ω or less.
3. These are test signals for factory use only and must be pulled up to OV_{DD} for normal operation. During normal operation, L2_TSTCLK can be connected to GND if required.
4. These pins are reserved for potential future use as additional L2 address pins.
5. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core.
6. Internally tied to $L2OV_{DD}$ in the 750 360 CBGA package. This is NOT a supply pin.

PowerPC 750 Package

Package Type	Ceramic Ball Grid Array (CBGA)
Package outline	25 x 25mm
Interconnects	360 (19 x 19 ball array - 1)
Pitch	1.27mm (50mil)
Minimum module height	2.65mm
Maximum module height	3.20mm
Ball diameter	0.89mm (35mil)

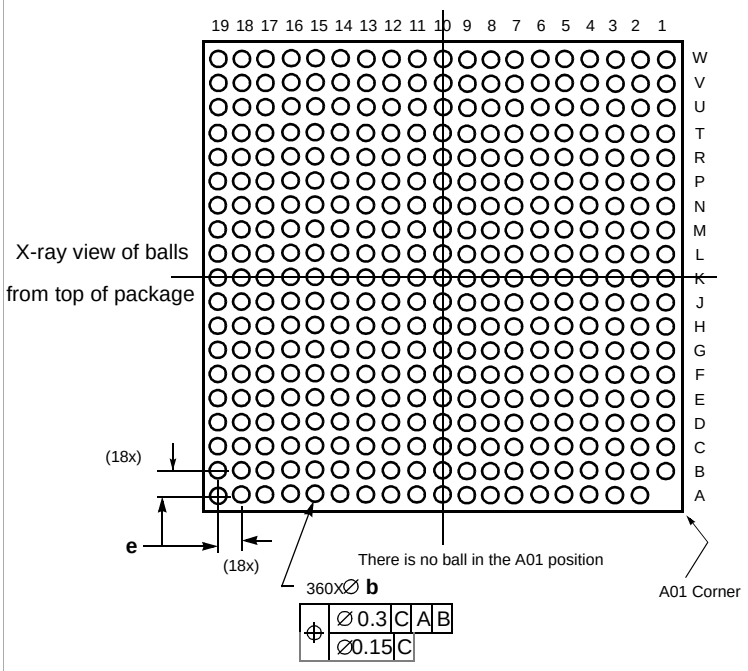
Mechanical Dimensions of the PowerPC 750 360 CBGA Package

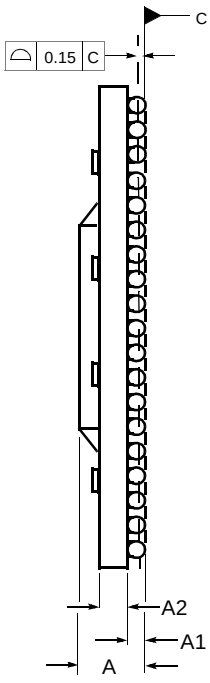
Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature of the 360 CBGA Package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	MILLIMETERS	
DIM	Minimum	Maximum
A	2.65	3.20
A1	0.80	1.00
A2	1.10	1.30
b	0.82	0.93
D	25.00 BSC	
D1	5.443	
D2	2.48	
D3	6.3	
e	1.27 BSC	
E	25.00 BSC	
E1	8.075	
E2	2.48	
E3	7.43	

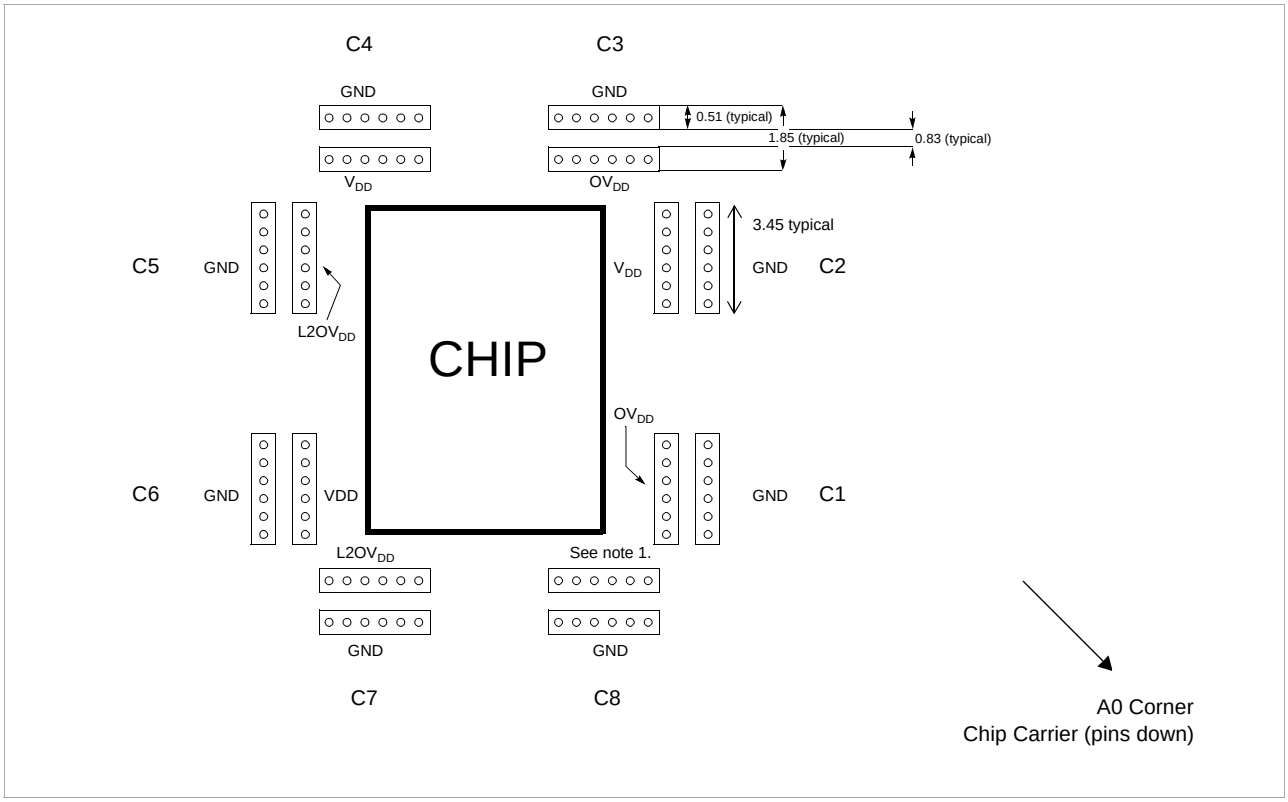




Not To Scale

Note: All caps on the SCM are lower in height than the processor die.

Figure 18. 360 CBGA Decoupling Capacitors



Notes:

1. For PID8 - 750 dd2.x, this capacitor is connected to V_{DD}. For dd3.x, this capacitor is connected to AV_{DD}.
2. For dd3.x, AV_{DD} is no longer brought to the BGA pin.
3. All installed caps are 47 nF.

System Design Information

Thermal Assist Unit Specifications

Num	Characteristic	Minimum	Maximum	Unit	Notes
1	Temperature range	0	128	°C	1
2	Comparator settling time	20	—	ms	2
3	Resolution	4	—	°C	3

Note:

1. The temperature is the junction temperature of the die. The thermal assist unit's (TAU) raw output does not indicate an absolute temperature, but it must be interpreted by software to derive the absolute junction temperature. For information on how to use and calibrate the TAU, contact ppc-supp@us.ibm.com. This specification reflects the temperature span supported by the design.
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR. For parts with nominal operating frequencies (speed sort) above 266 MHz, the settling time = 20 µs × (266/nominal frequency). For example: for 500 MHz parts, settling time = 20 µs × (266/500) = 10.6 µs. It is recommended that the maximum value be set in THRM3 under all conditions.
3. This value is guaranteed by design and is not tested.

Thermal Assist Unit Accuracy

Some previous versions of this Datasheet incorrectly specified the accuracy of the Thermal Assist Unit (TAU). See the *PowerPC 750-PID8p Microprocessor Errata List*, Version 4.4 for details.

A Design Margin has been issued, which describes a fault in the TAU of certain dd3.2 parts, which prevents them from attaining the accuracy specified in this Datasheet. See *Design Margin, PPC750L dd3.2 TAU False High Reading Fault* for more details.

The TAU is an analog device whose accuracy can be affected by various error sources. The cumulative effects of these error sources is shown in the table sin this section. IBM strongly recommends that at least a single-point calibration be performed on the TAU before use. More information on calibrating and improving the accuracy of the TAU is provided in the IBM Application Note, *Calibrating the Thermal Assist Unit in the IBM25PPC750L Processors*.

The table “Selected Worst Case Maximum and Minimum Readings” shows, for selected actual junction temperatures, the highest and lowest TAU reading at which an exception could be signalled by the TAU. This table applies only to uncalibrated units. Readings for temperatures not shown can be extrapolated from the points in the table.

Selected Worst Case Maximum and Minimum Readings

Actual	Highest TAU Reading	Lowest TAU Reading
22	32	2
35	46	13
45	56	21
55	67	29
65	77	37
75	88	45
85	98	53
95	109	61
105	119	69

The table “Worst Case Actual Junction Temperature for Selected TAU Readings” shows, for selected TAU readings (register settings at which the TAU is programmed to signal an exception), the worst case highest and lowest actual junction temperatures at which the TAU could signal the interrupt. This table applies only to uncalibrated units. Readings for temperatures not shown can be extrapolated from the points in the table.

Worst Case Actual Junction Temperature for Selected TAU Readings

Tau Reading	Lowest Actual	Highest Actual		Tau Reading	Lowest Actual	Highest Actual
22	12	47		76	64	113
24	14	49		80	68	118
28	18	54		84	72	123
32	22	59		88	75	128
36	26	64		92	79	133
40	30	69		96	83	138
44	33	74		100	87	143
48	37	79		104	91	148
52	41	84		108	94	153
56	45	89		112	98	158
60	49	94		116	102	163
64	52	99		120	106	168
68	56	103		124	110	173
72	60	108		128	113	178

PLL Configuration

The 750 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation.

PLL Configuration

PLL_CFG (0:3)		Processor to Bus Frequency Ratio
bin	dec	
0000	0	Rsv[1]
0001	1	7.5x
0010	2	7x
0011	3	PLL Bypass[3]
0100	4	2x[6]
0101	5	6.5x
0110	6	10x
0111	7	4.5x
1000	8	3x
1001	9	5.5x
1010	10	4x
1011	11	5x
1100	12	8x
1101	13	6x
1110	14	3.5x
1111	15	Off[4]

Note:

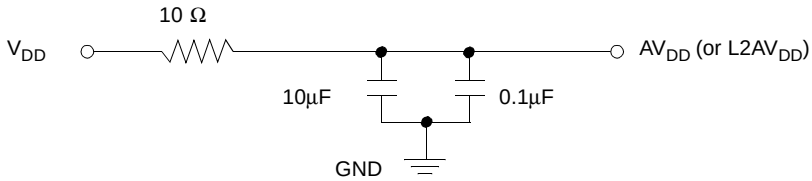
1. Reserved settings.
2. SYSCLK min is limited by the lowest frequency that manufacturing will support, see Section , “Clock AC Specifications,” for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. **Note:** The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. In Clock-off mode, no clocking occurs inside the 750 regardless of the SYSCLK input.
5. The VCO to core clock ratio is 2x for 740/750. This simplifies clock frequency calculations so the user can disregard the VCO frequency. The VCO will operate correctly when the core clock is within specification.
6. Not tested.

PLL Power Supply Filtering

The AV_{DD} and L2AVdd are power signals provided on the 750 to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered using a circuit similar to the one shown in Figure 19. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible.

For dd3.2, AVdd is filtered on the module from V_{DD} for the 750 only and can be connected or not, at the designer's convenience. For the 750, the $L2AV_{DD}$ must be connected as shown. The 740 requires AV_{DD} to be supplied as usual.

Figure 19. PLL Power Supply Filter Circuit



Decoupling Recommendations

Due to the dynamic power management of the 750, which features large address and data buses, as well as high operating frequencies, the 750 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 750 system, and the 750 itself requires a clean, tightly regulated source of power. Therefore, it is strongly recommended that the system designer place at least one decoupling capacitor with a low ESR (effective series resistance) rating at each V_{DD} and OV_{DD} pin (and $L2OV_{DD}$ for the 360 CBGA) of the 750. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should range in value from 220pF to 10μF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated V_{DD} or OV_{DD} pins. Suggested values for the V_{DD} pins – 220pF (ceramic), 0.01μF (ceramic), and 0.1μf (ceramic). Suggested values for the OV_{DD} and $L2OV_{DD}$ pins – 0.01μF (ceramic), 0.1μf (ceramic), and 10μF (tantalum). Only SMT (surface-mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors – 100μF (tantalum) or 330μF (tantalum).

Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to V_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND, pins of the 750.

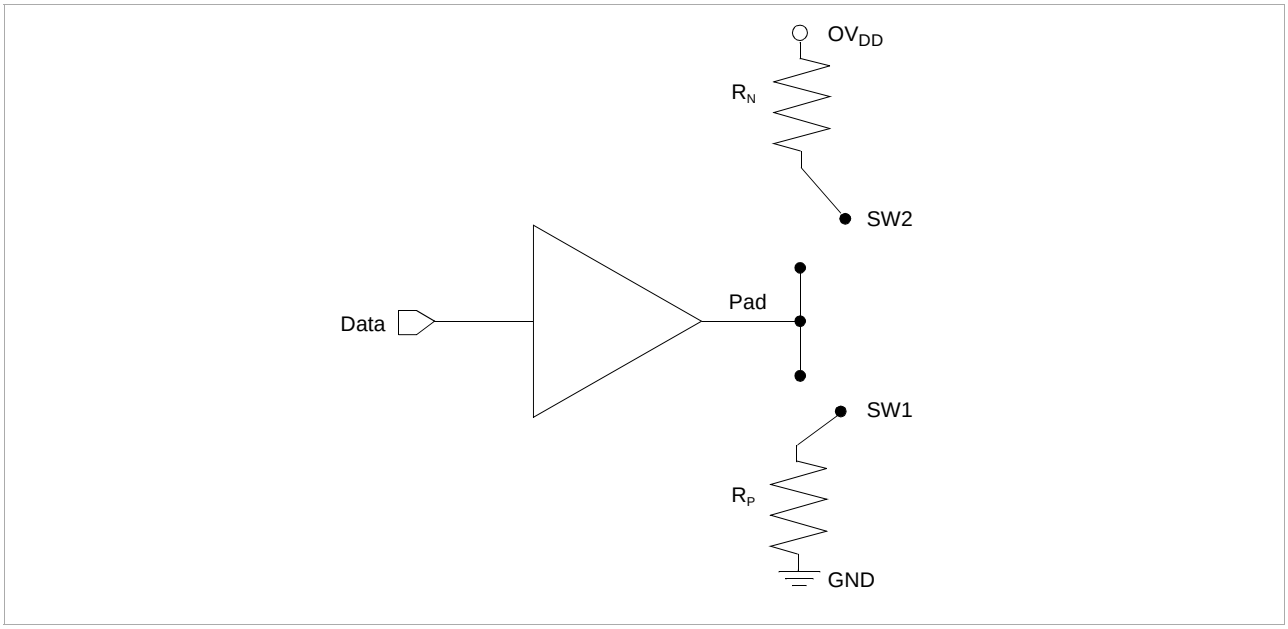
External clock routing should ensure that the rising edge of the L2 clock is coincident at the CLK input of all SRAMs and at the L2SYNC_IN input of the 750. The L2CLKOUTA network could be used only, or the L2CLKOUTB network could also be used depending on the loading, frequency, and number of SRAMs.

Output Buffer DC Impedance

The 750 60x and L2 I/O drivers were characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected to the chip pad, either to OV_{DD} or GND. Then the value of such resistor is varied until the pad voltage is $OV_{DD}/2$; see Figure 20, “Driver Impedance Measurement,” below.

The output impedance is actually the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW1 is closed (SW2 is open), and R_N is trimmed until Pad = $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW2 is closed (SW1 is open), and R_P is trimmed until Pad = $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. With a properly designed driver R_P and R_N are close to each other in value, then $Z_0 = (R_P + R_N)/2$.

Figure 20. Driver Impedance Measurement



The following table summarizes the impedance a board designer would design to for a typical process. These values were derived by simulation at 65°C. As the process improves, the output impedance will be lower by several ohms than this typical value.

Impedance Characteristics
V_{DD} = 1.9V, $L2OV_{DD}$=OV_{DD} = 3.3V, T_J = 65°C

Process	60x	L2	Symbol	Unit
Typical	43	38	Z_0	Ω

Pull-up Resistor Requirements

The 750 requires high-resistive (weak: 10KΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the 750 or other bus masters. These signals are: $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{TBST}$, $\overline{GBL}$, and $\overline{ARTRY}$.

In addition, the 750 has one open-drain style output ($\overline{CKSTP\_OUT}$) that requires a pull-up resistor (weak or strong: 4.7KΩ–1KΩ) if it is used by the system.

If address or data parity is not used by the system, it should be disabled using HID0. This also disables the parity input receivers. In most systems, the unused (and disabled) parity pins can be left unconnected; however, in some systems, these parity pins must be pulled up to OV_{DD} by a weak (or stronger) pull-up.

No pull-up resistors are normally required for the L2 interface, the 60x bus address and AP lines, or the 60x bus data and DP lines. The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus.

$\overline{HRESET}$ and $\overline{GBL}$ must be actively driven.

Resistor Pull-up / Pull-down Requirements

Required or Recommended Actions	Signals
Strong pull-up required	$\overline{CKSTP\_OUT}$
Weak pull-up required	$\overline{TLBISYNC}$, $\overline{LSSD\_MODE}$, L1_TSTCLK, L2TSTCLK, $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{ARTRY}$, $\overline{GBL}$, $\overline{TBST}$
Weak pull-up or pull-down required	TCK
Weak pull-up recommended	$\overline{SRESET}$, $\overline{SMI}$, $\overline{INT}$, $\overline{MCP}$, $\overline{CKSTP\_IN}$
Weak pull-up recommended if pin not used	AP[0:3], DP[0:3]

Errata Summary

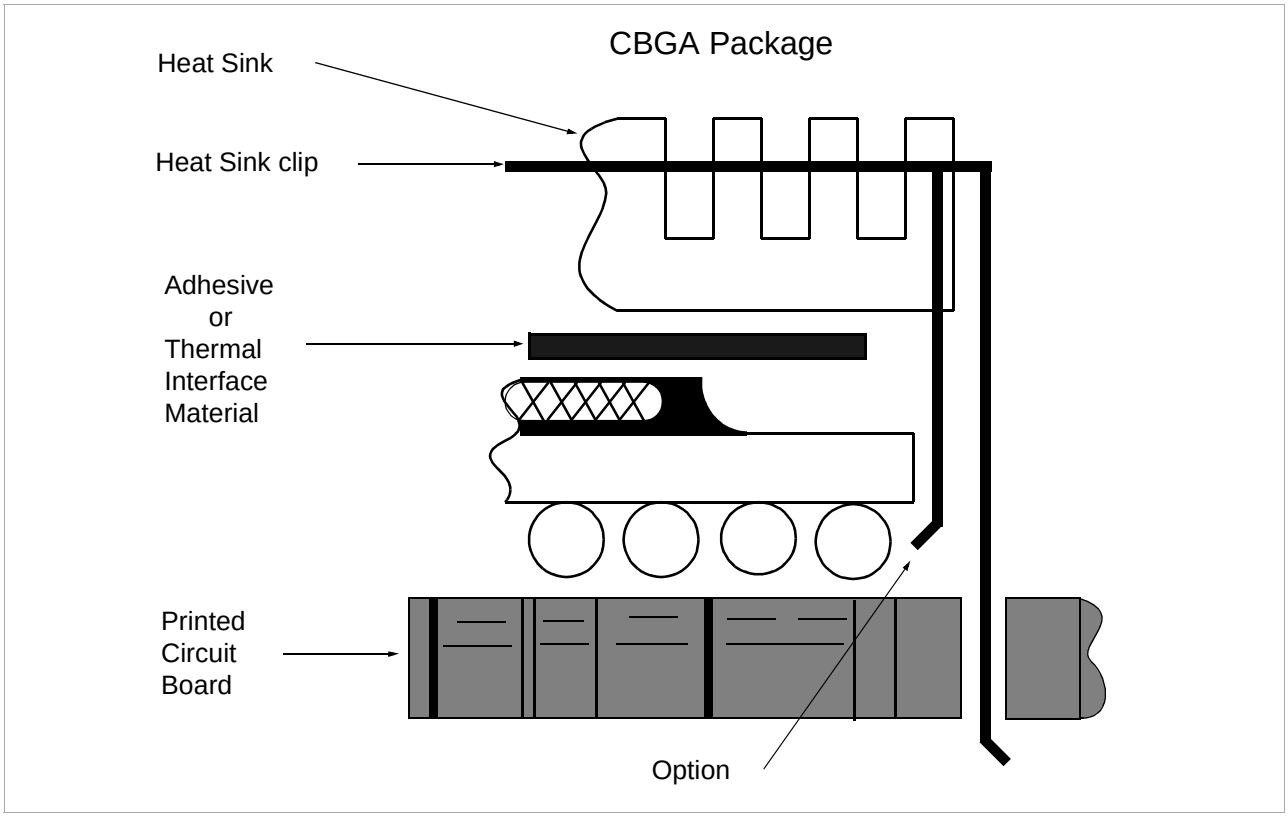
For errata details, see the PowerPC 750-PID 8p Microprocessor Errata List

#	Problem	Description	Impact	Solution(s)	Applies to Version 3.2
1	L2 cache invalidate may fail with DPM enabled.	If DPM is enabled during a global invalidate of the L2 cache, the global invalidate may not invalidate all the L2's tags.	Possible system failure after L2 initialization and start-up.	Turn DPM off during a L2 tag invalidate.	Yes
3	dcbz that hits in L1 cache may not retry snoop.	If a dcbz hits in the L1 cache, a snoop received at the same time to that address may not be serviced or get retried.	Stale data from system memory may be read by the other bus master, and the line may become valid in multiple caches.	Limit use of dcbz to data that is protected through software synchronization.	Yes
5	Segment register updates may corrupt data translation.	mtsr<in> followed by an instruction causing a page data address translation can cause contention for the segment registers.	Possible access to incorrect real address locations or false translation and data access exceptions.	Insert isync, sc, or rfi between andy mtsr<in> and instructions that cause a page data address translation.	Yes
8 (**Advisory**)	Stfd of uninitialized FPR can hang part.	A stfd will hang the part if its source FPR has powered up in a certain state.	Any system using a stfd.	Initialize all FPRs at POR.	Yes
11	Thermal Assist Unit (TAU) accuracy specification error in dd3.2 Datasheet	Actual TAU errors are different than those specificed.	If TAU reads higher than expected, false temperature alarms can occur. If TAU reads lower than expected, it can fail to signal a temperature alarm.	Re-evaluate system thermal design requirements and calibrate the TAU.	Yes

Thermal Management Information

This section provides thermal management information for the CBGA package for air cooled applications. Proper thermal control design is primarily dependent upon the system-level design; that is, the heat sink, air flow, and the thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly. See Figure 21.

Figure 21. Package Exploded Cross-Sectional View with Several Heat Sink Options



Maximum Heatsink Weight Limit for the 360 CBGA

Force	Maximum (pounds)
Dynamic Compression	10.0
Dynamic Tensile	2.5
Static Constant (Spring Force)	8.2

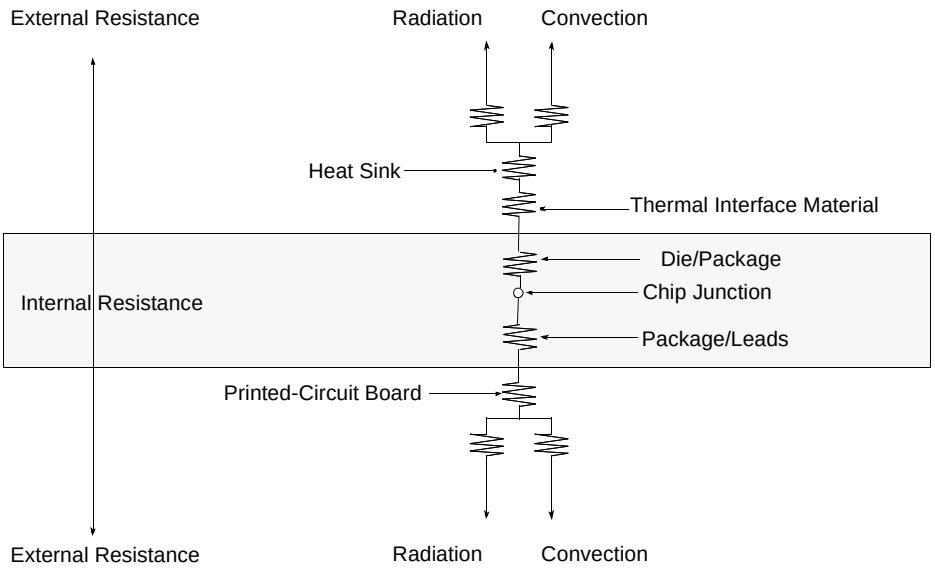
Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in ”Package Thermal Characteristics1,” on page 11, the intrinsic conduction thermal resistance paths are as follows.

- Die junction-to-case thermal resistance
- Die junction-to-ball thermal resistance

Figure 22 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 22. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



(Note the internal versus external package resistance.)

Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink; where it is removed by forced-air convection. Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

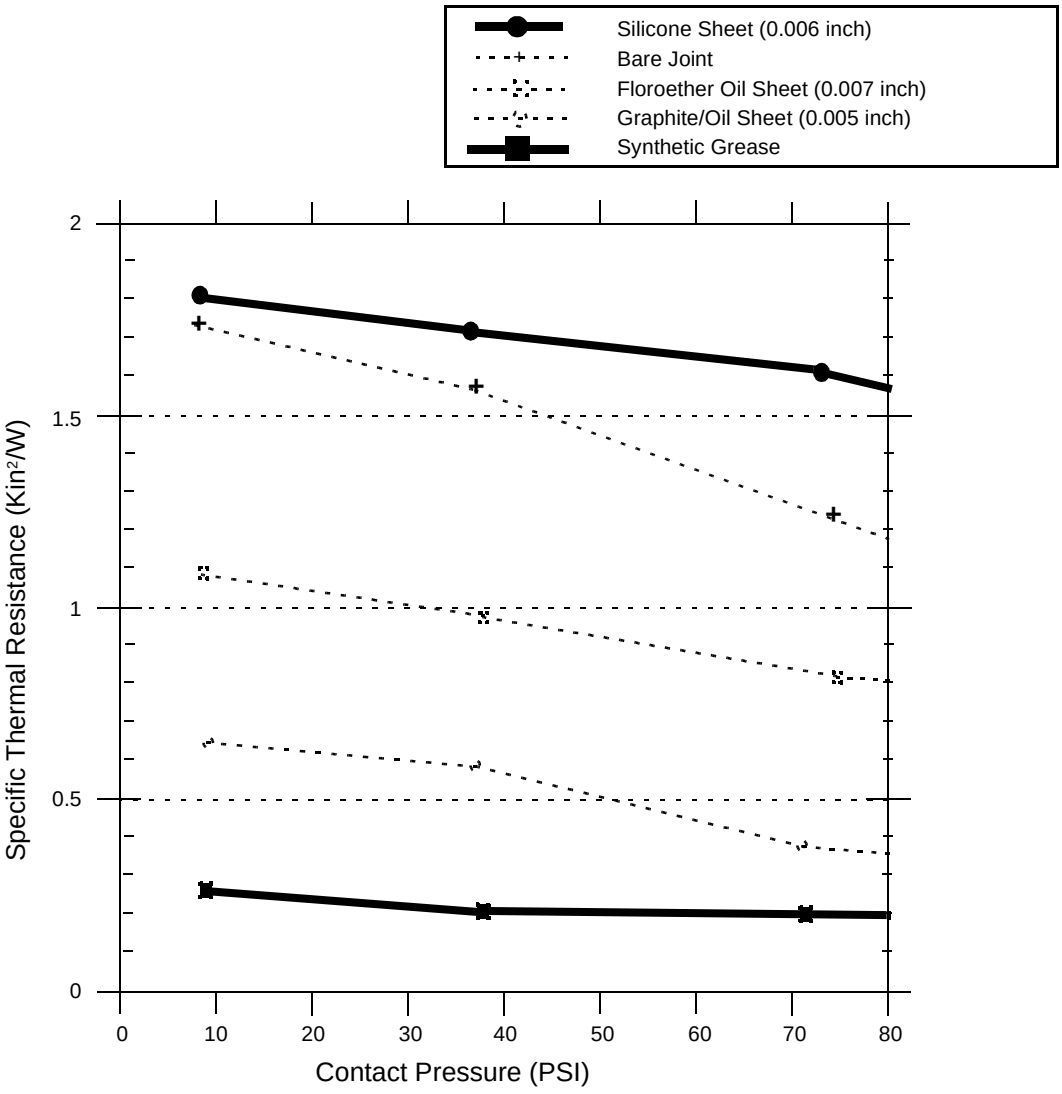
Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by a spring clip mechanism, Figure 23 shows the thermal performance of three thin-sheet thermal-interface materials (silicon, graphite/oil, flouroether oil), a bare joint, and a joint with thermal grease, as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal

resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 21). Therefore the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

Figure 23. Thermal Performance of Select Thermal Interface Material



Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements.

The following section provides a heat sink selection example using one of the commercially available heat sinks.

Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows.

$$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

Where:

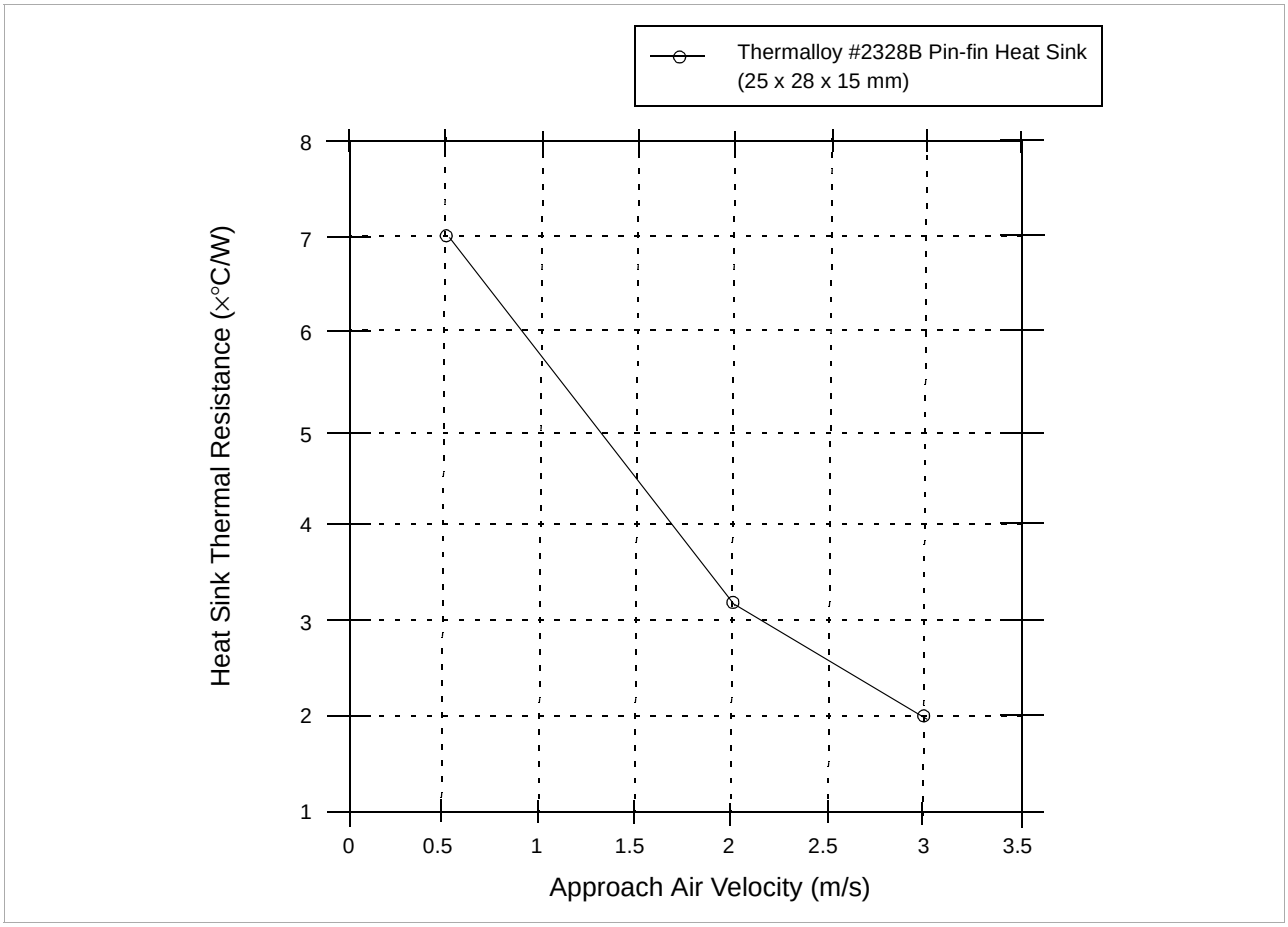
T_J is the die-junction temperature
T_A is the inlet cabinet ambient temperature
T_R is the air temperature rise within the system cabinet
θ_{JC} is the junction-to-case thermal resistance
θ_{INT} is the thermal resistance of the thermal interface material
θ_{SA} is the heat sink-to-ambient thermal resistance
P_D is the power dissipated by the device

Typical die-junction temperatures (T_J) should be maintained less than the value specified in Table “Package Thermal Characteristics1,” on page 11. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30 to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5 to 10°C. The thermal resistance of the interface material (θ_{INT}) is typically about 1°C/W. Assuming a T_A of 30°C, a T_R of 5°C, a CBGA package θ_{JC} = 0.03, and a power dissipation (P_D) of 5.0 watts, the following expression for T_J is obtained.

$$\text{Die-junction temperature: } T_J = 30°C + 5°C + (0.03°C/W + 1.0°C/W + \theta_{SA}) \times 5W$$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{SA}) versus air flow velocity is shown in Figure 24.

Figure 24. Thermalloy #2328B Pin-Fin Heat Sink-to-Ambient Thermal Resistance vs. Air flow Velocity



Assuming an air velocity of 0.5m/s, we have an effective θ_{SA} of 7°C/W, thus

$T_J = 30°C + 5°C + (.03°C/W + 1.0°C/W + 7°C/W) \times 4.5W,$

resulting in a junction temperature of approximately 71°C which is well within the maximum operating temperature of the component.

Other heat sinks are offered by other manufacturers.

Though the junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power dissipation, a number of factors affect the final operating die-junction temperature. These factors might include air flow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, next-level interconnect technology, system air temperature rise, etc.

Product Manufacturers

The following companies advertise thermal management products that may be of interest to PowerPC designers:

3M
http://www.3m.com

Aavid Thermal Technologies
Thermalloy
http://www.aavid.com/

The Berquist Company
http://www.bergquistcompany.com/

ChipCoolers
http://www.chipcoolers.com/

Chromerics, Division of Parker Hannifin Corporation
http://www.chomerics.com/

Dow Corning
http://www.dowcorning.com/

IERC (CTS Corporation)
http://www.ctscorp.com/

Loctite, A Henkel Company
http://www.loctite.com/

Power Devices, Incorporated
http://www.powerdevices.com/

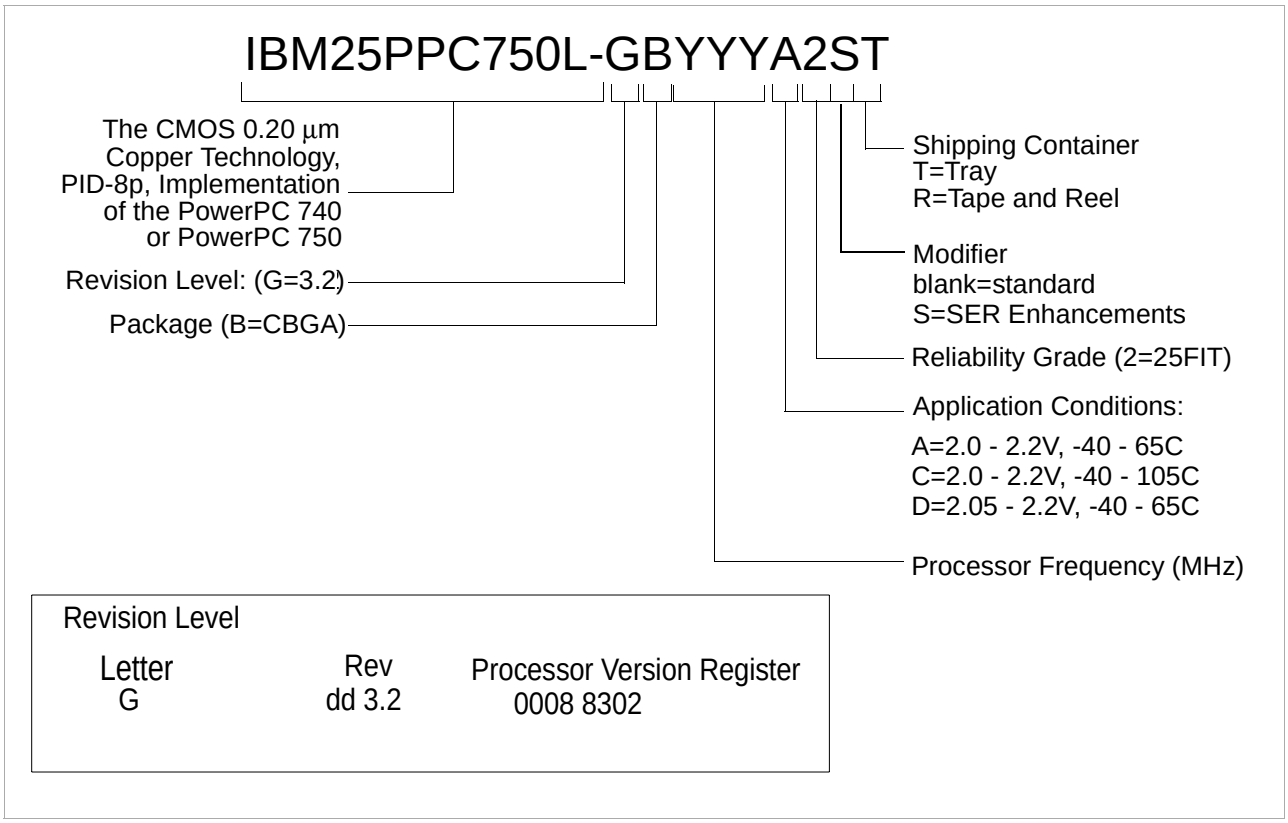
Thermagon, Inc.
http://www.thermagon.com/script/templates/default.asp

Wakefield Engineering
http://www.wakefield.com/

Ordering Information

This section provides the part numbering nomenclature for the 750. Note that the individual part numbers correspond to a maximum processor core frequency. For available devices contact your local IBM sales office.

Figure 25. Part Number Key



Inside of back cover

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