# IBM Microelectronics 486DX2 Common Socket Specification For 168 PGA Socket

## *Application Note*

### Overview

This document provides detailed information regarding the differences in pinouts between IBM 486DX/DX2, Intel® SL Enhanced™ 486DX/DX2 and Intel 486DX4 PGA devices and specifies electrical connections that allow a single motherboard design to support all of the devices listed. This specification is intended to be a guideline to eliminate conflicts due to pinout differences and does not address register or electrical (AC/DC) differences that may exist.

This common socket specification is intended to support the following 486 devices:

IBM 486DX/DX2
IBM 486DX/DX2-V
Intel SL Enhanced i486DX/DX2
IntelDX4

For additional 486DX/DX2 and 486DX/DX2-V information, please refer to the IBM 486DX/DX2 Data Book or contact IBM Microelectronics. Information in this document is subject to change without notification. The following documents were used as references for the Intel devices: SL Enhanced Intel486 Microprocessor Data Sheet Addendum, and IntelDX4 Processor Data Sheet. Any functions not disclosed in the referenced documents are NOT covered by the scope of this specification.

### CPU Features

Each of the CPU's supported in this common socket specification is 486 bus compatible yet has a unique set of features that impact the device pinout. Table 2-1 lists the differences in the CPU feature sets.

**Table 2-1 CPU Features**

| CPU | 5 VOLT SUPPLY | 3 VOLT SUPPLY (5 VOLT I/O) | WRITE-BACK CACHE | SMM | CPU POWER MANAGEMENT | CORE CLOCK CONTROL | JTAG |
|---|---|---|---|---|---|---|---|
| IBM 486DX/DX2 | X | | X | X | X | | |
| IBM 486DX/DX2-V | | X | X | X | X | | |
| Intel I486DX/DX2 SL Enhanced | X | | | X | X | | X |
| Intel DX4 | | X | | X | X | X | X |

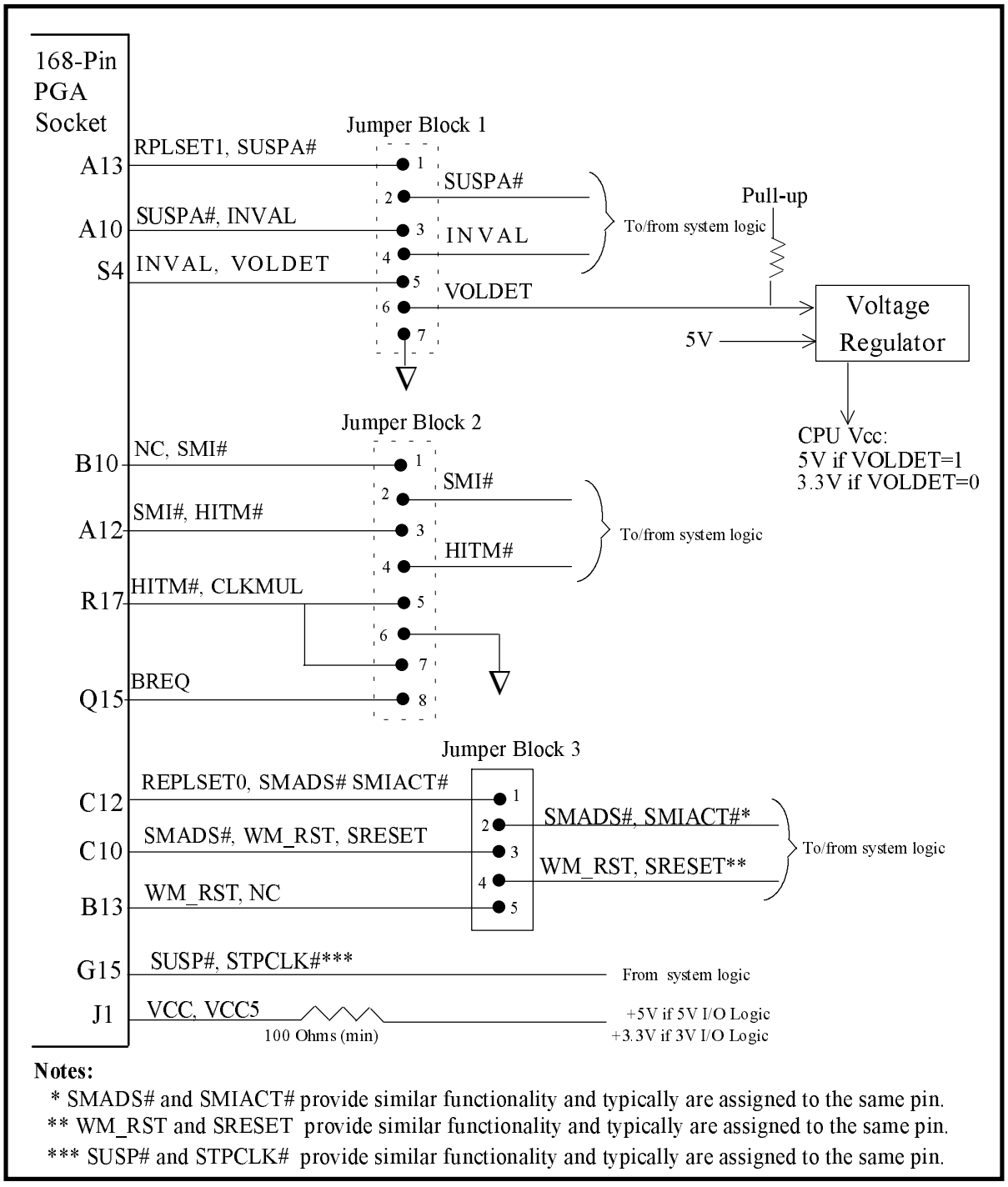
## Pin Differences

Table 3-1 lists those pins with signal assignments that are not consistent for all of the CPUs. Table 3-1 also specifies the appropriate connections for a common socket implementation. All pins that are not listed have identical signal assignments for all CPUs shown in the table. Therefore when implementing a common socket, all pins not listed should have identical connections to the system logic regardless of the CPU type.

**Table 3-1 CPU Pin Assignment**

| PIN NUMBER | SIGNAL NAME | | | | COMMON SOCKET IMPLEMENTATION |
|---|---|---|---|---|---|
| | 486DX, 486DX2 | 486DX-V 486DX2-V | i486DX, i486DX2 SL Enhanced | INTELDX4 | |
| A3 | NC | NC | TCK | TCK | No connection unless JTAG supported |
| A10 | SUSPA# | SUSPA# | NC | NC | Jumper block 1. |
| A12 | SMI# | SMI# | NC | NC | Jumper block 2. |
| A13 | RPLSET1 | RPLSET1 | NC | NC | Jumper block 1. |
| A14 | NC | NC | TDI | TDI | No connection unless JTAG supported |
| B10 | NC | NC | SMI# | SMI# | Jumper block 2. |
| B12 | TEST | TEST | NC | NC | No connection |
| B13 | WM_RST | WM_RST | NC | NC | Jumper block 3. |
| B14 | NC | NC | TMS | TMS | No connection unless JTAG supported |
| B16 | NC | NC | TDO | TDO | No connection unless JTAG supported |
| C10 | SMADS# | SMADS# | SRESET | SRESET | Jumper block 3. |
| C12 | RPLSET0 | RPLSET0 | SMIACT# | SMIACT# | Jumper block 3. |
| C13 | RPLVAL# | RPLVAL# | NC | NC | No connection |
| G15 | SUSP# | SUSP# | STPCLK# | STPCLK# | Connect to SUSP#/STPCLK# output from system logic. |
| R17 | HITM# | HITM# | NC | CLKMUL | Jumper block 2. |
| S4 | INVAL | INVAL | NC | VOLDET | Jumper block 1. |
| B7,B9,B11, C4,C5,E2,E16, G2,G16,H16, K2,K16, L16,M2, M16,P16, R3,R6,R8, R9,R10, R11,R14 | Vcc=5V | Vcc=3.3V | Vcc=5V | Vcc=3.3V | Connect to CPU Vcc output of power supply circuitry. CPU Vcc output of power supply circuitry should vary based on the VOLDET output of jumper block 1. All CPU Vcc pins should be connected in the board using a power plane. The CPU power plane should be electrically separated from the rest of the board's power plane so that the CPU can be powered independent of the system. |
| J1 | Vcc=5V | NC | Vcc=5V | Vcc5 | For 5V I/O logic, connect Vcc5 to 5V. For 3V I/O logic connect Vcc5 to 3.3V. |

A schematic for the common socket connections is shown in Figure 3-1. The corresponding jumper settings are listed in Table 3-2.




**Notes:**

* SMADS# and SMIACT# provide similar functionality and typically are assigned to the same pin.

** WM_RST and SRESET provide similar functionality and typically are assigned to the same pin.

*** SUSP# and STPCLK# provide similar functionality and typically are assigned to the same pin.

**Table 3-2. Jumper Settings**

| CPU | JUMPER BLOCK 1 | JUMPER BLOCK 2 | JUMPER BLOCK 3 |
|---|---|---|---|
| BL486DX/DX2 | 2-3, 4-5 | 2-3, 4-5 | 2-3, 4-5 |
| BL486DX/DX2-V | 2-3, 4-5, 6-7 | 2-3, 4-5 | 2-3, 4-5 |
| i486DX/DX2 | None | 1-2 | 1-2, 3-4 |
| IntelDX4 | 5-6 | 5-6 for 2X core,<br>7-8 for 2.5X core | 1-2, 3-4 |