Numeric Coprocessor 2C87

OVERVIEW

The IIT-2C87 is a high performance numerics processor extension that is plug and object-code compatible with the 80287. The IIT-2C87 is a low power CMOS device capable of operating at clock rates up to 20 MHz. The IIT-2C87 performs most of its functions in far fewer clock cycles than is required by the 80287. When combined with the faster clock frequency (the IIT-2C87 can operate on the

same clock as the 80286), the floating point processor achieves performance at least two times faster than the 80287. When used with an 80286 processor the computing system fully conforms to the IEEE Floating Point Standard. The IIT-2C87 is packaged in a 40-pin ceramic package.

Object code and plug compatible with the 80287 and 80C287A Low power CMOS device, ideal for lap-top	 Directly extends 80286 instructions set to incle trigonometric, logarithmic, exponential and arithmetic instructions 	ude
applications	☐ Full range transcendental operations for sine,	
High performance 80-bit internal architecture	cosine, tangent, arctangent and logarithm	
Implements ANSI/IEEE standard 754-1985 for	☐ Built-in exception handling	
binary floating point arithmetic	Operates in both real and protected mode of	
Up to 200% faster than the 80287	the 80286	
Upward object code compatible from 8087	☐ Thirty-two 80-bit numeric registers, 24 usable	as
Expands 80286 data types to include 32-, 64-,	3 banks of 8 register stacks	
80 bit floating point, 32-, 64-, bit integers and	☐ Built-in instruction to calculate 4x4 matrix	
18-digit BCD operands	transformation	
Available in 40-pin dual in-line package	Operates at clock rates up to 20 MHz (can use 80286 clock)	

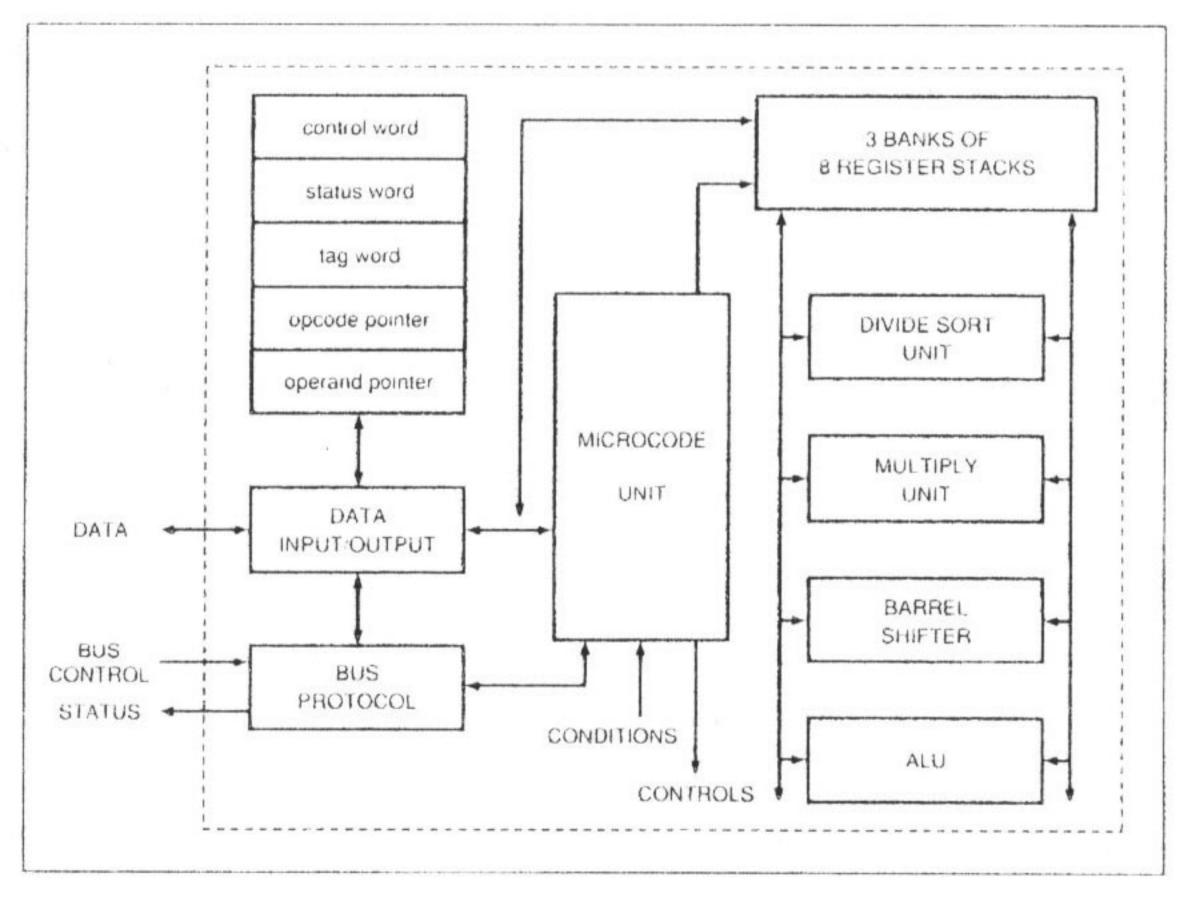


Figure 1. IIT-2C87 Block Diagram

NOF	Γ.	5	40	1
NCE			40	DNC.
NCE	5		39	□ CKM
NCE	3		38	DNC
NCC	4		37	DNC
D15 [5		36	PEACK
D14 [6		35	RESET
D13 [7		34	NPS1
D12 □	8		33	NPS2
Vcc [9		32	D CLK
VSS C	10	2C87	31	☐ CMD1
711	11		30	□ v _{ss}
D10 [12		29	CMD0
NC	13		28	NPWR
D9 [14		27	NPRD
D8 [15		26	ERROR
D7 [16		25	BUSY
D6 [17		24	PEREQ
05 🗆	18		23	D0
D4 []	19		22	D D1
D3 [20		21	D2

Figure 2. 2C87 Pin Configuration

2C87 Numeric Coprocessor

ENHANCED PERFORMANCE

In addition to operating at clock speeds up to 20 MHz, the IIT-2C87 requires far fewer clock cycles than the 80287 in Instruction execution. Table 1 compares the range of clock cycles required to perform typical floating point instructions.

CLOCK CYCLES REQUIRED							
INSTRUCTION	IIT-2C87	80287					
ADD	15-17	70-100					
MPY	19	90-145					
DIV	48	193-203					
SQRT	49	180-186					
COMPARE	17	40-50					
REM	58	15-190					
TAN	196	30-540					
LOG	235	900-1100					

FUNCTIONALITY

The IIT-2C87 is object code and plug compatible with the 80287. The IIT-2C87 includes all of the instructions of the 80287. In addition the IIT-2C87 provides all the 80387 instructions and enhancements (SIN, COS, IEEE COMPARE, IEEE REMAINDER, larger range for transcendental functions).

The IIT-2C87 provides extra functions which are not available on the 80287.

There are thirty-two 80-bit floating point registers, 24 of which are usable as 3 banks of register stacks.

The IIT-2C87 includes a built-in instruction to calculate a 4x4 matrix transformation. This results in the capability to perform matrix transformations 6 to 8 times faster than the 80287.

FEATURES:

CMOS IMPLEMENTATION

The IIT-2C87 numeric co-processor is implemented in advanced 1.2 micron CMOS technology. The device dissipation is typical at 0.5 Watt. The advantages of low power 1.2 micron CMOS implementation include higher reliability and enhanced system performance. The IIT-2C87

is capable of operating at clock frequencies up to 20 MHz.

The device may be operated using the 80286 clock.

The IIT-2C87 is ideally suited for LAP-TOP computer.

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