80C196NU, 83C196NU SPECIFICATION UPDATE

Release Date: July, 1997
Order Number: 272864-003

The 80C196NU, 83C196NU may contain design defects or errors known as errata. Characterized errata that may cause the 80C196NU, 83C196NU's behavior to deviate from published specifications are documented in this specification update.

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REVISION HISTORY

Rev. Date	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.
10/21/96	002	Deleted specification changes 002, 003, and 005, and deleted documentation change 009–013 and 015. (These changes were incorporated into revision -003 of the datasheet.) Added specification changes 006, 007, and 008. Added documentation changes 020, 021, 022, and 023.
6/5/97	003	Deleted documentation changes 023, 024 and deleted specification changes 006, 007 and 008. (These changes were incorporated into Revision - 004 of the data sheet). Added document change 025.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
8XC196NP, 80C196NU Microcontroller User's Manual	272644-002
8XC196NU Commercial CHMOS 16-Bit Microcontroller datasheet	272479-004

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8XC196NU product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark)
or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page): Page location of item in this document.

Status

Doc: Document change or update will be implemented.

Fix: This erratum is intended to be fixed in a future step of the component.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Eval: Plans to fix this erratum are under evaluation.

Row

| Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

REV. Date	80C196NU Stepping							83C196NU Stepping		Page	Status	ERRATA
	A-0	A-1	A-2	A-3	B-0	B-1	B-2	B-0	B-3			
9600001	X									9	Fixed	Incoming Interrupt While Interrupt Pending Register Is Being Read
9600002	X	X		X				X	X	9	Fixed	HOLD#, HLDA# Repeated Data Cycles
9600003	X	X	X	X				X	X	9	Fixed	HOLD#, HLDA# Corrupted Data
9600004	X	X	X	X						10	Fixed	Jump Instructions at 64KB Page Boundary
9600005	X	X	X	X						10	Fixed	EBR Instruction at 64KB Page Boundary in 1MB Mode
9600006	X	X	X	X						11	Fixed	Illegal Opcode Interrupt Vector
9600007	X	X	X	X						11	Fixed	Register 02H
9600008	X	X	X	X						11	Fixed	WR#/WRH# Timing Mismatch
9600009	X	X	X	X	X			X	X	12	Fixed	HOLD#, HLDA# Assertion Window
9600010	X	X	X		X	X		X		12	Fixed	Exiting Powerdown
9600011	X	X	X	X	X	X	X	X	X	13	Fix	64-Kbyte Addressing Mode with Multiplexed Bus
9600012	X	X	X	X	X	X	X	X	X	13	NoFix	Single Source Multiplication Using the Accumulator

Specification Changes

Number	80C196NU Stepping							83C196NU Stepping		Page	Status	Specification Changes
	A-0	A-1	A-2	A-3	B-0	B-1	B-2	B-0	B-3			
001		X	X	X	X	X	X	X	X	14	Doc	PLLEN1 Pullup Removed
004					X	X	X	X	X	14	Doc	PFSTOP Logic Removed

Specification Clarifications

Number	80C196NU Stepping							83C196NU Stepping		Page	Status	Specification Clarifications
	A-0	A-1	A-2	A-3	B-0	B-1	B-2	B-0	B-3			
001	X	X	X	X	X	X	X	X	X	15	Doc	BREQ# Signal
002	X	X	X	X	X	X	X	X	X	15	Doc	HLDA# Signal
003	X	X	X	X	X	X	X	X	X	15	Doc	HOLD# Signal
004	X	X	X	X	X	X	X	X	X	15	Doc	RESET# Signal
005	X	X	X	X	X	X	X	X	X	15	Doc	RPD Signal
006	X	X	X	X	X	X	X	X	X	16	Doc	Indirect Addressing with Autoincrement
007	X	X	X	X	X	X	X	X	X	17	Doc	Reserved Memory Locations

Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
001	272479-002	18	Doc	Indirect Addressing With the Stack Pointer
002	272479-002	18	Doc	Stack Operation
003	272479-002	18	Doc	Counter Overflow Interrupt
004	272479-002	19	Doc	PSW Overflow Flag Values for DIV and DIVB
005	272479-002	19	Doc	PLLENx Values Are Reversed
006	272479-002	20	Doc	Serial Port Control and Status Registers
007	272479-002	20	Doc	TIJMP Instruction Must Use Long-Indexed Addressing
008	272479-002	21	Doc	Shift Instructions
014	272479-002	22	Doc	Count Register for Block Move (BMOVI and EBMOVI) Cannot Be Windowed
016	272479-002	22	Doc	Special-purpose Memory Addresses
017	272479-002	22	Doc	ONCE Mode Pin Status
018	272479-002	24	Doc	Reading the EPA_PEND Register
019	272479-002	27	Doc	83C196NU QFP Package Designator
020	272479-002	25	Doc	Port 2 SFR Addresses
021	272479-002	25	Doc	Generating an External Reset
022	272479-002	25	Doc	Generating a Hardware Reset
025	272479-003	25	Doc	System Bus Timings

IDENTIFICATION INFORMATION

Markings

80C196NU

A-1 has no marking at the end of the topside tracking number.

A-3 step denoted by “A” at the end of the topside tracking number.

B-1 step denoted by “B” at the end of the topside tracking number.

B-2 step denoted by “C” or “D” at the end of the topside tracking number.

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B-0 has no marking at the end of the topside tracking number.

B-3 step denoted by “E” at the end of the topside tracking number.

ERRATA

9600001. Incoming Interrupt While Interrupt Pending Register Is Being Read

PROBLEM: When an interrupt occurs while the interrupt pending register is being read, the interrupt pending register is not updated. As a result, the incoming interrupt is never acknowledged.

IMPLICATION: Interrupts occurring while the interrupt pending register is being read will not be acknowledged.

WORKAROUND: Disable interrupts before reading the interrupt pending register.

```
DI

LDB  TEMP,INT_PEND

EI
```

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600002. HOLD#, HLDA# Repeated Data Cycles

PROBLEM: The problem occurs when an instruction that results in an external data access is the last instruction in the queue prior to assertion of HLDA#. This sequence allows the queue to be emptied of instructions with a data access pending. Since data accesses have priority, the bus controller does not receive a request for an instruction fetch, leaving the instruction queue empty. This results in uninterruptible repeating of external data cycles.

IMPLICATION: The HOLD#, HLDA# feature is unreliable.

WORKAROUND: None

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600003. HOLD#, HLDA# Corrupted Data

PROBLEM: The problem occurs when an instruction that results in an external data access is the last instruction in the queue prior to assertion of HLDA#. This sequence allows the queue to be emptied of instructions with a data access pending. Undefined data from the data bus is loaded.

IMPLICATION: The HOLD#, HLDA feature is unreliable.

WORKAROUND: None

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600004. Jump Instructions at 64KB Page Boundary

PROBLEM: Any jump, conditional jump, or call instruction located within six bytes of the top of any 64K page boundary (e.g., 1FFFAH-1FFFFH) may cause a jump to the wrong page.

When an jump instruction with a negative offset lies across a page boundary (instruction begins on one page, executes on the next page, and jumps back to the first page), the page number is decremented one page too many.

Example: Current instruction code fetch crosses from page F1xxxxH to F2xxxxH and executes a short jump back to page F1xxxxH. The error causes the jump to go to page F0xxxxH.

IMPLICATION: SJMP, LJMP, SCALL, LCALL, and conditional jump instructions located near a page boundary will not function properly.

WORKAROUND: Do not place SJMP, LJMP, SCALL, LCALL, and conditional jump instructions within 6 bytes of a page boundary (e.g., FFFA-FFFFH). Place 6 NOPs at the top of each page.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600005. EBR Instruction at 64KB Page Boundary in 1MB Mode

PROBLEM: Execution of the EBR instruction across a page boundary results in an extra code fetch at the address formed by the lower 16 bits of the branch destination address and the upper 4 bits of the address of the beginning byte of the instruction.

IMPLICATION: While fetching an EBR instruction that crosses a page boundary, an extra prefetch to an improper address occurs, but does not affect proper code flow. For example, if an EBR instruction is located across the page boundary at FFxxxxH and 00xxxxH and branches to page F1yyyyH, an extra instruction fetch will occur with address 00yyyyH.

WORKAROUND: Do not place EBR instructions near page boundaries. Place 6 NOPs at top of each page (e.g., FFFA-FFFFH).

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600006. Illegal Opcode Interrupt Vector

PROBLEM: The illegal opcode interrupt should be generated when there is an attempt to execute an undefined opcode, and should vector to address FF2012H to handle the interrupt. But in 1-Mbyte mode only, the vector address for the illegal opcode interrupt is not generated correctly and a random vector address is generated.

IMPLICATION: Code that executes an illegal opcode (10h or E5h) will vector to a random address.

WORKAROUND: Use a C-compiler or Assembler that will flag the illegal opcode or put a reset opcode (FFh) at the end of any data tables or unused memory locations.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600007. Register 02H

PROBLEM: The ONES_REG, location 02H, was nonfunctional in early steppings.

IMPLICATION: Code expecting register 02H to contain the constant FFFFH will not operate properly.

WORKAROUND: Do not use register 02H for the constant FFFFH.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600008. WR#/WRH# Timing Mismatch

PROBLEM: When in 8-bit demultiplexed bus mode, the WR# and WRH# signals do not assert at the same time with two instructions (STB and XCHB) when accessing external memory.

IMPLICATION: STB and XCHB instructions executed while in 8-bit demultiplexed bus mode will not assert WR# and WRH# at the same time.

WORKAROUND: Use external logic to AND the WR# and WRH# signals.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600009. HOLD#, HLDA# Assertion Window

PROBLEM: When an external device asserts HOLD# within a window near the falling edge of CLKOUT (approximately 1 nanosecond wide), the 8XC196NU asserts HLDA# and continues to perform the current bus cycle. When the 8XC196NU asserts HLDA#, its address and control lines float, so the data that it reads depends on how the external device drives the bus. The result is that the 8XC196NU reads invalid data or an invalid instruction

IMPLICATION: The HOLD#, HLDA feature is unreliable.

WORKAROUND: Synchronize the external device's assertion of HOLD# with the rising edge of CLKOUT. This will ensure that the 8XC196NU does not assert HLDA# until the current bus cycle is complete.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600010. Exiting Powerdown

PROBLEM: The EXTINTx signals used to return from powerdown are edge-triggered inputs, not level-sensitive as the documentation states. That is, a transition must occur to cause an action. If an EXTINTx signal is high when the microcontroller enters powerdown or standby, the system must deassert the EXTINTx signal to cause the microcontroller to resume normal operation.

When the microcontroller is in powerdown mode, asserting EXTINTx for at least 50 ns will not always cause it to resume normal operation as stated in the documentation. If a single transition occurs on EXTINTx during the time that IDLPD instruction is executing, the 8XC196NU can miss the edge and remain in standby or powerdown.

During powerdown or standby, a transition on any EXTINTx pin causes the 8XC196NU to exit the power-saving mode and return to normal operation, even if the pin is configured as general-purpose I/O.

If the EXTINTx pin is configured as a special-function signal and interrupts are enabled, a rising edge will cause the microcontroller to exit powerdown and process the interrupt service routine; a falling edge will cause the microcontroller to exit powerdown and process the next instruction (the interrupt service routine will not be processed). If the EXTINTx pin is configured as a special-function signal and interrupts are disabled, or if the EXTINTx pin is configured as a general-purpose I/O, any transition will cause the microcontroller to exit powerdown and process the next instruction.

IMPLICATION: Systems must be designed to account for edge-triggered EXTINTx inputs in order to return from powerdown.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600011. 64-Kbyte Addressing Mode with Multiplexed Bus

PROBLEM: When using 64-Kbyte addressing mode and a multiplexed bus with either 8- or 16-bit bus widths, the 8XC196NU fails coming out of reset. Soon after the 8XC196NU comes out of reset (around address 0FF2094h), the CS0# deasserts and the 8XC196NU fails. This only occurs when using 64KB addressing with a multiplexed bus.

IMPLICATION: The NU cannot be used in 64KB mode with a multiplexed bus.

WORKAROUND: Use 1-Mbyte addressing mode, or use 64-Kbyte mode with a demultiplexed bus.

STATUS: Fix. Refer to Summary Table of Changes to determine the affected stepping(s).

9600012. Single Source Multiplication Using the Accumulator

PROBLEM: Multiplication operations that use the accumulator and a single source operand do not function properly. This applies to both signed (MUL) and unsigned (MULU) multiplication.

When bit 3 of the destination address is clear (address 00H, 01H, …, 07H), the result of the multiplication is not added to the accumulator. Instead, the original value of the accumulator is retained, as though no multiplication operation has occurred.

When the destination address is either 08H or 09H, the value 03C0H is placed into the accumulator, regardless of the values being multiplied.

IMPLICATION: Single-source multiplication using the accumulator requires special handling.

WORKAROUND: To clear the accumulator before storing the result of the multiplication operation, use a destination address with both bit 3 and bit 1 set (0AH, 0BH, 0CH, 0DH, 0EH, 0FH). To add the result of the multiplication to the existing value of the accumulator, use a double-source multiplication instruction. For example, to obtain the expected result of “MULU 04H, #4H” use the following instructions:

```
LD             TEMP_REG, ACC_00   ;load value of accumulator into temporary register
MULU      04H, TEMP_REG, #4H      ;multiply TEMP_REG by 4 and place result into
                                  ; accumulator
```

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

001. PLLEN1 Pullup Removed

PROBLEM: The weak pullup resistor on the PLLEN1 pin was removed to reduce power consumption during powerdown.

IMPLICATION: The PLLEN1 pin will now need to be driven high or low.

004. PFSTOP Logic Removed

PROBLEM: On older MCS® 96 Microcontrollers, PFSTOP is asserted for one state whenever there is a change in bus width. This caused the next instruction prefetch to be inhibited long enough to adjust the slave program counter to account for the new bus width. On the 8XC196NU, the chip-select unit automatically adjusts for the change in bus width, so there is no need to halt the prefetch. This logic to stop the prefetch for one cycle was deactivated on the A steppings and was removed entirely in B0.

IMPLICATION: None.

SPECIFICATION CLARIFICATIONS

001. BREQ# Signal

PROBLEM: This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. When the bus-hold protocol is enabled (WSR.7 is set), the P2.3/BREQ# pin can function only as BREQ#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared).

002. HLDA# Signal

PROBLEM: This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD#. When the bus-hold protocol is enabled (WSR.7 is set), the P2.6/HLDA# pin can function only as HLDA#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared).

003. HOLD# Signal

PROBLEM: An external device uses this active-low input signal to request control of the bus. When the bus-hold protocol is enabled (WSR.7 is set), the P2.5/HOLD# pin can function only as HOLD#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared).

004. RESET# Signal

PROBLEM: In the powerdown, standby, and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. If the phase-locked loop (PLL) clock circuitry is enabled, you must hold RESET# low for at least 2 ms to allow the PLL to stabilize before the internal CPU and peripheral clocks are enabled.

005. RPD Signal

PROBLEM: If your application uses an external interrupt input to return to normal operation from powerdown mode, and the phase-locked loop (PLL) circuitry is enabled (see PLLEN2:1 signal description), connect a capacitor between RPD and V_{SS}. The capacitor is used to establish a delay of at least 2 ms to allow the PLL circuitry to stabilize before the internal CPU and peripheral clocks are enabled.

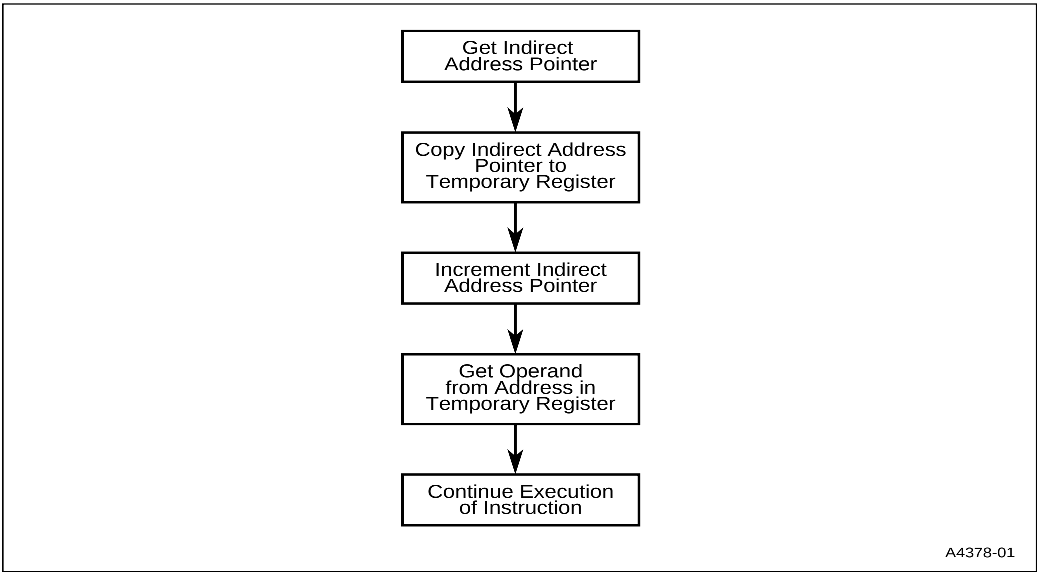
If your application uses powerdown mode, but the phase-locked loop (PLL) circuitry is disabled, the capacitor is not required.

If your application does not use the powerdown mode, leave the RPD pin unconnected.

006. Indirect Addressing with Autoincrement

PROBLEM: For indirect addressing with autoincrement, a pointer that points to itself results in an access to the incremented pointer address rather than the original pointer address.

The CPU stores the pointer's value in a temporary register, increments the pointer, then accesses the operand at the address contained in the temporary register, as shown in this flowchart.


Get Indirect Address Pointer
Copy Indirect Address Pointer to Temporary Register
Increment Indirect Address Pointer
Get Operand from Address in Temporary Register
Continue Execution of Instruction
A4378-01

Therefore, if the pointer points to itself, the CPU accesses the operand at the incremented address contained in the pointer.

For example, assume ax = 1CH and bx = 40H. The following code causes the CPU to access the operand at the incremented address:

```
ld     ax,#ax
ldb    bx,[ax]+

ld     1CH,#1CH;1CH ( 1CH;load location 1CH with value 1CH
ldb    40H,[1CH]+;temp ( 1CH;save 1CH into temp register
             ;1CH ( 1DH;increment the contents of 1CH
             ;40H ( 1DH;load the contents of location 1CH (location 1CH
                     ;now contains the value 1DH) into 40H
```

007. Reserved Memory Locations

PROBLEM: Customers should not use reserved memory locations on the 8XC196NU. While many locations are reserved for future use, others are used internally by Intel. The values in reserved memory are subject to change without notice; therefore, reserved locations should not be used as references of any kind.

DOCUMENTATION CHANGES

001. Indirect Addressing With the Stack Pointer

ITEM: Page 4-9, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

The explanatory comments for the PUSH [SP] instruction are incorrect. The stack pointer is decremented by 2, not incremented by 2 in this instruction. The correct text is as follows:

```
PUSH [SP]    ; duplicate top of stack
             ; SP ← SP – 2
```

002. Stack Operation

ITEM: Page 4-13, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

The stack order shows the low word of param2 pushed onto the stack before the high word. This is reversed. The correct stack order is as follows:

```
param3
high word of param2
low word of param2
undefined;param1
return address              ← stack pointer
```

003. Counter Overflow Interrupt

ITEM: Page 10-6, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

The counter-overflow interrupt pending bit is also set when 0FFFFH or 0000H is loaded directly into the counter. An actual transition from 0FFFEH to 0FFFFH when counting up or a transition from 0001H to 0000H when counting down is not required for the interrupt to occur.

004. PSW Overflow Flag Values for DIV and DIVB

ITEM: Page A-4, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

The "V Flag Set if Quotient Is" values are incorrect for the DIV and DIVB instructions. The correct values for all divide instructions are as follows:

Instruction	Quotient Stored in:	V Flag Set if Quotient is:
DIVB	Short Integer	< -127 or > +128 (<81 H or > 80H)
DIV	Integer	< -32767 or > +32768 (< 8001H or > 8000H)
DIVUB	Byte	>255 (>FFH)
DIVU	Word	>65535 (>FFFFH)

005. PLLENx Values Are Reversed

ITEM: Page 12-13, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

In the table on page 12-13, the values for PLLENx to achieve the various phase-locked loop (PLL) modes are incorrect. The correct values are as follows:

PLLEN2	PLLEN1	Mode
0	0	Clock-multiplier circuitry disabled.
1	0	Reserved. **CAUTION:** This combination causes the device to enter an unsupported test mode.
0	1	Doubled; clock doubling circuitry enabled. Internal clock is twice the XTAL1 input.
1	1	Quadrupled; clock quadrupling circuitry enabled. Internal clock is four times the XTAL1 input.

006. Serial Port Control and Status Registers

ITEM: Page 8-2, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

In Table 8-2, the fields that describe programming of P1_DIR and P2_DIR are incorrect. The correct text is as follows:

P1_DIR	This register selects the direction of each port 1 pin. To use T1CLK as the input clock to the baud-rate generator, **set** P1_DIR.4.
P2_DIR	This register selects the direction of each port 2 pin. **Set** P2_DIR.1 to configureRXD (P2.1) as a high-impedance input/open-drain output, and **clear** P2_DIR.0 to configure TXD (P2.0) as a complementary output.

007. TIJMP Instruction Must Use Long-Indexed Addressing

ITEM: Page A-57, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

TIJMP cannot be executed using direct or immediate addressing as stated in Table 8. TIJMP can be executed only using long-indexed addressing; it is a 4-byte instruction with opcode E2H.

Mnemonic	Direct		Immediate		Indirect		Indexed	
	Length	Opcode	Length	Opcode	Length	Opcode	Length S/L	Opcode
TIJMP	----	----	----	----	----	----	----/4	E2

008. Shift Instructions

ITEM: Page A-59, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

The shift instructions can be executed using immediate addressing. The instruction lengths and opcodes are the same as those for direct addressing.

Shift								
Mnemonic	**Direct**		**Immediate**		**Indirect**		**Indexed**	
	Length	**Opcode**	**Length**	**Opcode**	**Length**	**Opcode**	**Length**	**Opcode**
NORML	3	0F	3	0F	----	----	----	----
SHL	3	09	3	09	----	----	----	----
SHLB	3	19	3	19	----	----	----	----
SHLL	3	0D	3	0D	----	----	----	----
SHR	3	08	3	08	----	----	----	----
SHRA	3	0A	3	0A	----	----	----	----
SHRAB	3	1A	3	1A	----	----	----	----
SHRAL	3	0E	3	0E	----	----	----	----
SHRB	3	18	3	18	----	----	----	----
SHRL	3	0C	3	0C	----	----	----	----

013. External Memory Interface Signals

ITEM: Pages 13-3 and 13-5, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

In Table 13-2, the "Multiplexed With" column contains incorrect information for the BHE# and WRH# signals. The BHE# and WRH# signals are multiplexed with one another, but are not multiplexed with P5.5. (The 8XC196NP and 8XC196NU have no port 5.) For the BHE# signal, the "multiplexed with" column should contain only WRH#. For the WRH# signal, the "multiplexed with" column should contain only BHE#.

014. Count Register for Block Move (BMOVI and EBMOVI) Cannot Be Windowed

ITEM: Pages A-10 and A-16, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

For the BMOVI or EBMOVI instruction, the count register (CNTREG) cannot be windowed; therefore, it must reside in the lower register file.

016. Special-purpose Memory Addresses

ITEM: Page 5-6, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

Some of the addresses listed in Table 5-3 are incorrect for the NU. The NU has the same Special-purpose Memory Addresses as the NP. The corrected table appears below.

8XC196NP/8XC196NU Address (Hex)	Description
FF207F – FF205E	Reserved (each byte must contain FFH)
FF205D – FF2040	PTS Vectors
FF203F – FF2030	Upper interrupt vectors
FF202F – FF201B	Reserved (each byte must contain FFH)
FF201A	CCB1
FF2019	Reserved (must contain 20H)
FF2018	CCB0
FF2017 – FF2014	Reserved (each byte must contain FFH)
FF2013 – FF2000	Lower interrupt vectors

017. ONCE Mode Pin Status

ITEM: Pages B-13 and B-14, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

The table found in the user's manual does not include data for the 80C196NU in ONCE mode. This information is found in the new table below.

Table 1. 8XC196NP and 80C196NU Pin Status

Port Pins	Alternate Functions	During RESET# Active	Upon RESET# Inactive (Note 11)	Idle	Powerdown (NP/NU) and Standby (NU only)	Hold	Bus Idle	ONCE
P1.3:0	EPA3:0	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P1.4	T1CLK	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P1.5	T1DIR	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P1.6	T2CLK	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P1.7	T2DIR	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P2.0	TXD	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P2.1	RXD	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P2.2	EXTINT0	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P2.3	BREQ#	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P2.4	EXTINT1	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P2.5	HOLD#	WK1	WK1	(Note 1)	(Note 1)	Force 0	----	HiZ
P2.6	HLDA#	WK1	WK1	(Note 1)	(Note 1)	0	----	HiZ
P2.7	CLKOUT	CLKOUT active; LoZ0/1	CLKOUT active; LoZ0/1	(Note 1)	(Note 2)	(Note 1)	----	HiZ
P3.0	CS0#	WK1	1 (NP only) 0 (NUonly)	(Note 3)	(Note 3)	(Note 4)	----	HiZ
P3.5:1	CS5:1#	WK1	WK1	(Note 3)	(Note 3)	(Note 4)	----	HiZ
P3.6	EXTINT2	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P3.7	EXTINT3	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P4.2:0	PWM2:0	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
P4.3	----	WK1	WK1	(Note 1)	(Note 1)	(Note 1)	----	HiZ
EPORT.3:0	A19:A16	WK1	1	(Note 5)	(Note 5)	(Note 6)	(Note 8)	WK1
----	A15:0	WK1	LoZ0	(Note 7)	(Note 7)	(Note 7)	LoZ0	WK1
----	AD15:0	WK1	LoZ0	(Note 7)	(Note 7)	(Note 7)	LoZ0	WK1
----	ALE	WK0	0	(Note 9)	(Note 9)	WK0	LoZ0	HiZ
----	BHE#	WK1	1	(Note 10)	(Note 10)	WK1	LoZ1	HiZ
----	EA#	HiZ	HiZ	HiZ	HiZ	HiZ	----	HiZ
----	INST	WK0	0	(Note 9)	(Note 9)	WK0	LoZ0	HiZ
----	NMI	WK0	WK0	WK0	WK0	WK0	----	WK0
----	ONCE	MD0	MD0	MD0	MD0	MD0	----	WK0
----	PLLEN1 (NU only)	HiZ	HiZ	HiZ	HiZ	HiZ	----	HiZ

Table 1. 8XC196NP and 80C196NU Pin Status (Continued)

Port Pins	Alternate Functions	During RESET# Active	Upon RESET# Inactive (Note 11)	Idle	Powerdown (NP/NU) and Standby (NU only)	Hold	Bus Idle	ONCE
----	PLLEN2 (NU only)	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ
----	RD#	WK1	1	(Note 10)	(Note 10)	WK1	LoZ1	HiZ
----	READY	WK1	WK1	WK1	WK1	WK1	----	WK1
----	RESET#	0	WK1	WK1	WK1	WK1	----	HiZ
----	RPD	LoZ1	LoZ1	LoZ1	LoZ1	LoZ1	----	HiZ
----	WR#	WK1	1	(Note 10)	(Note 10)	WK1	LoZ1	HiZ
XTAL1	----	Osc input, HiZ	Osc input, HiZ	Osc input, HiZ	Osc input, HiZ	Osc input, HiZ	----	HiZ
XTAL2	----	Osc output, LoZ0/1	Osc output, LoZ0/1	Osc output, LoZ0/1	HiZ	Osc output, LoZ0/1	----	Osc output, LoZ0/1

018. Reading the EPA_PEND Register

ITEM: Pages 10-22, 10-23, *8XC196NP, 80C196NU Microcontroller User’s Manual* (272479-002)

After the EPA_PEND register is read directly by the user’s code, the EPA_PEND register bits are cleared. If these bits need to be preserved for use again after the initial read, the user’s code must save the value of the EPA_PEND register.

020. Port 2 SFR Addresses

ITEM: Page 7-3, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

Table 7-3 shows incorrect addresses for port 2 special-function registers (SFRs). The correct addresses, listed below, are shown on page 5-8 and page C-3. This change will be included in the next revision of the user's manual.

P2_DIR	1FD3H
P2_MODE	1FD1H
P2_PIN	1FD7H
P2_REG	1FD5H

021. Generating an External Reset

ITEM: Page 11-10, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

The third sentence of the first paragraph on page 11-10 will be clarified in the next revision of the user's manual to read as follows:

RESET# should remain asserted for at least one state time after Vcc, **the oscillator, and the phase-locked loop (PLL) circuitry** have stabilized and met the operating conditions specified in the datasheet.

022. Generating a Hardware Reset

ITEM: Page 12-8, *8XC196NP, 80C196NU Microcontroller User's Manual* (272479-002)

The second sentence of the paragraph in section 12.5.3.1 will be corrected in the next revision of the user's manual to read as follows:

The device will exit powerdown if RESET# is asserted. If the phase-locked loop circuitry is **disabled** or if the design uses an external clock input signal rather than the on-chip oscillator, RESET# must remain low for at least 16 state times. If the design uses the on-chip oscillator, then RESET# must be held low until the oscillator and phase-locked loop circuitry have stabilized.

025. System Bus Timings

ITEM: Pages 30 and 34, 8XC196NU Commercial CHMOS 16-Bit Microcontroller (272644-004).

The READY timing figures for multiplex and demultiplex bus are swapped. Figure 10 shows demultiplex figure and figure 12 shows multiplex figure.