8XC196EA Microcontroller

Specification Update

November, 1998

Notice: The 8XC196EA microcontrollers may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 272872-006

Contents

Revision History

Date	Version	Description
07/11/98	006	Added Errata 24 and 25. Changed document title to *8XC196EA Microcontroller Specification Update* to reflect inclusion of the 80C196EA and the 83C196EA microcontrollers. Corrected status marking for Errata 22. Added C-1 stepping information to the Summary Table of Changes.
06/25/98	005	Added Errata 22 and 23. Added Specification Changes 8 through 12.
03/15/98	004	Added Document Changes 22 - 29. Added Specification Clarification 7.
12/16/97	003	Added Document Changes 16 through 21.
07/01/97	002	Added Errata 16 through 21. Added Specification Changes 1 through 7. Added Specification Clarifications 1 through 6. Added Document Changes 1 through 15.
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order #
83C196EA CHMOS 16-Bit Microcontroller datasheet (Automotive)	272788
80C196EA CHMOS 16-Bit Microcontroller datasheet	273153
83C196EA Microcontroller User's Manual	272804

Nomenclature

Errata are design defects or errors. These may cause the 80C196EA/83C196EA microprocessor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 80C196EA/83C196EA microprocessor product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings				Page	Status	ERRATA
	A	B	C	C-1			
1	X				8	Fixed	Incorrect A/D Channels Converted
2	X				8	Fixed	P5.4 Pullup Not Disabled During ONCE Mode (I/O three-state)
3	X				9	Fixed	A/D Scan Mode Does Not Function
4	X				9	Fixed	A/D Inaccuracy
5	X				9	Fixed	Serial Port Default Baud Rate 4800 Baud in Test ROM Mode
6	X				10	Fixed	PTS Block Move
7	X				10	Fixed	TIJMP / PIH Missed Interrupts
8	X				10	Fixed	On-Chip RISM “next” Commands
9	X				10	Fixed	SDU Interrupt on Branch with Wait States
10	X				10	Fixed	WR# Active Low on Falling Edge of ALE
11	X				11	Fixed	P2.6 Pullup
12	X				11	Fixed	Emulator CLKE Pin Inactive During Reset
13	X				11	Fixed	Emulator Peripheral Interrupt Handler Conflict
14	X				11	Fixed	Emulator Missed Data Match
15	X				11	Fixed	READY# Function Not Enabled in ICE Mode
16	X	X			12	Fixed	Interrupts Lost Due to Read from PIH-Index Register
17	X	X			12	Fixed	Interrupts Lost Due to Read from PIH-Pending Register
18	X	X			12	Fixed	PIH Interrupt Lost Due to Dummy Interrupt
19	X	X			12	Fixed	PIH PTS Interrupt Lost Due to Dummy Interrupt
20	X	X	X	X	12	NoFix	NMIE Interrupt Lost when PIH Interrupt Pending
21	X	X	X	X	12	NoFix	NMI Interrupt Lost when NMIE Interrupt Pending
22	X	X	X		13	Fixed	Reset During Code RAM Read Operation
23	X	X	X	X	13	No Fix	RSTSRC Register Clear on VCC Powerup
24	X	X	X		13	Fixed	VCC Powerup Code RAM Integrity
25				X	13	No Fix	Reset During Code RAM Write Operation

Specification Changes

No.	Steppings				Page	Status	SPECIFICATION CHANGES
	A	B	C	C-1			
1			X		14	Doc	Nomenclature Overview
2			X		14	Doc	DC Characteristics at VCC = 4.5 V - 5.5 V
3			X		15	Doc	AC Characteristics - Multiplexed Bus Mode
4			X		16	Doc	AC Characteristics - Demultiplexed Bus Mode
5			X		17	Doc	AC Characteristics - Synchronous Serial Port
6			X		17	Doc	AC Characteristics - A/D Converter, 8-Bit Mode
7			X		17	Doc	External Clock Drive
8			X		18	Doc	DC Characteristics at VCC = 4.5 V - 5.5 V
9			X		18	Doc	AC Characteristics - Multiplexed Bus Mode
10			X		18	Doc	AC Characteristics - Demultiplexed Bus Mode
11			X		18	Doc	AC Characteristics - Synchronous Serial Port
12			X		18	Doc	Nomenclature Change

Specification Clarifications

No.	Steppings				Page	Status	SPECIFICATION CLARIFICATIONS
	A	B	C	C-1			
1	X	X	X	X	19	Doc	PLLEN Pin Must be Held Low along with the ONCE# Pin to Enter On-Circuit Emulation Mode
2	X	X	X	X	19	Doc	T2CLK can be Used for the External Clock for the Serial I/O Baud Rate Generator Input (not T1CLK)
3	X	X	X	X	19	Doc	IOH2 Units are in µA, not mA
4	X	X	X	X	19	Doc	IOH3 Units are in µA, not mA
5	X	X	X	X	19	Doc	IOH3 is the Output High Current in Reset on Port 11 (not Port 12)
6	X	X	X	X	19	Doc	IDLPD Illegal Keys are Any Value >3 (not >2)
7	X	X	X	X	20	Doc	A/D Accuracy in Auto Scan Mode

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	272788-002	21	Doc	Page 2, Table 1
2	272788-002	21	Doc	Pages 7 through 14, Table 4
3	272788-002	21	Doc	Pages 17 and 18, Table 6
4	272788-002	22	Doc	Pages 19 and 20, Table 7
5	272788-002	22	Doc	Pages 23 and 24, Table 9
6	272788-002	22	Doc	Page 29, Table 11
7	272788-002	22	Doc	Page 29, Figure 10
8	272788-002	23	Doc	Page 31, Table 13
9	272788-002	23	Doc	Page 33, Table 15
10	272788-002	23	Doc	Page 34, Table 16
11	272804-001	23	Doc	Page 13-12, Section 13.6.3
12	272804-001	23	Doc	Page 14-11, First Paragraph
13	272804-001	24	Doc	Page A-20, IDLPD Description
14	272804-001	24	Doc	Page B-8, ONCE# Pin Description
15	272804-001	24	Doc	Page B-10, PLLEN Pin Description
16	272804-001	24	Doc	Page 2-18, Figure 2-9
17	272804-001	25	Doc	Page 6-6, Table 6-3
19	272804-001	25	Doc	Page 9-19, Figure 9-10
18	272804-001	25	Doc	Page 9-17, Section 9.4.2.4
20	272804-001	25	Doc	Page 9-22, Section 9.5.3
21	272804-001	25	Doc	Page 9-23, section 9.5.4
22	272788-003	26	Doc	Page 15, Table 5
23	272804-001	26	Doc	Page 11-16, Figure 11-11, Timer x Control (TxCONTROL) Register
24	272804-001	26	Doc	Page 11-8, Section 11.3, Timer/Counter Functional Overview
25	272804-001	27	Doc	Page 6-3, Figure 6-2 Interrupt Service Flow Diagram
26	272804-001	27	Doc	Page 12-9, Figure 12-5 A/D Command (AD_COMMAND)_Register
27	272804-001	27	Doc	Page 12-11, Section 12.5, Determining A/D Status and Conversion Results
28	272804-001	27	Doc	Page 16-6, Section 16.3.3, Minimizing Latency
29	272804-001	28	Doc	Page 11-7, Figure 11-2, EPA Timer/Counters

Identification Information

Markings

Bottom mark: AS83C196EA, S80C196EA.

Errata

1. Incorrect A/D Channels Converted

Problem: PROBLEM: Bits 0 and 1 and bits 2 and 3 of the A/D channel decoder were incorrectly swapped. This causes a different channel than expected to be converted. For example, writing the A/D command register bits ACH3-ACH0 with 0001B will cause channel 2 to be converted instead of the expected channel 1.

Implication: Mapping of A/D channels differs from intended design.

Workaround: Use the table below to find what value written to the A/D command register corresponds to the desired actual channel conversion.

Write A/D Command Register (ACH3-ACH0)	Converts Channel/Pin	
	A-Step	B-Step
0	0	0
1	2	1
2	1	2
3	3	3
4	8	4
5	10	5
6	9	6
7	11	7
8	4	8
9	6	9
10	5	10
11	7	11
12	12	12
13	14	13
14	13	14
15	15	15

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

2. P5.4 Pullup Not Disabled During ONCE Mode (I/O three-state)

Problem: During ONCE mode, P5.4 is actively pulled up. ONCE mode is used to electrically isolate the component during testing or programming of other devices connected to an application (most often external EPROM or flash memories).

Implication: Any device that expects P5.4 to be three-stated in ONCE mode will instead see a logic ‘1’ driven on P5.4. Since P5.4 is typically not used for interfacing to external memories, this erratum is not expected to impact the intended usage of ONCE mode.

Workaround: If this pin needs to be three-stated during ONCE mode, the user must supply an isolation buffer/device.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

3. A/D Scan Mode Does Not Function

Problem: A-step scanning could get stuck on one channel for some V_{CC}/Temp conditions.

Implication: A/D scan mode is not usable.

Workaround: Use an interrupt service routine to read a channel result and start an A/D conversion on the next desired channel.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

4. A/D Inaccuracy

Problem: The analog-to-digital converter on the 8XC196EA is a successive approximation type. There is a resistor ladder with 255 taps that are used to directly generate the first 8 bits of the conversion. A capacitive voltage divider is used with the resistor ladder to generate the two LSBs. The upper 8 bits of the result directly address the ladder; the lower two bits select another ladder tap, which is capacitively summed with the tap selected by the upper 8 bits.

As a conversion starts, the result register is loaded with 10 0000 0000b**.** This selects the middle tap of the ladder. A binary search is then performed to find the voltage that most closely matches the sampled voltage. For example, if the voltage is greater than the midpoint, tap 11 0000 0000b will be tried next. If not, 01 0000 0000b will be tested.

Inaccuracy on the 8XC196EA A-step

The analog-to-digital converter has exhibited an inaccuracy of about 6 LSBs with missed codes throughout the operating range. The missed codes are systematic in that the two LSBs always appear to return 11; thus, codes ending in 00, 01, and 10 tend to be missed.

Implication: The root cause was traced to a layout error in which signals in the analog portion of the converter were incorrectly wired. This error caused the selected test voltage to **decrease** as the two LSBs of a 10-bit conversion incremented from 00 to 11. Thus, when the current voltage being tested was within about 4 LSBs of (but less than) the sampled voltage, the A/D would incorrectly continue the search lower than the current point.

Workaround: None

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

5. Serial Port Default Baud Rate 4800 Baud in Test ROM Mode

Problem: The default baud rate for the serial port in test-ROM execution mode is 4800 baud (should be 9600 baud).

Implication: Default baud rate of most tools is 9600 baud. This erratum causes a baud rate of 4800 baud, requiring changes to tools (emulators, etc.) from the normal convention.

Workaround: External devices must connect at 4800 baud and may use RISM calls to set the EA baud rate register to 9600 baud (or other speeds desired).

Status: Fixed. Intended fix on B-step. Refer to Summary Table of Changes to determine the affected stepping(s).

6. PTS Block Move

Problem: It was found that the PTS block move routine always updated the destination pointer, regardless of the state of the DU bit in the PTS control block. This was traced to an error in the microcode for the PTS block move instruction and has been fixed.

Implication: PTS block move is not usable on the A-step.

Workaround: None

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

7. TIJMP / PIH Missed Interrupts

Problem: If an interrupt to a PIH block occurs at the same time as the PIH_VEC_IDX SFR is being read, the interrupt will be lost. The root cause was found to be a signal to load the PIH interrupt pending register occurred one state too early. This caused the slave pending register to be loaded from the master at the same time as interrupts were being cleared from the slave due to the read of PIH_VEC_IDX SFR.

Implication: Interrupts may be missed under above described conditions.

Workaround: Intended fix on B-step. The fix was to delay the transfer from master to slave when the PIH_VEC_IDX SFR is being read.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

8. On-Chip RISM “next” Commands

Problem: The test ROM code that implements the “next” form (write_next_byte, ...) of the RISM commands incorrectly tested the wrong bit to decode “next” commands from standard commands (write_byte).

Implication: “Next” RISM commands (in test ROM mode) do not work correctly.

Workaround: Use only standard RISM commands write_word, write_byte, read_word, read_byte.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9. SDU Interrupt on Branch with Wait States

Problem: The SDU is able to generate an interrupt breakpoint based on an address match. If the breakpoint is located in memory that is accessed with wait states, and the breakpoint location is a branch instruction, the breakpoint will not be detected.

Implication: The SDU breakpoint detection does not work if the breakpoint is on a branch instruction and is located in memory using wait states.

Workaround: None. Do not set SDU breakpoints on branch instructions.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

10. WR# Active Low on Falling Edge of ALE

Problem: The EA bus controller has the ability to dynamically change its external bus width and type (6/8 bit bus and multiplexed/demultiplexed types). For the first 8-bit demultiplexed bus cycle following a 16-bit multiplexed bus cycle, the WR# signal incorrectly goes low on the falling edge of ALE on the A-step instead of near the rising edge of ALE.

Implication: In systems that interface to both 16-bit multiplexed and 8-bit demultiplexed memory devices, the 8XC196EA presents the WR# signal to the external memory devices for a shorter period of time than expected.

Workaround: None.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

11. P2.6 Pullup

Problem: By holding certain pins on the 8XC196EA low/high upon reset, test modes can be entered. To prevent unwanted entry into these modes, the pins are typically pulled up/down on reset. On the A-step, P2.6 was weakly pulled high. Design methodology dictates that this pin should have a medium pullup. It is important to note, however, that no test mode entry problems have been observed.

Implication: None expected. Improvement made to match design methodology for more secure prevention of unwanted test mode entry.

Workaround: None.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

12. Emulator CLKE Pin Inactive During Reset

Problem: During reset, the CLKE signal is inactive on the A-step.

Implication: Affects in-circuit emulator designs only.

Workaround: Emulator dependent.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

13. Emulator Peripheral Interrupt Handler Conflict

Problem: When the 8XC196EA in-circuit emulation circuitry (ICE) is enabled, there is a bus conflict between the peripheral interrupt handlers and the ICE.

Implication: Affects in-circuit emulator designs only. Interrupts from the PIHs will not work on the A-step.

Workaround: None.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

14. Emulator Missed Data Match

Problem: For some locations, ICE breakpoint circuitry looking for a data match does not get internally transferred correctly, resulting in a missed data match.

Implication: Affects in-circuit emulator designs only. Breakpoint on data will not work correctly in all cases.

Workaround: None.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

15. READY# Function Not Enabled in ICE Mode

Problem: Upon ICE mode entry, the READY# pin/function was incorrectly not enabled on the A-step.

Implication: Affects in-circuit emulator designs only. Since READY# is usually reconstructed, this errata is expected to have little effect.

Workaround: Emulator initialization software needs to configure the port pin P5.6/READY# for system function.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

16. Interrupts Lost Due to Read from PIH-Index Register

Problem: When the PIH-index register is read from at the same time as an interrupt occurs, the new interrupt is lost. The PIH-index register is accessed during a TIJMP instruction.

Implication: Interrupts may be missed under above described conditions.

Workaround: Do not use the TIJMP instruction as an interrupt polling method.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

17. Interrupts Lost Due to Read from PIH-Pending Register

Problem: When the PIH interrupt pending register is read from at the same time as an interrupt occurs, the new interrupt is lost.

Implication: Interrupts may be missed under above described conditions.

Workaround: None.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

18. PIH Interrupt Lost Due to Dummy Interrupt

Problem: When a PIH interrupt occurs, at the same time as a dummy interrupt, the PIH interrupt will be lost and will never be serviced.

Implication: Interrupts may be missed under above described conditions.

Workaround: None.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

19. PIH PTS Interrupt Lost Due to Dummy Interrupt

Problem: When a PIH PTS interrupt occurs at the same time as a dummy interrupt, the PIH PTS interrupt will be lost and will never be serviced.

Implication: Interrupts may be missed under above described conditions.

Workaround: None.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

20. NMIE Interrupt Lost when PIH Interrupt Pending

Problem: When a PIH interrupt is pending, a NMIE interrupt will not be serviced. Instead, the pending PIH interrupt will be serviced even if it is globally disabled.

Implication: Interrupts will be incorrectly serviced under above described conditions. Affects in-circuit emulator designs only.

Workaround: None.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

21. NMI Interrupt Lost when NMIE Interrupt Pending

Problem: When a NMIE interrupt occurs with a NMI interrupt pending, the NMI pending bit will be erroneously cleared without being serviced.

Implication: Interrupts may be missed under above described conditions. Affects in-circuit emulator designs only.

Workaround: None.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

22. Reset During Code RAM Read Operation

Problem: During the time that the device is reading data from code RAM, a code RAM corruption may occur if:

- a device reset occurs from a falling edge on the RESET# pin
- a watchdog time-out event occurs or
- a clock fail detect event occurs

Implication: Code RAM data corruption may occur as a result of the reset event.

Workaround: Prevent external resets, watchdog time-out events, and clock fail detect events from occurring during a code RAM read operation if code RAM data integrity must be maintained after the reset event.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

23. RSTSRC Register Clear on V_{CC} Powerup

Problem: The four least-significant bits in the RSTSRC register (CFDRST, WDTRST, SFWRST, and EXTRST) are supposed to be cleared when V_{CC} is powered up. These bits may get erroneously set on V_{CC} powerup and cannot be guaranteed to be cleared.

Implication: Applications which are relying on these bits to be cleared on V_{CC} power-up may be adversely affected.

Workaround: None.

Status: No Fix. Refer to Summary Table of Changes to determine the affected stepping(s).

24. V_{CC} Powerup Code RAM Integrity

Problem: During the time that the core V_{CC} is powered down and back up (while CRV_{CC} is maintained at 5 V), code RAM corruption may occur.

Implication: Code RAM integrity cannot be relied upon when the device is powered down while CRV_{CC} is maintained at 5 V.

Workaround: None

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

25. Reset During Code RAM Write Operation

Problem: During the time that the device is writing data to code RAM, a code RAM corruption may occur if:

- a device reset occurs from a falling edge on the RESET# pin
- a watchdog time-out event occurs or
- a clock fail detect event occurs

Implication: Code RAM data corruption may occur as a result of the reset event.

Workaround: Prevent external resets, watchdog time-out events, and clock fail detect events from occurring during a code RAM write operation if code RAM data integrity must be maintained after the reset event.

Status: No Fix. Refer to Summary Table of Changes to determine the affected stepping(s).

Specification Changes

1. Nomenclature Overview

Issue: Added 80C196EA Device.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 1, Description of Product Nomenclature:

- Program Memory Options - Added Options “0” and Description “CPU only - no internal ROM”

Parameter	Options	Description
Program Memory Options	3	Internal ROM
	0	CPU only - no internal ROM

2. DC Characteristics at V_{CC} = 4.5 V - 5.5 V

Issue:

- TBD values in Table 6 changed to real values
- Added I_{CRVCC} specification
- Loosened minimum limits for I_{OH2}

Implication: Applications designed to the old I_{OH2} specification may be affected.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 6, DC Characteristics at V_{CC}=4.5 V - 5.5 V:

- I_{REF} - Max - Changed from TBD to 5
- Added I_{CRVCC} row
- I_{OH2} - Min - Changed from -75 to -65 and -90 to -75; all Units changed to µA
- I_{OH3} -Parameter - Changed to Port 11; Min changed from TBD to -5, -8 and -10; all Units changed to µA

Sym	Parameter	Min	Typ	Max	Units	Test Conditions
I_{REF}	A/D reference supply current			5	mA	XTAL1 = 40 MHz $V_{CC} = V_{REF}$ = 5.5 V Device in Reset
I_{CRVCC}	Code RAM V_{CC} Supply Current			110	µA	V_{CC}=5.5 V
I_{OH2}	Output high current in reset	–30 –65 –75		–120 –240 –280	µA µA µA	$V_{OH2} = V_{CC} – 1.0$ V $V_{OH2} = V_{CC} – 2.5$ V $V_{OH2} = V_{CC} – 4.0$ V
I_{OH3}	Output high current in reset on Port 11	–5 –8 –10		–50 –110 –130	µA µA µA	$V_{OH3} = V_{CC} – 1.0$ V $V_{OH3} = V_{CC} – 2.5$ V $V_{OH3} = V_{CC} – 4.0$ V

3. AC Characteristics - Multiplexed Bus Mode

Issue:

- Minimum specification for frequency changed from 16 MHz to 20 MHz
- T_{RLRH} and T_{CHWH} specifications loosened for better manufacturability

Implication: Applications designed to the old minimum T_{RLRH} specification may be affected.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 7, AC Characteristics - Multiplexed Bus Mode:

- F_{XTAL1} 1x Min changed to 20, 2x Min changed to 10
- f Min changed to 20
- t Max changed to 50
- T_{RLRH} Min changed to t-12
- T_{CHWH} Max changed to 10
- Note 1 changed to 20 MHz

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	20	40	MHz (1, 8)
	Frequency on XTAL1, PLL in 2x mode	10	20	MHz (8)
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	20	40	MHz (8)
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
t	Period, t = 1/f	25	50	ns
T_{RLRH}	RD# Low to RD# High	t – 12		ns (2)
T_{CHWH}	CLKOUT High to WR# Rising Edge	– 10	10	ns (9)

NOTE:
1. 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.

4. AC Characteristics - Demultiplexed Bus Mode

Issue:

- Minimum specification for frequency changed from 16 MHz to 20 MHz to reflect manufacturing test conditions
- T_{CHCL}, T_{CLLH}, T_{RLRH}, T_{WLWH} and T_{AVYV} loosened for better manufacturability

Implication: Applications designed to the minimum T_{RLRH} and T_{WLWH} specifications may be affected.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 9, AC Characteristics - Demultiplexed Bus Mode:

- F_{XTAL1} 1x Min changed to 20, 2x Min changed to 10
- f Min changed to 20
- t Max changed to 50
- T_{CHCL} Min changed to t-10, Max changed to t+10
- T_{CLLH} Min changed to -10, Max changed to 10
- T_{RLRH} Min changed to 3t-12
- T_{WLWH} Min changed to 3t-15
- T_{AVYV} Min changed to 3t-25
- Note 1 changed to 20 MHz

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	20	40	MHz (1,8)
	Frequency on XTAL1, PLL in 2x mode	10	20	MHz (8)
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	20	40	Mhz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
t	Period, t = 1/f	25	50	ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 10	ns (9)
T_{CLLH}	CLKOUT Falling ALE Rising	– 10	10	ns (9)
T_{RLRH}	RD# Low to RD# High	3t – 12		ns (2)
T_{WLWH}	WR# Low to WR# High	3t – 15		ns (2)
T_{AVYV}	A20:0 Valid to READY Setup		3t – 25	ns (4)

NOTE:
1. 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.

5. AC Characteristics - Synchronous Serial Port

Issue: TBD value for T_{D1DV} changed to real value.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 11, Synchronous Serial Port Timing:

- T_{D1DV} - Min changed from TBD to 2t

Symbol	Parameter	Min	Max	Units
T_{D1DV}	**Setup time for MSB output**	2t		ns

6. AC Characteristics - A/D Converter, 8-Bit Mode

Issue: A/D DC input leakage corrected to reflect manufacturing test conditions.

Implication: Applications that cannot handle negative leakage on A/D input pins may be affected.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 15, 8-Bit Mode A/D Characteristics Over Specified Operating Conditions:

- DC Input Leakage - Typical changed to ±100, Min changed to -300

Parameter	Typical (2)	Min	Max	Units (1)	Notes
DC Input Leakage	±100	-300	300	nA	8

7. External Clock Drive

Issue:

- Minimum oscillator frequency changed from 8 MHz to 10 MHz to reflect manufacturing test conditions
- Minimum specification for frequency changed from 16 MHz to 20 MHz to reflect manufacturing test conditions

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 16, External Clock Drive:

- $1/T_{XLXL}$ - Min changed to 10
- T_{XLXL} Max changed to 100
- Note 1 - 16 MHZ changed to 20 MHz

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency (F_{XTAL1})	10	40 (1)	MHz (2)
T_{XLXL}	Oscillator Period (T_{XTAL1})	25	100	ns

NOTE:
1. 20 MHz is the maximum input frequency when using an external crystal oscillator; however, 40 MHz can be applied with an external clock source.

8. DC Characteristics at V_{CC} = 4.5 V - 5.5 V

Issue: I_{CC} and I_{IDLE} at 40 MHz loosened for better manufacturability.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788

From/To Ref: I_{CC} Max changed from 135 mA to 140 mA.
I_{IDLE} Max changed from 95 mA to 100 mA.

9. AC Characteristics - Multiplexed Bus Mode

Issue: T_{RLDV}, T_{LLAX}, T_{RLAZ} and T_{QVWH} loosened for better manufacturability. T_{WHQX} tightened to meet customer specifications.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788

From/To Ref: T_{RLDV} Max changed from t-18 ns to t-23 ns.
T_{LLAX} Min changed from t-15 ns to t-16 ns.
T_{RLAZ} Max changed from 5 ns to 7 ns.
T_{QVWH} Min changed from t-14 ns to t-15 ns.
T_{WHQX} Min changed from t-20 ns to t-16 ns.

10. AC Characteristics - Demultiplexed Bus Mode

Issue: T_{WLCL} loosened for better manufacturability.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788

From/To Ref: T_{WLCL} Min changed from -12 ns to -13 ns.

11. AC Characteristics - Synchronous Serial Port

Issue: T_{CXDV} loosened for better manufacturability.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788

From/To Ref: T_{CXDV} Max changed from 3t-20 ns to3t+24 ns.

12. Nomenclature Change

Issue: Removed 80C196EA device from Automotive data sheet.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788

Specification Clarifications

1. PLLEN Pin Must be Held Low along with the ONCE# Pin to Enter On-Circuit Emulation Mode

Issue: Original documentation stated that only the ONCE# pin needed to be held low to enter on-circuit emulation mode. However, the PLLEN pin must also be held low.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 4, Signal Descriptions: (see Document Change #2)

2. T2CLK can be Used for the External Clock for the Serial I/O Baud Rate Generator Input (not T1CLK)

Issue: T1CLK was incorrectly documented in the datasheet as the external clock source for the serial I/O baud rate generator. The external clock source is actually the T2CLK pin.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 4, Signal Descriptions: (see Document Change #2)

3. I_{OH2} Units are in µA, not mA

Issue: I_{OH2} units incorrectly stated in datasheet as mA instead of µA.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 6, DC Characteristics at V_{CC} =4.5 V - 5.5 V: (see Document Change #3)

4. I_{OH3} Units are in µA, not mA

Issue: I_{OH3} units incorrectly stated in datasheet as mA instead of µA.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 6, DC Characteristics at V_{CC} =4.5 V - 5.5 V: (see Document Change #3)

5. I_{OH3} is the Output High Current in Reset on Port 11 (not Port 12)

Issue: Datasheet incorrectly specified I_{OH3} as the Port 12 output high current in reset, instead of Port 11.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Table 6, DC Characteristics at V_{CC} =4.5 V - 5.5 V: (see Document Change #3)

6. IDLPD Illegal Keys are Any Value >3 (not >2)

Issue: Illegal keys for the IDLPD command, that reset the device, are any value greater than 3. A value of 3 will not reset the device.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788 and
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

From/To Ref: Appendix A, IDLPD Description:

- Change IDLE/POWERDOWN description text (see Document Change #13)

7. A/D Accuracy in Auto Scan Mode

Issue: A/D Absolute Error Specification does not apply to the A/D when running in auto scan mode. Accuracy in auto scan mode can be degraded 1-3 LSB from the accuracy in normal conversion mode depending on the application.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
83C196EA Microcontroller User's Manual - 272804

Documentation Changes

1. Page 2, Table 1

Issue: New/Omitted/Corrected data or Typos.

- Program Memory Options - Added Options “0” and Description “CPU only - no internal ROM”

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

2. Pages 7 through 14, Table 4

Problem: New/Omitted/Corrected data or Typos.

- AD15:0 - Description - 8-bit Demultiplexed Mode: Added last two sentences “AD7:0 share package pins P3.7:0. AD15:8 share package pins P4.7:0.”
- CRIN - Description - Changed “byte” to “bit” in last sentence.
- CROUT - Description - Changed “byte” to “bit” in last sentence.
- ONCE# - Description - First paragraph - Added second sentence “PLLEN must also be held low.”
- PLLEN - Description - Added second sentence “This pin must be held low when entering on-circuit emulation (ONCE) mode.”
- T1CLK - Description - Deleted second paragraph “External clock for the serial I/O baud-rate generator input (program selectable).”
- T2CLK - Description - Added paragraph “External clock for the serial I/O baud-rate generator input (program selectable).”
- XTAL1 - Description - Corrected “sourcel” (misspelled, should be source).

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

3. Pages 17 and 18, Table 6

Issue: New/Omitted/Corrected data or Typos.

- I_{REF} - Max - Changed TBD to “5”
- I_{CRVCC} - Added entire row (code ram V_{CC} supply current) and set max to 110µA. Test conditions: X_{TAL1}=40 Mhz, V_{CC} = 5.5 V.
- I_{OH2} - Min - Changed (V_{OH2}=V_{CC}-2.5v) to -65 and (V_{OH2}=V_{CC}-4.0v) to -75; Units - Changed all “mA” to “µA”.
- I_{OH3} - Parameter - Changed “Port 12” to “Port 11”; Min - Changed TBD (V_{OH3}=V_{CC}-1.0v) to -5, (V_{OH3}=V_{CC}-2.5v) to -8, (V_{OH3}=V_{CC}-4.0v) to -10; Units - Changed all “mA” to “µA”.

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

4. Pages 19 and 20, Table 7

Issue: New/Omitted/Corrected data or Typos.

- F_{XTAL1} - Min - Changed PLL in 1x mode to 20, PLL in 2x mode to 10
- f - Min Changed to 20
- t - Max - Changed 62.5 to 50
- T_{RLRH} - Min - Changed to t-12
- Note 1 - Changed 16 Mhz to 20 Mhz
- T_{CHWH} - Max - Changed to 10
- T_{WHQX} - Min - Changed to t-20

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

5. Pages 23 and 24, Table 9

Issue: New/Omitted/Corrected data or Typos.

- F_{XTAL1} - Min - Changed PLL in 1x mode to 20, PLL in 2x mode to 10
- f - Min Changed to 20
- t - Max - Changed 62.5 to 50
- T_{CHCL} - Min - Changed to t-10; Max - Changed to t+10
- T_{CLLH} - Min - Changed to -10; Max - Changed to 10
- T_{RLRH} - Min - Changed to 3t-12
- Note 1 - Changed 16 Mhz to 20 Mhz
- T_{WLWH} - Min - Changed to 3t-15
- T_{AVYV} - Max - Changed to 3t-25

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

6. Page 29, Table 11

Issue: New/Omitted/Corrected data or Typos.

- T_{D1VD} - Min - Changed TBD to 2t

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

7. Page 29, Figure 10

Issue: New/Omitted/Corrected data or Typos.

- Changed T_{CHCH} to T_{CLCL} in Figure 10 and lined it up with falling edges of SCx.
- Removed T_{CHCL} from Figure 10
- Moved T_{CLCH} in Figure 10 to line up with falling edge of SCx
- Fixed T_{CXDX} to be from falling edge of SCx to data invalid in Figure 10

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

8. Page 31, Table 13

Issue: New/Omitted/Corrected data or Typos.

- Note 2 - Changed “need” to “meet”

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

9. Page 33, Table 15

Issue: New/Omitted/Corrected data or Typos.

- DC Input Leakage - Typical (2) - Changed to ±100; Min - Changed to -300

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

10. Page 34, Table 16

Issue: New/Omitted/Corrected data or Typos.

- 1/TXLXL - Min - Changed to 10
- TXLXL - Max - Changed to 100; Min - Changed to 25
- Note 1 - Changed 16 MHz to 20 MHz and 32 MHz to 40 MHz

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153

11. Page 13-12, Section 13.6.3

Issue: Paragraph should read: “The device resets itself if an illegal key operand is used with the idle/powerdown (IDLPD) command. The legal keys are “1” for idle mode and “2” for powerdown mode. Any key greater than “3” will cause the device to execute a reset sequence. (See Appendix A for a description of the IDLPD command.)

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

12. Page 14-11, First Paragraph

Issue: Paragraph should read: “Holding the ONCE# signal low during the rising edge of RESET# causes the microcontroller to enter ONCE mode. THE PLLEN pin must also be held low. The ONCE signal is latched when RESET# goes inactive. Internally, the ONCE pin is tied to a medium-strength pull-up. To prevent accidental entry into ONCE mode, connect the ONCE pin to V_{CC}.”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

13. Page A-20, IDLPD Description

Issue: Description should read: IDLE/POWERDOWN. Depending on the 8-bit value of the KEY operand, this instruction causes the device to:

- enter idle mode, if KEY=1
- enter powerdown mode, if KEY=2
- execute a reset sequence, if KEY > 3.

The bus controller completes any prefetch cycle in progress before the CPU stops or resets.

- If KEY = 1 then enter idle
- else if KEY = 2 then enter powerdown
- else if KEY > 3 then execute reset

In PSW Flag Settings, 5th row should read: “KEY = any value other than 1, 2, or 3”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

14. Page B-8, ONCE# Pin Description

Issue: ONCE# pin description, first sentence of second paragraph should read: “Holding ONCE# low during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. (The PLLEN pin must also be held low.)”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

15. Page B-10, PLLEN Pin Description

Issue: Add paragraph to PLLEN pin description:

“The PLLEN pin must be held low along with the ONCE# pin to enter on-circuit emulation (ONCE) mode.”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

16. Page 2-18, Figure 2-9

Issue: Bit functionality definition reversed:

- Old:
  0 = enable clock-failure detection circuitry
  1 = disables clock-failure detection circuitry
- New:
  0 = disable clock-failure detection circuitry
  1 = enables clock-failure detection circuitry

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

17. Page 6-6, Table 6-3

Issue: Typo correction to SIO0 Transmit Interrupt Name:

At the bottom of the table, “SIO1 Transmit” (INT00) should be “SIO0 Transmit.”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

18. Page 9-17, Section 9.4.2.4

Issue: Remove 2nd paragraph which states:

“For standard mode operations, use this register to configure the serial clock for channel 1. For duplex and channel-select operations, use SSIO0_CLK to configure the common clock.”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

19. Page 9-19, Figure 9-10

Issue: Changes to Figure 9-10 and accompanying description:

SSIO 1 Clock (SSIO1_CLK) Register definition changes:

- Add Bit 0, POLS under Bit 1, PHAS (should look like page 9-17, Figure 9-9).
- Delete 2nd to last paragraph in PHAS/POLS bit description.
- Change last paragraph in PHAS/POLS bit description to read:
  - — “These bits are ignored for handshaking transfers. Use SSIO1_CON to select the type of data transfer (normal or handshaking) for channel 1".

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

20. Page 9-22, Section 9.5.3

Issue: Change first paragraph to read:

“For duplex operations, the serial channels function as a pair with SC0 as the common clock signal. However, the PHAS and POLS bits in the SSIO0_CLK and SSIO1_CLK registers still affect the internal clocking of channel 0 and channel 1 respectively. Therefore, these bits should be set accordingly for each channel. Use SSIO1_CLK to select duplex mode. In duplex mode, the paired channels can function as master or slave. Use SSIO0_CON to configure the channel pair as master or slave. For master operations, use SSIO_BAUD to enable the baud-rate generator and define the baud clock. In this mode, channel 0's clock signal is internally connected to channel 1's serial clock signal; therefore, you must configure channel 1 as a slave, using SSIO1_CON. This allows serial clock 0 to be input on serial clock 1.”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

21. Page 9-23, section 9.5.4

Issue: New/Omitted/Corrected data or Typos:

- Remove last sentence in first paragraph, “Since SC0 is the common clock, use SSIO0_CLK to configure the clock signal.”
- Change last sentence in third paragraph to:
  - — “Use SSIO1_CLK to configure the internal SC0 clock to channel 1, select channel-select half-duplex operations and enable or disable the master contention interrupt request.”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804.

22. Page 15, Table 5

Issue: Special-purpose memory (PIH vectors) and Program memory directly above address range is incorrect:

- Old

FF23FF FF2200	Program memory (Note 3)
FF21FF FF20C0	Special-purpose memory (PIH Vectors; Note 3)

- New

FF23FF FF2140	Program memory (Note 3)
FF213F FF20C0	Special-purpose memory (PIH Vectors; Note 3)

Affected Docs: *83C196EA Automotive CHMOS 16-Bit Microcontroller* datasheet - 272788
80C196EA CHMOS 16-Bit Microcontroller datasheet - 273153.

23. Page 11-16, Figure 11-11, Timer x Control (TxCONTROL) Register

Issue: UD bit description incorrectly states that the T2CONTROL direction bit controls the direction of both timers 1 and 2 when in concatenation mode and that the T4CONTROL direction bit controls the direction of both timers 3 and 4 when in concatenation mode. Actually, the T1CONTROL direction bit controls the direction of both timers 1 and 2 when in concatenation mode and the T3CONTROL direction bit controls the direction of both timers 3 and 4 when in concatenation mode.

- Old:

If T2CONTROL.7 is set, this bit in T2CONTROL controls the direction of both timers 2 and 1.

If T4CONTROL.7 is set, this bit in T4CONTROL controls the direction of both timers 4 and 3.

- New:

If T2CONTROL.7 is set, this bit in T1CONTROL controls the direction of both timers 2 and 1.

If T4CONTROL.7 is set, this bit in T3CONTROL controls the direction of both timers 4 and 3.

Affected Docs: *83C196EA Microcontroller User's Manual* - 272804

24. Page 11-8, Section 11.3, Timer/Counter Functional Overview

Issue: The second sentence in second paragraph is incorrect. The counter-overflow/underflow interrupt pending bit gets set when the timer decrements from 0001h to 0000h, not 0000h to FFFFh.

- Old:

When a counter increments from FFFEh to FFFFh or decrements from 0000H to FFFFh, the counter-overflow/underflow interrupt pending bit is set.

- New:

When a counter increments from FFFEh to FFFFh or decrements from 0001H to 0000h, the counter-overflow/underflow interrupt pending bit is set.

Affected Docs: *83C196EA Microcontroller User's Manual* - 272804

25. Page 6-3, Figure 6-2 Interrupt Service Flow Diagram

Issue: Interrupt service flow diagram is incorrect. A normal interrupt will not be serviced if the PTSSEL.x bit is set to 1. To make correct, the following change needs to be made: Add “PTSEL.x bit =0?” conditional branch after yes branch of “Interrupts Enabled?” If conditional answer is “yes”, continue to “priority resolver” block. If conditional answer is “no”, then continue to “return”.

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

26. Page 12-9, Figure 12-5 A/D Command (AD_COMMAND)_Register

Issue: Added sentence to “GO bit” note, “GO bit must be set to 0 for A/D SCAN to work.”

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

27. Page 12-11, Section 12.5, Determining A/D Status and Conversion Results

Issue: The last sentence of the first paragraph is incorrect. The AD_RESULTx register may be read at any time during an A/D conversion.

- Old:

If you read the AD_RESULT or AD_RESULTx before the conversion is complete, the result is not guaranteed to be accurate.

- New:

If you read the AD_RESULT register before the conversion is complete, the result is not guaranteed to be accurate. The AD_RESULTx register can be read at any time.

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

28. Page 16-6, Section 16.3.3, Minimizing Latency

Issue: Entire section is not worded correctly.

- Old:

The issue of latency arises when the SDU starts a cycle and the bus controller wants to use the code RAM in the next state. If any user application is executing from code RAM when the SDU is attempting to access the code RAM, you will incur a significant performance decline in your code RAM accesses. Even if the bus controller is idle, the SDU cannot access the code RAM without some small effect.

Because access to the code RAM by the SDU require at least two CPU state times, it is necessary to understand what the bus controller is doing at all times to ensure that any latency will be minimized.”

- New:

The SDU can only access the code RAM when the bus controller is starting an access to memory other than code RAM (i.e., Flash or external memory). Accesses to register RAM do not count in most cases, since the CPU directly accesses the register file. Therefore, it is necessary to understand what the bus controller is doing in the user application at all times to minimize latency.

Affected Docs: *83C196EA Microcontroller User’s Manual* - 272804

29. Page 11-7, Figure 11-2, EPA Timer/Counters

Issue: When timer concatenation is enabled, the OVRTM1 signal from timer 1 does not go through the timer 2 prescalar module. To fix the diagram, the 2x1 multiplier for T2CONTROL.7 should be switched with the Prescalar module. The input to the prescalar module will now be the output from the 2x1 multiplexer for T2CONTROL.4:3 and the output will go into the 2x1 multiplexer for T2CONTROL.7 along with the OVRTM1 signal. The output of the 2x1 multiplexer for T2CONTROL.7 will go to clock.

Affected Docs: *83C196EA Microcontroller User's Manual* - 272804