80C186EC/80C188EC AND 80L186EC/80L188EC EMBEDDED MICROPROCESSORS SPECIFICATION UPDATE

Release Date: June, 1997
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The 80C186EC/80C188EC and 80L186EC/80L188EC microprocessors may contain design defects or errors known as errata which may cause the products to deviate from published specifications. Current characterized errata are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Rev. Date	Version	Description
06/17/97	002	Added Documentation Changes 7 and 8.
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
80C186 Datasheet Errata	272027-001
80C188 Datasheet Errata	272076-001
80C186EC/80C188EC Microprocessor User's Manual	272047-003

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 186EC/188EC MICROPROCESSOR product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A	B	AB BB CB			
1	X	X	X	8	NoFix	NMI Entering Powerdown Mode on the 80C18x EA/EB/EC
2	X			10	Fixed	Early Exit From Reset
3	X			11	Fixed	Clock Divider At Reset
4	X	X	X	11	NoFix	Watchdog Timer Cannot be Reloaded or Disabled When the Peripheral Control Block (PCB) Is Located in Memory Space

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	272047-003	15	Doc	Rewording of Clock Generation Circuit Paragraph
2	272047-003	15	Doc	Rewording of Spurious Interrupts Paragraph
3	272047-003	15	Doc	Error in Function Description for Bit Mnemonic T7:3
4	272047-003	15	Doc	Incorrect Flow Chart Labels
5	272047-003	16	Doc	Reload Watchdog Timer Example Code Changed
6	272047-003	17	Doc	Disable Watchdog Timer Example Code Changed
7	272047-003	18	Doc	Incorrect AX Register Contents
8	272047-003	18	Doc	Clarification in Spurious Interrupts Paragraphs

IDENTIFICATION INFORMATION

Markings

186EC/188EC MICROPROCESSOR processors may be identified electrically according to device type and stepping. Refer to the data sheet for instructions on how to obtain the identifier number.

A-Step sample devices can be identified in two ways:

1. The product is marked with a five character QDF number just below the product identifier. The table below can help you quickly identify which product you have:

Product	QDF Numbers (all packages)
80C186EC	Q8566, Q8568
80C188EC	Q8567, Q8569

2. There is a STEPID register which may be examined through software. For A-step devices, the register contains a value of 01H.

ERRATA

1. NMI Entering Powerdown Mode on the 80C18xEA/EB/EC

PROBLEM: If an NMI can be received during execution of the HLT instruction when entering Powerdown mode, certain considerations must be made.

IMPLICATION: If an NMI occurs during execution of the HLT instruction when entering Powerdown mode, the processor may to enter Powerdown or may not service the NMI. To avoid this, the NMI pulse width must be extended to allow recognition.

WORKAROUND:

NMI Functionality - NMI is the highest priority interrupt. It cannot be masked by software. To be recognized, NMI must be active for a minimum of one CLKOUT period and meet required setup and hold times (for recognition at a specific clock edge). If these requirements are met, NMI servicing begins at the next valid instruction boundary.

Powerdown Mode Functionality - Powerdown mode on the 186 processors causes the clock input to the CPU and peripherals to be disabled. To enter Powerdown mode, two things must happen. First, the PWRDN bit in the PWRCON Register must be set. Second, the HLT instruction must be executed. During the HLT instruction, the clock signal to the CPU and integrated peripherals stop (at a logic low level) at the end of the T2 bus state. The CLKOUT signal stops (at a logic high level) at the end of the T3 bus state. To exit Powerdown, an NMI or processor reset must occur.

NMI During HLT Execution - If an NMI occurs before the HLT instruction executes, everything functions properly. The NMI is recognized at the instruction boundary preceding the HLT instruction, the NMI is serviced and the processor then enters powerdown mode.

The problem occurs when an NMI occurs during execution of the HLT instruction. NMI is only serviced at valid instruction boundaries. The HLT instruction, when entering Powerdown, does not really have a boundary, it extends until Powerdown is exited. If NMI occurs between the beginning the T1 bus state and the end of the T2 state, but does not extend into T3, it will not be recognized, and the processor will enter Powerdown mode. The processor does not recognize the NMI request during the HLT instruction until the internal clock has stopped (at the end of T2).

For the NMI to be recognized during the execution of the HLT instruction, the pulse must extend into T3. At this point, the processor has entered Powerdown and synchronized the NMI pulse. The NMI will be processed, but the processor will never enter Powerdown. Essentially, because NMI is active, the processor exits Powerdown as soon as it enters.

In a typical system design using Powerdown mode, NMI can only occur after Powerdown is entered and the clock is stopped. The simplest solution to the problem is to not assert NMI unless the processor has entered Powerdown Mode.

If the system requires periodic NMI pulses, then the NMI pulse width must be long enough to ensure that it will extend into the T3 state of the HLT instruction. A NMI pulse width of three CLKOUT periods guarantees this.

The figures below show NMI occurring at different times during execution of the HLT instruction. Two cases are shown. Figure 1 shows cases where NMI is not recognized. Figure 2 shows cases where NMI is recognized. Both cases assume setup and hold time requirements are met for the NMI input.

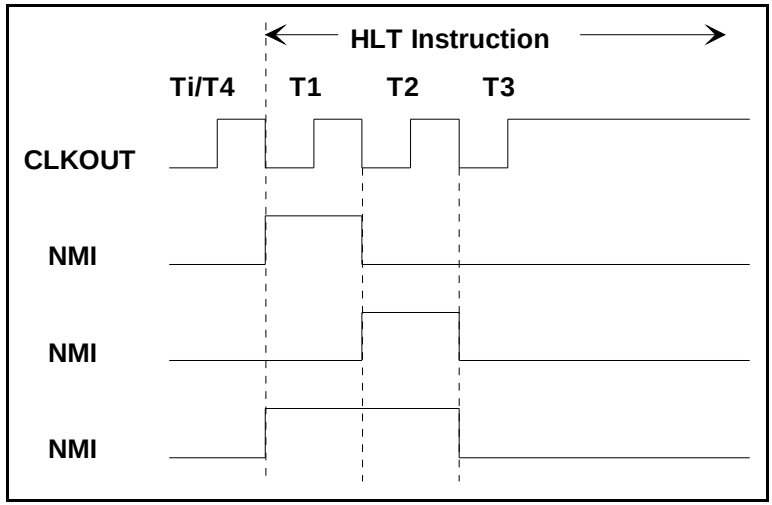

Figure 1. NMI Ignored During HLT Entering Powerdown

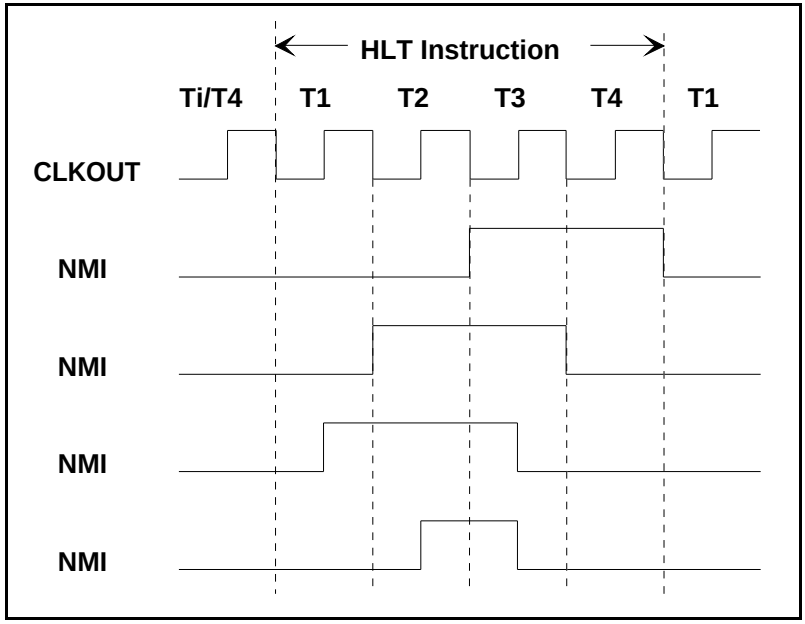

Figure 2. NMI Recognized During HLT Entering Powerdown

STATUS: There are no plans to correct this errata. Refer to Summary Table of Changes to determine the affected stepping(s).

2. Early Exit From Reset

PROBLEM: At high V_{CC} voltages and/or low operating temperatures, the 80C186EC/80C188EC will exit reset one CLKOUT cycle too early due to an internal race condition. The device resets correctly and executes code normally (just one clock too early). The problem is aggravated by conditions that tend to cause higher speed internal operation (i.e., high V_{CC} and low temperatures). The voltage and temperature points at which the anomaly occurs vary from device to device.

IMPLICATION: In most operations this errata causes no impact.

WORKAROUND: None.

STATUS: Fixed in B step. Refer to Summary Table of Changes to determine the affected stepping(s).

3. Clock Divider At Reset

PROBLEM: The clock division circuitry that is used in Powersave Mode may not be reset immediately. The correct design would have reset the Powersave divider immediately upon reset. Instead, the divider is not reset until the first low phase of CLKOUT following a reset.

IMPLICATION: Because the divider is not reset, it is possible that the device could be operating in a divide-by mode. This could have the effect of extending the period of CLKOUT by as much as 64 times the undivided rate for the first cycle out of reset. A minimum of 128 CLKIN pulses are required after RESIN# is asserted to ensure that the Powersave divider is properly cleared after a reset. The 128 CLKIN pulses ensure that at least one full CLKOUT cycle occur for the worst case of divide-by-64 mode.

WORKAROUND: The problem can occur both at cold and warm reset. For a cold reset the fix involves insuring that RESIN# is held low at least 128 CLKIN pulses. Note that the datasheet and handbooks both specify RESIN time with respect to CLKOUT. If these specifications are followed no problems will occur (since it only takes one full CLKOUT after RESIN# is asserted to reset the divider). For a warm reset (including Watchdog Timer reset), if the 4 CLKOUT period minimum is followed no problems will occur if Powersave mode is not being used. If Powersave Mode is active when a warm reset occurs, then the first CLKOUT during reset will be at the divided rate. The subsequent 3 (or more) CLKOUTs will be at full speed.

STATUS: Fixed in B step. Refer to Summary Table of Changes to determine the affected stepping(s).

4. Watchdog Timer Cannot Be Reloaded or Disabled When the Peripheral Control Block (PCB) Is Located in Memory Space

PROBLEM:

RELOADING THE WATCHDOG TIMER - The Watchdog Timer counter is reloaded by a locked sequence of two separate byte write operations to the Watchdog Timer Clear register (WDTCLR). The first byte of data is 0AAH, and the second byte is 55H. A special LOCKed instruction is required to accomplish this.

The use of the LOCK REP MOVS instruction not only increments/decrements the source address, but also the destination address (WDTCLR). Therefore, the first byte would be written correctly to the WDTCLR register, while the second byte would be written to WDTCLR+1 in memory. This causes the Watchdog Timer not to reload and the WDT to expire.

DISABLING THE WATCHDOG TIMER - A similar two byte write sequence is used to disable the Watchdog Timer. The first byte of data is 55H, and the second byte is 0AAH. This data is written to the Watchdog Timer Disable register (WDTDIS).

Again, it is not possible to disable the Watchdog Timer when the PCB is in memory space because there is no LOCKed string instruction that can be used to write two consecutive bytes to a single memory address (i.e., the MOVS instruction adjusts both the source and destination operands).

IMPLICATION: It is not possible to reload or disable the WDT when the PCB is in memory space because there is no instruction that supports a locked byte string sequence in which the destination address (WDTCLR) stays fixed while the source increments/decrements.

WORKAROUND: Reloading and disabling operations of the Watchdog Timer must be performed with the PCB located in I/O space. If the PCB is to be located in memory space, it must be temporarily moved back into I/O space for reloading or disabling.

NOTE: All serial and “DMA to Internal Peripheral” operations must be temporally disabled prior to switching the PCB to I/O space. Once the PCB is mapped back to memory space, the serial and “DMA to Internal Peripheral” operations can be re-enabled.

STATUS: There are no plans to correct this errata. Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

1. Rewording of Clock Generation Circuit Paragraph

ITEM: On page 5-1 of the *80C186EC/80C188EC Microprocessor User's Manual*, the paragraph in section 5.1 should read: "The clock generation circuit (Figure 5-1) includes a crystal oscillator, a divide-by-two counter, power-down, idle, and reset circuitry. See "Power Management" on page 5-10 for a discussion of power management options."

AFFECTED DOCUMENTS: *80C186EC/80C188EC Microprocessor User's Manual*, order #272047-003

2. Rewording of Spurious Interrupts Paragraph

ITEM: The first sentence of Section 8.3.2.3 of the *80C186EC/80C188EC Microprocessor User's Manual* should be changed to: "For both level- and edge-sensitive interrupts, a high value must be maintained on the IR line until after the falling edge of the first INTA# pulse (see Figure 8-5)."

AFFECTED DOCUMENTS: *80C186EC/80C188EC Microprocessor User's Manual*, order #272047-003

3. Error in Function Description for Bit Mnemonic T7:3

ITEM: In Figure 8-13 on page 8-25 of the 8*0C186EC/80C188EC Microprocessor User's Manual*, the sentence "For example, write 20H to these bits to specify a Type 8 interrupt" should be changed to "For example, write 20H to these bits to specify a Type 32 interrupt"

AFFECTED DOCUMENTS: *80C186EC/80C188EC Microprocessor User's Manual*, order #272047-003

4. Incorrect Flow Chart Labels

ITEM: On page 9-5 of the *80C186EC/80C188EC Microprocessor User's Manual*, Figure 9-3 contains incorrect flow chart labels. The stem below Conditional statement "Counter = Compare 'A' ?" should be a "YES" and the stem to the right should be a "NO."

AFFECTED DOCUMENTS: *80C186EC/80C188EC Microprocessor User's Manual*, order #272047-003

5. Reload Watchdog Timer Example Code Changed

ITEM: In example 12-1 on page 12-4 of the *80C186EC/80C188EC Microprocessor User's Manual*, the code for reloading the watchdog timer down counter has been changed to the following.

```
wdt_data segment
wdt_rel         db          0AAH, 055H          ;WDT Reload Constants
wdt_data ends
wdt_reload      segment
                assume cs: wdt_reload, ds: wdt_data
                mov     ax, seg wdt_rel
                mov     ds, ax
                mov     si, offset wdt_rel      ;DS:SI points to the Disable Constants
                cld                             ;Clear direction flag (autoincrement)
                mov cx, 2                       ;2 byte string operation
                mov     dx, 0FF28h              ;I/O address of WDTCLR
lock rep        outs    dx, byte ptr ds: [si]   ;LOCKed WDT reload sequence
wdt_reload      ends
```

AFFECTED DOCUMENTS: *80C186EC/80C188EC Microprocessor User's Manual*, order #272047-003

6. Disable Watchdog Timer Example Code Changed

ITEM: In example 12-3 on page 12-7 of the *80C186EC/80C188EC Microprocessor User's Manual*, the code for disabling the watchdog timer down counter has been changed to that shown below.

If the WDT is to be disabled, it must be done prior to the first expiration and prior to it being reloaded by either a software or hardware reload (time-out).

```
wdt_data segment
wdt_dis         db              055H,0AAH               ;WDT Disable Constants
wdt_data ends
wdt_disable     segment
                assume cs: wdt_disable, ds: wdt_data
                mov     ax, seg wdt_dis
                mov     ds, ax
                mov     si, offset wdt_dis      ;DS:SI points to the Disable Constants
                cld                                     ;Clear direction flag (autoincrement)
                mov cx, 2                       ;2 byte string operation
                mov     dx, 0FF2Ah                      ;I/O address of WDTDIS
lock rep        outs    dx, byte ptr ds: [si]   ;LOCKed WDT disable sequence
wdt_disable     ends
```

AFFECTED DOCUMENTS: *80C186EC/80C188EC Microprocessor User's Manual*, order #272047-003

7. Incorrect AX Register Contents

ITEM: On page 2-16 of the *80C186EC/80C188EC Microprocessor User's Manual*, the contents of the AX Register in Figure 2-10, "Stack Operation," should be 12 34, not 10 50. (See the top box on the third step of the example, top right hand side of figure.)

AFFECTED DOCUMENTS: *80C186EC/80C188EC Microprocessor User's Manual*, order #272047-003

8. Clarification in Spurious Interrupts Paragraphs

ITEM: In Section 8.3.6.6 on page 8-18 of the *80C186EC/80C188EC Microprocessor User's Manual*, the first sentence of the first paragraph should be changed to read, "A spurious interrupt on the master IR lines INT0 through INT6 will generate a spurious IR type 7."

The first sentence of the second paragraph should be changed to read, "A spurious interrupt on the slave IR line INT7 can cause one of two scenarios (Figure 8-10)."

AFFECTED DOCUMENTS: *80C186EC/80C188EC Microprocessor User's Manual*, order #272047-003