National Semiconductor

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COP424C, COP425C, COP426C, COP324C, COP325C, COP326C and COP444C, COP445C, COP344C, COP345C Single-Chip 1k and 2k CMOS Microcontrollers

General Description

The COP424C, COP425C, COP426C, COP444C and COP445C fully static, Single-Chip CMOS Microcontrollers are members of the COPS™ family, fabricated using double-poly, silicon gate microCMOS technology. These Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP424C and COP444C are 28 pin chips. The COP425C and COP445C are 24-pin versions (4 inputs removed) and COP426C is 20-pin version with 15 I/O lines. Standard test procedures and reliable high-density techniques provide the medium to large volume customers with a customized microcontroller at a low end-product cost. These microcontrollers are appropriate choices in many demanding control environments especially those with human interface.

The COP424C is an improved product which replaces the COP420C.

Features

- Lowest power dissipation (50 μW typical)
- Fully static (can turn off the clock)
- Power saving IDLE state and HALT mode
- 4 μs instruction time, plus software selectable clocks
- 2k x 8 ROM, 128 x 4 RAM (COP444C/COP445C)
- 1k x 8 ROM, 64 x 4 RAM (COP424C/COP425C/COP426C)
- 23 I/O lines (COP444C and COP424C)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- Single supply operation (2.4V to 5.5V)
- Programmable read/write 8-bit timer/event counter
- Internal binary counter register with MICROWIRE™ serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS output compatible
- Microbus™ compatible
- Software/hardware compatible with COP400 family
- Extended temperature range devices COP324C/COP325C/COP326C and COP344C/COP345C (−40°C to +85°C)
- Military devices (−55°C to +125°C) to be available

Block Diagram

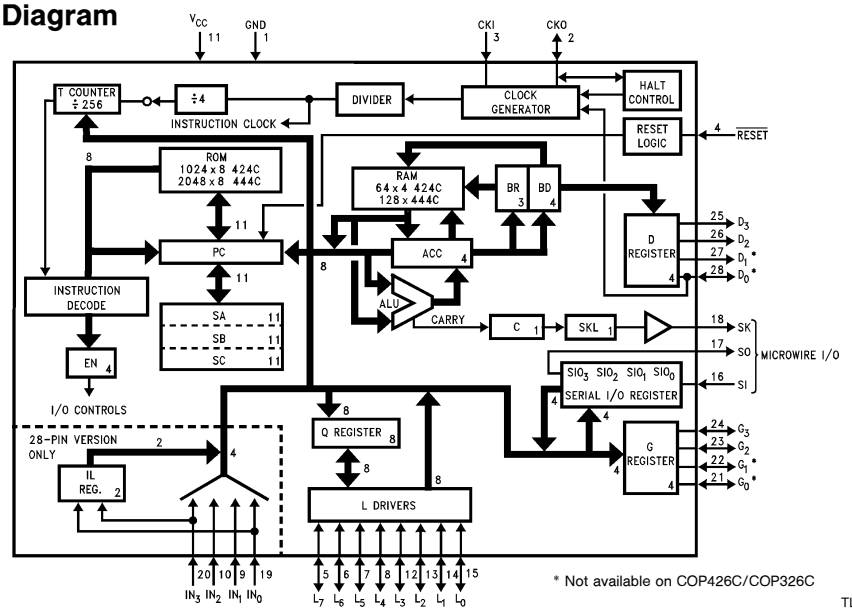


FIGURE 1

RRD-B30M105/Printed in U. S. A.

COP424C, COP425C, COP426C, COP324C, COP325C, COP326C and COP444C, COP445C, COP344C, COP345C Single-Chip 1k and 2k CMOS Microcontrollers

Absolute Maximum Ratings

Supply Voltage (V_{CC})	6V
Voltage at any Pin	−0.3V to V_{CC} + 0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics 0°C ≤ T_A ≤ 70°C unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (Notes 4, 5)	Peak to Peak		0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 2.4V, tc = 64 μs		120	μA
	V_{CC} = 5.0V, tc = 16 μs		700	μA
	V_{CC} = 5.0V, tc = 4 μs		3000	μA
	(tc is instruction cycle time)			
HALT Mode Current (Note 2)	V_{CC} = 5.0V, F_{IN} = 0 kHz		40	μA
	V_{CC} = 2.4V, F_{IN} = 0 kHz		12	μA
Input Voltage Levels				
$\overline{RESET}$, CKI, D_0 (clock input)				
Logic High		0.9 V_{CC}		V
Logic Low			0.1 V_{CC}	V
All Other Inputs				
Logic High		0.7 V_{CC}		V
Logic Low			0.2 V_{CC}	V
Input Pull-Up Current	V_{CC} = 4.5V, V_{IN} = 0	−30	−330	μA
Hi-Z Input Leakage		−1	+1	μA
Input Capacitance (Note 4)			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ± 10%			
Logic High	I_{OH} = −100 μA	2.7		V
Logic Low	I_{OL} = 400 μA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 μA	V_{CC} − 0.2		V
Logic Low	I_{OL} = 10 μA		0.2	V
Output Current Levels (except CKO)				
Sink (Note 6)	V_{CC} = 4.5V, V_{OUT} = V_{CC}	1.2		mA
	V_{CC} = 2.4V, V_{OUT} = V_{CC}	0.2		mA
Source (Standard Option)	V_{CC} = 4.5V, V_{OUT} = 0V	−0.5		mA
	V_{CC} = 2.4V, V_{OUT} = 0V	−0.1		mA
Source (Low Current Option)	V_{CC} = 4.5V, V_{OUT} = 0V	−30	−330	μA
	V_{CC} = 2.4V, V_{OUT} = 0V	−6	−80	μA
CKO Current Levels (As Clock Out)				
Sink ÷4	V_{CC} = 4.5V, CKI = V_{CC}, V_{OUT} = V_{CC}	0.3		mA
Sink ÷8		0.6		mA
Sink ÷16		1.2		mA
Source ÷4	V_{CC} = 4.5V, CKI = 0V, V_{OUT} = 0V	−0.3		mA
Source ÷8		−0.6		mA
Source ÷16		−1.2		mA
Allowable Sink/Source Current per Pin (Note 6)			5	mA
Allowable Loading on CKO (as HALT)			100	pF
Current Needed to Over-Ride HALT (Note 3)				
To Continue	V_{CC} = 4.5V, V_{IN} = 0.2V_{CC}		0.7	mA
To Halt	V_{CC} = 4.5V, V_{IN} = 0.7V_{CC}		1.6	mA
TRI-STATE or Open Drain Leakage Current		−2.5	+2.5	μA

Absolute Maximum Ratings

Supply Voltage	6V
Voltage at any Pin	−0.3V to V_{CC} + 0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics −40°C ≤ T_A ≤ +85°C unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		3.0	5.5	V
Power Supply Ripple (Notes 4, 5)	Peak to Peak		0.1 V_{CC}	V
Supply Current (Note 1)	V_{CC} = 3.0V, tc = 64 μs		180	μA
	V_{CC} = 5.0V, tc = 16 μs		800	μA
	V_{CC} = 5.0V, tc = 4 μs		3600	μA
	(tc is instruction cycle time)			
HALT Mode Current (Note 2)	V_{CC} = 5.0V, F_{IN} = 0 kHz		60	μA
	V_{CC} = 3.0V, F_{IN} = 0 kHz		30	μA
Input Voltage Levels				
RESET, CKI, D_O (clock input)				
Logic High		0.9 V_{CC}		V
Logic Low			0.1 V_{CC}	V
All Other Inputs				
Logic High		0.7 V_{CC}		V
Logic Low			0.2 V_{CC}	V
Input Pull-Up Current	V_{CC} = 4.5V, V_{IN} = 0	−30	−440	μA
Hi-Z Input Leakage		−2	+2	μA
Input Capacitance (Note 4)			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ±10%			
Logic High	I_{OH} = −100 μA	2.7		V
Logic Low	I_{OL} = 400 μA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 μA	V_{CC} − 0.2		V
Logic Low	I_{OL} = 10 μA		0.2	V
Output Current Levels (except CKO)				
Sink (Note 6)	V_{CC} = 4.5V, V_{OUT} = V_{CC}	1.2		mA
	V_{CC} = 3.0V, V_{OUT} = V_{CC}	0.2		mA
Source (Standard Option)	V_{CC} = 4.5V, V_{OUT} = 0V	−0.5		mA
	V_{CC} = 3.0V, V_{OUT} = 0V	−0.1		mA
Source (Low Current Option)	V_{CC} = 4.5V, V_{OUT} = 0V	−30	−440	μA
	V_{CC} = 3.0V, V_{OUT} = 0V	−8	−200	μA
CKO Current Levels (As Clock Out)				
Sink ÷4	V_{CC} = 4.5V, CKI = V_{CC}, V_{OUT} = V_{CC}	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Source ÷4	V_{CC} = 4.5V, CKI = 0V, V_{OUT} = 0V	−0.3		mA
÷8		−0.6		mA
÷16		−1.2		mA
Allowable Sink/Source Current per Pin (Note 6)			5	mA
Allowable Loading on CKO (as HALT)			100	pF
Current Needed to Over-Ride HALT (Note 3)				
To Continue	V_{CC} = 4.5V, V_{IN} = 0.2V_{CC}		0.9	mA
To Halt	V_{CC} = 4.5V, V_{IN} = 0.7V_{CC}		2.1	mA
TRI-STATE or Open Drain Leakage Current		−5	+5	μA

COP424C/COP425C/COP426C and COP444C/COP445C

AC Electrical Characteristics $0°C \le T_A \le 70°C$ unless otherwise specified.

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (tc)	$V_{CC} \ge 4.5V$	4	DC	μs
	$4.5V > V_{CC} \ge 2.4V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \ge 4.5V$	DC	1.0	MHz
÷8 mode	$V_{CC} \ge 4.5V$	DC	2.0	MHz
÷16 mode	$V_{CC} \ge 4.5V$	DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \ge 2.4V$	DC	250	kHz
÷8 mode	$4.5V > V_{CC} \ge 2.4V$	DC	500	kHz
÷16 mode	$4.5V > V_{CC} \ge 2.4V$	DC	1.0	MHz
Duty Cycle (Note 4)	$f_1 = 4$ MHz	40	60	%
Rise Time (Note 4)	$f_1 = 4$ MHz External Clock		60	ns
Fall Time (Note 4)	$f_1 = 4$ MHz External Clock		40	ns
Instruction Cycle Time RC Oscillator (Note 4)	$R = 30k \pm 5\%$, $V_{CC} = 5V$ $C = 82$ pF $\pm 5\%$ (÷4 Mode)	5	11	μs
Inputs: (See *Figure 3*)				
t_{SETUP} G Inputs	$V_{CC} \ge 4.5V$	tc/4 + .7		μs
t_{SETUP} SI Input	$V_{CC} \ge 4.5V$	0.3		μs
t_{SETUP} All Others	$V_{CC} \ge 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \ge 4.5V$	0.25		μs
	$4.5V > V_{CC} \ge 2.4V$	1.0		μs
Output Propagation Delay	$V_{OUT} = 1.5V$, $C_L = 100$ pF, $R_L = 5k$			
t_{PD1}, t_{PD0}	$V_{CC} \ge 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$4.5V > V_{CC} \ge 2.4V$		4.0	μs
Microbus Timing	$CL = 50$ pF, $V_{CC} = 5V \pm 5\%$			
Read Operation (*Figure 4*)				
Chip Select Stable before $\overline{RD}$ $-t_{CSR}$		65		ns
Chip Select Hold Time for $\overline{RD}$ $-t_{RCS}$		20		ns
$\overline{RD}$ Pulse Width $-t_{RR}$		400		ns
Data Delay from $\overline{RD}$ $-t_{RD}$			375	ns
$\overline{RD}$ to Data Floating $-t_{DF}$ (Note 4)			250	ns
Write Operation (*Figure 5*)				
Chip Select Stable before $\overline{WR}$ $-t_{CSW}$		65		ns
Chip Select Hold Time for $\overline{WR}$ $-t_{WCS}$		20		ns
$\overline{WR}$ Pulse Width $-t_{WW}$		400		ns
Data Set-Up Time for $\overline{WR}$ $-t_{DW}$		320		ns
Data Hold Time for $\overline{WR}$ $-t_{WD}$		100		ns
INTR Transition Time from $\overline{WR}$ $-t_{WI}$			700	ns

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 5k resistors. See current drain equation on page 17.

Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions: all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all outputs low and tied to ground.

Note 3: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 4: This parameter is only sampled and not 100% tested. Variation due to the device included.

Note 5: Voltage change must be less than 0.5 volts in a 1 ms period.

Note 6: SO output sink current must be limited to keep V_{OL} less than $0.2V_{CC}$ when part is running in order to prevent entering test mode.

COP324C/COP325C/COP326C and COP344C/COP345C

AC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified.

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (tc)	$V_{CC} \ge 4.5V$	4	DC	μs
	$4.5V > V_{CC} \ge 3.0V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \ge 4.5V$	DC	1.0	MHz
÷8 mode	$V_{CC} \ge 4.5V$	DC	2.0	MHz
÷16 mode	$V_{CC} \ge 4.5V$	DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \ge 3.0V$	DC	250	kHz
÷8 mode	$4.5V > V_{CC} \ge 3.0V$	DC	500	kHz
÷16 mode	$4.5V > V_{CC} \ge 3.0V$	DC	1.0	MHz
Duty Cycle (Note 4)	$f_1 = 4$ MHz	40	60	%
Rise Time (Note 4)	$f_1 = 4$ MHz external clock		60	ns
Fall Time (Note 4)	$f_1 = 4$ MHz external clock		40	ns
Instruction Cycle Time RC Oscillator (Note 4)	R = 30k ±5%, V_{CC} = 5V C = 82 pF ±5% (÷4 Mode)	5	11	μs
Inputs: (See *Figure 3*)				
t_{SETUP} G Inputs	$V_{CC} \ge 4.5V$	tc/4+.7		μs
t_{SETUP} SI Inputs	$V_{CC} \ge 4.5V$	0.3		μs
t_{SETUP} All Others	$V_{CC} \ge 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \ge 4.5V$	0.25		μs
	$4.5V > V_{CC} \ge 3.0V$	1.0		μs
Output Propagation Delay	$V_{OUT} = 1.5V$, $C_L = 100$ pF, $R_L = 5k$			
t_{PD1}, t_{PD0}	$V_{CC} \ge 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$4.5V > V_{CC} \ge 3.0V$		4.0	μs
Microbus Timing	$C_L = 50$ pF, $V_{CC} = 5V \pm 5\%$			
Read Operation (*Figure 4*)				
Chip Select Stable before $\overline{RD}$ $-t_{CSR}$		65		ns
Chip Select Hold Time for $\overline{RD}$ $-t_{RCS}$		20		ns
$\overline{RD}$ Pulse Width $-t_{RR}$		400		ns
Data Delay from $\overline{RD}$ $-t_{RD}$			375	ns
$\overline{RD}$ to Data Floating $-t_{DF}$ (Note 4)			250	ns
Write Operation (*Figure 5*)				
Chip Select Stable before $\overline{WR}$ $-t_{CSW}$		65		ns
Chip Select Hold Time for $\overline{WR}$ $-t_{WCS}$		20		ns
$\overline{WR}$ Pulse Width $-t_{WW}$		400		ns
Data Set-Up Time for $\overline{WR}$ $-t_{DW}$		320		ns
Data Hold Time for $\overline{WR}$ $-t_{WD}$		100		ns
INTR Transition Time from $\overline{WR}$ $-t_{WI}$			700	ns

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 5k resistors. See current drain equation on page 17.

Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions: all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all outputs low and tied to ground.

Note 3: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

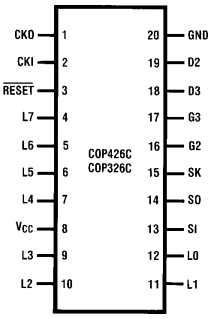
Note 4: This parameter is only sampled and not 100% tested. Variation due to the device included.

Note 5: Voltage change must be less than 0.5 volts in a 1 ms period.

Note 6: SO output sink current must be limited to keep V_{OL} less than $0.2V_{CC}$ when part is running in order to prevent entering test mode.

Connection Diagrams

DIP and S.O. Wide



TL/DD/5259–16

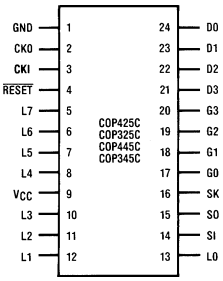
Top View

Order Number COP326C-XXX/D or COP426C-XXX/D
See NS Hermetic Package D20A
(Prototype Package Only)

Order Number COP326C-XXX/N or COP426C-XXX/N
See NS Molded Package N20A

Order Number COP326C-XXX/WM or COP426C-XXX/WM
See NS Surface Mount Package M20B

DIP and S.O. Wide



TL/DD/5259–2

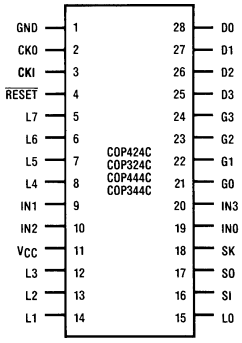
Top View

Order Number COP325C-XXX/D, COP445C-XXX/D, COP425C-XXX/D or COP345C-XXX/D
See NS Hermetic Package D24C
(Prototype Package Only)

Order Number COP325C-XXX/N, COP345C-XXX/N, COP425C-XXX/N or COP445C-XXX/N
See NS Molded Package N24A

Order Number COP325C-XXX/WM, COP345C-XXX/WM, COP425C-XXX/WM or COP445C-XXX/WM
See NS Surface Mount Package M24B

Dual-In-Line Package



TL/DD/5259–3

Top View

Order Number COP324C-XXX/D, COPC324-XXX/WM, COP344C-XXX/D, COP424C-XXX/D, COPC424-XXX/WM or COP444C-XXX/D
See NS Hermetic Package D28C
(Prototype Package Only)

Order Number COP324C-XXX/N, COP344C-XXX/N, COPC344-XXX/WM, COP424C-XXX/N, COP444C-XXX/N or COPC444-XXX/WM
See NS Molded Package N28B

FIGURE 2

Pin	Description
L7–L0	8-bit bidirectional port with TRI-STATE
G3–G0	4-bit bidirectional I/O port
D3–D0	4-bit output port
IN3–IN0	4-bit input port (28-pin package only)
SI	Serial input or counter input
SO	Serial or general purpose output

Pin	Description
SK	Logic controlled clock output
CKI	Chip oscillator input
CKO	Oscillator output, HALT I/O port or general purpose input
$\overline{\text{RESET}}$	Reset input
V_{CC}	Most positive power supply
GND	Ground

Functional Description

The internal architecture is shown in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic ''1'', when a bit is reset, it is a logic ''0''.

For ease of reading only the COP424C/425C/COP426C/444C/445C are referenced; however, all such references apply equally to COP324C/325C/COP326C/344C/345C.

PROGRAM MEMORY

Program Memory consists of ROM, 1024 bytes for the COP424C/425C/426C and 2048 bytes for the COP444C/445C. These bytes of ROM may be program instructions, constants or ROM addressing data.

ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call or interrupt pushes the next PC address into the stack. Each return pops the stack back into the PC register.

DATA MEMORY

Data memory consists of a 512-bit RAM for the COP444C/445C, organized as 8 data registers of 16 $\times$ 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register.

Data memory consists of a 256-bit RAM for the COP424C/425C/426C, organized as 4 data registers of 16 $\times$ 4-bits digits. The B register is 6 bits long. Upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or T counter or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

The processor contains its own 4-bit A register (accumulator) which is the source and destination register for most I/O, arithmetic, logic, and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch or T counter, to input 4 bits of L I/O ports data, to input 4-bit G, or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. When the T counter overflows, an overflow flag will be set (see SKT and IT instructions below). The T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in *Figure 10a*.

Four general-purpose inputs, IN3-IN0, are provided. IN1, IN2 and IN3 may be selected, by a mask-programmable option as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in Microbus application.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. In the dual clock mode, D0 latch controls the clock selection (see dual oscillator below).

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G0 may be mask-programmed as an output for Microbus applications.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control. With the Microbus option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU.

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O port. Also, the contents of L may be read directly into A and M. As explained above, the Microbus option allows L I/O port data to be latched into the Q register.

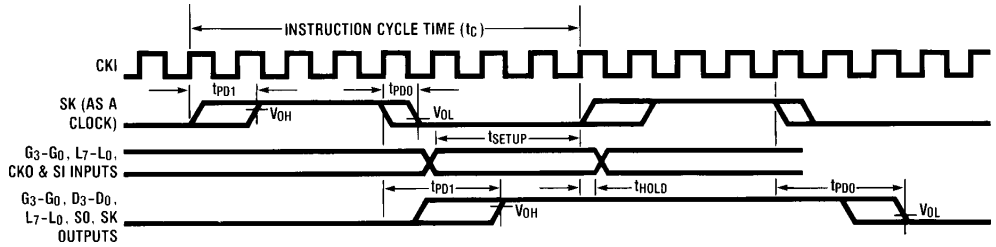
Functional Description (Continued)

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and COPS peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

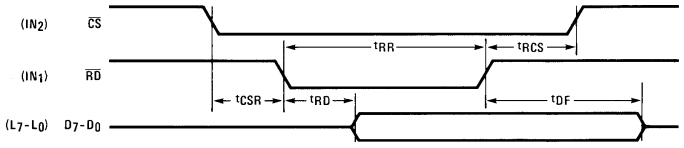
EN is an internal 4-bit register loaded by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register:

0. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse (''1'' to ''0'') occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output equals the value of EN3. With EN0 reset, SIO is a serial shift register left shifting 1 bit each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. The SK outputs SKL ANDed with the instruction cycle clock.
1. With EN1 set, interrupt is enabled. Immediately following an interrupt, EN1 is reset to disable further interrupts.
2. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O port. Resetting EN2 disables the L drivers, placing the L I/O port in a high-impedance input state.



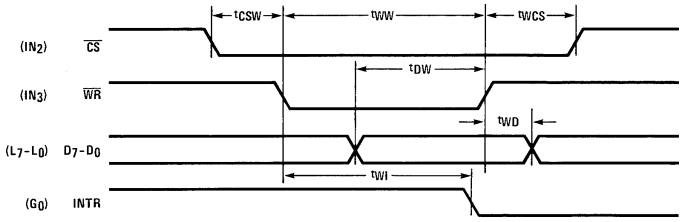
TL/DD/5259–4

FIGURE 3. Input/Output Timing Diagrams (divide by 8 mode)



TL/DD/5259–5

FIGURE 4. Microbus Read Operation Timing



TL/DD/5259–6

FIGURE 5. Microbus Write Operation Timing

Functional Description (Continued)

3. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected) SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains set to ''0''.

INTERRUPT

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once recognized as explained below, pushes the next sequential program counter address (PC + 1) onto the stack. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN1 is reset.

b. An interrupt will be recognized only on the following conditions:
   1. EN1 has been set.
   2. A low-going pulse (''1'' to ''0'') at least two instruction cycles wide has occurred on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g. if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to pop the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines should not be nested within the interrupt service routine, since their popping of the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The instruction at hex address 0FF must be a NOP.

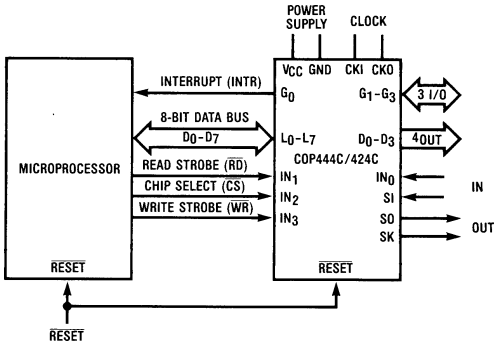
e. An LEI instruction may be put immediately before the RET instruction to re-enable interrupts.

MICROBUS INTERFACE

The COP444C/424C has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (μP). IN1, IN2 and IN3 general purpose inputs become Microbus compatible read-strobe, chip-select, and write-strobe lines, respectively. IN1 becomes $\overline{RD}$ — a logic ''0'' on this input will cause Q latch data to be enabled to the L ports for input to the uP. IN2 becomes $\overline{CS}$ — a logic ''0'' on this line selects the COP444C/424C as the uP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components.

IN3 becomes $\overline{WR}$ — a logic ''0'' on this line will write bus data from the L ports to the Q latches for input to the COP444C/424C. G0 becomes INTR a ''ready'' output, reset by a write pulse from the uP on the $\overline{WR}$ line, providing the ''handshaking'' capability necessary for asynchronous data transfer between the host CPU and the COP444C/424C.

This option has been designed for compatibility with National's Microbus — a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See Microbus National Publication.) The functioning and timing relationships between the signal lines affected by this option are as specified for the Microbus interface, and are given in the AC electrical characteristics and shown in the timing diagrams (*Figures 4* and *5*). Connection of the COP444C/424C to the Microbus is shown in *Figure 6*.



TL/DD/5259–7

FIGURE 6. Microbus Option Interconnect

TABLE I. Enable Register Modes — Bits EN0 and EN3

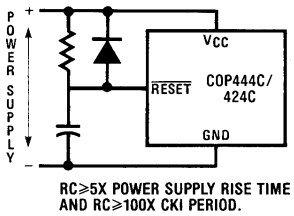
EN0	EN3	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary Counter	Input to Counter	0	SK = SKL
1	1	Binary Counter	Input to Counter	1	SK = SKL

Functional Description (Continued)

INITIALIZATION

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency at CKI is greater than 32 kHz, otherwise the external RC network shown in *Figure 7* must be connected to the $\overline{\text{RESET}}$ pin (the conditions in *Figure 7* must be met). The $\overline{\text{RESET}}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{\text{RESET}}$ input, providing it stays low for at least three instruction cycle times.

Note: If CKI clock is less than 32 kHz, the internal reset logic (option #29 = 1) MUST be disabled and the external RC circuit must be used.



TL/DD/5259–8

FIGURE 7. Power-Up Circuit

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL, T and G registers are cleared. The SKL latch is set, thus enabling SK as a clock output. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

TIMER

The timer can be operated as a time-base counter.

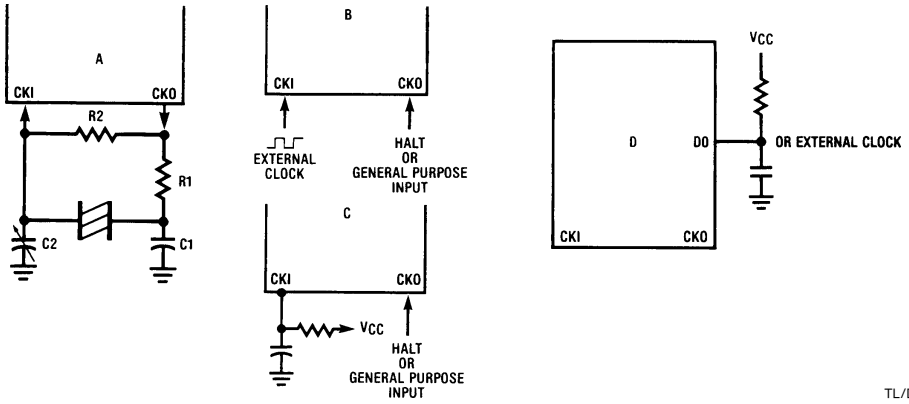
The instruction cycle frequency generated from CKI passes through a 2-bit divide-by-4 prescaler. The output of this prescaler increments the 8-bit T counter thus providing a 10-bit timer. The pre-scaler is cleared during execution of a CAMT instruction and on reset.

For example, using a 4 MHz crystal with a divide-by-16 option, the instruction cycle frequency of 250 kHz increments the 10-bit timer every 4 μs. By presetting the counter and detecting overflow, accurate timeouts between 16 μs (4 counts) and 4.096 ms (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

HALT MODE

The COP444C/445C/424C/425C/426C is a FULLY STATIC circuit; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may also be halted by the HALT instruction or by forcing CKO high when it is mask-programmed as an HALT I/O port. Once in the HALT mode, the internal circuitry does not receive any clock signal and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The chip may be awakened by one of two different methods:

- Continue function: by forcing CKO low, if it mask-programmed as an HALT I/O port, the system clock is re-enabled and the circuit continues to operate from the point where it was stopped.
- Restart: by forcing the $\overline{\text{RESET}}$ pin low (see Initialization).



TL/DD/5259–9

Crystal or Resonator

Crystal Value	Component Values			
	R1	R2	C1(pF)	C2(pF)
32 kHz	220k	20M	30	6–36
455 kHz	5k	10M	80	40
2.096 MHz	2k	1M	30	6–36
4.0 MHz	1k	1M	30	6–36

RC Controlled Oscillator (±5% R, ±5% C)

R	C	Cycle Time	V_{CC}
30k	82 pF	5–11 μs	≥4.5V
60k	100 pF	12–24 μs	2.4–4.5V

Note: 15k ≤ R ≤ 150k
50 pF ≤ C ≤ 150 pF

FIGURE 8. Oscillator Component Values

Functional Description (Continued)

The HALT mode is the minimum power dissipation state.

Note: If the user has selected dual-clock with D0 as external oscillator (option 30=2) AND the COP444C/424C is running with the D0 clock, the HALT mode — either hardware or software — will NOT be entered. Thus, the user should switch to the CKI clock to HALT. Alternatively, the user may stop the D0 clock to minimize power.

CKO PIN OPTIONS

a. Two-pin oscillator — (Crystal). See *Figure 9A*.

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. The HALT mode may be entered by program control (HALT instruction) which forces CKO high, thus inhibiting the crystal network. The circuit can be awakened only by forcing the $\overline{\text{RESET}}$ pin to a logic "0" (restart).

b. One-pin oscillator — (RC or external). See *Figure 9B*.

If a one-pin oscillator system is chosen, two options are available for CKO:

- CKO can be selected as the HALT I/O port. In that case, it is an I/O flip-flop which is an indicator of the HALT status. An external signal can over-ride this pin to start and stop the chip. By forcing a high level to CKO, the chip will stop as soon as CKI is high and CKO output will stay high to keep the chip stopped if the external driver returns to high impedance state. By forcing a low level to CKO, the chip will continue and CKO will stay low.
- As another option, CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction.

OSCILLATOR OPTIONS

There are four basic clock oscillator configurations available as shown by *Figure 8*.

a. Crystal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency optionally divided by 4, 8 or 16.

b. External Oscillator. The external frequency is optionally divided by 4, 8 or 16 to give the instruction cycle time. CKO is the HALT I/O port or a general purpose input.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port or a general purpose input.

d. Dual oscillator. By selecting the dual clock option, pin D0 is now a single pin oscillator input. Two configurations are available: RC controlled Schmitt trigger oscillator or external oscillator.

The user may software select between the D0 oscillator (in that case, the instruction cycle time equals the D0 oscillation frequency divided by 4) by setting the D0 latch high or the CKI (CKO) oscillator by resetting D0 latch low. Note that even in dual clock mode, the counter, if mask-programmed as a time-base counter, is always connected to the CKI oscillator.

For example, the user may connect up to a 1 MHz RC circuit to D0 for faster processing and a 32 kHz watch crystal to CKI and CKO for minimum current drain and time keeping.

Note: CTMA instruction is not allowed when chip is running from D0 clock.

Figures 10A and *10B* show the clock and timer diagrams with and without Dual clock.

COP445C AND COP425C 24-PIN PACKAGE OPTION

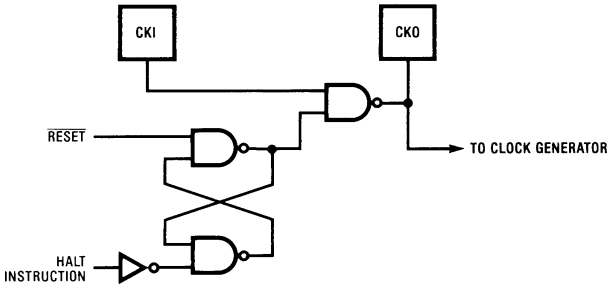
If the COP444C/424C is bonded in a 24-pin package, it becomes the COP445C/425C, illustrated in *Figure 2*, Connection diagrams. Note that the COP445C/425C does not contain the four general purpose IN inputs (IN3–IN0). Use of this option precludes, of course, use of the IN options, interrupt feature, external event counter feature, and the Microbus option which uses IN1–IN3. All other options are available for the COP445C/425C.

Note: If user selects the 24-pin package, options 9, 10, 19 and 20 must be selected as a "0" (load to V_{CC} on the IN inputs). See option list.

COP426C 20-PIN PACKAGE OPTION

If the COP425C is bonded as 20-pin device it becomes the COP426C. Note that the COP426C contains all the COP425C pins except D_0, D_1, G_0, and G_1.

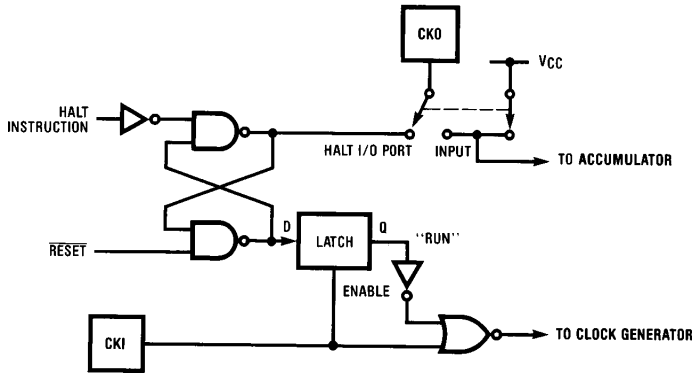
Block Diagram (Continued)



TL/DD/5259–10

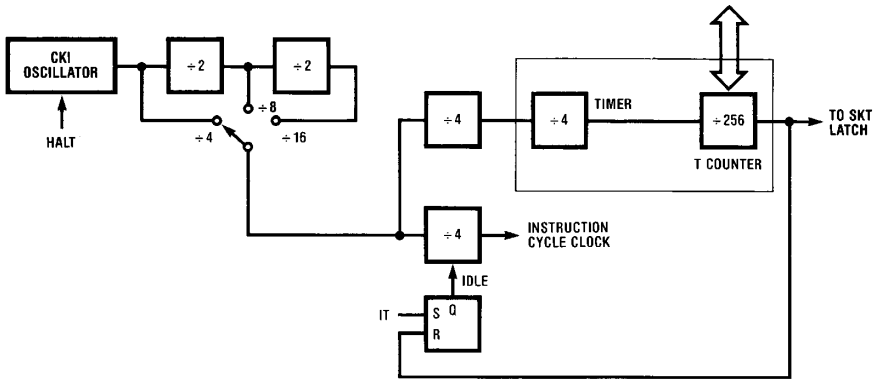
FIGURE 9A. Halt Mode — Two-Pin Oscillator

Block Diagram (Continued)



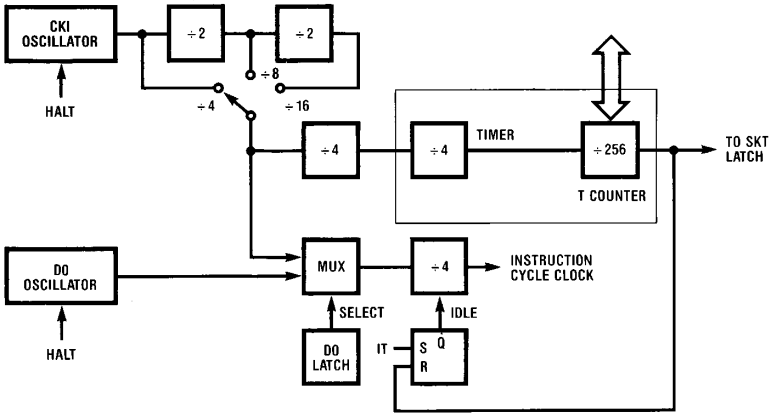
TL/DD/5259–11

FIGURE 9B. Halt Mode — One-Pin Oscillator



TL/DD/5259–12

FIGURE 10A. Clock and Timer without Dual-Clock



TL/DD/5259–13

FIGURE 10B. Clock and Timer with Dual-Clock

Instruction Set

Table II is a symbol table providing internal architecture, instruction operan and operation symbols used in the instruction set table.

TABLE II. Instruction Set Table Symbols

Symbol	Definition
Internal Architecture Symbols	
A	4-bit accumulator
B	7-bit RAM address register (6-bit for COP424C)
Br	Upper 3 bits of B (register address) (2-bit for COP424C)
Bd	Lower 4 bits of B (digit address)
C	1-bit carry register
D	4-bit data output port
EN	4-bit enable register
G	4-bit general purpose I/O port
IL	two 1-bit (IN0 and IN3) latches
IN	4-bit input port
L	8-bit TRI-STATE I/O port
M	4-bit contents of RAM addressed by B
PC	11-bit ROM address program counter
Q	8-bit latch for L port
SA,SB,SC	11-bit 3-level subroutine stack
SIO	4-bit shift register and counter
SK	Logic-controlled clock output
SKL	1-bit latch for SK output
T	8-bit timer

Table III provides the mnemonic, operand, machine code data flow, skip conditions and description of each instruction.

Instruction Operand Symbols	
d	4-bit operand field, 0–15 binary (RAM digit select)
r	3(2)-bit operand field, 0–7(3) binary (RAM register select)
a	11-bit operand field, 0–2047 (1023)
y	4-bit operand field, 0–15 (immediate data)
RAM(x)	RAM addressed by variable x
ROM(x)	ROM addressed by variable x

Operational Symbols	
+	Plus
−	Minus
$\rightarrow$	Replaces
$\longleftrightarrow$	Is exchanged with
=	Is equal to
$\overline{A}$	One's complement of A
$\oplus$	Exclusive-or
:	Range of values

TABLE III. COP444C/445C Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011 | 0000	A + C + RAM(B) $\rightarrow$ A Carry $\rightarrow$ C	Carry	Add with Carry, Skip on Carry
ADD		31	0011 | 0001	A + RAM(B) $\rightarrow$ A	None	Add RAM to A
ADT		4A	0100 | 1010	A + 10_{10} $\rightarrow$ A	None	Add Ten to A
AISC	y	5−	0101 | y	A + y $\rightarrow$ A	Carry	Add Immediate. Skip on Carry (y $\neq$ 0)
CASC		10	0001 | 0000	$\overline{A}$ + RAM(B) + C $\rightarrow$ A Carry $\rightarrow$ C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0000 | 0000	0 $\rightarrow$ A	None	Clear A
COMP		40	0100 | 0000	$\overline{A}$ $\rightarrow$ A	None	Ones complement of A to A
NOP		44	0100 | 0100	None	None	No Operation
RC		32	0011 | 0010	"0" $\rightarrow$ C	None	Reset C
SC		22	0010 | 0010	"1" $\rightarrow$ C	None	Set C
XOR		02	0000 | 0010	A $\oplus$ RAM(B) $\rightarrow$ A	None	Exclusive-OR RAM with A

Instruction Set (Continued)

Table III. COP444C/445C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER CONTROL INSTRUCTIONS						
JID		FF	1111 1111	ROM ($PC_{10:8}$ A,M) → $PC_{7:0}$	None	Jump Indirect (Notes 1, 3)
JMP	a	6–	0110 0 $a_{10:8}$	a → PC	None	Jump
		––	$a_{7:0}$			
JP	a	––	1 $a_{6:0}$ (pages 2,3 only) or	a → $PC_{6:0}$	None	Jump within Page (Note 4)
		––	11 $a_{5:0}$ (all other pages)	a → $PC_{5:0}$		
JSRP	a	––	10 $a_{5:0}$	PC + 1 → SA → SB → SC 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6–	0110 1 $a_{10:8}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
		––	$a_{7:0}$			
RET		48	0100 1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100 1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33	0011 0011		None	HALT Processor
		38	0011 1000			
IT		33	0011 0011			IDLE till Timer
		39	0011 1001		None	Overflows then Continues
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33	0011 0011	A → $T_{7:4}$		
		3F	0011 1111	RAM(B) → $T_{3:0}$	None	Copy A, RAM to T
CTMA		33	0011 0011	$T_{7:4}$ → RAM(B)		
		2F	0010 1111	$T_{3:0}$ → A	None	Copy T to RAM, A (Note 9)
CAMQ		33	0011 0011	A → $Q_{7:4}$	None	Copy A, RAM to Q
		3C	0011 1100	RAM(B) → $Q_{3:0}$		
CQMA		33	0011 0011	$Q_{7:4}$ → RAM(B)	None	Copy Q to RAM, A
		2C	0010 1100	$Q_{3:0}$ → A		
LD	r	–5	00 r 0101 (r = 0:3)	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23	0010 0011	RAM(r,d) → A	None	Load A with RAM pointed to directly by r,d
		––	0 r d			
LQID		BF	1011 1111	ROM($PC_{10:8}$,A,M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0	4C	0100 1100	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	0100 0101	0 → $RAM(B)_1$		
	2	42	0100 0010	0 → $RAM(B)_2$		
	3	43	0100 0011	0 → $RAM(B)_3$		
SMB	0	4D	0100 1101	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	0100 0111	1 → $RAM(B)_1$		
	2	46	0100 0110	1 → $RAM(B)_2$		
	3	4B	0100 1011	1 → $RAM(B)_3$		

Instruction Set (Continued)

Table III. COP444C/445C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (Continued)						
STII	y	7−	0111 | y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate 1 and Increment Bd
X	r	−6	00 | r | 0110 (r=0:3)	RAM(B) ⟷ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 −−	0010 | 0011 1 | r | d	RAM(r,d) ⟷ A	None	Exchange A with RAM Pointed to Directly by r,d
XDS	r	−7	00 | r | 0111 (r=0:3)	RAM(B) ⟷ A Bd−1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd. Exclusive-OR Br with r
XIS	r	−4	00 | r | 0100 (r=0:3)	RAM(B) ⟷ A Bd+1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 | 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 | 1110	Bd → A	None	Copy Bd to A
LBI	r,d	−−	00 | r | (d−1) (r=0:3: d=0,9:15) or	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 6)
		33 −−	0011 | 0011 1 | r | d (any r, any d)			
LEI	y	33 6−	0011 | 0011 0110 | y	y → EN	None	Load EN Immediate (Note 7)
XABR		12	0001 | 0010	A ⟷ Br	None	Exchange A with Br (Note 8)
TEST INSTRUCTIONS						
SKC		20	0010 | 0000		C = "1"	Skip if C is True
SKE		21	0010 | 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011 | 0011 0010 | 0001		$G_{3:0}=0$	Skip if G is Zero (all 4 bits)
SKGBZ		33	0011 | 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 | 0001	2nd byte	$G_0=0$	
	1	11	0001 | 0001		$G_1=0$	
	2	03	0000 | 0011		$G_2=0$	
	3	13	0001 | 0011		$G_3=0$	
SKMBZ	0	01	0000 | 0001		$RAM(B)_0=0$	Skip if RAM Bit is Zero
	1	11	0001 | 0001		$RAM(B)_1=0$	
	2	03	0000 | 0011		$RAM(B)_2=0$	
	3	13	0001 | 0011		$RAM(B)_3=0$	
SKT		41	0100 | 0001		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)

Instruction Set (Continued)

Table III. COP444C/445C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33	0011 0011	G ⟶ A	None	Input G Ports to A
		2A	0010 1010			
ININ		33	0011 0011	IN ⟶ A	None	Input IN Inputs to A (Note 2)
		28	0010 1000			
INIL		33	0011 0011	IL_3, CKO,''0'', IL_0 ⟶ A	None	Input IL Latches to A (Note 3)
		29	0010 1001			
INL		33	0011 0011	$L_{7:4}$ ⟶ RAM(B)	None	Input L Ports to RAM,A
		2E	0010 1110	$L_{3:0}$ ⟶ A		
OBD		33	0011 0011	Bd ⟶ D	None	Output Bd to D Outputs
		3E	0011 1110			
OGI	y	33	0011 0011	y ⟶ G	None	Output to G Ports Immediate
		5—	0101 y			
OMG		33	0011 0011	RAM(B) ⟶ G	None	Output RAM to G Ports
		3A	0011 1010			
XAS		4F	0100 1111	A ⟷ SIO, C ⟶ SKL	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ instruction is not available on the 24-pin packages since these devices do not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the ''d'' data *minus 1*, e.g., to load the lower four bits of B(Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a ''1'' or ''0'' in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

Note 8: For 2K ROM devices, A ⟷ Br (0 ⟶ A3). For 1K ROM devices, A ⟷ Br (0,0 ⟶ A3, A2).

Note 9: Do not use CTMA instruction when dual-clock option is selected and part is running from D_0 clocks.

Description of Selected Instructions

XAS INSTRUCTION

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. If SIO is selected as a shift register, an XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC10:PC8,A,M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction ''pushes'' the stack (PC + 1 ⟶ SA ⟶ SB ⟶ SC) and replaces the least significant 8 bits of the PC as follows: A ⟶ PC(7:4), RAM(B) ⟶ PC(3:0), leaving PC(10), PC(9) and PC(8) unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is ''popped'' (SC ⟶ SB ⟶ SA ⟶ PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB ⟶ SC, the previous contents of SC are lost.

Note: LQID uses 2 instruction cycles if executed, one if skipped.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, PC10:8,A,M. PC10,PC9 and PC8 are not affected by JID.

Note: JID uses 2 instruction cycles if executed, one if skipped.

SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

Note: If the most significant bit of the T counter is a 1 when a CAMT instruction loads the counter, the overflow flag will be set. The following sample of codes should be used when loading the counter:

```
CAMT   ; load T counter
SKT    ; skip if overflow flag is set and reset it
NOP
```

IT INSTRUCTION

The IT (idle till timer) instruction halts the processor and puts it in an idle state until the time-base counter overflows. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped.

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL3 and IL0, CKO and 0 into A. The IL3 and IL0 latches are set if a low-going pulse (''1'' to ''0'') has occurred on the IN3 and IN0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a ''1'' will be placed in A2. A0 is input into A1. IL latches are cleared on reset. IL latches are not available on the COP445C/425C, and COP426C.

INSTRUCTION SET NOTES

a. The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.

c. The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID is the last word of a page, it operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

Note: The COP424C/425C/426C needs only 10 bits to address its ROM. Therefore, the eleventh bit (P10) is ignored.

Power Dissipation

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal or resonator generated clock input will draw additional current. An R/C oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate operating current drain.

$$I_{CO} = I_Q + V \times 40 \times Fi + V \times 1400 \times Fi/Dv$$

where I_{CO} = chip operating current drain in microamps

I_Q = quiescent leakage current (from curve)

Fi = CKI frequency in MegaHertz

V = chip V_{CC} in volts

Dv = divide by option selected

For example at 5 volts V_{CC} and 400 kHz (divide by 4)

$$I_{CO} = 20 + 5 \times 40 \times 0.4 + 5 \times 1400 \times 0.4/4$$

$$I_{CO} = 20 + 80 + 700 = 800\ \mu A$$

At 2.4 volts V_{CC} and 30 kHz (divide by 4)

$$I_{CO} = 6 + 2.4 \times 40 \times 0.03 + 2.4 \times 1400 \times 0.03/4$$

$$I_{CO} = 6 + 2.88 + 25.2 = 34.08\ \mu A$$

Power Dissipation (Continued)

If an IT instruction is executed, the chip goes into the IDLE mode until the timer overflows. In IDLE mode, the current drain can be calculated from the following equation:

$$Ici = I_Q + V \times 40 \times Fi$$

For example, at 5 volts V_{CC} and 400 kHz

$$Ici = 20 + 5 \times 40 \times 0.4 = 100\ \mu A$$

The total average current will then be the weighted average of the operating current and the idle current:

$$Ita = I_{CO} \times \frac{To}{To + Ti} + Ici \times \frac{Ti}{To + Ti}$$

where: Ita = total average current
I_{CO} = operating current
Ici = idle current
To = operating time
Ti = idle time

I/O OPTIONS

Outputs have the following optional configurations, illustrated in *Figure 11*:

a. Standard — A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b. Low Current — This is the same configuration as a. above except that the sourcing current is much less.

c. Open Drain — An N-channel device to ground only, allowing external pull-up as required by the user's application.

d. Standard TRI-STATE L Output — A CMOS output buffer similar to a. which may be disabled by program control.

e. Low-Current TRI-STATE L Output — This is the same as d. above except that the sourcing current is much less.

f. Open-Drain TRI-STATE L Output — This has the N-channel device to ground only.

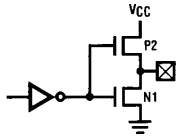
All inputs have the following options:

g. Input with on chip load device to V_{CC}.

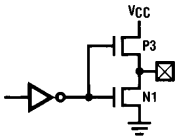
h. Hi-Z input which must be driven by the users logic.

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available: Select the low-current output option. Now, by setting the output registers to a logic ''1'' level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic ''1'' level and the L drivers MUST BE ENABLED by an LEI instruction (see description above).

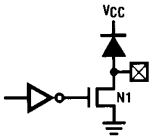
All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 12* for each of these devices to allow the designer to effectively use these I/O configurations.



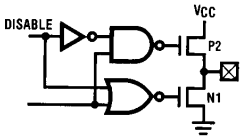
a. Standard Push-Pull Output



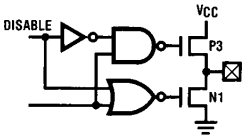
b. Low Current Push-Pull Output



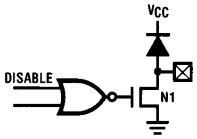
c. Open-Drain Output



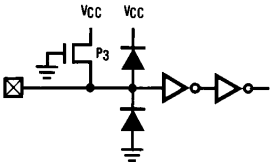
d. Standard TRI-STATE "L" Output



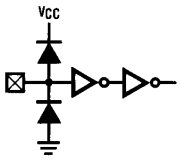
e. Low Current TRI-STATE "L" Output



f. Open Drain TRI-STATE "L" Output



g. Input with Load

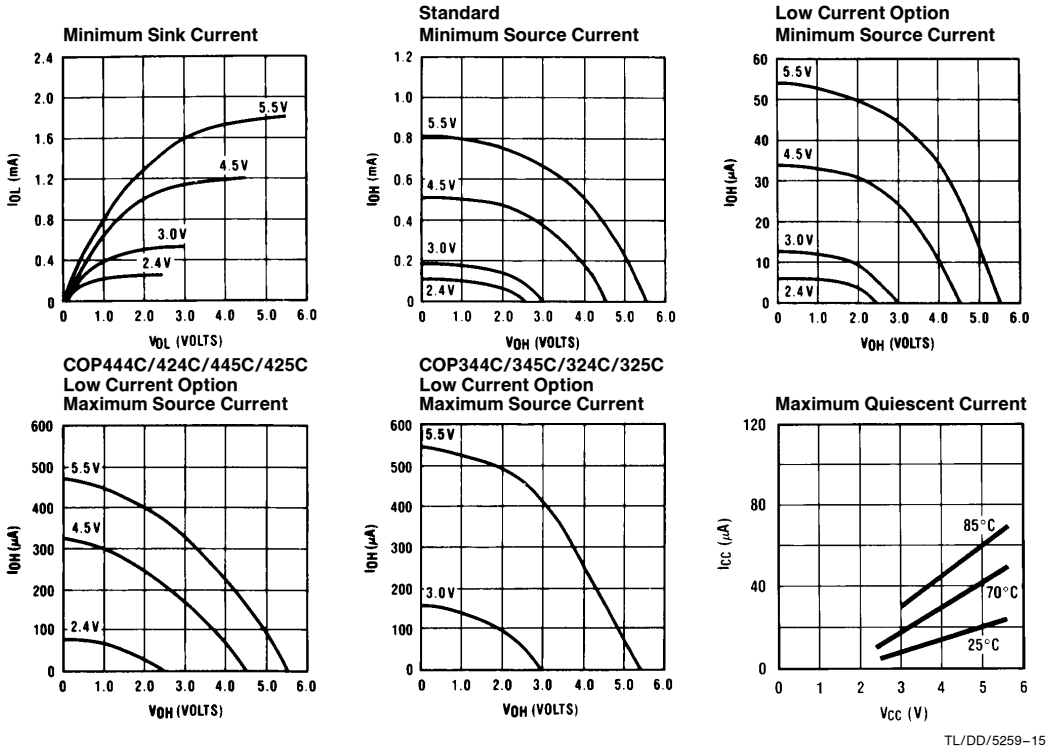


h. Hi-Z Input

TL/DD/5259–14

FIGURE 11. Input/Output Configurations

Power Dissipation (Continued)



TL/DD/5259–15

FIGURE 12. Input/Output Characteristics

Option List

The COP444C/445C/424C/425C/COP426C mask-programmable options are assigned numbers which correspond with the COP444C/424C pins.

The following is a list of options. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

PLEASE FILL OUT THE OPTION TABLE on the next page. Xerox the option data and send it in with your disk or EPROM.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Pin
- = 0: clock generator output to crystal/resonator
- = 1: HALT I/O port
- = 2: general purpose input with load device to V_{CC}
- = 3: general purpose input, high-Z

Option 3: CKI input
- = 0: Crystal controlled oscillator input divide by 4
- = 1: Crystal controlled oscillator input divide by 8
- = 2: Crystal controlled oscillator input divide by 16
- = 4: Single-pin RC controlled oscillator (divide by 4)
- = 5: External oscillator input divide by 4
- = 6: External oscillator input divide by 8
- = 7: External oscillator input divide by 16

Option 4: $\overline{\text{RESET}}$ input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 5: L7 Driver
- = 0: Standard TRI-STATE push-pull output
- = 1: Low-current TRI-STATE push-pull output
- = 2: Open-drain TRI-STATE output

Option 6: L6 Driver — (same as option 5)

Option 7: L5 Driver — (same as option 5)

Option 8: L4 Driver — (same as option 5)

Option 9: IN1 input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 10: IN2 input — (same as option 9)

Option 11 = 0: V_{CC} Pin — no option available

Option 12: L3 Driver — (same as option 5)

Option 13: L2 Driver — (same as option 5)

Option 14: L1 Driver — (same as option 5)

Option 15: L0 Driver — (same as option 5)

Option 16: SI input — (same as option 9)

Option 17: SO Driver
- = 0: Standard push-pull output
- = 1: Low-current push-pull output
- = 2: Open-drain output

Option List (Continued)

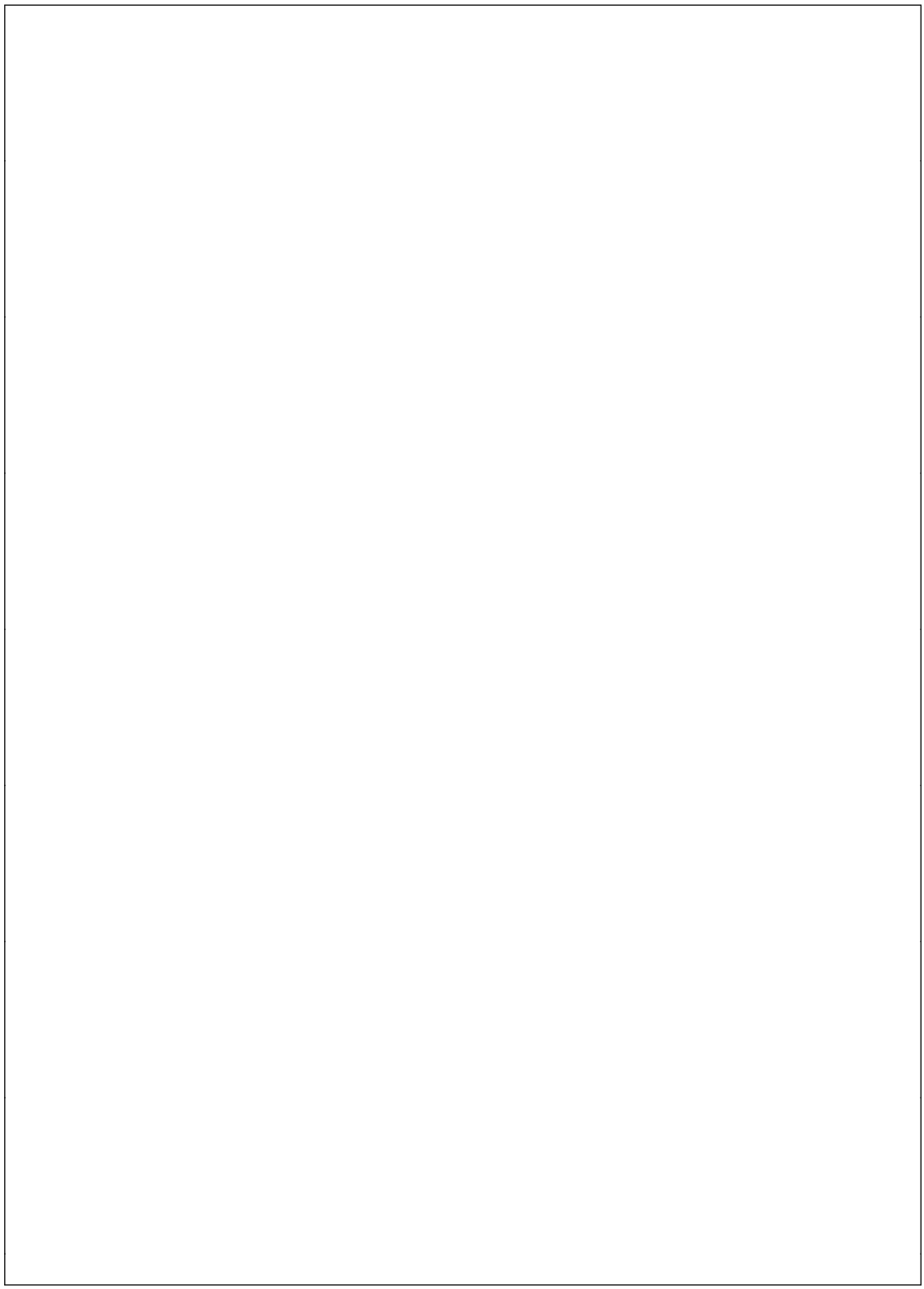
Option 18: SK Driver — (same as option 17)
Option 19: IN0 Input — (same as option 9)
Option 20: IN3 Input — (same as option 9)
Option 21: G0 I/O Port — (same as option 17)
Option 22: G1 I/O Port — (same as option 17)
Option 23: G2 I/O Port — (same as option 17)
Option 24: G3 I/O Port — (same as option 17)
Option 25: D3 Output — (same as option 17)
Option 26: D2 Output — (same as option 17)
Option 27: D1 Output — (same as option 17)
Option 28: D0 Output — (same as option 17)
Option 29: Internal Initialization Logic
= 0: Normal operation
= 1: No internal initialization logic
Option 30: Dual Clock
= 0: Normal operation
= 1: Dual Clock. D0 RC oscillator
= 2: Dual Clock. D0 ext. clock input
} (opt. #28 must = 2)
Option 31: Timer
= 0: No Option Available
Option 32: Microbus
= 0: Normal
= 1: Microbus (opt. #31 must = 0)
Option 33: COP bonding
(1k and 2K Microcontroller)
= 0: 28-pin package
= 1: 24-pin package
= 2: Same die purchased in both 24 and 28 pin version.
(1K Microcontroller only)
= 3: 20-pin package
= 4: 28- and 20-pin package
= 5: 24- and 20-pin package
= 6: 28-, 24- and 20-pin package

Note:—if opt. #33 = 1 or 2 then opt. #9, 10, 19, 20 and 32 must = 0—if opt. #33 = 3, 4, 5 or 6 then opt. #9, 10, 19, 20, 21, 22, 30 and 32 must = 0.

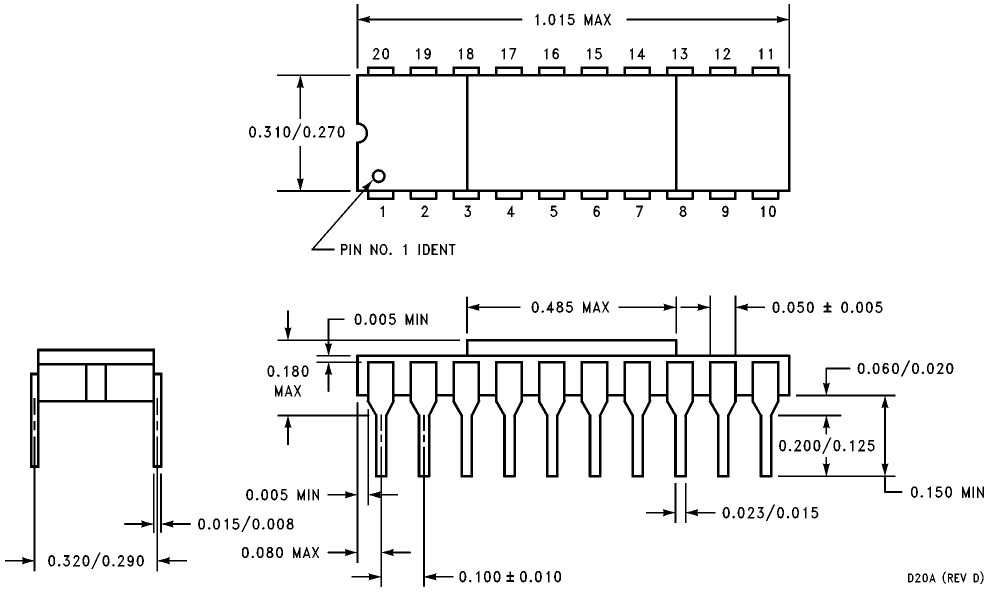
Option Table

The following option information is to be sent to National along with the EPROM.

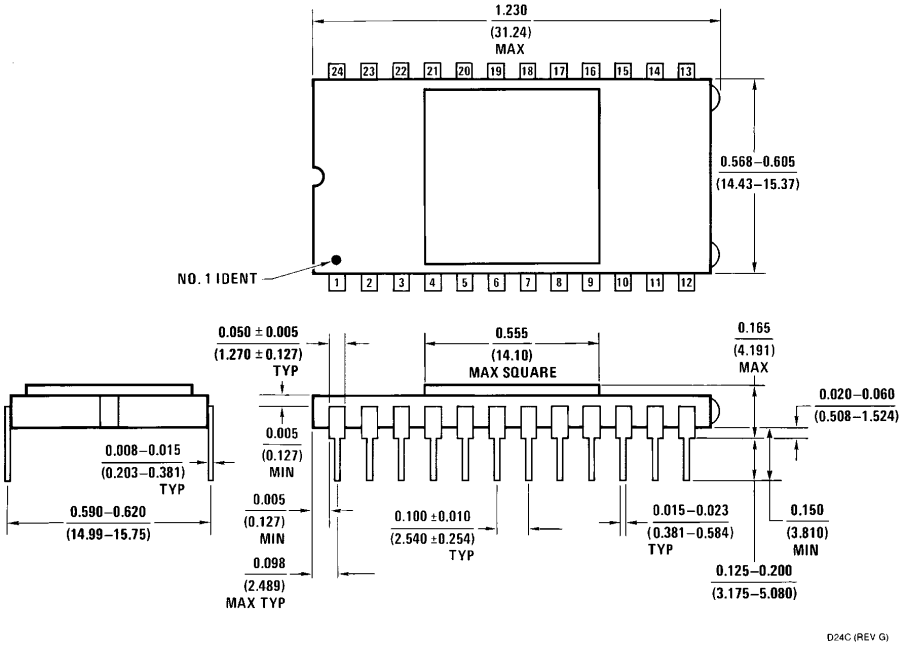
OPTION DATA			OPTION DATA		
OPTION 1 VALUE =	0	IS: GROUND PIN	OPTION 17 VALUE =		IS: SO DRIVER
OPTION 2 VALUE =		IS: CKO PIN	OPTION 18 VALUE =		IS: SK DRIVER
OPTION 3 VALUE =		IS: CKI INPUT	OPTION 19 VALUE =		IS: IN0 INPUT
OPTION 4 VALUE =		IS: RESET INPUT	OPTION 20 VALUE =		IS: IN3 INPUT
OPTION 5 VALUE =		IS: L(7) DRIVER	OPTION 21 VALUE =		IS: G0 I/O PORT
OPTION 6 VALUE =		IS: L(6) DRIVER	OPTION 22 VALUE =		IS: G1 I/O PORT
OPTION 7 VALUE =		IS: L(5) DRIVER	OPTION 23 VALUE =		IS: G2 I/O PORT
OPTION 8 VALUE =		IS: L(4) DRIVER	OPTION 24 VALUE =		IS: G3 I/O PORT
OPTION 9 VALUE =		IS: IN1 INPUT	OPTION 25 VALUE =		IS: D3 OUTPUT
OPTION 10 VALUE =		IS: IN2 INPUT	OPTION 26 VALUE =		IS: D2 OUTPUT
OPTION 11 VALUE =		IS: VCC PIN	OPTION 27 VALUE =		IS: D1 OUTPUT
OPTION 12 VALUE =		IS: L(3) DRIVER	OPTION 28 VALUE =		IS: D0 OUTPUT
OPTION 13 VALUE =		IS: L(2) DRIVER	OPTION 29 VALUE =		IS: INT INIT LOGIC
OPTION 14 VALUE =		IS: L(1) DRIVER	OPTION 30 VALUE =		IS: DUAL CLOCK
OPTION 15 VALUE =		IS: L(0) DRIVER	OPTION 31 VALUE =	0	IS: TIMER
OPTION 16 VALUE =		IS: SI INPUT	OPTION 32 VALUE =		IS: MICROBUS
			OPTION 33 VALUE =		IS: COP BONDING



Physical Dimensions inches (millimeters)

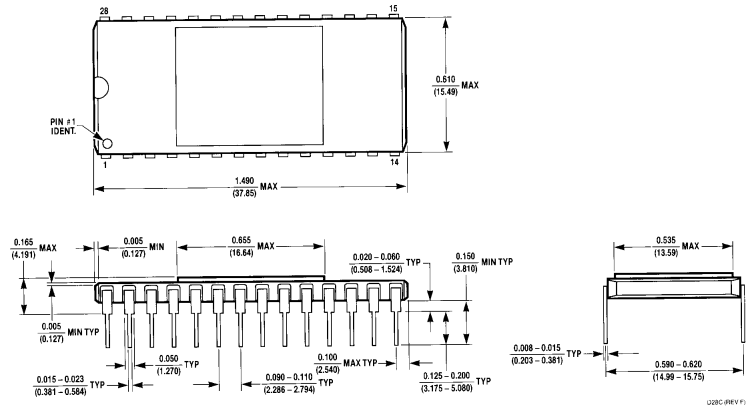


20-Lead Hermetic Dual-In-Line Package (D)
Order Number COP326C-XXX/D, COP426C-XXX/D
NS Package Number D20A

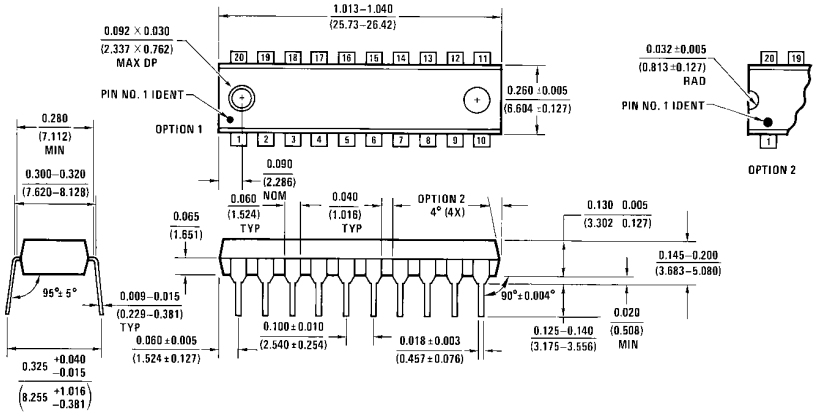


24-Lead Hermetic Dual-In-Line Package (D)
Order Number COP425C-XXX/D, COP325C-XXX/D,
COP445C-XXX/D, COP345C-XXX/D
NS Package Number D24C

Physical Dimensions inches (millimeters) (Continued)

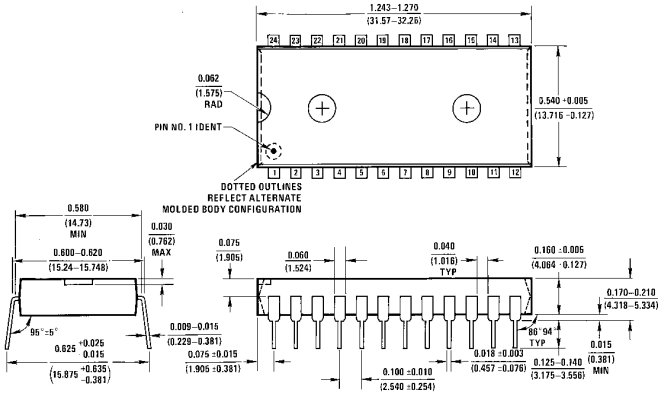


28-Lead Hermetic Dual-In-Line Package (D)
Order Number COP424C-XXX/D, COP324C-XXX/D,
COP444C-XXX/D, COP344C-XXX/D
NS Package Number D28C

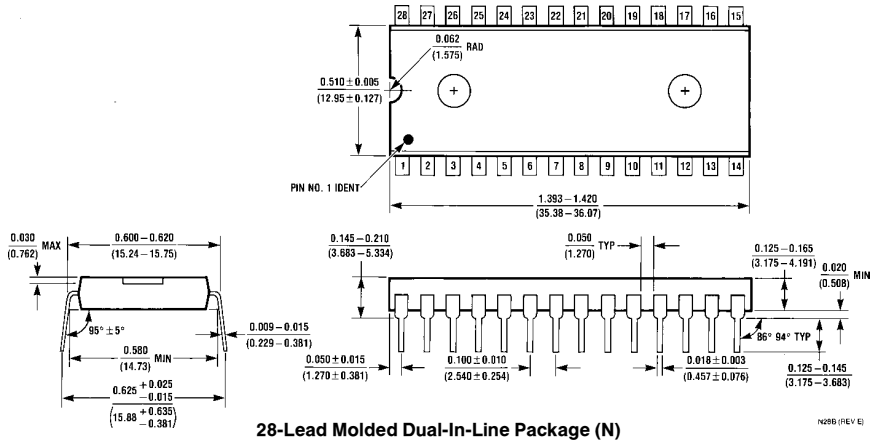


20-Lead Molded Dual-In-Line Package (N)
Order Number COP426C-XXX/N and COP326C-XXX/N
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



24-Lead Molded Dual-In-Line Package (N)
Order Number COP425C-XXX/N, COP325C-XXX/N,
COP445C-XXX/N, COP345C-XXX/N
NS Package Number N24A



28-Lead Molded Dual-In-Line Package (N)
Order Number COP424C-XXX/N, COP324C-XXX/N,
COP444C-XXX/N, COP344C-XXX/N
NS Package Number N28B

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
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National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
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Tel: (852) 2737-1600
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Tel: 81-043-299-2309
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