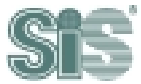

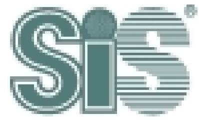

SiS55x System Design Guide

Preliminary

Rev. 0.9

March 14, 2001

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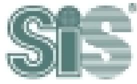

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1 Introduction

The SiS55x integrates the high performance Host Bus interface, the DRAM controller, the IDE controller, the PCI interface, 2D Graphics accelerator, Digital Visual Interface (DVI) interface, and Super South-Bridge. The super south-bridge consists of ACPI, KBC, RTC, USB, and LPC. The SiS55x system block diagram is illustrated below:

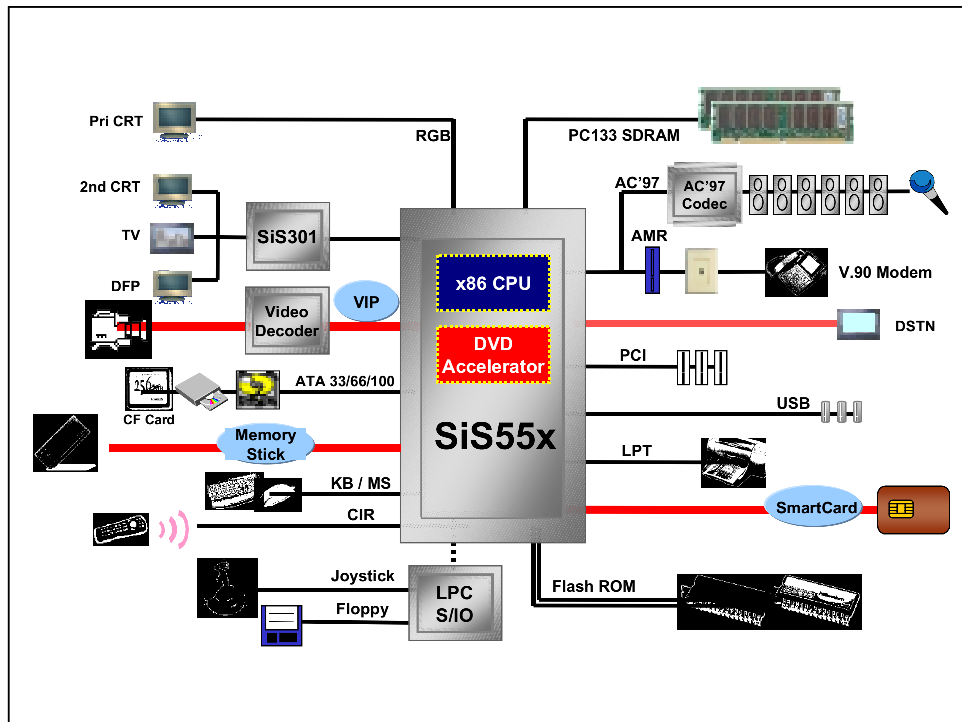


Figure 1. SiS55x System Block Diagram

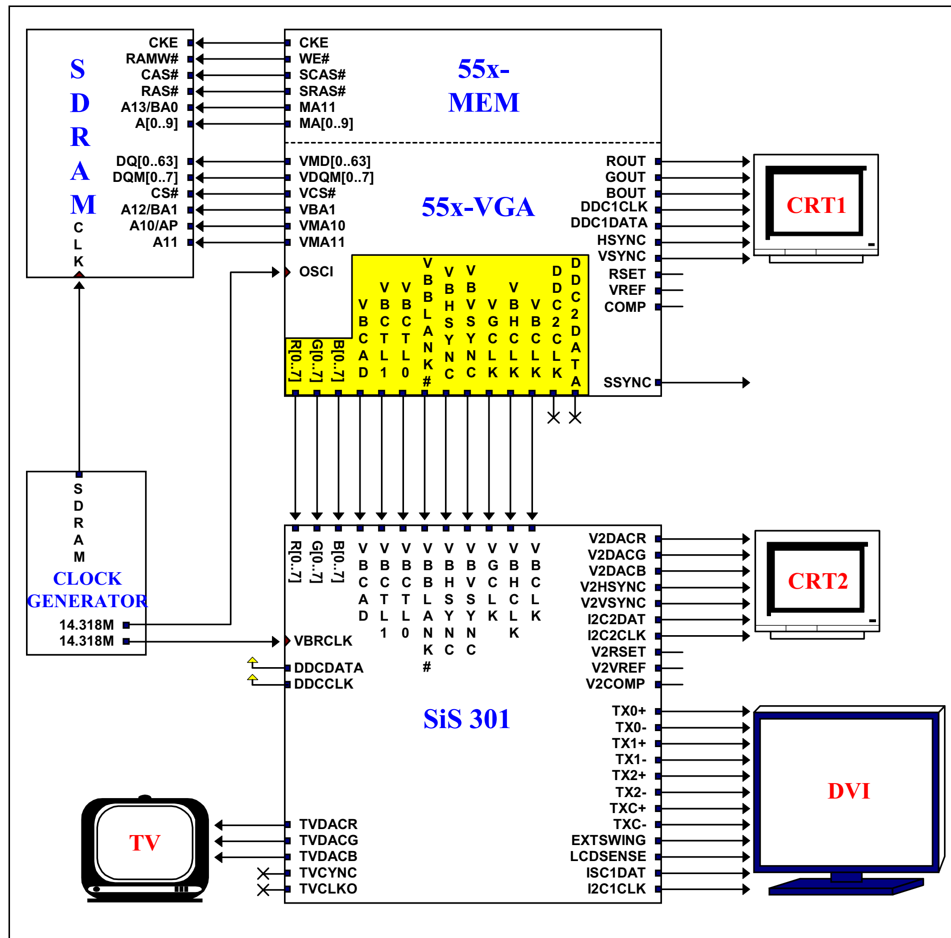


Figure 2. SiS55x Integrated VGA Subsystem Block Diagram

1.1 Preface

This document provides valuable references and design guidelines for developing SiS55x based on Socket 7 system. To shorten the design cycle and minimize the debugging period, subjects related with motherboard design and layout phases are covered in this document.

Chapter two indicates general motherboard design considerations. This chapter begins with the pin assignment, component placement and BGA layout guidelines, which are essential for achieving a cost-effective and compact 4-layer motherboard. Followed with motherboard stack-up and impedance control these two topics are increasingly important for high-speed digital interconnections. The system power requirement of SiS55x is discussed in the last section of this chapter.

In chapter three, most of the major design guidelines are presented. The signal integrity and noise immunity are crucial for some critical signals. Moreover, the layout considerations, topology and length constrain, are described for these

signals.

In chapter four, the signal connectivity is listed. Developer can employ this chapter as a quick checklist for their application circuit reviews of SiS55x design.

2 Motherboard Considerations

2.1 Pin Assignments

To route all signals in a four-layer motherboard, not only the pin assignment in SiS55x was able to minimize the crossover between different kinds of signals, but also the signal arrangement in SiS55x followed the bus orders.

On the basis of the Connector placement factor, the SiS55x signal arrangements are illustrated in Figure 3.

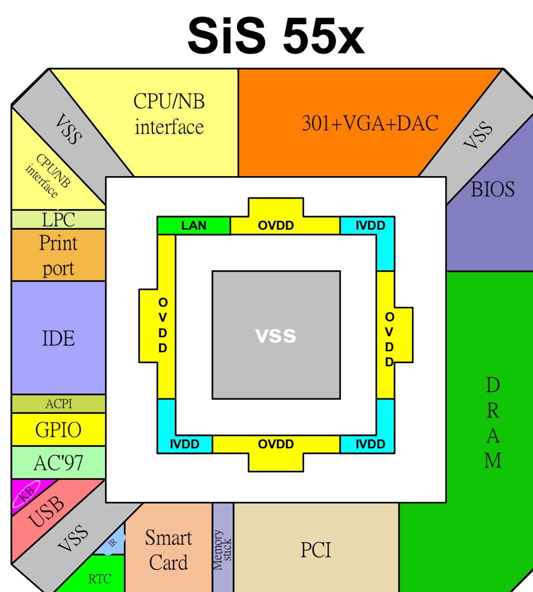


Figure 3. Signal Arrangement of SiS55x

2.2 Motherboard Placement

The component placement examples describing the recommended placements and signal routing like a Micro-ATX motherboard are illustrated as following figures:

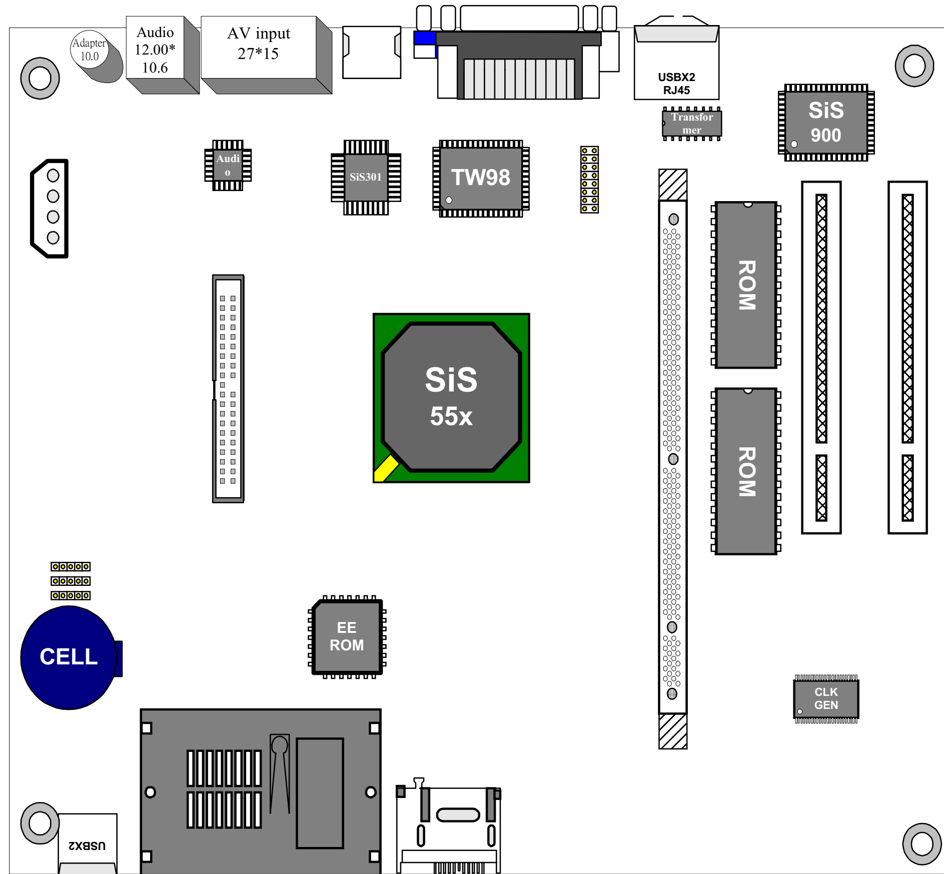


Figure 4. Component Placement and Signal Routing for Micro-ATX Form Factor

2.3 BGA Component Layout Guideline

SiS55x package is a 686 ball BGA. There are 6 rows of balls arranged along the edge of SiS55x package. To achieve a 4-layer motherboard, some routing techniques are required and narrated in the following text. The signals on the outer 3 rows can be routed on the component side and the signals on the inner 3 rows can be routed on the solder side. Therefore, it is necessary to put two traces between two nearby pads. The suggested dimensions are listed below and drawn in Figure 5 ~Figure 8**.**

Traces for Signals:

Trace Width: 6 mils

Trace Space: 6 mils

Pads for Signals:

Pad Diameter: 20 mils

Vias for Signals:

Via Pad Diameter: 24 mils

Via Hole Diameter: 12 mils

Trace for Power and Ground:

Trace Width: at lease 12 mils

Pads for Power and Ground:

Pad Diameter: 24 mils

Vias for Power and Ground:

Via Pad Diameter: 32 mils

Via Hole Diameter: 16 mils

Note: All the Vias must be covered by solder mask. The center distance of two nearby balls is 50 mils.

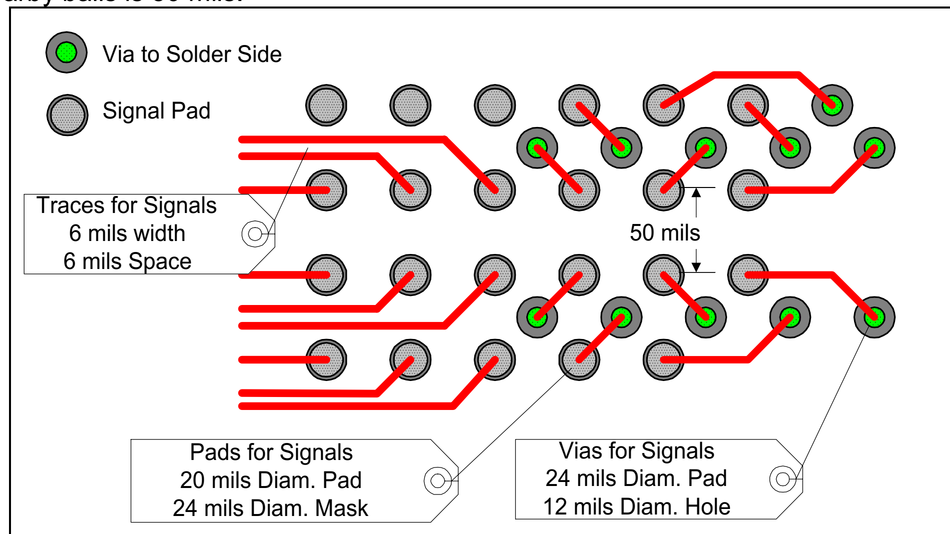


Figure 5. Dimension for BGA Signal Routing

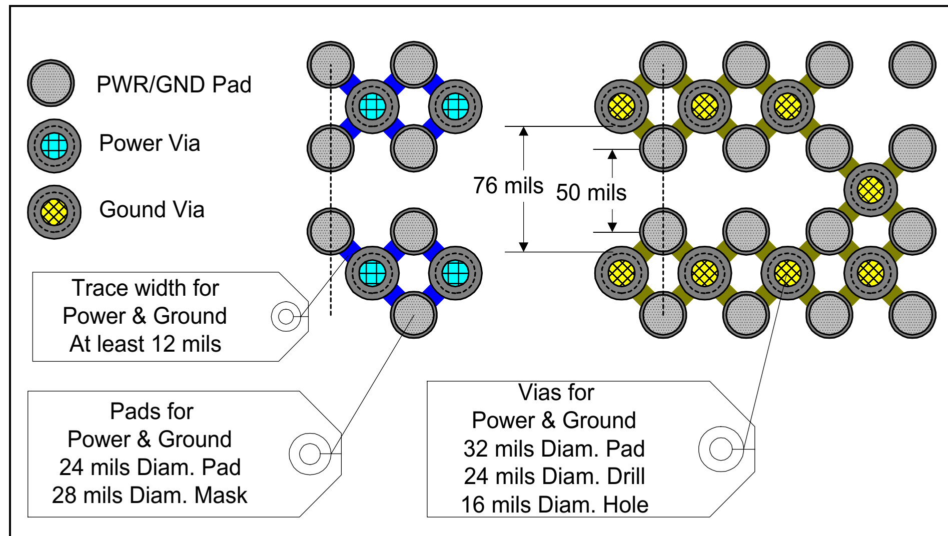


Figure 6. Dimension for BGA Power/Ground Routing

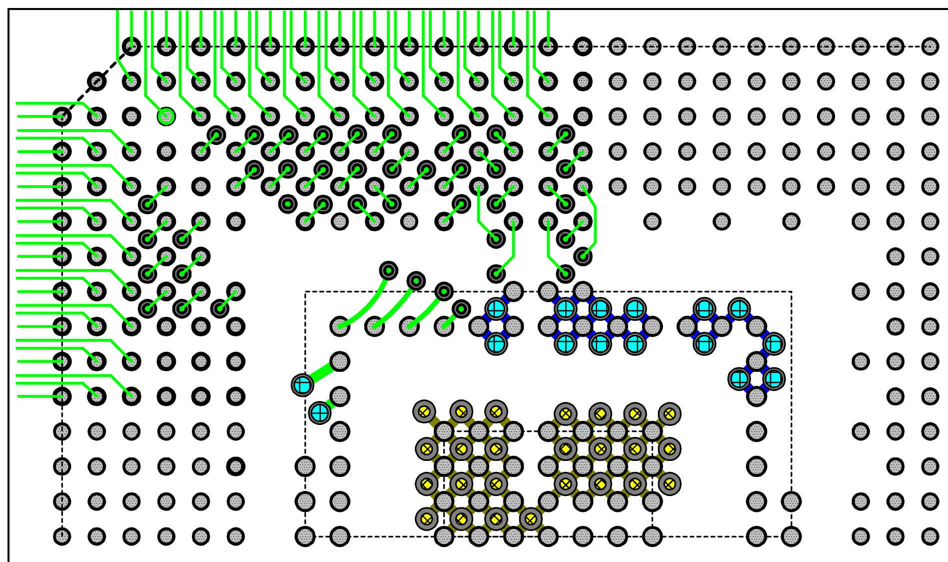


Figure 7. Example for BGA Layout

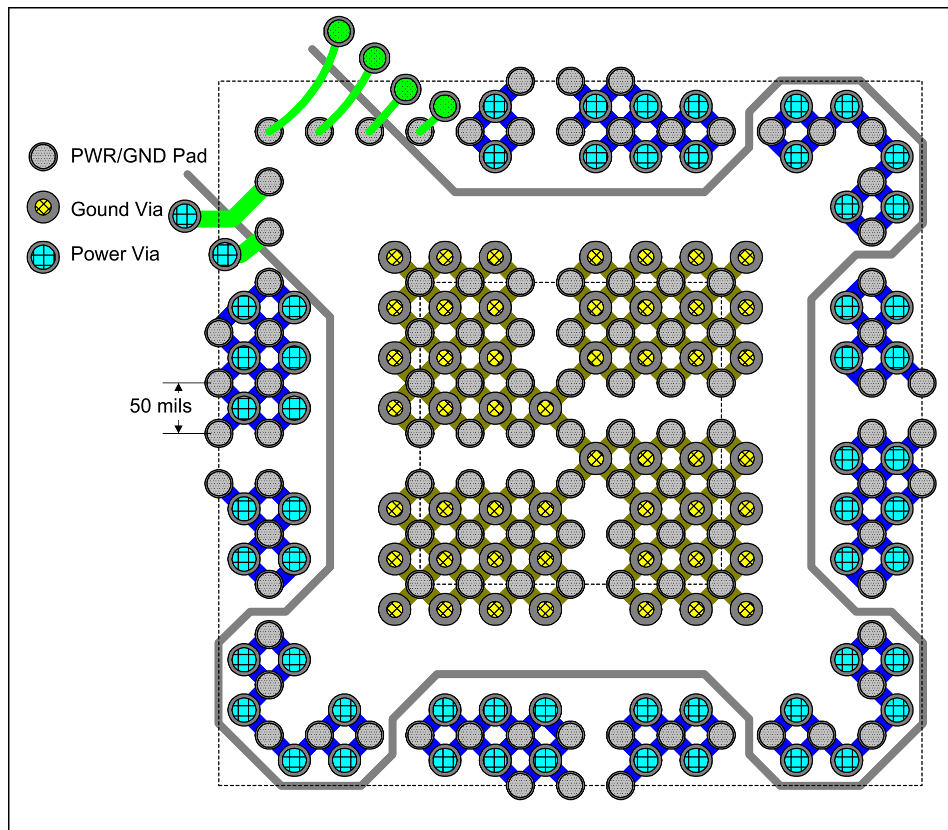


Figure 8. The Example for BGA Power/Ground Routing

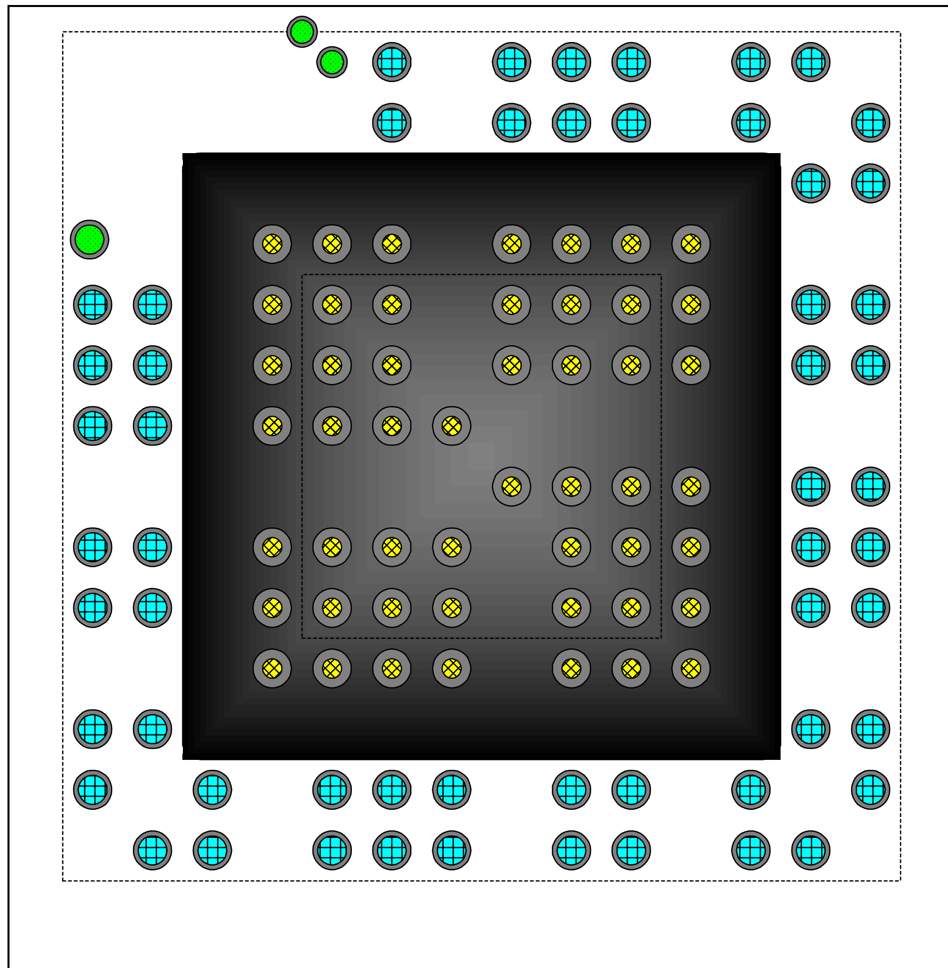


Figure 9. The Example for BGA Ground Vias Mask (Solder Side)

Note: For reasons of heat sink, SiS suggests lapping the copper foil over all the BGA ground Vias on the solder side.

The BGA 686L (37.5X37.5 mm) package drawing and dimensions is illustrated in Figure 10.

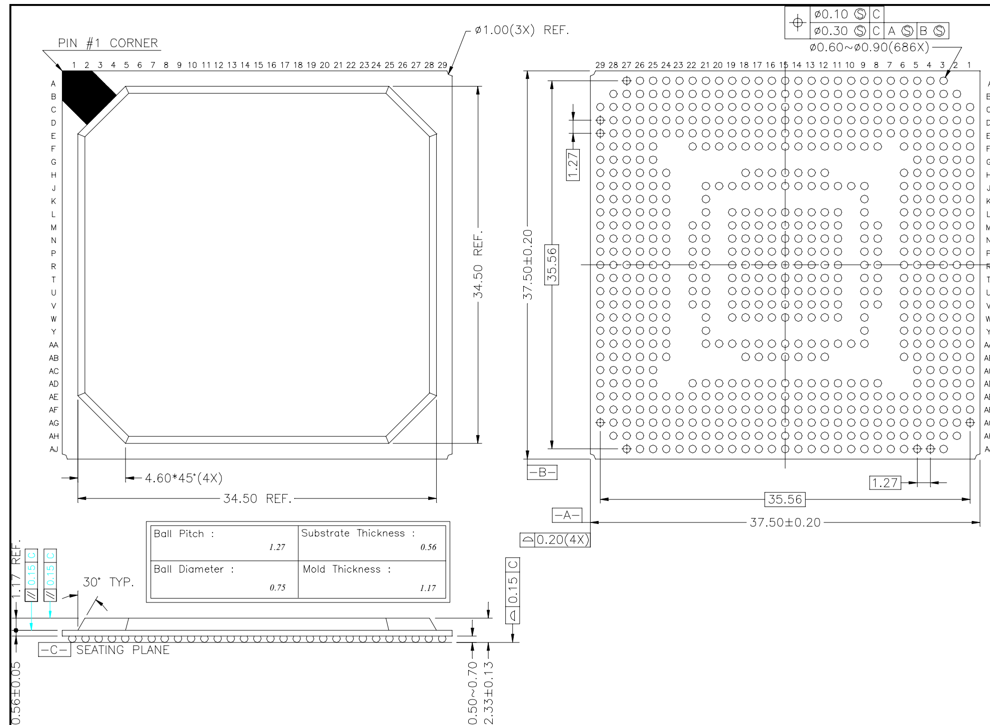


Figure 10. BGA 686 Ball Package

2.4 Board Description

2.4.1 Recommendations

A SiS55x based system can be designed with a 4-layer board. The stack-up arrangement is crucial for reducing EMI problem. The most common stack-up arrangement is in the sequence of component plane, ground plane, power plane and solder plane.

Note that the power plane and ground plane had better not be separated by any signal. If there is a signal, which has to be routed on the internal layers, it should be only on the power plane and the trace length must be as short as possible.

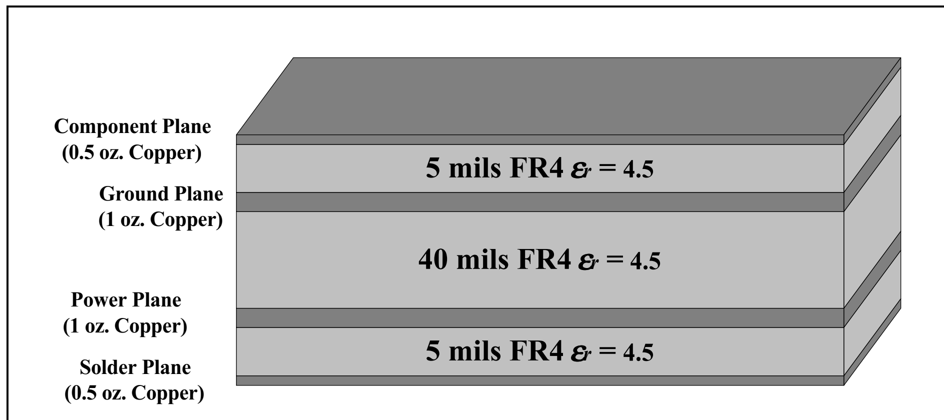


Figure 11. 4-Layer PCB Stack-up

SiS recommends that the copper thickness of component layer is 0.7 mils (0.5 Oz); the ground layer is 1.4 mils (1.0 Oz); the power layer is 1.4 mils (1.0 Oz); and the solder layer is 0.7 mils (0.5 Oz). The thickness of dielectric layer between Signal layer and its Reference plane is 5 mils; between Power plane and Ground plane is 40 mils. The thinner material, the metal of signal line or the substrate of transmission line, works better for high frequency signal shielding, against the Crosstalk and Electromagnetic Interference (EMI). The dielectric constant of substrate is recommended between 4.5 with 0.3 tolerance.

2.4.2 Miscellaneous Boards and Crosstalk Effects

For miscellaneous motherboard designs, SiS provides information for several trace models. Table 1 includes the two parameters of importance in the characteristics of transmission lines, characteristic impedance and propagation delay. It also contains the capacitance and inductance of three parallel lines. The simulation structure of transmission line is illustrated in Figure 12 below. In addition, all the data in Table 1 are simulated by XNS, the Quad Design's Crosstalk Network Simulator.

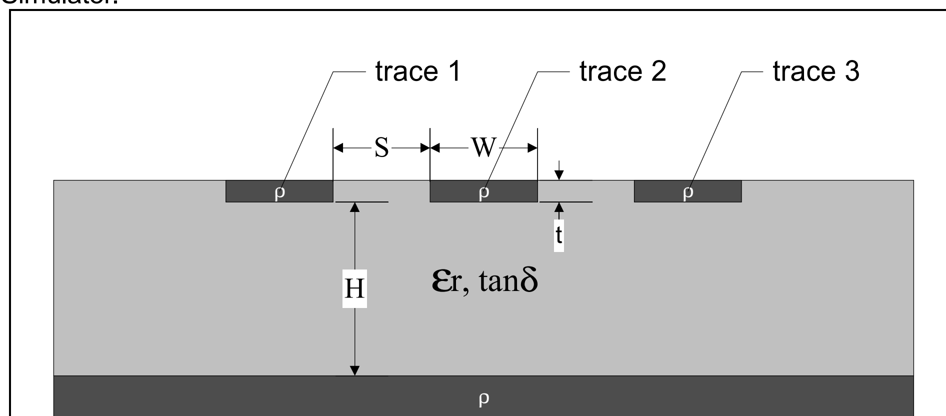


Figure 12. Transmission Line Structure

Table 1. Characteristics of Miscellaneous Boards

Height (mil)	Width (mil)	Spacing (mil)	Z0 (Ω)	Ze (Ω)	Zo (Ω)	S0 (ns/ft)	Se (ns/ft)	So (ns/ft)	C0 (pf/in)	Cm (pf/in)	L0 (nh/in)	Lm (nh/in)
5	5	5	63.53	72.36	51.13	1.86	1.96	1.81	2.598	0.346	9.746	2.051
		10	63.88	68.53	58.66	1.87	1.93	1.81	2.459	0.114	9.932	1.081
		15	63.59	66.19	60.83	1.87	1.91	1.83	2.458	0.049	9.916	0.641
	6	6	57.94	65.16	49.10	1.86	1.95	1.81	2.782	0.285	8.996	1.603
		12	58.44	61.77	54.81	1.88	1.93	1.83	2.693	0.087	9.147	0.795
		18	58.68	60.49	56.80	1.88	1.92	1.85	2.677	0.035	9.206	0.460
	8	8	51.02	55.37	46.4	1.88	1.95	1.83	3.124	0.183	8.012	1.004
		16	50.28	52.11	48.35	1.90	1.94	1.86	3.147	0.051	7.942	0.465
	10	10	44.95	47.91	41.66	1.90	1.96	1.84	3.550	0.134	7.117	0.725
		20	45.29	46.47	44.05	1.91	1.94	1.88	3.513	0.036	7.198	0.312
6	5	5	68.33	79.99	52.71	1.84	1.96	1.80	2.441	0.401	10.47	2.578
		10	69.32	75.61	62.03	1.85	1.92	1.79	2.263	0.144	10.69	1.426
		15	69.48	73.17	65.47	1.86	1.91	1.81	2.241	0.067	10.77	0.873
	6	6	63.64	72.90	51.82	1.85	1.95	1.79	2.555	0.325	9.793	2.059
		12	64.26	68.85	59.13	1.86	1.92	1.81	2.439	0.111	9.976	1.059
		18	64.62	67.18	61.89	1.86	1.91	1.82	2.410	0.046	10.04	0.632
	8	8	55.43	61.36	48.37	1.87	1.95	1.80	2.878	0.230	8.619	1.348
		16	55.93	58.52	53.14	1.88	1.93	1.83	2.809	0.065	8.758	0.641
	10	10	51.20	55.32	46.51	1.88	1.95	1.82	3.101	0.161	8.026	0.970
		20	50.40	52.12	48.60	1.89	1.93	1.85	3.133	0.046	7.948	0.440
8	5	5	78.19	93.78	55.65	1.81	1.96	1.79	2.209	0.467	11.80	3.515
		10	80.22	90.04	68.29	1.83	1.91	1.78	1.970	0.203	12.23	2.096
		15	79.02	85.13	72.12	1.84	1.90	1.78	1.959	0.102	12.09	1.366
	6	6	73.57	86.83	55.46	1.82	1.95	1.79	2.279	0.411	11.18	2.903
		12	73.79	81.19	65.11	1.84	1.91	1.78	2.122	0.159	11.30	1.633
		18	73.61	78.01	68.78	1.85	1.90	1.80	2.103	0.075	11.32	1.021
	8	8	64.87	73.89	53.53	1.84	1.94	1.79	2.488	0.298	9.969	1.986
		16	64.87	69.31	59.92	1.85	1.91	1.80	2.402	0.101	10.02	1.032
	10	10	59.91	66.56	51.94	1.85	1.94	1.79	2.652	0.225	9.257	1.493
		20	59.02	61.92	55.88	1.87	1.92	1.82	2.646	0.068	9.181	0.706
10	5	5	85.69	104.2	57.13	1.81	1.99	1.80	2.111	0.521	12.93	4.343
		10	86.78	99.81	70.08	1.81	1.91	1.77	1.848	0.252	13.11	2.792
		15	86.07	94.69	75.96	1.82	1.89	1.77	1.804	0.138	13.07	1.865
	6	6	80.58	96.77	56.98	1.80	1.96	1.78	2.143	0.458	12.12	3.667
		12	82.34	92.63	69.77	1.82	1.91	1.77	1.916	0.201	12.51	2.206
		18	83.14	89.62	75.81	1.83	1.89	1.78	1.858	0.101	12.69	1.424
	8	8	70.86	82.71	55.01	1.82	1.94	1.77	2.319	0.361	10.75	2.642
		16	72.94	79.18	65.78	1.84	1.91	1.78	2.134	0.124	11.18	1.413
	10	10	66.32	75.43	54.88	1.84	1.93	1.78	2.419	0.281	10.15	2.014

		20	67.75	72.20	62.80	1.85	1.91	1.80	2.293	0.093	10.44	1.030

Z0, S0, C0 and L0 are the characteristic impedance, propagation delay, self-capacitance and self-inductance, respectively. These parameters are calculated in the condition that the victim (trace 2) is switching, and the aggressors (trace 1 & trace 3) are quiet.

The definition of odd mode is that the aggressors (trace 1 & trace 3) are both switching in the opposite direction of the victim (trace 2). On the other hand, all the signals are switching in the same direction defined as even mode. The characteristic impedance and propagation delay varies in the even and odd mode. The calculated even mode and odd mode parameters are:

Zo: odd mode characteristic impedance

So: odd mode propagation delay

Ze: even mode characteristic impedance

Se: even mode propagation delay

The Cm and Lm are mutual capacitance and mutual inductance.

Refer to Table 1, Increasing trace width decreases characteristic impedance and the deviation of impedance between even mode and odd mode concurrently. Increasing trace space has more effect on decreasing deviation of impedance between even mode and odd mode than changing the characteristic impedance. In addition, the thicker substrate could cause higher characteristic impedance and larger deviation of impedance between even mode and odd mode. There are two important parameters related to crosstalk effects, Cm and Lm. Lower mutual capacitance and mutual inductance would have less crosstalk than higher mutual capacitance and mutual inductance. However, the lower characteristic impedance could reduce signal edge rates and decrease over/undershoot and ringback.

Briefly, SiS recommends using the thinner substrate and wider trace with sufficient spacing for motherboard layout.

Power requirements

Generally speaking, there are two types of decoupling capacitance, one is called bulk decoupling and another is called high frequency decoupling. It will be introduced the fundamentals of decoupling by the two types in more detail below.

2.4.3 Bulk Decoupling

First, we see an effective lump circuit for power distribution of motherboard in Figure 13.

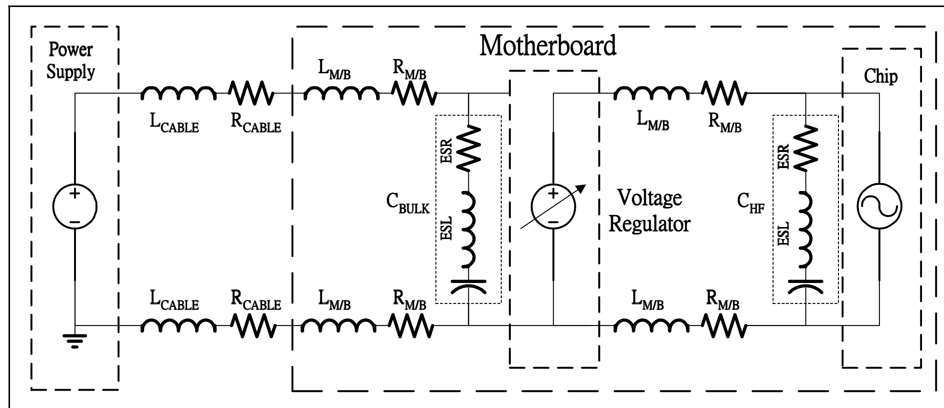


Figure 13. Lump Effective Circuit of Motherboard for Power Distribution

The cable (VCC and GND) connected power supply to PCB and the power (VCC and GND) traces on motherboard can be equivalent to a series of inductor and resistor. For the duration of turning on power or waking up from lower power states, there is a large current providing from power supply to voltage regulator. Therefore, the series of inductors and resistors on cable and power trace will induce a voltage drop. For this reason, we need to add some capacitors near voltage regulator to steady voltage, i.e. bulk decoupling. On the other hand, a real capacitor should be realistically equal to an effective series inductor (ESL), an effective series resistor (ESR) and a capacitor in series. When the decoupling capacitor provides current for the consumer, its ESL and ESR will induce a voltage drop concurrently. Therefore, the maximum voltage drop $(\Delta V)_{max}$ can be calculated by

$$(\Delta V)_{\max} = ESL \times \left(\frac{\Delta I}{\Delta t}\right)_{\max} + ESR \times (\Delta I)_{\max}.$$

Here $(\Delta I/\Delta t)_{max}$ is the maximum current slew rate and $(\Delta I)_{max}$ is the maximum supplied current. For bulk decoupling, ESR is more significant than ESL because it can be regarded as a DC transceiver.

2.4.4 High Frequency Decoupling

As illustrated in Figure 13, the power traces connected voltage regulator to IC chip on motherboard can be equally regarded as the series of inductor and resistor. Comparing the duration of bus busy to bus idle, there is a large deviation of current required by IC chip. Therefore, if the insufficient current supplies entirely by the voltage regulator, then the effective inductors and resistors on power trace will generate a voltage drop. Accordingly, we need to add some capacitors near IC chip to keep voltage stable, i.e. high frequency decoupling. For high frequency decoupling, ESL is more significant than ESR because it can be regarded as an AC transceiver.

2.4.5 Calculation of the Decoupling Capacitance (C)

To simplify calculation of the decoupling capacitance and the number of decoupling

capacitors with considering ESL and ESR, SiS provides a simple estimated method.

$$C = I_{\max} \times \frac{\Delta t}{\Delta V}.$$

Here I_{max} is the maximum required current, ΔV is the budget of voltage tolerance and Δt is the response time of voltage regulator.

2.4.6 Calculation of the Number of Decoupling Capacitors (N)

When the ESL and ESR are not examined, the number of capacitors (N_P) is

$$N_P = \frac{C}{C_P}.$$

And C_P is the capacitance of a single capacitor.

If the ESR is considered, the decoupling capacitance (C') and the number of the capacitor (N_{ESR}) will be

$$C' = I_{\max} \times \frac{\Delta t}{\Delta V - I_{\max} \times ESR},$$

$$N_{ESR} = \frac{C'}{C_P}.$$

To consider ESL, the budget of voltage drop on ESL (ΔV) is

$$\Delta V = L_{\min} \times \left(\frac{\Delta I}{\Delta t} \right)_{\max}.$$

Here $(\Delta I/\Delta t)_{max}$ is the current slew rate of maximum, and L_{min} is defined as the tolerable inductance of minimum of decoupling capacitors. Hence the number of capacitors (N_{ESL}) is

$$N_{ESL} = \frac{ESL}{L_{\min}}.$$

So the safety number of decoupling capacitors is

$$N = MAX(N_P, N_{ESR}, N_{ESL}).$$

2.4.7 SiS55x Decoupling

The decoupling capacitors for SiS55x should be placed at 4 corners of the chips. They are illustrated in Figure 14. Each corner should place two capacitors of 0.1 µF and 0.01 µF.

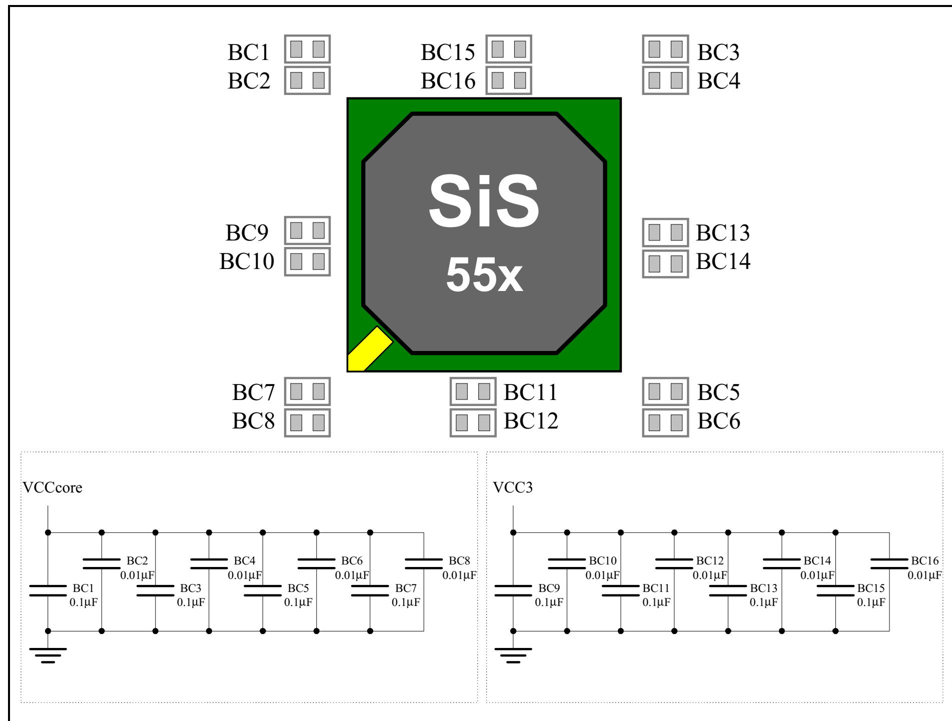


Figure 14. Decoupling Capacitors for SiS55x

2.4.8 Power Islands

There are many different voltage sources required by SiS55x based systems. In a 4-layer motherboard, only one layer was assigned to the power plane, therefore, it is necessary to divide a power plane into several power islands. The required voltages include VCC (5V), VCC3 (3.3V), VCCcore (1.9V), 1.9VSBY, 3VSBY, 5VSBY, +12V, VCC3_DIMM etc.

The recommended power scheme of VCCcore, VCC3, and VCC are illustrated in Figure 15. These power sources should be routed on the power plane and constructed as islands. The Voltage Island should be a whole plane and cover all of the pins of the source and load.

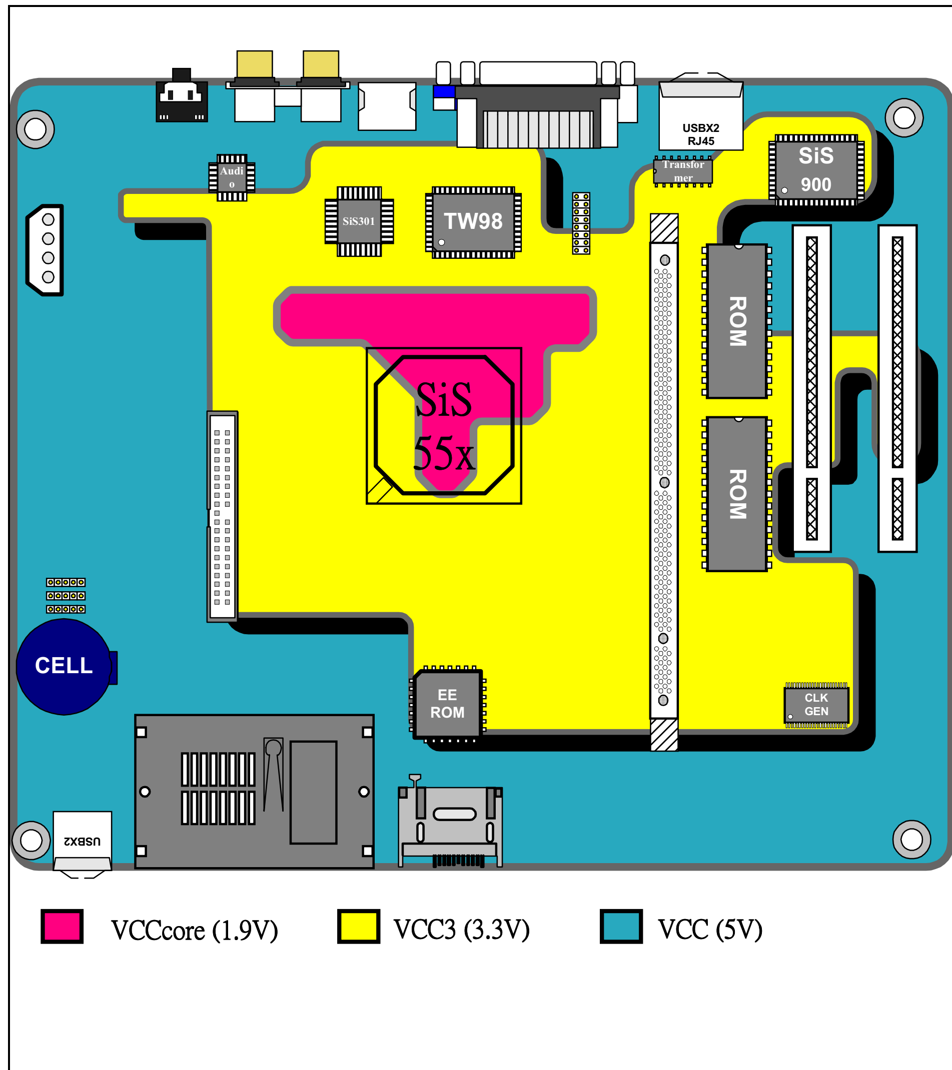


Figure 15. Power Islands Map (Socket 7 System)

Note:

The split power plane of VCC3 and VCC3_DIMM may cause serious EMI and signal integrity problems in high-speed signals. To minimize these problems, some decoupling capacitors should be placed between VCC3 and VCC3DIMM planes. Six-layer or eight-layer M/B could eliminate these problems by routing DRAM signals in the layer that is not adjacent to the power plane.

If STD (suspend to DRAM) function is not supported, SiS strongly recommends to merge the VCC3 and VCC3_DIMM planes into a single plane.

In addition, the voltages RTCVDD, KBVDD, USBVDD, SB3V, and SB1.9V, they must be laid as traces. Moreover, to reduce the trace inductance, the minimum trace width of VTT should be at least 50 mils, and the others should be not less than 30mils, as listed in Table 2.

Table 2. Recommended Trace Width for Power Signals

SIGNAL NAME	RECOMMENDED TRACE WIDTH
RTCVDD	30 mils
KBVDD	30 mils
USBVDD	30 mils
SB3V	30 mils
SB1.9V	30 mils

Here, SiS provides a rough procedure to synthesize the safe width of power trace.

First, determine the budget of voltage drop (ΔV) caused by the inductance of trace. Moreover,

$$\Delta V \geq L(w) \times l_{\max} \times \left(\frac{\Delta I}{\Delta t} \right)_{\max}.$$

In above equation, L(w) a function of trace width (w) is the trace inductance of unit length, and l_{max} is the maximum length from power producer to consumer, and $(\Delta I/\Delta t)_{max}$ is the maximum current slew rate.

Second, find out the maximum current slew rate from IC specifications, and calculate the trace inductance of unit length by a definite trace width. Therefore, the limit of maximum length (l_{max}) from power producer to consumer can be written as

$$l_{\max} \leq \frac{\Delta V}{L(w) \times \left(\frac{\Delta I}{\Delta t} \right)_{\max}}.$$

For miscellaneous power distribution designs on motherboard, SiS provides the calculated trace inductance of several microstrip structures, listed in Table 3.

Table 3. Inductance of Several Microstrip Structures

HEIGHT (H) (mil)	TRACE WIDTH (W) (mil)	L(W) (nh/in)	C(W) (pf/in)	Z0 (Ω)
5	10	7.171	3.540	45.01
	20	4.753	5.581	29.18
	30	3.588	7.694	21.60
	40	2.900	9.719	17.27
	50	2.432	11.803	14.35
6	10	7.972	3.125	50.50
	20	5.369	4.858	33.25
	30	4.097	6.619	24.88
	40	3.336	8.329	20.01
	50	2.830	9.915	16.89
8	10	9.212	2.640	59.07
	20	6.436	3.966	40.28

	30	5.005	5.259	30.85
	40	4.167	6.472	25.37
	50	3.521	7.827	21.21
10	10	10.356	2.296	67.16
	20	7.355	3.402	46.50
	30	5.775	4.448	36.03
	40	4.880	5.379	30.12
	50	4.136	6.495	25.24
The dielectric constant (ε_r) is 4.5, and metal thickness of trace is 0.7 mils.				

Last, from Table 3 we will be able to choose an appropriate trace width, and let the trace inductance satisfy the budget of voltage drop (ΔV).

2.4.9 Adapter Power Supply

The most important feature of Power Supply is Suspend to DRAM (STD) function. STD mode is equivalent to ACPI S3 state which is supported by SiS55x, and it is also the most economic power saving mode. When a system is set into STD mode, all the parts of system are power off except for the main memory, which is in the self-refresh mode and only consumes a little power. The other merit of STD is that system can be resumed very quickly, thus the recovery time is only few seconds in general. Power Supply makes the STD mode possible in the desktop system by providing dual power VCC3_DIMM that are controlled by 550CKE signal. In Figure 16, we depict the power sources for DIMMs and PCI slots. For backward compatibility, the VCC3_DIMM can be powered by VCC3 from PWM regulator, respectively. Please refer to the SiS55x reference schematics for more information.

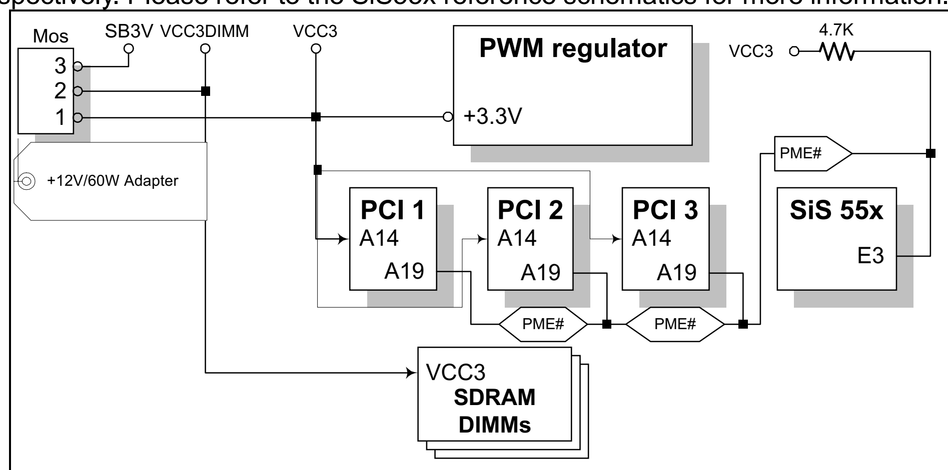


Figure 16. Power Source for DIMM

2.5 Noise Filter for PLL Function

There are 3 analog power pins for SiS55x internal phase locked loop (PLL): they are CPUAVDD, SDAVDD and IDEAVDD. The parasite noise on these power pins will produce jitter on internal clock that may cause internal logic failure. To ensure

that PLL function can work properly, the noise filters at their power pins are necessary. The schematics and recommended layout of the noise filters are illustrated in Figure 17 ~ Figure 19.

To get a high quality noise filter, please follow the below rules:

- Place the circuit of noise filters as close to SiS55x as possible.
- Every trace depicted in the figures should be kept as short as possible.
- The recommend trace width in the figures is at least 30 mils.

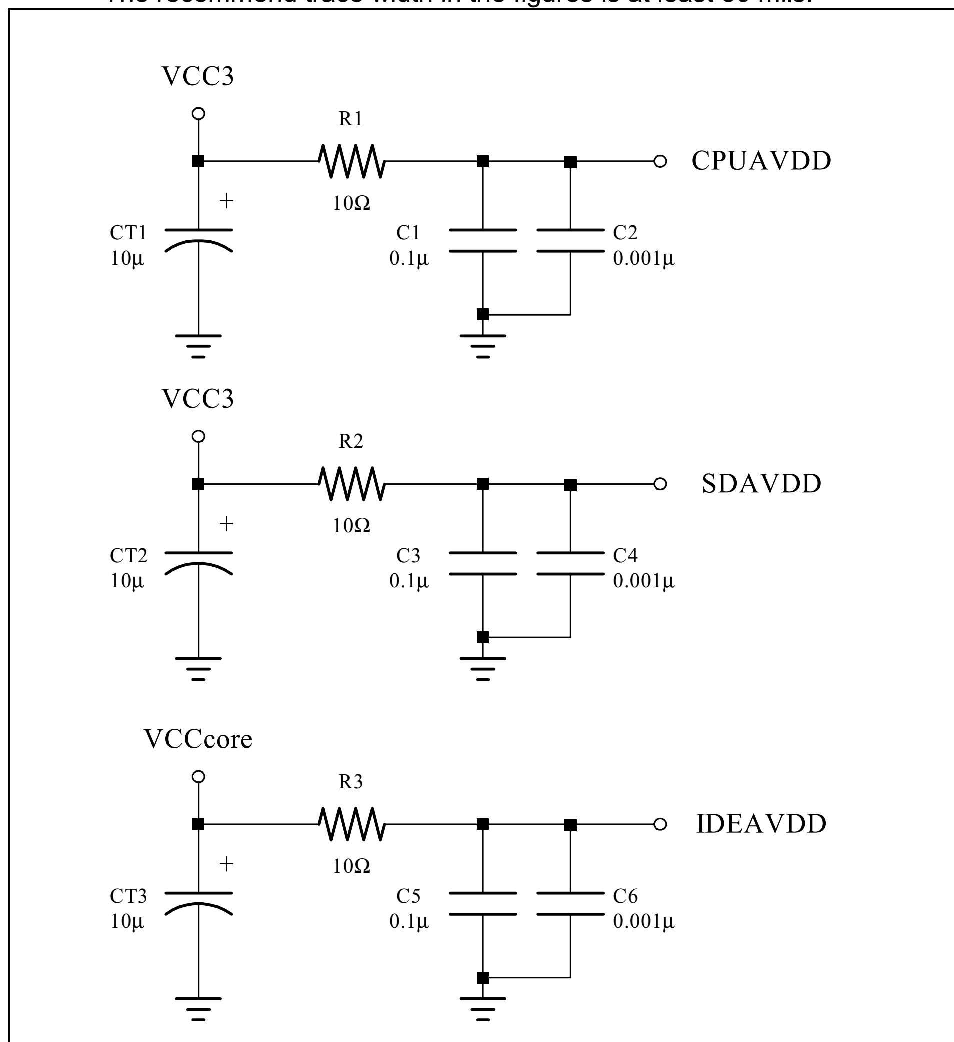


Figure 17. Example Circuitry for AVDD

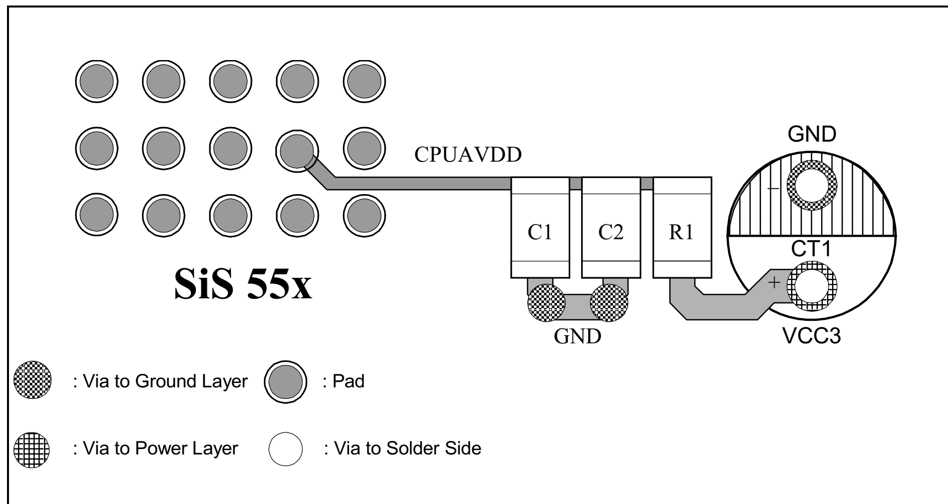


Figure 18. Layout Example for CPUAVDD

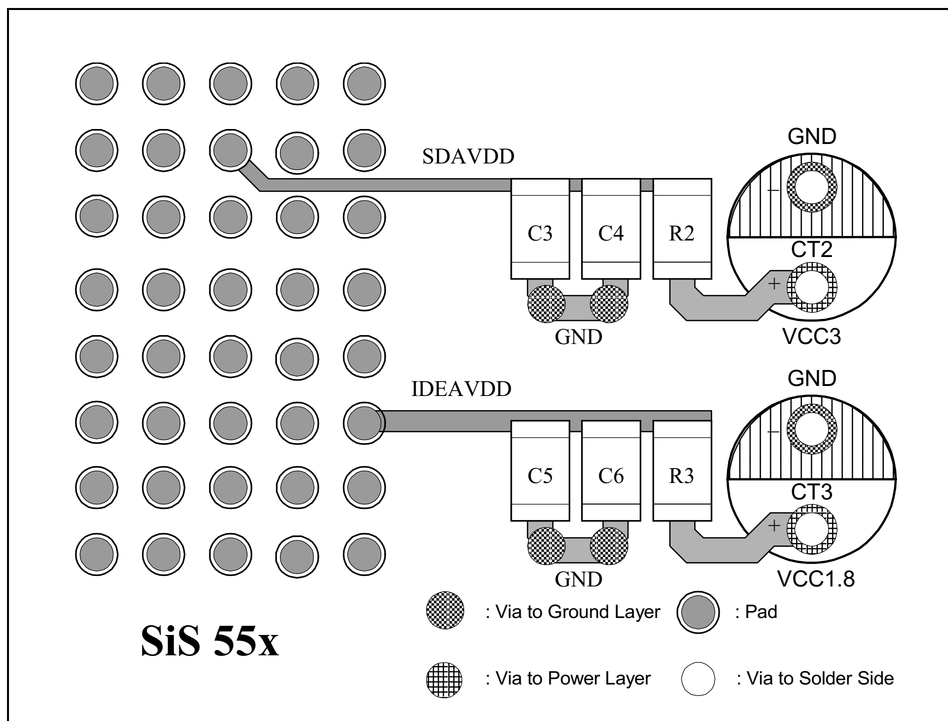


Figure 19. Layout Example for SDAVDD & IDEAVDD

3 Design Guidelines

3.1 General Layout Guidelines

In general, the signal integrity plays a very important role for the motherboard stability. The following list the general layout guidelines for the critical signals such as clocks and strobes.

- Minimize crossovers between voltage islands for high-speed signals.
- Minimize the use of vias to connect between signal traces.
- Clock signals should be routed on the layer, which is adjacent to the ground layer.

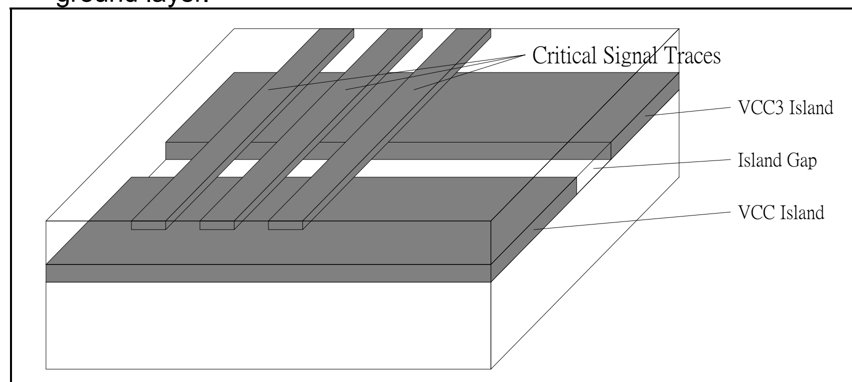


Figure 20. Crossover between Different Power Islands

Figure 20 illustrates an example of the crossover of signal traces and a gap between voltage islands.

3.2 Clock Routing Guidelines

3.2.1 Clock Requirements for Clock Generators

The clock generator requirements for SiS55x based system are listed below.

Table 4. Clock Requirements for Clock Generator

TYPE	FREQUENCY	VOLTAGE	NUMBER
XCPUCLK	66, 100 MHz	2.5V	3 (R1CPUCLK, R1CPUCLKBY, SiS55x)
SDCLK	66, 100 MHz	3.3V	5 (SiS55x, SDRAM)
PCICLK	33 MHz	3.3V	5 (SiS55x, LPC ROM, 2 PCI Slots), 4 for the minimum
USBCLK48M	48 MHz	3.3V	1 (SiS55x)
CLK66M	66MHz	3.3V	1 (SiS55x)
REFCLK	14.318 MHz	3.3V	3 (SiS55x, SiS301, TV Encoder)
VOSCI	48MHz	3.3V	1 (VGA)

PHYCLK	25MHz	3.3V	1 (Network)
XTAL	24.576MHz	3.3V	1 (AC 97 CODEC)

The limitations of clock trace length are described at next sections.

3.2.2 Clock Trace Routing Guidelines:

- It is recommended that the distance from one clock trace to other traces is 14 mils at least and the distance from one segment of a clock net to other segments of the same net is 18 mils at least.
- Keep clock traces away from the discontinuity of its reference plane to reduce EMI noise, as illustrated in Figure 21.
- Reduce the number vias on clock traces.
- Be careful on the clock of 14.318 MHz. It's recommended that the board designer use different 14.318 MHz clock outputs for different components to prevent signal reflection.

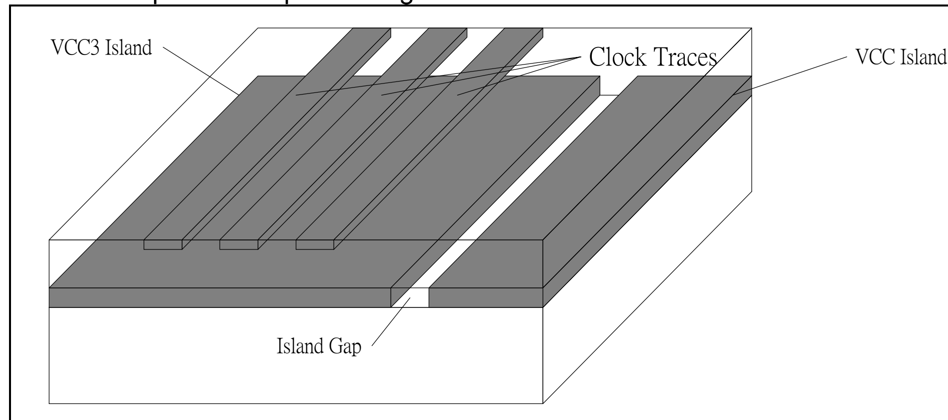


Figure 21. The Discontinuity of Reference Plane nearby the Clock Traces.

3.2.3 Requirement of Clock Trace Length

CPU & SDRAM Clocks:

In Figure 21, we demonstrate the clock scheme for SiS55x. In this clock scheme, the frequency of SDRAM clocks is the same as that of CPU clock. Although SiS55x supports with asynchronous mode between CPU and SDRAM, but yet SiS suggests that the clock layout for asynchronous mode is the same as Figure 22.

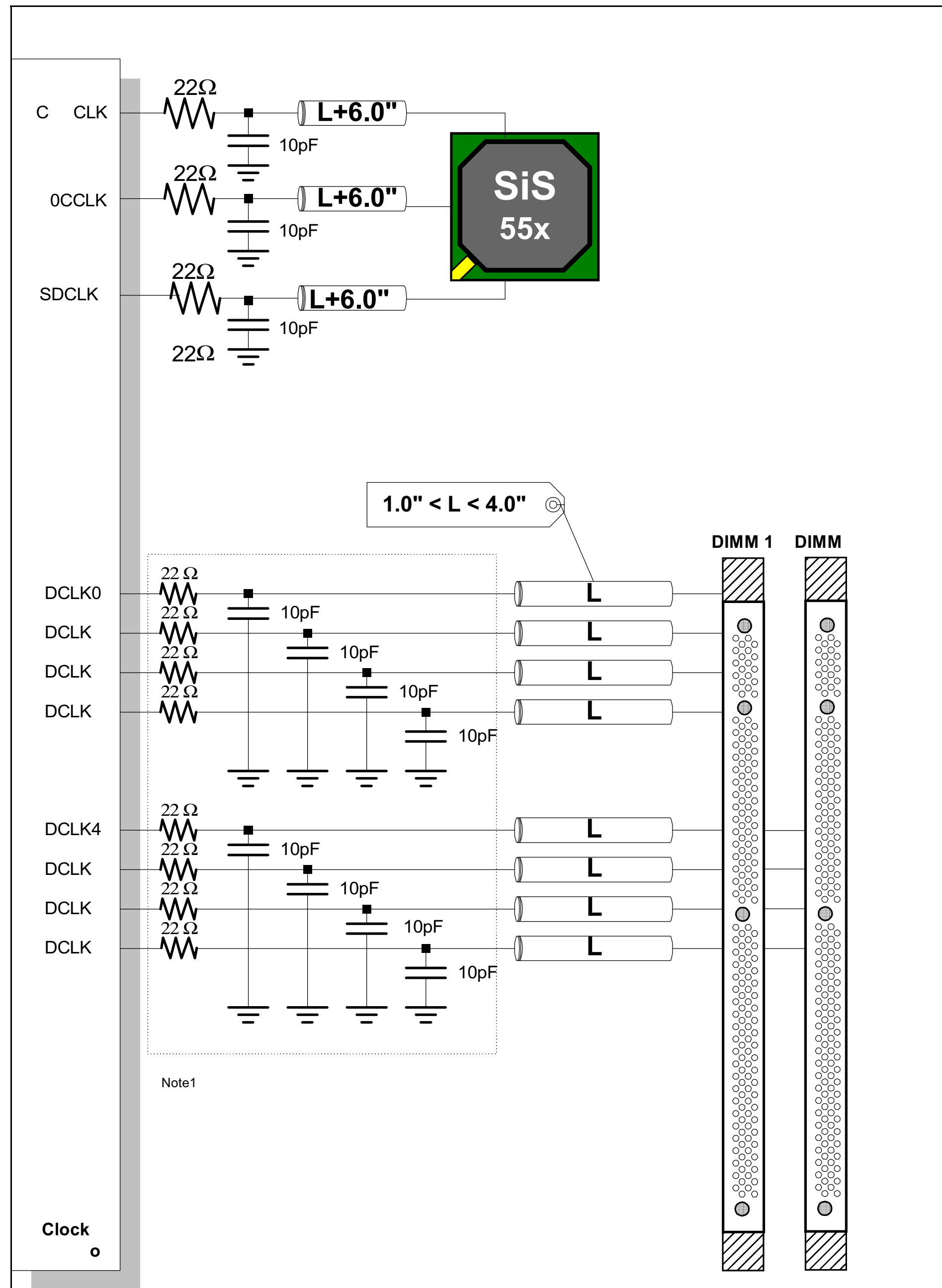


Figure 22. Host Bus Clocks Layout Guidelines (Socket 7 System)

Note 1: The purposes of serial resistors and bypass capacitors in the figure are for shaping clock waveform, impedance match and adjusting clock skew. The values of serial resistors and bypass capacitors depend on the motherboard layout.

The trace length 'L' should be minimum 1 inch and maximum 4 inches, and all of 'L' must be equivalent.

PCI Clocks:

The clock scheme for PCI clocks is illustrated in Figure 23. The trace length 'C' should be minimum 1 inch and maximum 12 inches, and all of 'C' must be equivalent.

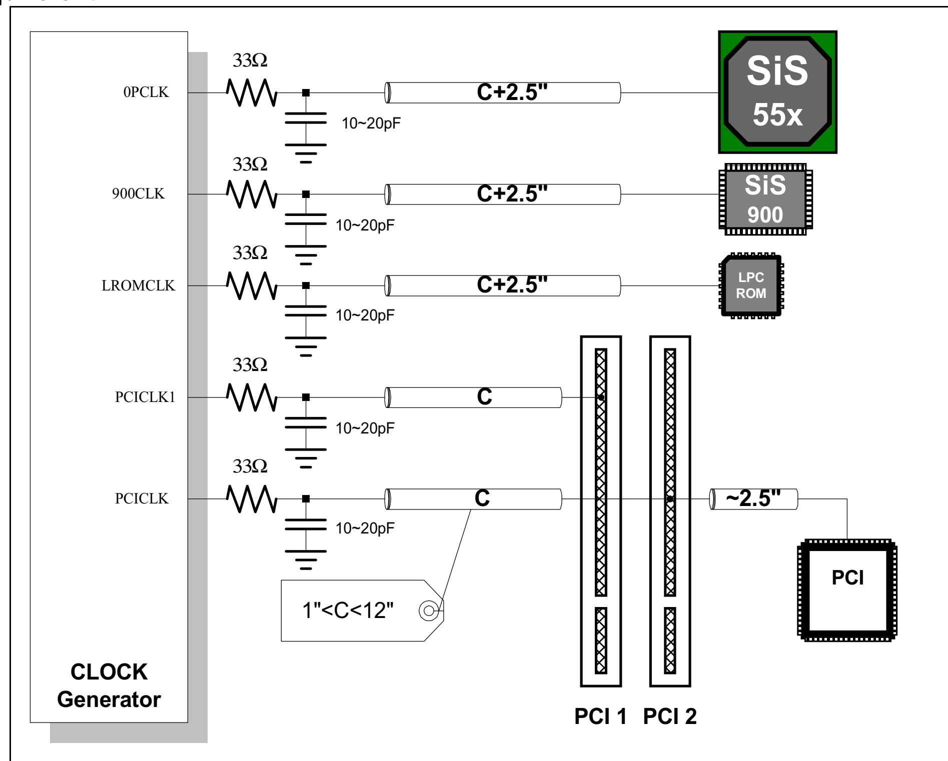


Figure 23. PCI Bus Clocks Layout Guidelines

3.3 SDRAM Design

The SiS55x DRAM controller supports 2-DIMM/4-Bank of 3.3V SDRAM. Each bank supports up to 512MB and the total memory size supported is 1GB. The memory clock frequency can be operated up to 133MHz and may run synchronously or asynchronously with front side bus. SiS55x supports various HOST/DRAM frequency combinations which can be reference from the frequency selection table provided by clock generators, such as ICS9248-146 (ICS), W257 (IC Works), FS6227-01 (AMI), W83194BR-635 (Winbond) and C9631 (IMI). For power saving, the SDRAM can be set into suspend mode. The basic DRAM configurations are illustrated as below:

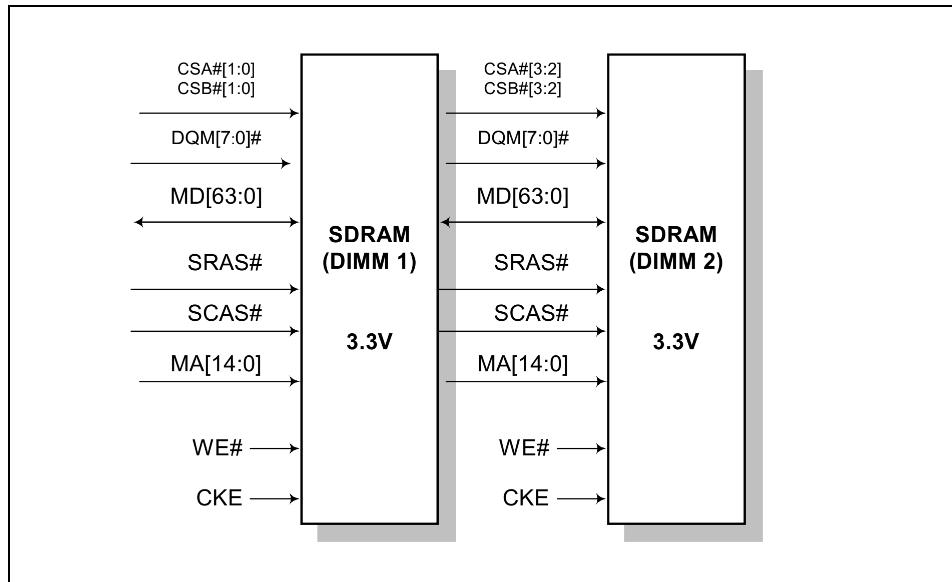


Figure 24. DRAM Configurations

3.3.1 SDRAM Layout Guideline

For the layout rules in details, please refer to the following figures, which indicate DIMM layout and routing recommendations:

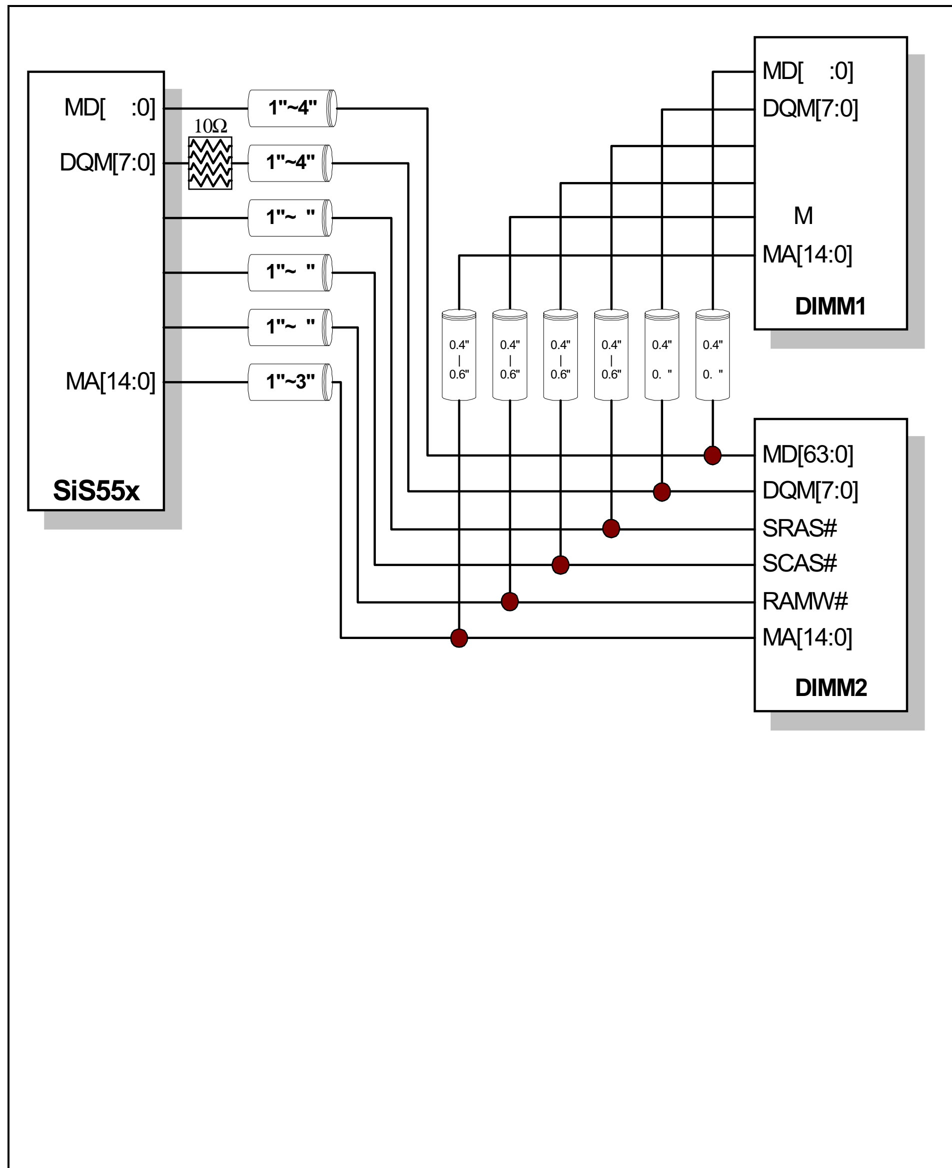


Figure 25. 1-to-2 SDRAM Signals Layout & Routing Topology

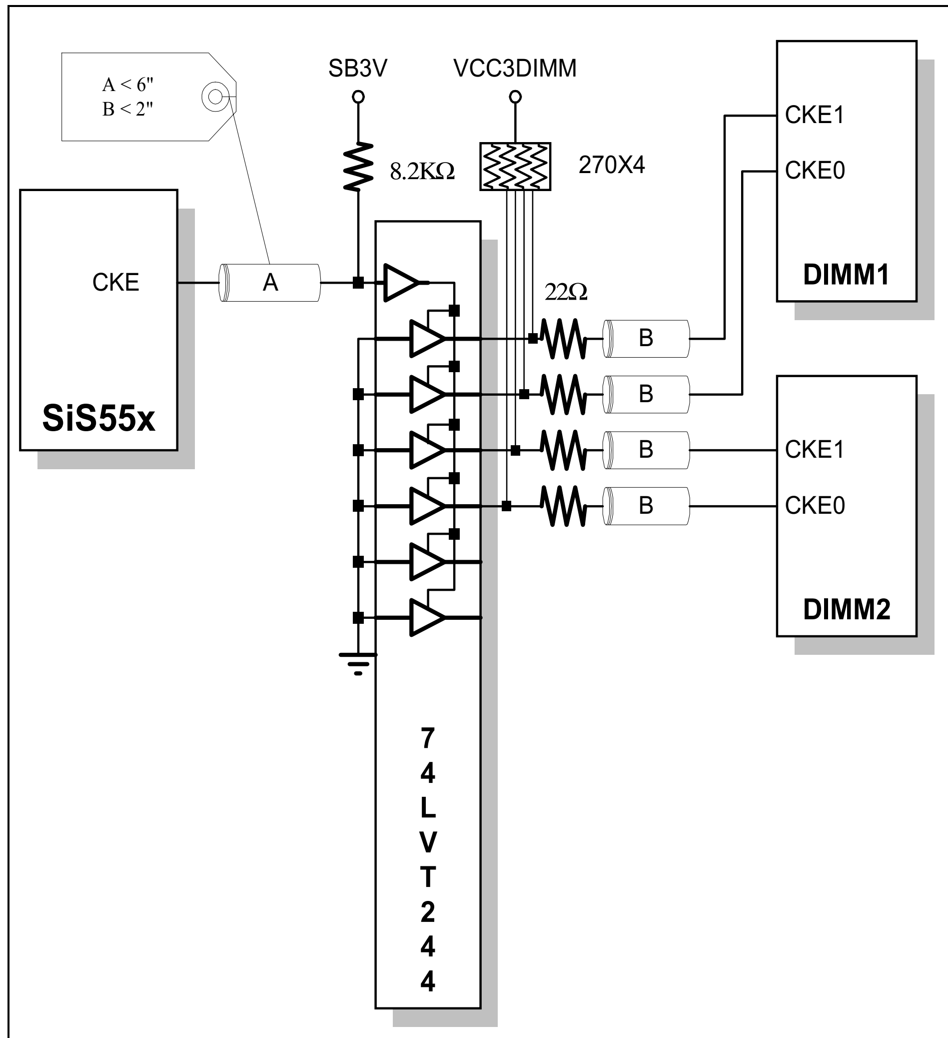


Figure 26. CKE Layout & Routing Topology (with TTL Buffer)

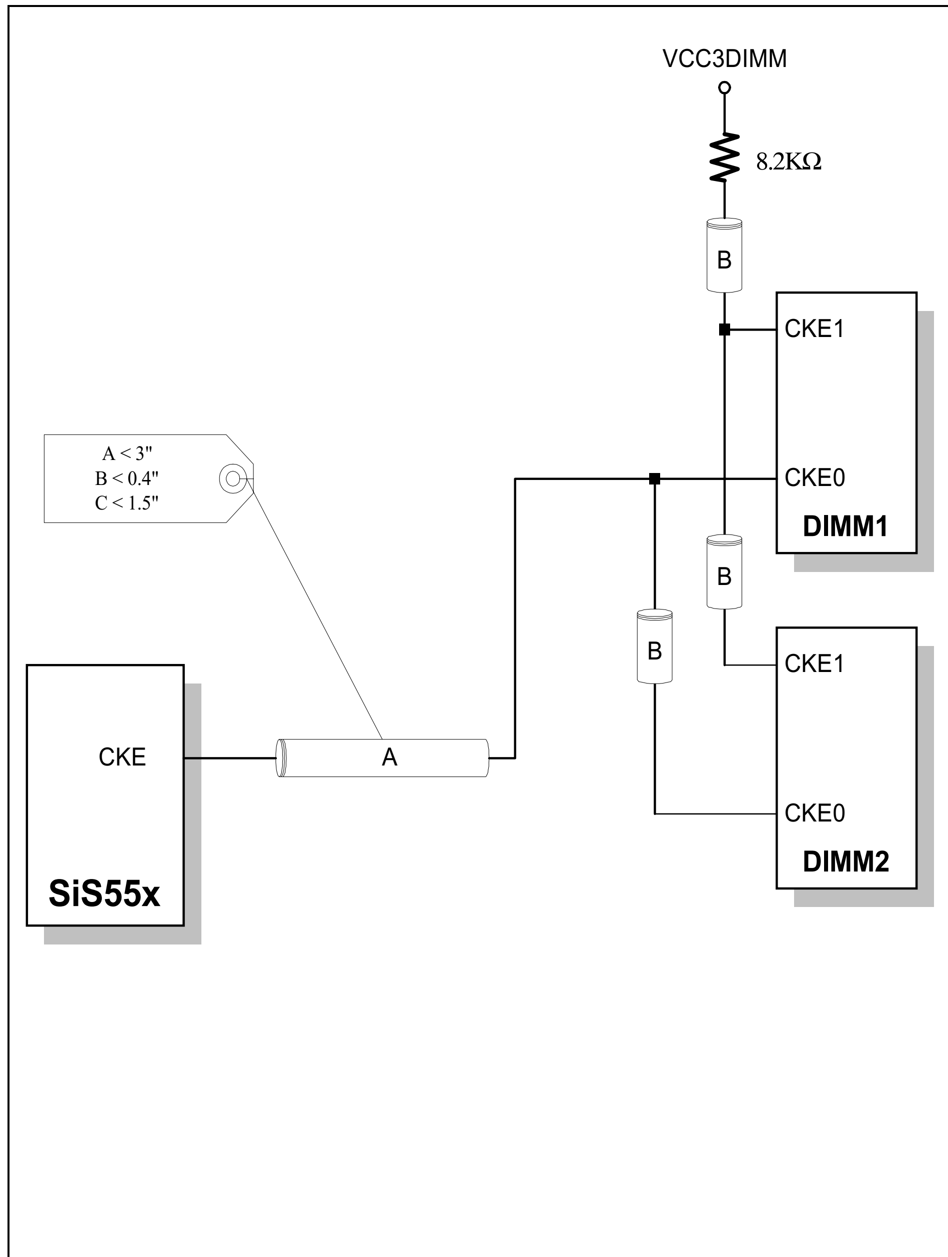


Figure 27. CKE Layout & Routing Topology (without TTL Buffer)

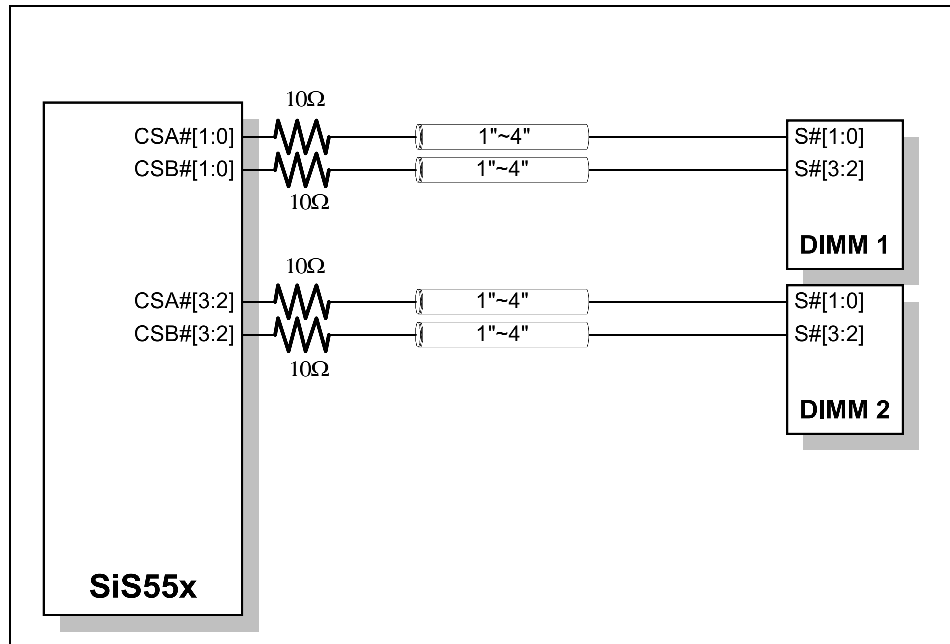


Figure 28. 1-to-1 SDRAM Signals Layout & Routing Topology

The topology recommendations are illustrated in Figure 25 that one pin of the signals in the memory controller of SiS55x must push three pins of the signals in the 2 DIMMs individually. Figure 27 shows the topology recommendations that one CKE pin pushes four pins of the signals in the 2 DIMMs separately. Besides the one-to-one signals' topology is recommended in Figure 28.

The true layout and routing examples for the memory signal lines as the categories in Figure 24 are illustrated in Figure 29.

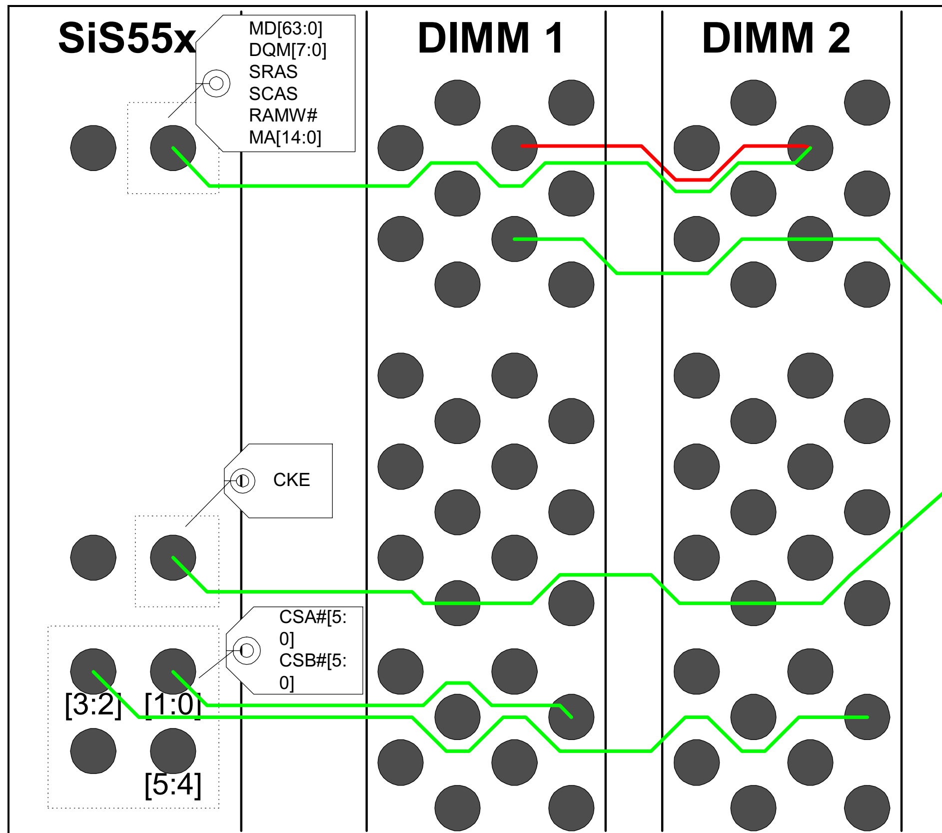


Figure 29. SDRAM Layout Examples

3.3.2 SDRAM Timing Analysis

To determine suitable recommended memory register setting, SiS performs an initial DRAM timing analysis based on the demo board simulation results. Table 5 illustrates the terms used in setup/hold time analysis equations, listed in Table 6.

Table 5. SiS55x Chipset Timing Terms

TERM	DESCRIPTION
T_{cycle}	System cycle time. Defined as the reciprocal of the system frequency.
$T_{co,max}$	Maximum driver delay from input clock to output data.
$T_{co,min}$	Minimum driver delay from input clock to output data.
$T_{flight,max}$	Maximum system flight time.
$T_{flight,min}$	Minimum system flight time.
T_{skew_jit}	Clock generator skew and clock jitter. Defined as the maximum delay variation between output clock signals from system clock generator and edge to edge variation in a given clock signal.
T_{sso}	Maximum delay variation due to the simultaneous switching outputs.
T_s	Minimum setup time. Defined as the time for which the input data must be valid prior to SDRAM input clock.

T_h	Minimum hold time. Defined as the time for which the input data must remain valid after SDRAM input clock.
T_{sdwclk}	Adjustable SDRAM write clock. This clock varies from 5.0ns ahead to 2.5ns behind with respect to SiS55x chipset clock.

Table 6. Timing Requirements for Validating SDRAM Setup/Hold Time

TERM	EQUATION
Setup	$T_{cycle} – T_{co,max} – T_{flight,max} – T_{skew_jit} – T_{sso} – T_s + T_{sdwclk} > 0$
Hold	$T_{co,min} + T_{flight,min} – T_{skew_jit} – T_h – T_{sdwclk} > 0$

Table 7 contains the timing values used to perform timing analysis. These values came from simulation results by SiS and JEDEC 133MHz SDRAM Specification.

Table 7. SiS55x 133MHz System Timing Parameters

TIMING TERM	VALUE
T_{cycle}(ns)	7.5
T_{skew_jit}(ns)	1.08
T_{sso}(ns)	0.3
T_s(ns)	1.5
T_h(ns)	0.8
T_{sdwclk}(ns)	+5.0 ~ -2.5
$T_{co,max}$ for CS#/DQM(ns)	4.18
$T_{co,min}$ for CS#/DQM(ns)	2.74
$T_{co,max}$ for MD(ns)	4.07
$T_{co,min}$ for MD(ns)	2.78
$T_{co,max}$ for MA/SRAS#/SCAS#/WE#(ns)	4.43
$T_{co,min}$ for MA/SRAS#/SCAS#/WE# (ns)	3.0

Table 8 contains simulation flight time based on SiS55x demo board. All of those values are for reference only.

Table 8. SDRAM Simulation Flight Time Based on SiS55x Demo Board

SIGNAL	LIGHT LOAD		HEAVY LOAD	
	FALLING	RISING	FALLING	RISING
CS#(ns)	1.42	1.7	2.2	3.39
DQM(ns)	1.46	1.89	2.29	3.44
MD(ns)	1.41	1.7	2.34	3.48
MA/SRAS#/SCAS#/WE# (ns)	3.06	2.95	5.79	5.76

Note:

The values showed in Light Load column, except MA/SRAS#/SCAS#/WE#, are calculated by using SiS55x fast corner parameters, fast pMOS/nMOS, with normal output buffer driving strength and only 1-DIMM populated.

The values showed in Light Load column for MA/SRAS#/SCAS#/WE# are calculated by using SiS55x fast corner parameters, fast pMOS/nMOS, with strongest output buffer driving strength and only 1-DIMM populated.

The values showed in Heavy Load column are calculated by using SiS55x slow corner parameters, slow pMOS/nMOS, with strongest output buffer driving strength and 2-DIMM populated.

According to setup/hold time equation and timing parameters listed in above tables, we can calculate adjustable SDWCLK valid window. Table 9 shows an example for DQM signal under 133MHz. From Table 9, we could conclude that the best SDWCLK setting for DQM under light load is 2.0ns earlier than SiS55x chipset clock and 3.0ns under heavy load system. Other SDRAM signals' best setting can be generated in the same way.

Table 9. DQM Adjustable SDWCLK Valid Window

SIGNAL DQM		133MHZ
Light Load	Falling	$7.5 – 4.18 – 1.46 – 1.08 – 0.3 – 1.5 + T_{sdwclk} > 0$ $2.74 + 1.46 – 1.08 – 0.8 – T_{sdwclk} > 0$ **T_{sdwclk} = +1.5~ +2.0 ns**
	Rising	$7.5 – 4.18 – 1.89 – 1.08 – 0.3 – 1.5 + T_{sdwclk} > 0$ $2.74 + 1.89 – 1.08 – 0.8 – T_{sdwclk} > 0$ **T_{sdwclk} = +1.5 ~ +2.5 ns**
Heavy Load	Falling	$7.5 – 4.18 – 2.29 – 1.08 – 0.3 – 1.5 + T_{sdwclk} > 0$ $2.74 + 2.29 – 1.08 – 0.8 – T_{sdwclk} > 0$ **T_{sdwclk} = +2.0 ~ +3.0 ns**
	Rising	$7.5 – 4.18 – 3.44 – 1.08 – 0.3 – 1.5 + T_{sdwclk} > 0$ $2.74 + 3.44 – 1.08 – 0.8 – T_{sdwclk} > 0$ **T_{sdwclk} = +3.0 ~ +4.0 ns**

Note: Adjustable SDWCLK varies from –2.5ns to + 5.0ns refer to SiS55x chipset clock.

Table 10 lists the recommended register setting for 133Mhz system and Table 11 for 100MHz system.

Table 10. Recommended Register Settings for 133MHz System

RANK POPULATED	MA1T/ MA2T	DELAY COMMAND	SDWCLK	DRIVING STRENGTH
1~2 ranks	MA1T	Delay	CS#: +2.0ns MA: +3.5ns MD: +2.0ns	CS#: normal MA: strong MD: normal
3~4 ranks	MA2T	Delay	CS#: +2.0ns MA: +1.0ns MD: +3.0ns	CS#: normal MA: strong MD: strong

Note:

MA1T means MA and CS# are issued at the same clock rising edge, while MA2T means CS# is issued one clock behind MA has been issued. Please refer to SiS55x data sheet R56b [6:5] for detail.

When delay command is enabled, all memory commands except self-refresh command will be driven one clock later than the normal operation and refer to

SDWCLK instead of SDCLK. Please refer to SiS55x data sheet R56b7 for detail.

SDWCLK is defined in SiS55x data sheet R8Ch and R8Dh.

Driving Strength is defined in SiS55x data sheet R59h and R5Ah.

Table 11. Recommended Register Settings for 100MHz System

RANK POPULATED	MA1T/MA2T	DELAY COMMAND	SDWCLK	DRIVING STRENGTH
1~2 ranks	MA1T	Delay	CS#: +1.5ns MA: +1.0ns MD: +0.5ns	CS#: normal MA: strong MD: normal
3~4 ranks	MA1T	Delay	CS#: +1.5ns MA: +3.5ns MD: +1.5ns	CS#: normal MA: strong MD: strong

Table 12 and Table 13 list CKE timing parameters and its flight time based on SiS55x demo board.

Table 12. SiS55x 133MHz CKE Timing Parameters

TIMING TERM	VALUE
$T_{co.max}$ for CKE(ns)	5.23
$T_{co.min}$ for CKE(ns)	3.8

Table 13. CKE Simulation Flight Time Based on SiS55x Demo Board

SIGNAL	FALLING	COMMENTS
CKE_4(ns)	1.87	Signal is driven by SiS55x
CKE(ns)	2.21	Signal is driven by 74LVT244

Table 14 shows the recommended register setting on the system using 74LVT244. The 74LVT244's propagation delay is required to be within 1.5 ~ 2.5ns to meet the design timing specification

Note:

CKE_4 means from SiS55x to 74LVT244.

1. CKE means from 74LVT244 to SDRAM DIMM modules.
2. The value for CKE_4 is calculated by using SiS55x fast corner parameters, fast pMOS/nMOS, with weak output buffer driving strength.

Table 14. CKE Recommended Register Setting Using 74LVT244

SYSTEM FREQ.	DELAY COMMAND	DELAY COMMAND FOR CKE I/O CELL	CKE ADJUSTABLE DELAY CELL	DRIVING STRENGTH
133MHz	Delay	Normal	+7ns	Normal
100MHz	Delay	Delay	+4ns	Normal

Note:

1. CKE adjustable delay cell varies from +1.0ns to +8.0ns.
2. Delay command for CKE I/O cell works like "Delay Command " and is defined in SiS55x data sheet R6Bh.

3.4 VGA Layout Rules

The following suggestions are proposed to optimize the layout and improve the signal quality. They are only for recommendations. Designers are desirous of implementing their own PCB based on these guidelines and qualify the overall performance and signal quality of the entire system before the designs are put into mass-production.

3.4.1 Analog Power and Analog Ground

- The analog power should be isolated from digital power plane. It is recommended that each analog power is divided by ferrite bead and is coupled with a 10uF tantalum capacitor and a 0.1uF capacitor.
- All traces of analog power and ground should be as short and wide as possible to reduce the impedance and inductance.
- The analog components (including trace, parts) should be far away from the high frequency parts or traces and as close to the related analog pins as possibly
- It is recommended to shield an analog power trace against high frequency noise by digital ground traces.

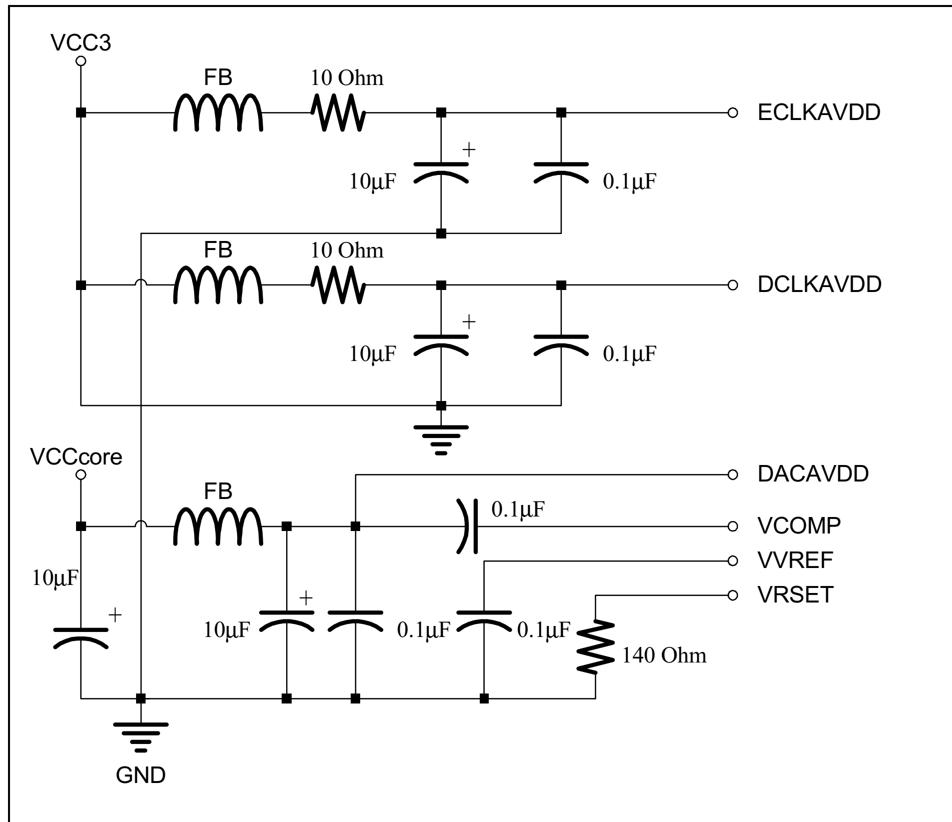


Figure 30. Schematics Example for VGA Analog Power/Ground Signals

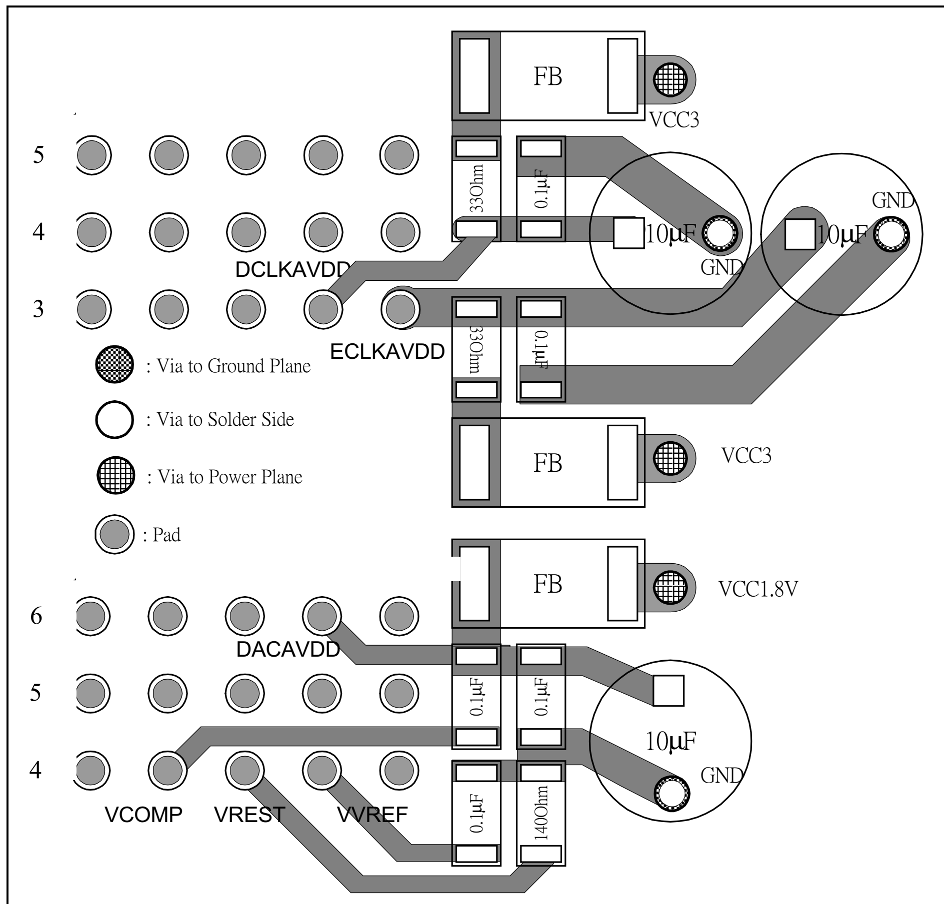


Figure 31. Layout Example for VGA Analog Power/Ground Signals

3.4.2 Sensitive Analog Signals

ROUT, GOUT and GOUT are the analog output traces. These traces should be far away from high frequency trace and should be shielded by ground trace. To reduce the impedance and inductance, a short and wide trace is fitted to implement.

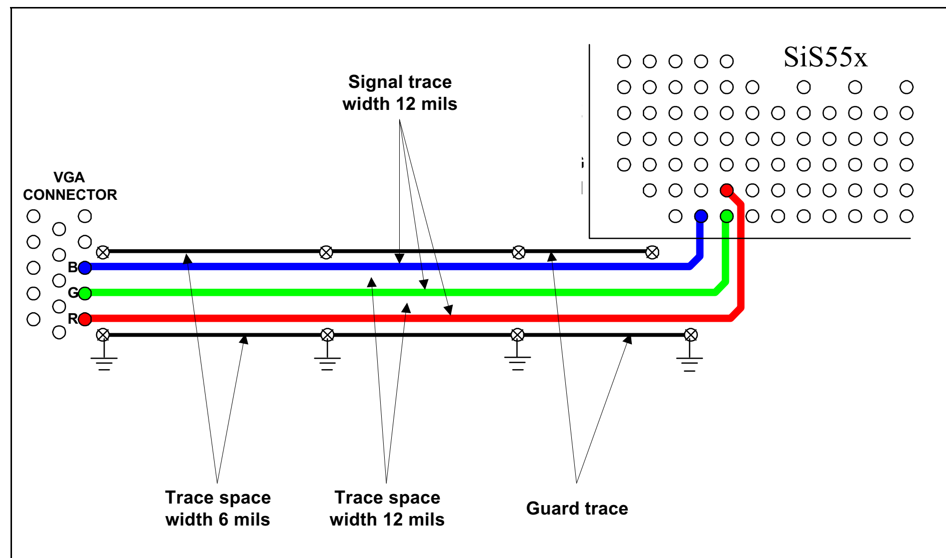


Figure 32. SiS55x DAC Routing Model

3.4.3 Clock Signals

VOSCI is a sensitive signal, and the clock trace should be short and at least 16 mills wide

3.5 IDE

The PIO mode 4 of ATA/ATAPI-6 defines a maximum rate of 16.7 MB/s. The Ultra DMA Mode 5(ATA100) even provides higher transfer rate of 100MB/s. To fulfill the shortened cycle time, the faster slew rate of I/O buffer for IDE signals should be from 0.4 V/ns to 1.9 V/ns. The transmission line effect and signal crosstalk emerges in the IDE related signals. To eliminate the ringing and reflection effect caused by transmission line effect, the trace length and impedance match must be taken into consideration. SiS provides several rules that can enhance the signal integrity and are listed below.

- The pull-up resistors on open-collector signals, such as IORDY, should be more than 1K ohm.
- Place the damping resistors for IDESA[2:0], IDECS[1:0][A], IIOR[A]#, IIOW[A]#, and IDACK[A]# near SiS55x.
- Place the damping resistors for IDA[15:0], IDREQ, ICHRDY, and IIRQ near IDE connectors.
- The 28th pin of IDE connectors (CSEL) should be pulled low.
- Route IDE cable away from chassis, power supplies and high speed circuits.
- As the shorter the IDE cable, the better signal integrity can be obtained.
- The IDE cable length must be less than 18 inches.

– The following signals that in the same channel should have the same length.

Channel 1: IDED[15:0], IDEIORA, ICHRDYA, IDEIOWA

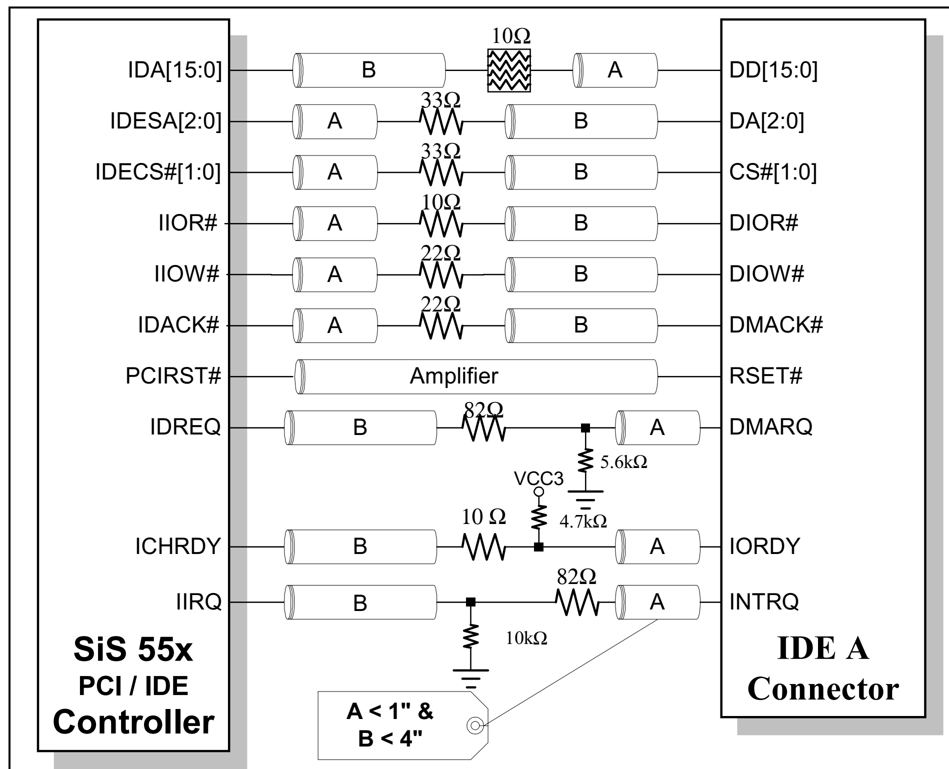


Figure 33. Topology of IDE signals

3.6 PCI Bus Design

The clock skew between any two PCI devices should be within 2.0 ns. The trace length of the PCI clocks must be less than 15 inches for on-board PCI devices, and less than 12 inches for each PCI add-in slot to minimize the clock skew. Please refer to the previous section for the PCI clock layout recommendations.

All PREQx# pins (PCI Request signals) should pull high even the corresponding PCI slot is not mounted. The IOR#, IOW#, MEMR#, MEMW#, SMEMR# and SMEMW# signals of ISA bus need damping resistors. The value of the damping resistors are 33~75 ohm depending on the motherboard layout.

Based on the ATX form factor, it is recommended that SiS55x should be placed on the end of the PCI Bus as the termination of PCI Bus signals. The layout example is illustrated in Figure 30.

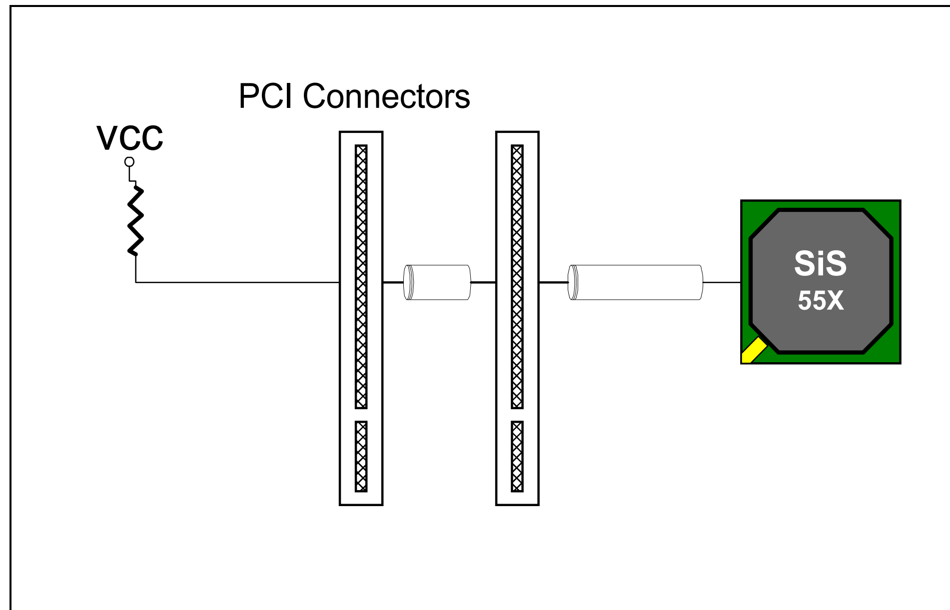


Figure 34. PCI Signal Layout Example

3.7 Keyboard Controller Design

It is also a requirement for RTC power transforming either from AUX5V To assure excellent power quality, it is recommended to add a 0.1uf capacitor close to the KBVDD and keep the trace width of KBVDD 30 mil in width at least.

Either using internal or external keyboard controller, PMCLK, PMDAT, KBCLK, KBDAT pins must be pulled high to VDD (5V power plane) by 10Kohm resistors. Two weak pull low resistors (200Kohm) are required for PMDAT and PMCLK to prevent these two nodes from floating while the power is off.

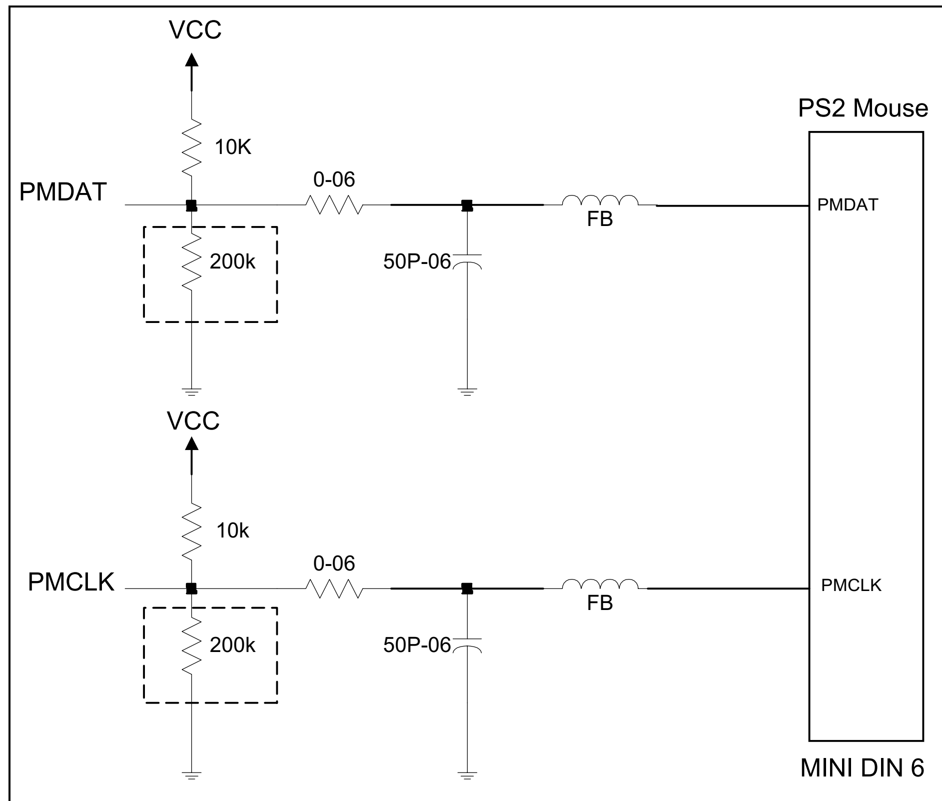


Figure 35. Schematics for PS2 Mouse

3.8 USB Controller

SiS55x integrates one USB controllers with up to 3 USB ports. It controls USB ports 0, 1, 2. If only 2 USB ports were used, the pull-low resistors for the other ports should not be removed and had better to use the port 0 and port 1 together.

3.8.1 USB Controller Layout Guidelines

The following are design requirements for USB related signals:

- 15K ohm pull-down resistors on the USB data lines (UV0+/- ~ UV2+/-) are required.
- USB data lines must be routed as “critical signals”. Locate the USB connector close toSiS55x. The UV+ and UV- signals in a pair must be routed in parallel to each other. Do not route these traces near high frequency signals. Guard ground traces on each side of the signal pair can minimize the induced common mode noise.
- Ferrite beads and bypass caps are for EMI purposes, thus these components should be placed close to the USB connectors.
- 33-ohm series termination resistors are for minimizing discontinuities in the USB line impedance. These resistors should be placed close to SiS55x.

– The 47pf capacitors provide for bypassing high frequency noise that is generated internally in SiS55x. These caps should be placed between the USB controller chip and the 33-ohm termination resistors.

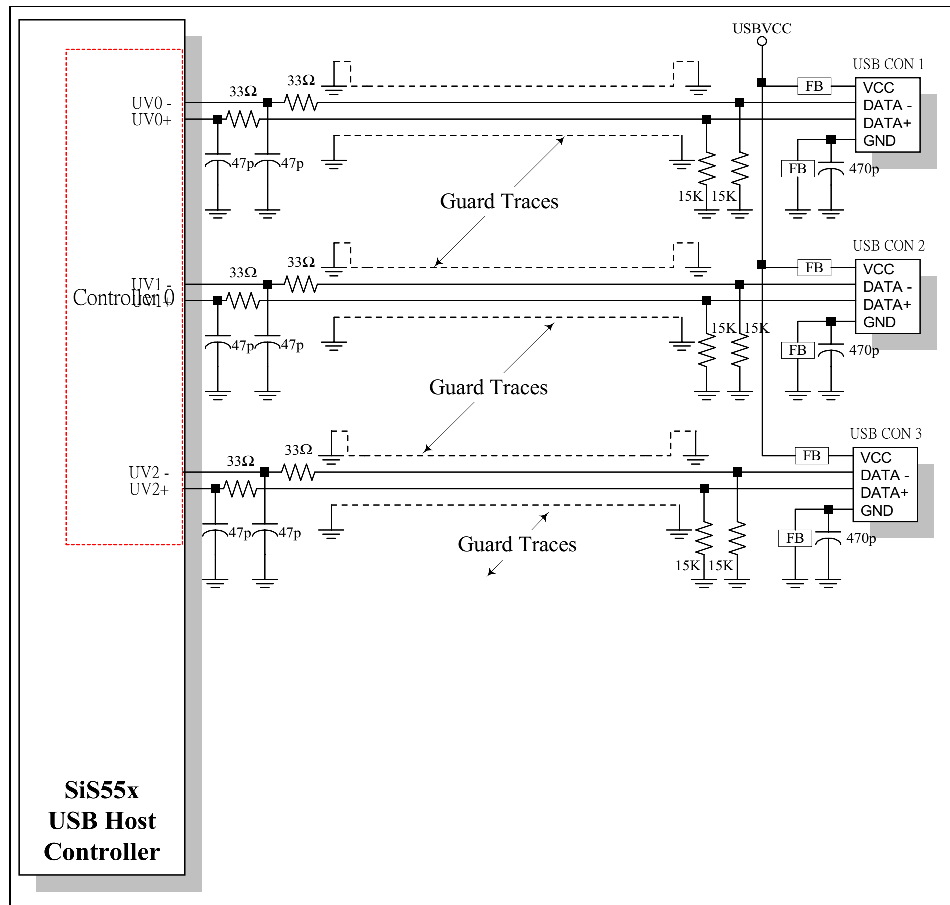


Figure 36. Schematics for USB

3.8.2 USB Hub Over-Current Solution

SiS55x supports over current detection and global power control functions which need external power distribution switches to remove power from all downstream ports and report the condition through the hub to host controller.

The application schematics are illustrated as below:

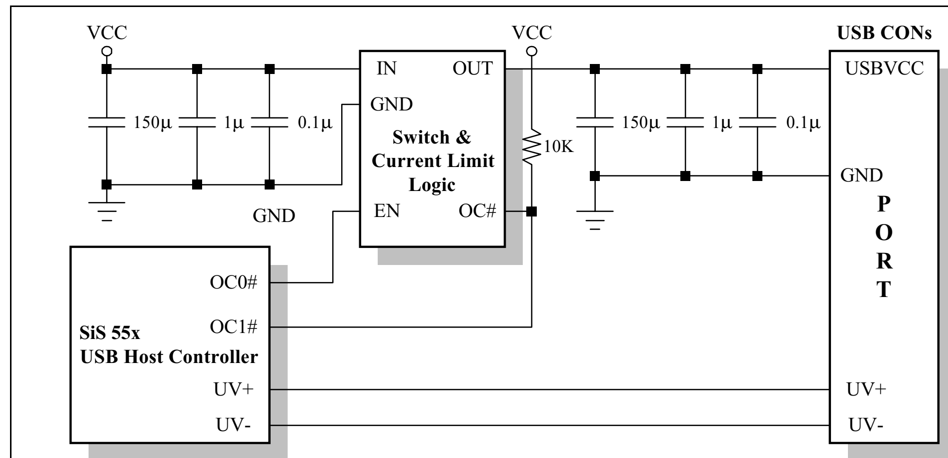


Figure 37. Schematics for USB with Current Limit Solution

Note: Providers of Switch & Current Limit Logic:

1. Texas Instruments: USB Power Supply Products, TPS2015
2. Micrel Semiconductor: USB Current limiter solution

In terms of cost-down consideration, SiS also supports another USB over-current solution that adopts the poly fuse. The drawback of poly fuse solution is that the user has to restart the system once the fuse is broken. The application circuit is illustrated as following:

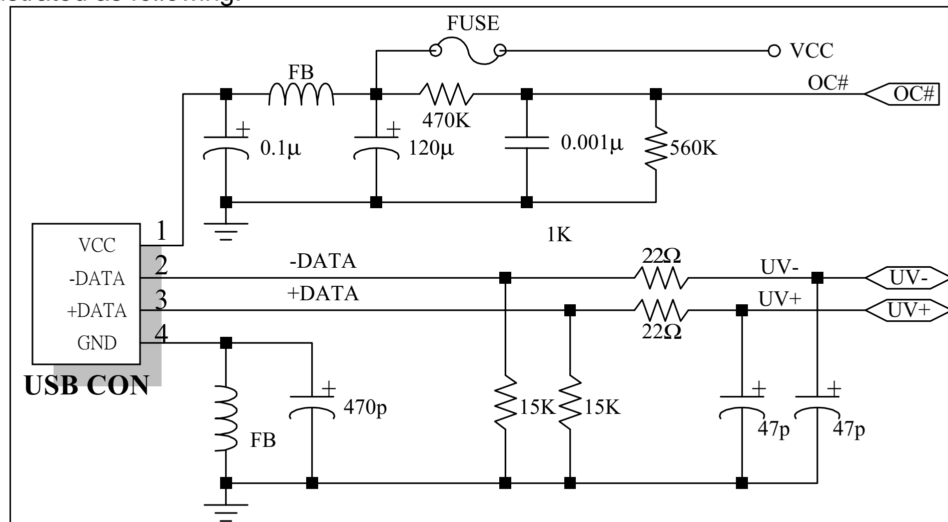


Figure 38. Schematics for USB Over-current Solution

Due to the poly fuse solution in no need of the PPS pin of SiS55x, SiS allows system designer to program this pin to OC1# pin as another USB over current detection signal for the second USB port. Please refer to the application circuit for more information.

3.8.3 Remove USB Function

When the USB interface is not mounted on the motherboard, OC[0…2] should be pulled up; UV[0…2] -/+ and UCLK48M should be pulled down; and FS0/48MHZ on the Clock Gen. side should be floated.

3.9 Fast Ethernet Lan Solution (SiS900)

The following are design requirements for LAN related signals (refers to Table 15):

1. The transmit and receive signals (TPO± and TPI±) should be coupled to the cable with a magnetic module. Hence a transformer inherent with common choke is required. Transformers provide voltage isolation, impedance matching to the cable and EMI control. A common choke is used to block the common mode energy from passing onto the cable. The required specification of the transformer is listed in Table 15. Sources for the transformer are listed in Table 16.

Table 15. TP Transformer Specification

PARAMETER	SPECIFICATION	
	Transmit	Receive
Turns Ratio	1:1 CT	1:1
Inductance, (μH Min)	350	350
Leakage Inductance, (μH)	0.05-0.15	0.2
Capacitance (pF Max)	15	15
DC Resistance (Ohms Max)	0.4	0.4

Table 16. TP Transformer Sources

VENDOR	PART NUMBER
Nano Pulse	NPI 7049-37, NPI 7050-37
Bel	S558-5999-J9
Pulse Engineering	H1089, H1102
Halo	TG22-3506ND, TG110-S050N2
YCL	20PMT04A, PH163112

2. The transmit output (TPO±) and receive input (TPI±) are terminated with external resistors tied to VDD. This is to meet the Input/output impedance and return loss requirements of IEEE802.3. (Refers to Figure 39)

3. A 0.01μF capacitor is placed between the center of the series resistor string and VDD in order to provide an AC ground for attenuating common mode signal at the input.

4. Common mode bundle termination may be needed and can be achieved by tying the receive secondary center tap and the unused pairs in the RJ45 to chassis ground through 75 ohm resistors and a 0.01 μF capacitor.

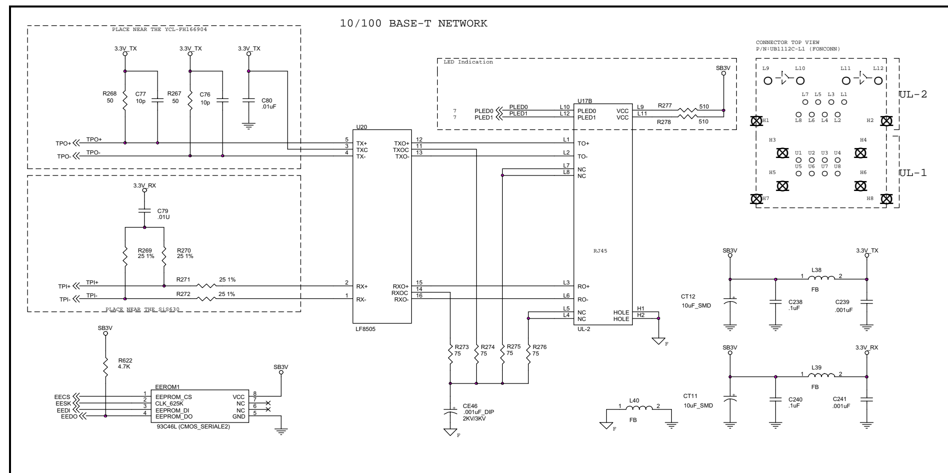


Figure 39. Schematics for LAN Signals

5. A 25 MHz reference frequency is required for internal LAN signal generation. This clock input pin OSC25MHI is driven by a 25 MHz crystal. The crystal must have the characteristics shown in Table 17. The crystal must be placed as close to SiS900 so that parasitic inductance on OSCIN is kept to a minimum.

Table 17. Crystal Specifications

PARAMETER	SPEC
Type	Parallel Resonant
Frequency	25 Mhz +/- 0.01%
Equivalent Series Resistance	25 ohms max
Load Capacitance	18 pF typ
Case Capacitance	7 pF max
Power Dissipation	1mW max

3.9.1 Placement AND TRACE ROUTING

The distance between SiS900 and transformer and the distance between transformer and RJ45/ RJ11 should be as short as possible, i.e. The traces TPO±/ TPI± of SiS900 and the traces TX±/ RX± should be as short and wide as possible. The recommended layout is illustrated in Figure 40.

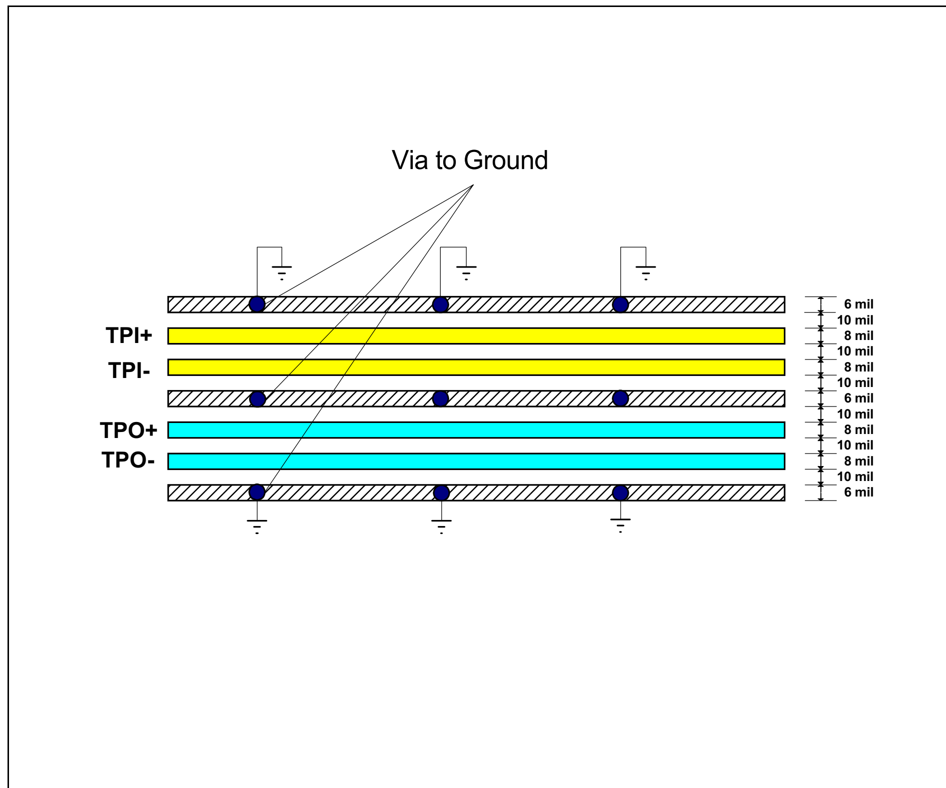


Figure 40. Layout Recommendation for TPO±, TPI±

- The two termination resistors of TPO± should be placed near transformer.
- The termination series resistor and grounding capacitor of TPI± should be placed near SiS900.
- Keep TX+ trace close and symmetry to TX- trace, RX+ trace close and symmetry to RX- trace (no more than 0.1”).
- It is recommended TX± and RX± traces turn using arcs and avoid using any vias and corners.
- The traces of TX± pair should be kept distant from RX± pair. It is best to place ground plane between these two pair of traces.
- For customer using a bracket instead of the back panel for one RJ45 plus two RJ11, the recommended interconnection between Motherboard and the bracket is shown in Figure 41.

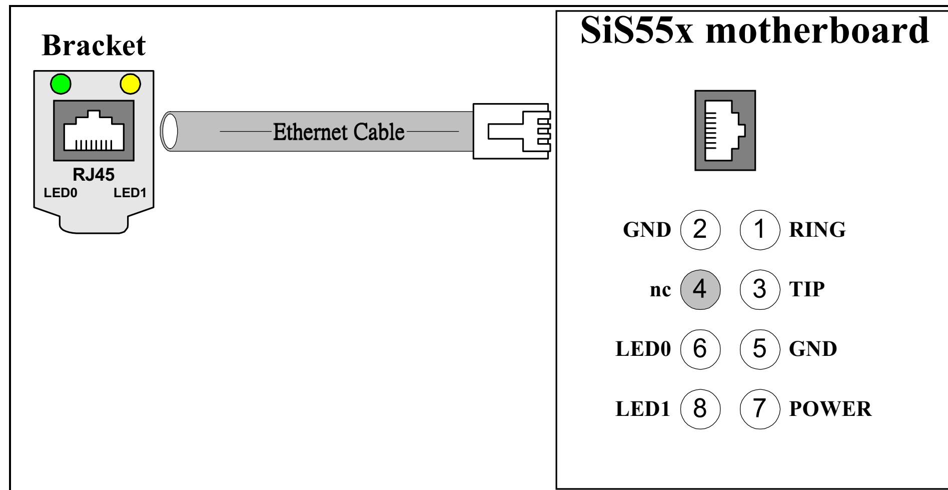


Figure 41. Interconnection between Motherboard and RJ45 Connector

3.9.2 Power and Ground Plane

- The RJ-45 and output side of transformer should use a separated ground plane (chassis ground) which is isolated with the ground plane of the input side of transformer and SiS900. Another way is using no ground plane under the output side of transformer.
- The chassis side ground and the input side ground of transformer should be separated by at least 0.1".
- If possible, partition the analog power/ground planes from noisy logic power/ground planes.
- To protect EMI issue, forbid laying power and ground plane under the transformer, as shown in Figure 42.

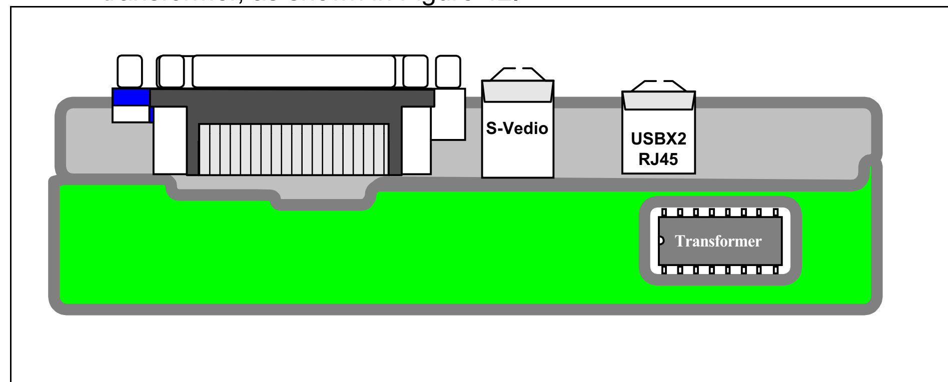


Figure 42. Power/ Ground Isolation for Transformer

3.10 AC'97 Digital Controller Layout Guidelines

The following are layout guidelines for AC'97 digital controller (Refers to Figure 43):

1. Partition audio circuitry on PCBs into three areas: digital, analog and I/O sections.
2. AC-link signals are digital signals and should avoid crossing into the analogue region, or otherwise keep as short as possible.
3. The analogue power should be isolated from digital power plane. It is recommended that each analogue power is provided through a ferrite bead.
4. Bypassing and decoupling capacitors should be close to IC pins.
5. Keep digital signal traces, especially the BIT_CLK trace, away from analogue input and voltage reference pins.
6. Locate the crystal close to the CODEC. Avoid overshoot and undershoot on the master clock for the CODEC.
7. Keep all digital power and signals over the digital ground plane and all analogue power and signals over the analogue ground plane. Do not overlap analogue related and digital related planes.
8. The analogue to digital ground plane connection should be near to the power supply connection to the board, or near the CODEC.

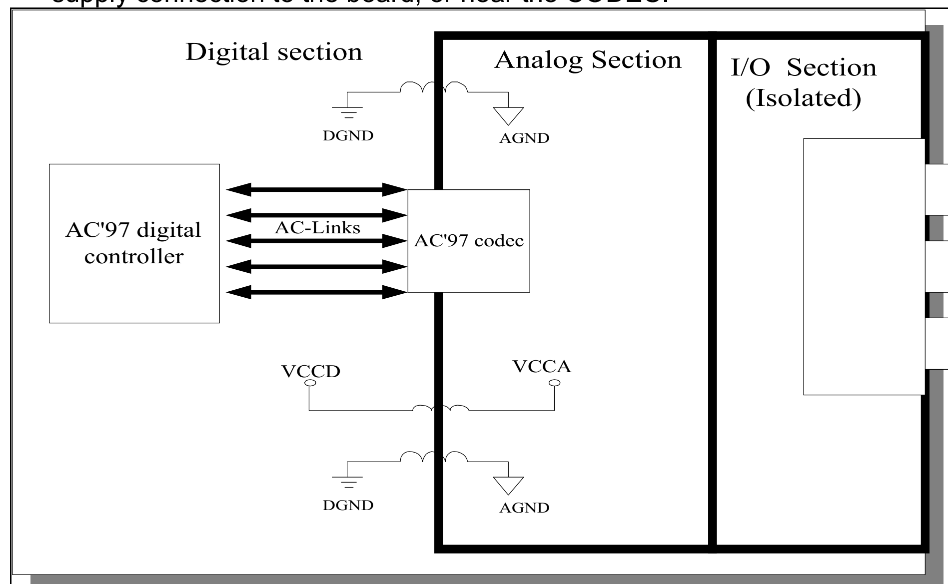


Figure 43. Audio Circuitry Layout

3.10.1 Remove AC’97 Function

When AC’97 is not mounted on the motherboard, AC_SDIN[0…2], AC_BIT_CLK, and CLK66M should be pulled down; and AGPCLK0 on the Clock Gen. side should be floated.

4 ACCOMPANIMENT

4.1 D.O.C (Disk On Chip)

4.1.1 General Future Description

– It combines a disk controller with flash memory on a single die. It's there a very attractive to conventional hard and floppy disk drives. Cascading up to 4 devices, without the need for additional logic, the DiskOnChip Millennium Plus delivers capacities up to 128MB for each device and as single drive disk. Some software .No need for extra hardware.

– The large boot-block (1KB) allows integration of the boot-code into the DiskOnChip Millenium in addition to saving any other non-volatile part from the motherboard (e.g.—the BIOS).

4.1.2 D.O.C. Hardware Design

The DiskOnChip Millennium Plus is connected as a standard memory device using standard SRAM memory interface signals. Figure 44 illustrates a typical interface of the DiskOnChip Millennium plus a system.

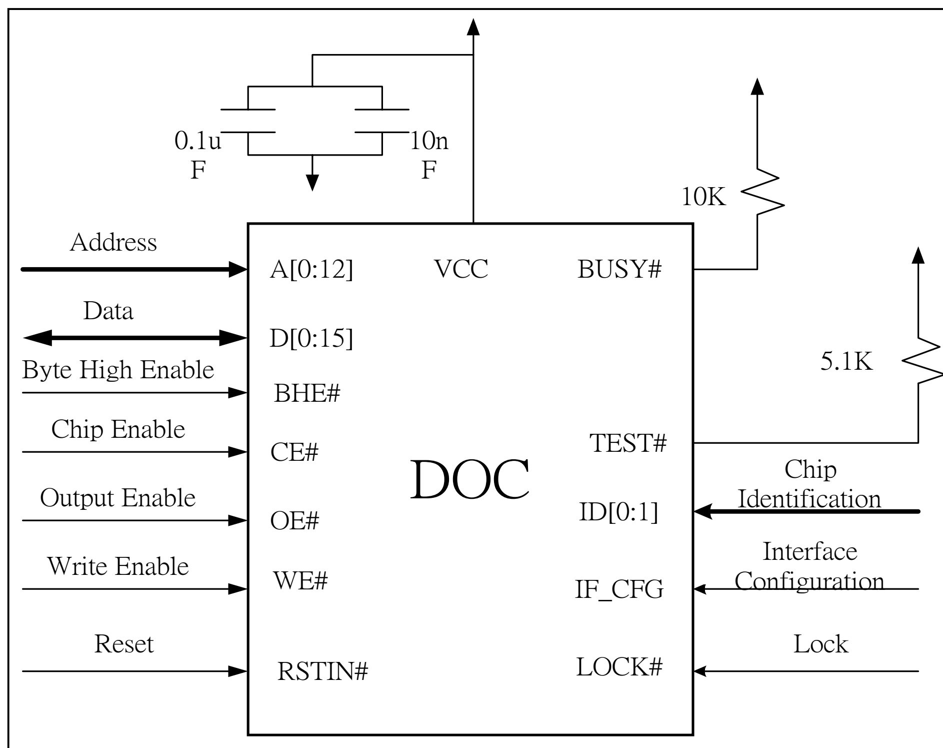


Figure 44. Millenium Plus Simplified I/O

Note: The 0.1uF and 10nF low-inductance high-frequency capacitors must be attached to each of the device's VCC and GND pins. These capacitors must be

placed as close as possible to the package leads to protect chip.

4.1.3 Absolute Maximum Ratings

Table 18. D.O.C. Absolute Maximum Rating

Parameter	Symbol	Rating	Units	Notes
DC supply voltage	Vcc	-0.6 to 4.6	V	
Input pin voltage[2]	Vin	-0.6 to Vcc+0.3	V	
Input pin current	Iin	-10 to 10	mA	25°C
Storage temperature	Tstg	-55 to 155	°C	
Lead temperature	Tlead	260	°C	10sec

4.1.4 DC Electrical Characteristics over Operating Range

Table 19. D.O.C. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
Vcc	Supply Vol.		3	3.3	3.6	V	
Vih	High-Level Input Vol.		2.1			V	
Vil	Low-level Input Vol.				0.7	V	
Vhys	Hysteresis		0.4			V	
Iohmax	Max High-level Output Current		-4			mA	
Iolhmax	Max Low-level Output current		8			mA	
Voh	High-level Output Voltage	Ioh=Iohmax	2.4			V	
V_{OL}	Low-level Output Voltage	Iol=Iolmax			0.4	V	
I_{IL}	Input Leakage Current				±10	uA	
I_{OZ}	Output Leakage Current				±10	uA	
Icc	Active Supply Current	Cycle Time=100ns		25	45	mA	1
Iccs	Standby Supply Current	CE#>Vcc-0.2V All other inputs 0V or VCC			100	uA	

Note: Vcc=3.3V,outputs open.

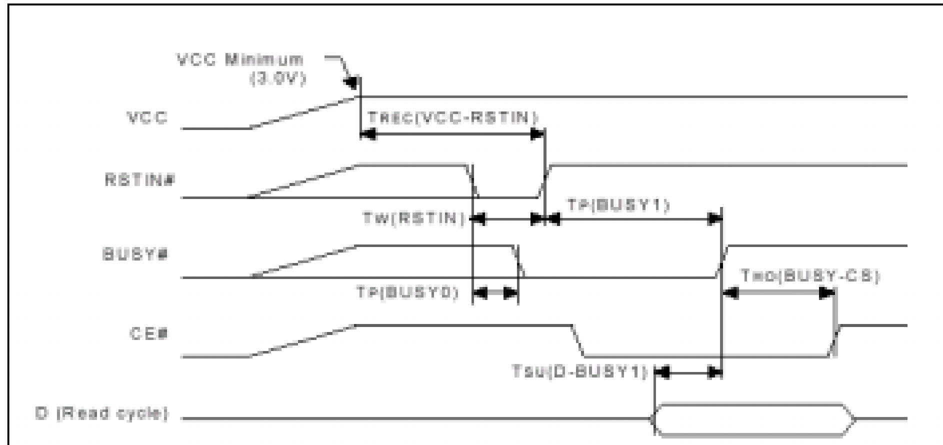


Figure 45. Reset Timing-TSOP Package

Table 20. D.O.C. Reset Timing

Symbol	Description	Min	Max	Units	Notes
TREC(VCC-RSTIN)	VCC stable to RSTIN# ↑	300		ns	1
TW(RSTIN)	RSTIN# asserted pulse width	20		ns	
TP(BUSY0)	RSTIN# ↓ to BUSY# ↓		50	ns	
TP(BUSY1)	RSTIN# ↑ to BUSY# ↑		1	ns	3
THO(BUSY-CE)	BUSY# ↑ to CE# ↑	0		ns	2
TSU(D-BUSY1)	Data valid to BUSY# ↑	0		ns	2

1. Specified as the first positive crossing above 0.5V to the final positive crossing above 2.7V.
2. Normal read/write cycle timing applies. This parameter applies only to the case when the cycle is extended until the negation of the BUSY# signal.
3. If the assertion of RSTIN# occurs during a flash erase cycle this time could be extended by up 500 us.

4.2 Smart Card

4.2.1 Introduction of Smart Card

The Smart Card is the youngest and cleverest member of the identification card family in the ID-1format.It is characterized by an integrated circuit incorporated in the card, which contains elements used for data transmission, storage and processing. Data transfer can take place either via the card's surface.

However, one of the most important advantages of Smart Cards consists in that their stored data can be protected against unauthorized access and tampering, As access to data takes place only via a serial interface supervised by the operating

system and by a security logic system, it is possible to write confidential data to the card which can never be read from outside. This secret data can then only ever be processed internally by the chip's arithmetic unit. In principle, the memory functions of writing, erasing and reading can be controlled both by hardware and by software, and be linked to specific conditions. This allows the construction of numerous security mechanisms, which can also be tailored to the special demands of the relevant application.

4.2.2 Feature of Smart Card

- Compliant with Personal Computer Smart Card (PC/SC) Working Group standard (*)
- Compliant with smart card (ISO 7816) protocols (*)
- Supports card present detection
- Supports smart card insertion power on feature
- Supports 8032 SMI# output

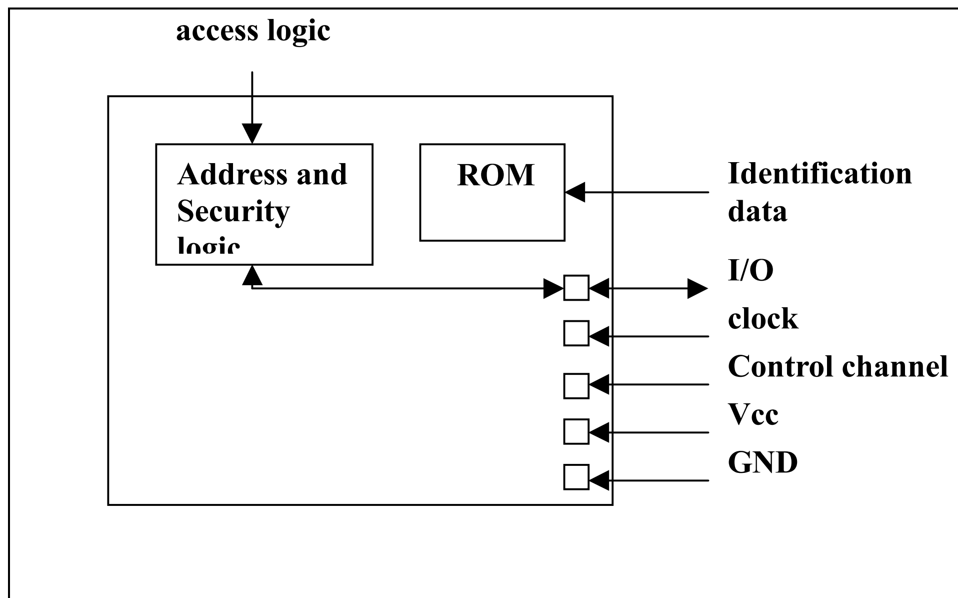


Figure 46. Typical Architecture of a Memory Card with Security Logic

Note (*):Except that SiS55x doesn't support the commands exceeding 64 bytes.

4.2.3 Remove Smart Card Function

When the Smart Card interface is not mounted on the motherboard, RADD6, RGPIO[0…3], and RDAT[0…7] should be pulled down; and RADD[10…15] and RCLK should be floated.

4.3 Memory Stick

Silicon Media is a revolutionary new kind of storage and transfer media that is

creating ever more possibilities for digital age.

Among these new types of media, Memory Stick offers content versatility and product compatibility at high-speed data exchange rate. Figure 47 show the architectural layers of Appliances and Memory Stick. Appliances using Memory Stick have several hardware and software architectural layers.

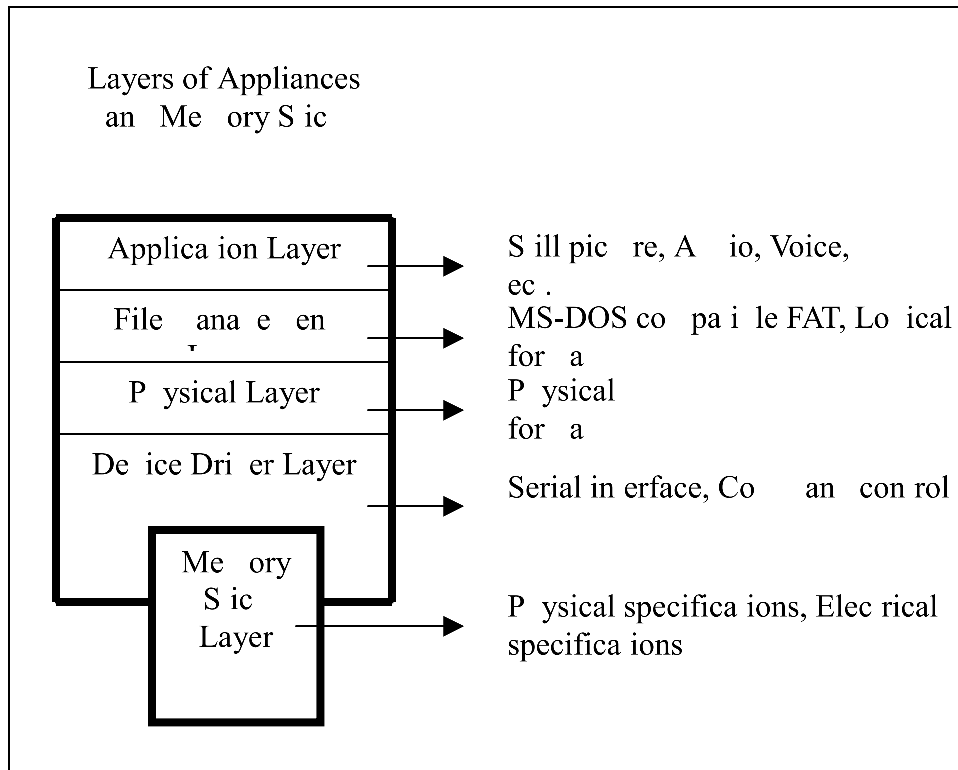
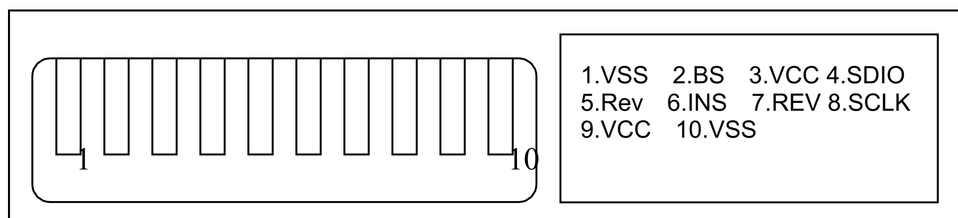


Figure 47. Architectural layers of Appliances and Memory Stick.

4.3.1 Memory Stick Pin Assignment



4.3.2 Electrical Characteristics

Table 21. Signal PINs Description

No.	Pin name	I/O	Pin function
1	VSS		Vss
2	BS	I	Serial protocol bus state signal

3	VCC	I	Vcc
4	SDIO	I/O	Serial protocol data signal
5	Rev.		Reserved
6	INS	O	Stick insertion/extraction detect-terminal
7	Rev.		Reserved
8	SCLK	I	Serial protocol clock signal
9	VCC	I	Vcc
10	VSS		Vss

Memory Stick shall be used in recommended operating conditions to secure the normal logical operation. Table 22 is recommended operating conditions.

Table 22. Recommended Operating Conditions

Parameter	Symbol	Standards			Unit
		Min.	Typ.	Max.	
Power source voltage	Vcc	2.7	---	3.6	V
H-level input voltage	V_{IH}	VccX0.7	---	Vcc	V
L-level input voltage	V_{IL}	0	---	VccX0.3	V
Operating ambient temperature	T_{OP}	-5	---	+65	°C

Note) Above voltage values are at Memory Stick terminal without voltage drop caused by contact resistance etc.

4.3.3 Insertion Detect

Insertion/extraction of Memory Stick is detected through signal of Pin 6.

Just like the reason of IDE connector at Pin3 (IDE7) have a 10K pull down resistor to tell system the present of IDE device. But in Memory Stick it’s 10K pull high at normal empty state, when insert Memory Stick, this signal will go low with whole system to show it’s here.

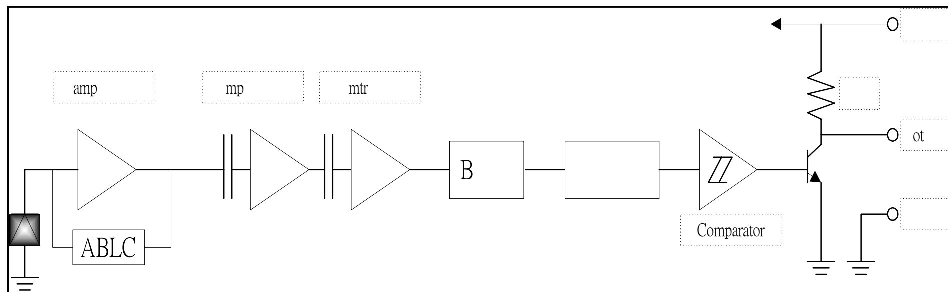
4.3.4 Remove Smart Card Function

When of the Memory Stick interface is not mounted on the motherboard, MS0~MS5 (MSBS, MSDIO, MSCLK, MSINS, MSPWRON and MSLED) should be pulled down.

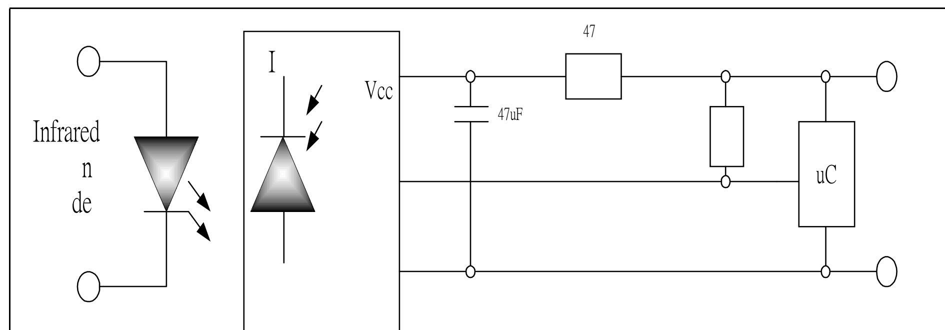
4.4 INFRARED REMOTE-CONTROL RECEIVER

For the security concerned, SiS build up a whole guard system, from smart card, memory stick to the infrared remote, can avoid data been stolen from outside.

4.4.1 Block Diagram



■ Application Circuit:



RC Filter should be connected closely between Vcc pin and GND pin.

Table 23. Electro Optical Characteristic (Ta=25ºC)

Parameter	Symbol	MIN	TYP	MAX	Unit	Condition
Supply Voltage	Vcc	4.5	5	5.5	V	DC voltage
Supply Current	Icc	—	—		mA	
B.P.F Center Frequency	fo	—	38	—	KHz	
Peak Wavelength	λ p	—	940	—	nm	
Transmission Distance	L_0	10	—	—	m	At the ray axis
	L_{45}	5	—	—		
Half Angle (Horizontal)	θ h	—	45	—	deg	
Half Angle (Vertical)	θ v	—	35	—	deg	
High Level Pulse Width	T_H	400	—	800	us	
Low Level Pulse Width	T_L	400	—	800	us	At the ray axis
High Level Output Voltage	V_H	4.5	—	—	V	
Low Level Output Voltage	V_L	—	0.2	0.5	V	

IR receiver should be placed in the front end of PCB edge to get the best data quality.

5 Video Bridge (SiS301)

SiS301, which is an accompany chip of SiS VGA chip, integrates

- A NTSC/PAL video encoder with Macrovision Ver.7.1.L1 option for TV display.
- A TMDS™ transmitter with bi-linear scaling capability for TFT LCD panel display.
- An analog RGB port to support a secondary CRT monitor display.

All the above functions can support dual-display features. It means that the second display device driven by SiS301 can display independent resolutions, color depths and frame rates different from the primary VGA chip. SiS301 receives digital video signals and control signals from the primary VGA chip then transforms them into composite, S or component video output for TV display, TMDS™ signals for LCD display and analog RGB signals for secondary CRT display. The package type of SiS301 is 100-pin TQFP.

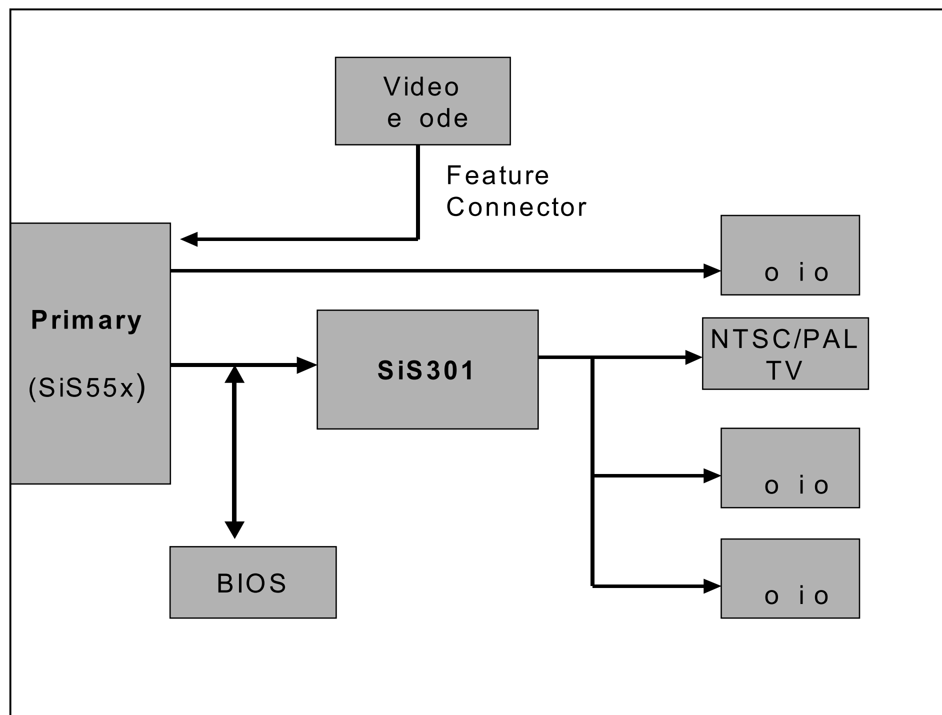


Figure 48. SiS301 Application Block Diagram

5.1 SiS301 DAC Signals Routing

Each of R, G, B signals on the board is to be loaded with a 75Ω resistor. Diodes can be used to protect the controller from any large transient voltage that may enter from the connector when the monitor is connected. The Π type filter must be

placed in series to RGB signals that is required to comply with FCC class B and CE requirements for radio frequency emissions and filter the high frequency noise.

To product better display quality, RGB signals tracing should be required to maintain (75Ω) impedance match and its nearby signals should be placed far away as possible to prevent noise interference. Using the ground to close the RGB signal is a better choice to solve the problem.

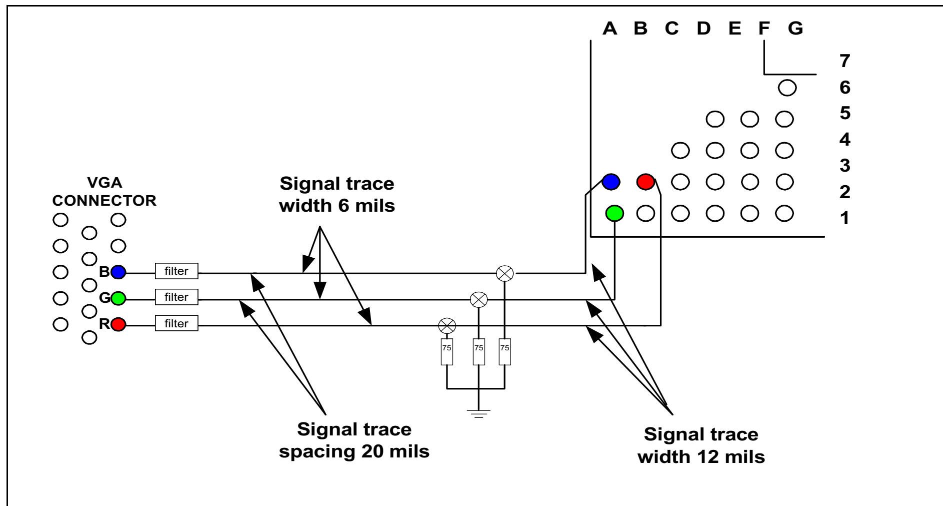


Figure 49. R, G and B Signals Tracing

A clear power and ground are necessary to provide internal DAC circuits. There are two sets of power and ground (AVDD6, AVSS6, AVDD7 and AVSS7) to supply DAC circuits. But AVSS6 is a very dirty signal. It will interfere through AVSS7 to internal DAC circuits. Therefore, AVSS6 and AVSS7 cannot route to ground simultaneously and need a distance of about 1cm to reduce this phenomenon.

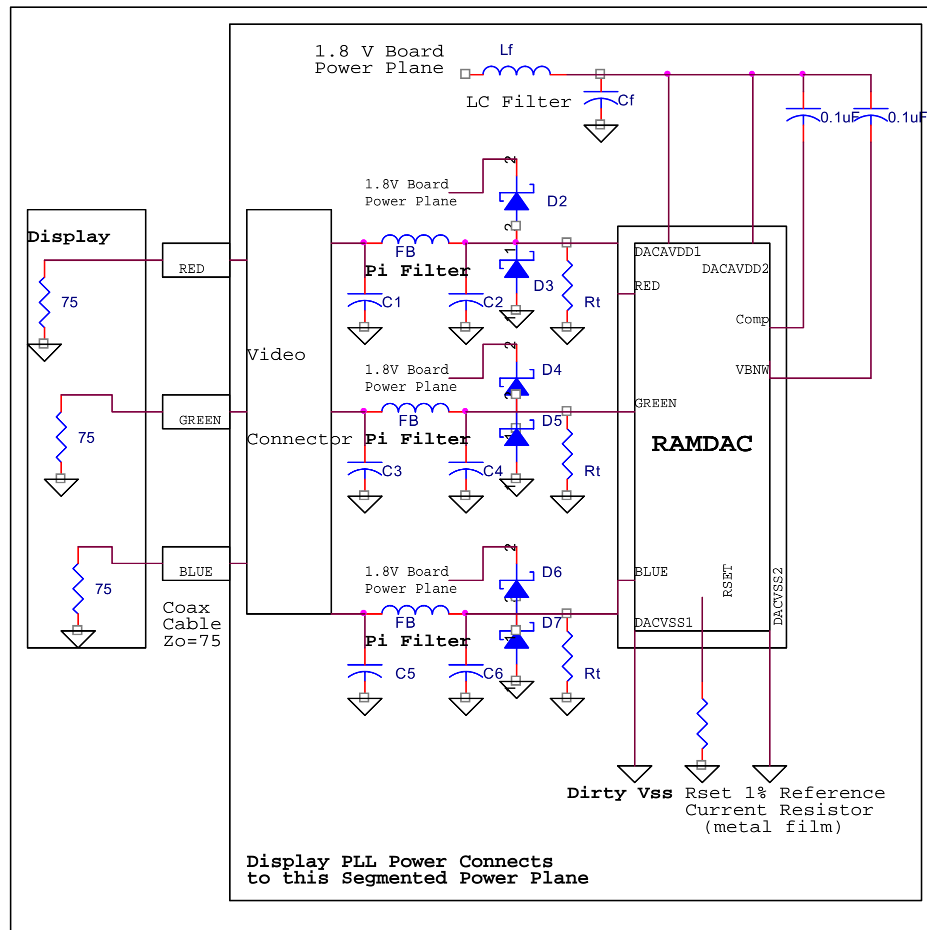


Figure 50. DAC AP Circuits for SiS301

5.2 SiS55x to SiS301 Signals Routing

5.2.1 Interface from SiS55x to SiS301

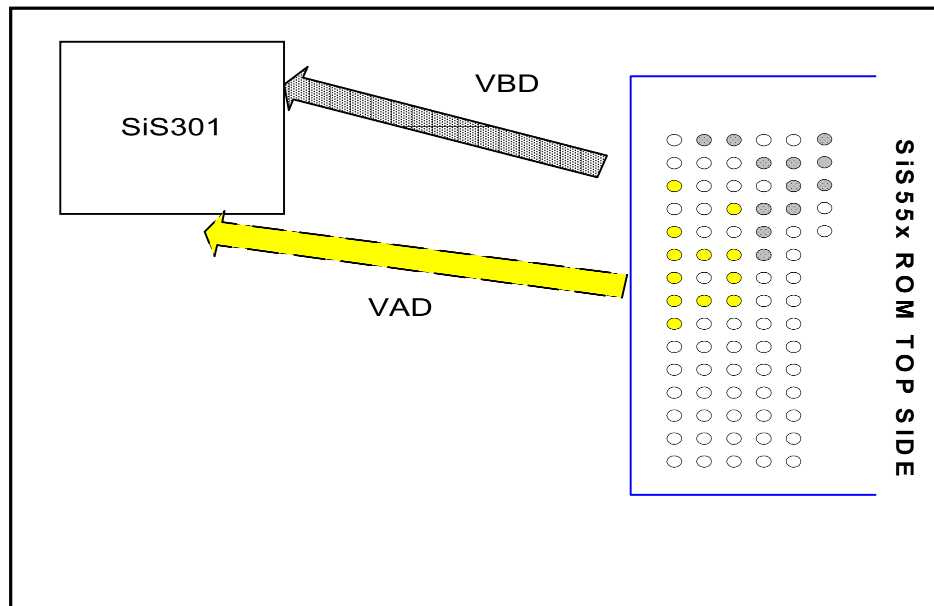


Figure 51. Connect from SiS55x to SiS301

5.2.2 Sensitive signals

- The CLK signals that include VBRCLK, VACLK, VBCLK, VAGCLK and VBGCLK should maintain double signal width spacing to reduce noise.
- The VAGCLK and VBGCLK should be placed on the center of their respective DATA signals (VAD[11…0] And VBD[11…0]) to minimize skew.
- The digital input signals are sensitive. Therefore, group the digital input signals and route away the noise signals are strongly recommended.
- Analog Output signals routing must take care signal quality.
- Include CRT2 (R, G and B), TV OUT (C, Y and TVBS) and TMDS (LVDS) differential pair signals. The LCD transmitter signals (TMDS/LVDS) must especially consider the characteristic impedance matching to prevent reflection problem. Shield with AGND or route far away from the noise signal to guaranty the signal quality.

5.2.3 TMDS\LVDS Transmission Line

The bandwidth of TMDS\LVDS transmission can over 1.6GHz. The impedance matching problem must be taken care. The characteristic impedance of the differential signal pair should be **50** Ω each, which is controlled by the width and space of the differential signal pair. Generally, to achieve the characteristic impedance mentioned above, the line width of each of the differential signal pair is about 8 mils and the space between them is 10mil when the height between the copper layer and the GND plane is 6mil (in 4 layer PCB board). For detail information, please refer to the Table 4. It will slightly change with the PCB's

thickness of the copper layer and the dielectric constant of the insulator layers. The SiS301 should be as near as possible to the output of connector and care should be taken to route each differential signal pair together and minimize the number of vias the signal lines are routed through.

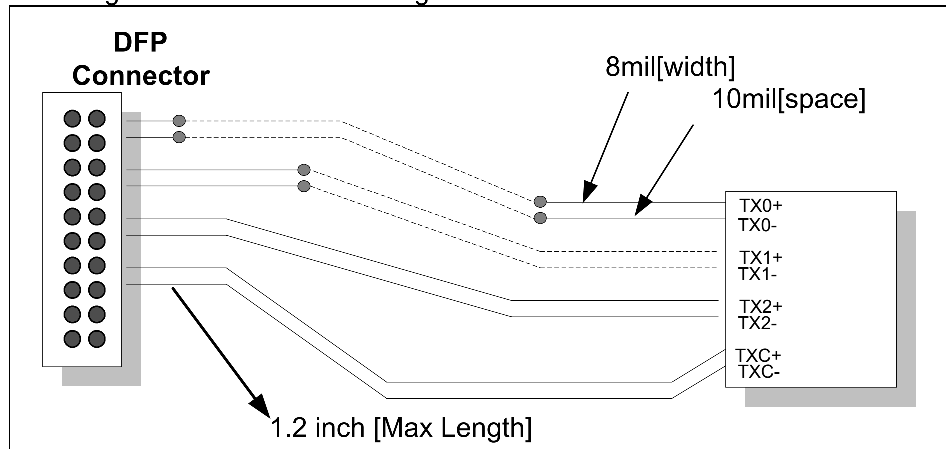


Figure 52. Example of Acceptable Differential Signal Routing

Do not split the pairs and minimize the number of vias. Vias are very inductive and can cause phase delay problems if applied unevenly within a pair.

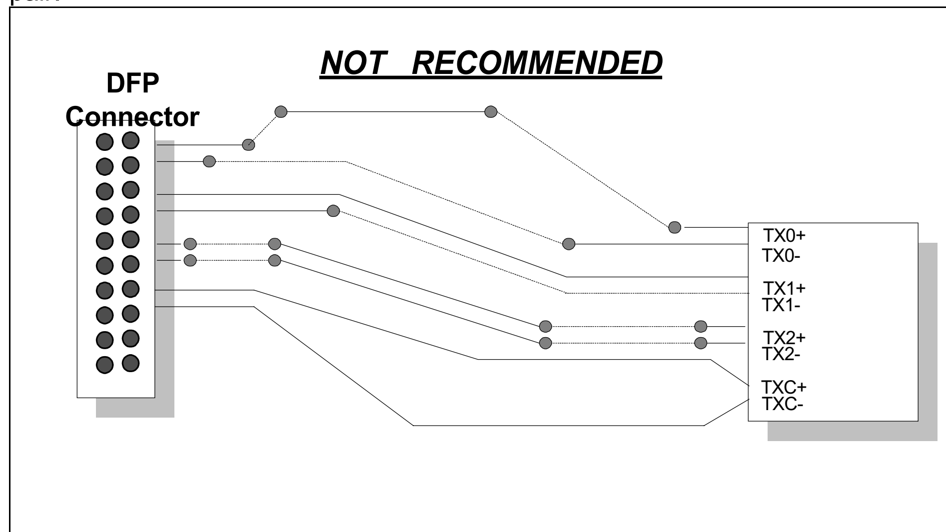


Figure 53. Separation and Excessive or Asymmetric via Routing are Not Recommended

Note: For better display quality of SiS301, it is not recommended to use 2 layers PCB board.

5.2.4 Disable VIDEO Bridge

When removing VAD channel / VBD channel function and reserving only CRT

function, VBCLK, DDC3DATA, and DDC3CLK should be pulled down; and other relative signals should be floated.

Revision History

Preliminary v.0.9 (3/14/2002) –

Changed VCC18 to VCCcore on definition and all figures.

Changed the Package Outlines to 686-pin package.

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